High Stability, Isolated Error Amplifier

Enhanced Product

ADuM4190-EP

FEATURES

- Stable over time and temperature
  - 0.5% initial error accuracy
  - 1% accuracy error over the full temperature range
- Compatible with Type II or Type III compensation networks
- Reference output voltage: 1.225 V
- Compatible with Distributed-power Open Standards Alliance (DOSA)
- Low power operation: <7 mA total
- Wide voltage supply range: 3.0 V to 20 V (V_{DD1} and V_{DD2})
- Output −3 dB bandwidth: 400 kHz typical
- Isolation voltage: 5000 V rms reinforced
- Safety and regulatory approvals
  - UL recognition: 5000 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
  - VDE certificate of conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
      - V_{IORM} = 849 V peak

ENHANCED FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Linear feedback power supplies
- Inverters
- Uninterruptible power supplies (UPS)
- DOSA-compatible modules
- Voltage monitors

GENERAL DESCRIPTION

The ADuM4190-EP[1] is an isolated error amplifier based on Analog Devices, Inc., *i*Coupler® technology. The ADuM4190-EP is ideal for linear feedback power supplies. The primary side controllers of the ADuM4190-EP enable improvements in transient response, power density, and stability as compared to commonly used optocoupler and shunt regulator solutions.

Unlike optocoupler-based solutions, which have an uncertain current transfer ratio over lifetime and at high temperatures, the ADuM4190-EP transfer function does not change over its lifetime and is stable over a wide temperature range of −55°C to +125°C.

Included in the ADuM4190-EP is a wideband operational amplifier for a variety of commonly used power supply loop compensation techniques. The ADuM4190-EP is fast enough to allow a feedback loop to react to fast transient conditions and overcurrent conditions. Also included is a high accuracy 1.225 V reference to compare with the supply output setpoint.

The ADuM4190-EP is packaged in a wide body, 16-lead SOIC package for a reinforced 5000 V rms isolation voltage rating.

Additional application and technical information can be found in the ADuM4190 data sheet.

FUNCTIONAL BLOCK DIAGRAM

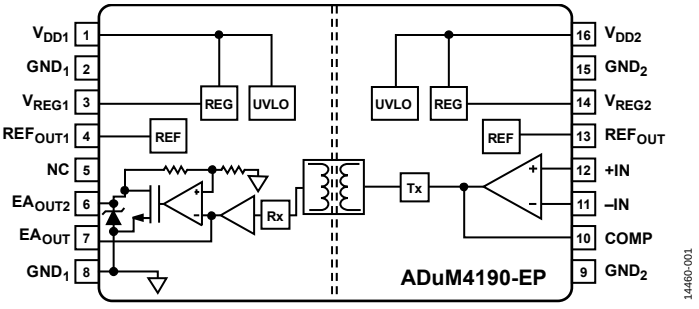

Figure 1.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,329; and 9,293,997.

Rev. 0 Document Feedback

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REVISION HISTORY

7/2016—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD1} = V_{DD2}$ = 3 V to 20 V for $T_A = T_{MIN}$ to T_{MAX}. All typical specifications are at T_A = 25°C and $V_{DD1} = V_{DD2}$ = 5 V, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ACCURACY	(1.225 V – EA_{OUT})/1.225 V × 100%; see Figure 27				
Initial Error	T_A = 25°C		0.25	0.5	%
Total Error	$T_A = T_{MIN}$ to T_{MAX}		0.5	1	%
OP AMP					
Offset Error		−5	±2.5	+5	mV
Open-Loop Gain		66	80		dB
Input Common-Mode Range		0.35		1.5	V
Gain Bandwidth Product			10		MHz
Common-Mode Rejection			72		dB
Input Capacitance			2		pF
Output Voltage Range	COMP pin	0.2		2.7	V
Input Bias Current			0.01		µA
REFERENCE					
Output Voltage	0 mA to 1 mA load, C_{REFOUT} = 15 pF				
	T_A = 25°C	1.215	1.225	1.235	V
	$T_A = T_{MIN}$ to T_{MAX}	1.213	1.225	1.237	V
Output Current	C_{REFOUT} = 15 pF	2.0			mA
UNDERVOLTATE LOCK OUT (UVLO)					
Positive Going Threshold			2.8	2.96	V
Negative Going Threshold		2.4	2.6		V
EA_{OUT} Impedance	V_{DD2} or V_{DD1} < UVLO threshold		High-Z		Ω
OUTPUT CHARACTERISTICS	See Figure 29				
Output Gain[1]	From COMP to EA_{OUT}, 0.4 V to 2.1 V, ±3 mA	0.83	1.0	1.17	V/V
	From EA_{OUT} to EA_{OUT2}, 0.4 V to 2.1 V, ±1 mA, V_{DD1} = 20 V	2.5	2.6	2.7	V/V
Output Offset Voltage	From COMP to EA_{OUT}, 0.4 V to 2.1 V, ±3 mA	−0.4	+0.05	+0.4	V
	From EA_{OUT} to EA_{OUT2}, 0.4 V to 2.1 V, ±1 mA, V_{DD1} = 20 V	−0.1	+0.01	+0.1	V
Output Linearity[2]	From COMP to EA_{OUT}, 0.4 V to 2.1 V, ±3 mA	−1.0	+0.15	+1.0	%
	From EA_{OUT} to EA_{OUT2}, 0.4 V to 2.1 V, ±1 mA, V_{DD1} = 20 V	−1.0	+0.1	+1.0	%
Output −3 dB Bandwidth	From COMP to EA_{OUT}, 0.4 V to 2.1 V, ±3 mA, and from COMP to EA_{OUT2}, 0.4 V to 2.1 V, ±1 mA, V_{DD1} = 20 V	250	400		kHz
Output Voltage	±3 mA output				
EA_{OUT}					
Low Voltage				0.4	V
High Voltage		2.4	2.5		V
EA_{OUT2}	±1 mA output				
Low Voltage	V_{DD1} = 4.5 V to 5.5 V		0.3	0.6	V
	V_{DD1} = 10 V to 20 V		0.3	0.6	V
High Voltage	V_{DD1} = 4.5 V to 5.5 V	4.8	4.9		V
	V_{DD1} = 10 V to 20 V	5.0	5.4		V
Noise	See Figure 15				
EA_{OUT}			1.7		mV rms
EA_{OUT2}			4.8		mV rms
POWER SUPPLY					
Operating Range					
Side 1	V_{DD1}	3.0		20	V
Side 2	V_{DD2}	3.0		20	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Power Supply Rejection	DC, $V_{DD1} = V_{DD2}$ = 3.0 V to 20 V	60			dB
Supply Current					
I_{DD1}	See Figure 4		1.4	2.0	mA
I_{DD2}	See Figure 5		2.9	5.0	mA

[1] Output gain is defined as the slope of the best-fit line of the output voltage vs. the input voltage over the specified input range, with the offset error adjusted out.
[2] Output linearity is defined as the peak-to-peak output deviation from the best-fit line of the output gain, expressed as a percentage of the full-scale output voltage.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE						
Input to Output[1]	R_{I-O}		10^{13}		Ω	
CAPACITANCE						
Input to Output[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC JUNCTION-TO-AMBIENT THERMAL RESISTANCE	θ_{JA}		45		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device; Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input pin to ground.

REGULATORY INFORMATION

The ADuM4190-EP is pending approval by the organizations listed in Table 3. See Table 8 for recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 3.

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
Recognized under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Certified by CQC11-471543-2015, GB4943.1-2011
Single Protection, 5000 V rms Isolation Voltage, 16-Lead SOIC	Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage Basic insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage	Reinforced insulation, 849 V peak	Reinforced insulation at 400 V rms (565 V peak), tropical climate, altitude ≤ 5000 meters
Certified temperature range: −40°C to +125°C	Certified temperature range: −40°C to +125°C	Certified temperature range: −40°C to +125°C	Certified temperature range: −40°C to +125°C
File E214100	File 205078	File 2471900-4880-0001	File CQC15001129480

[1] In accordance with UL 1577, each ADuM4190-EP is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, each ADuM4190-EP is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.0 min	mm	Measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PCB layout
Minimum External Tracking (Creepage)	L(I02)	8.3 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303, Part 1
Isolation Group		II		Material Group DIN VDE 0110, 1/89, Table 1

RECOMMENDED OPERATING CONDITIONS

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit
OPERATING TEMPERATURE	T_A	−55		+125	°C
SUPPLY VOLTAGES[1]	V_{DD1}, V_{DD2}	3.0		20	V
INPUT SIGNAL RISE AND FALL TIMES	t_R, t_F			1.0	ms

[1] All voltages are relative to their respective grounds.

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval for an 849 V peak working voltage.

Table 6.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input-to-Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1273	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1018	V peak
Highest Allowable Overvoltage		V_{IOTM}	6000	V peak
Surge Isolation Voltage	V peak = 10 kV; 1.2 µs rise time; 50 µs, 50% fall time	V_{IOSM}	6000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	2.78	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

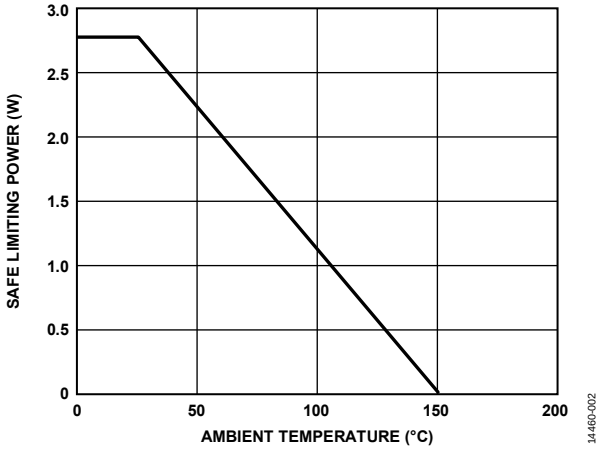

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−55°C to +125°C
Junction Temperature Range	−55°C to +150°C
Supply Voltage Range[1]	
V_{DD1}, V_{DD2}	−0.5 V to +24 V
V_{REG1}, V_{REG2}	−0.5 V to +3.6 V
Input Voltage Range (+IN, −IN)	−0.5 V to +3.6 V
Output Voltage Range	
REF_{OUT}, REF_{OUT1}, COMP, EA_{OUT}	−0.5 V to +3.6 V
EA_{OUT2}	−0.5 V to +5.5 V
Output Current per Output Pin Range	−11 mA to +11 mA
Common-Mode Transients Range[2]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective grounds.
[2] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 8. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage			50-year minimum lifetime
Bipolar Waveform	560	V peak	
Unipolar Waveform	1131	V peak	
DC Voltage	1131	V peak	50-year minimum lifetime

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

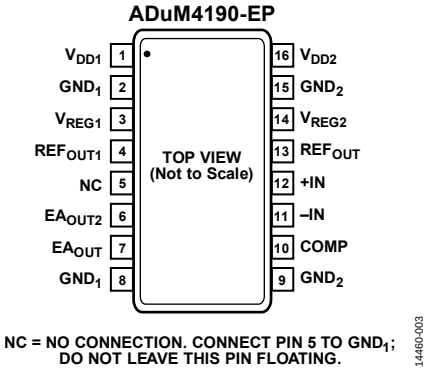

Figure 3. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Side 1 (3.0 V to 20 V). Connect a 1 µF capacitor between V_{DD1} and GND_1.
2, 8	GND_1	Ground Reference for Side 1.
3	V_{REG1}	Internal Supply Voltage for Side 1. Connect a 1 µF capacitor between V_{REG1} and GND_1.
4	REF_{OUT1}	Reference Output Voltage for Side 1. The maximum recommended capacitance for this pin ($C_{REFOUT1}$) is 15 pF.
5	NC	No Connection. Connect Pin 5 to GND_1; do not leave this pin floating.
6	EA_{OUT2}	Isolated Output Voltage 2, Open-Drain Output. Connect a pull-up resistor between EA_{OUT2} and V_{DD1} for current up to 1 mA.
7	EA_{OUT}	Isolated Output Voltage.
9, 15	GND_2	Ground Reference for Side 2.
10	COMP	Output of the Op Amp. A loop compensation network can be connected between the COMP pin and the –IN pin.
11	–IN	Inverting Op Amp Input. Pin 11 is the connection for the power supply setpoint and compensation network.
12	+IN	Noninverting Op Amp Input. Pin 12 can be used as a reference input.
13	REF_{OUT}	Reference Output Voltage for Side 2. The maximum recommended capacitance for this pin (C_{REFOUT}) is 15 pF.
14	V_{REG2}	Internal Supply Voltage for Side 2. Connect a 1 µF capacitor between V_{REG2} and GND_2.
16	V_{DD2}	Supply Voltage for Side 2 (3.0 V to 20 V). Connect a 1 µF capacitor between V_{DD2} and GND_2.

TYPICAL PERFORMANCE CHARACTERISTICS

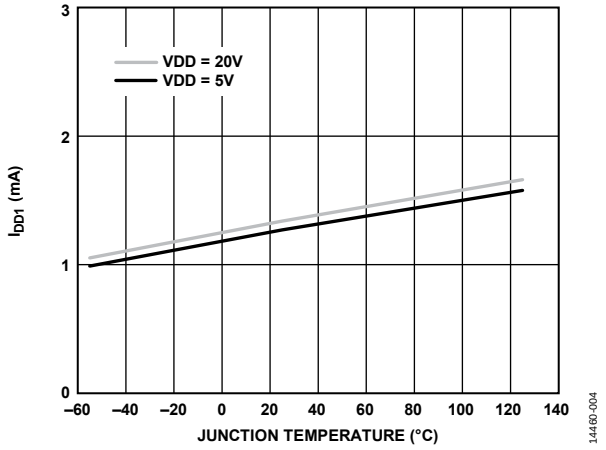

Figure 4. Typical I_{DD1} Supply Current vs. Junction Temperature for V_{DD} = 20 V and V_{DD} = 5 V

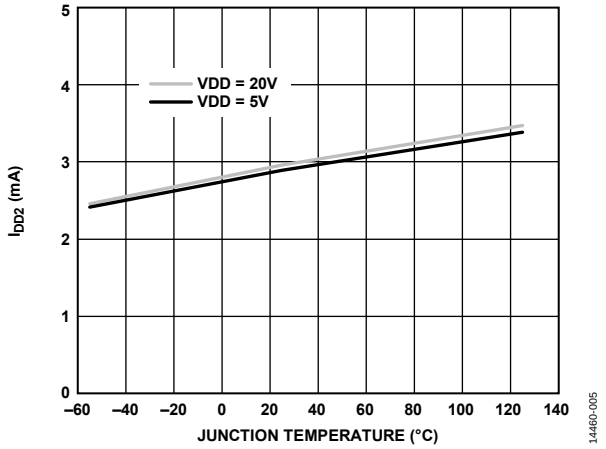

Figure 5. Typical I_{DD2} Supply Current vs. Junction Temperature for V_{DD} = 20 V and V_{DD} = 5 V

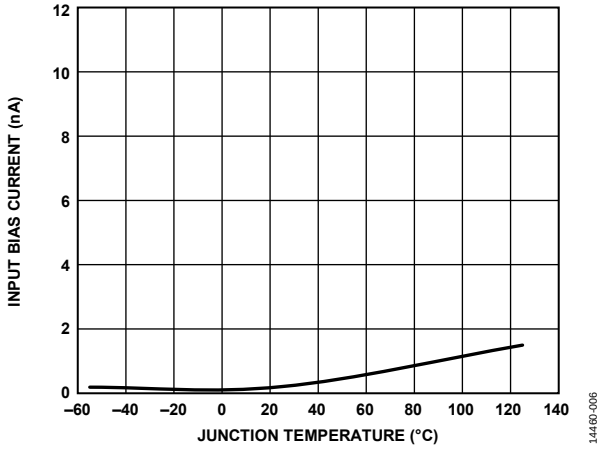

Figure 6. +IN, −IN Input Bias Current vs. Junction Temperature

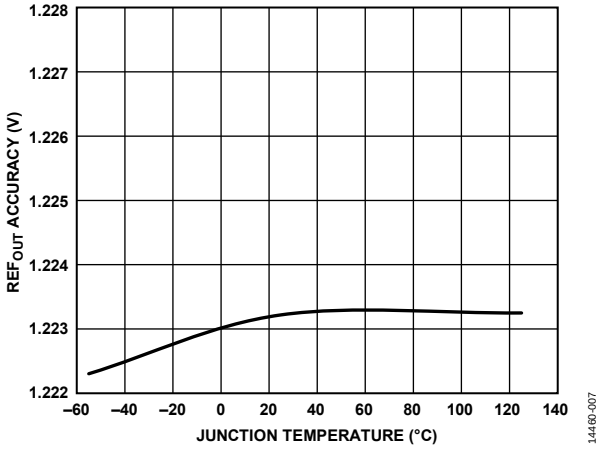

Figure 7. REF_{OUT} Accuracy vs. Junction Temperature

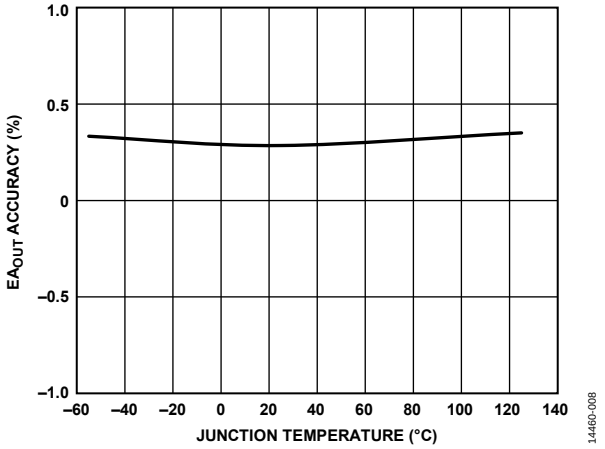

Figure 8. EA_{OUT} Accuracy vs. Junction Temperature

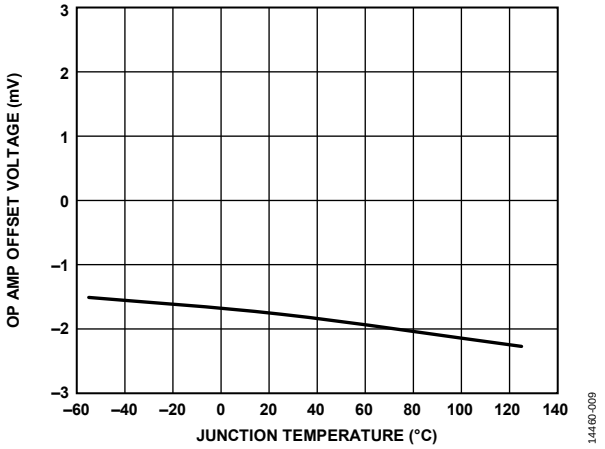

Figure 9. Op Amp Offset Voltage vs. Junction Temperature

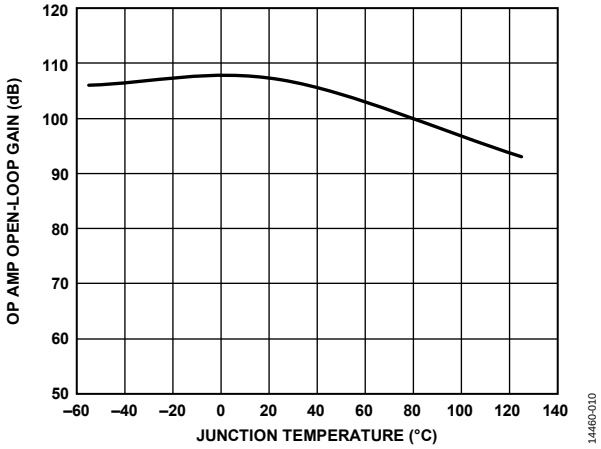

Figure 10. Op Amp Open-Loop Gain vs. Junction Temperature

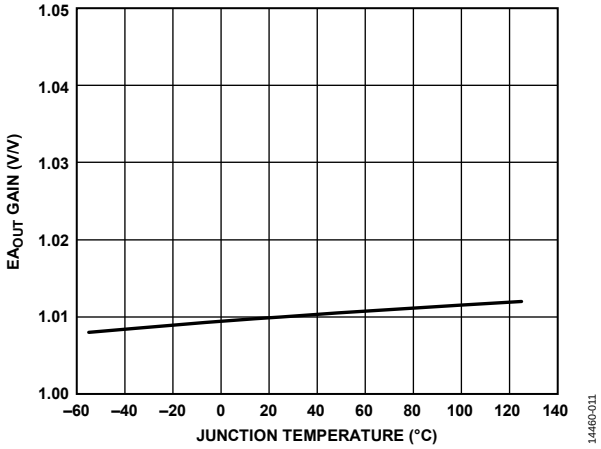

Figure 11. EA_{OUT} Gain vs. Junction Temperature

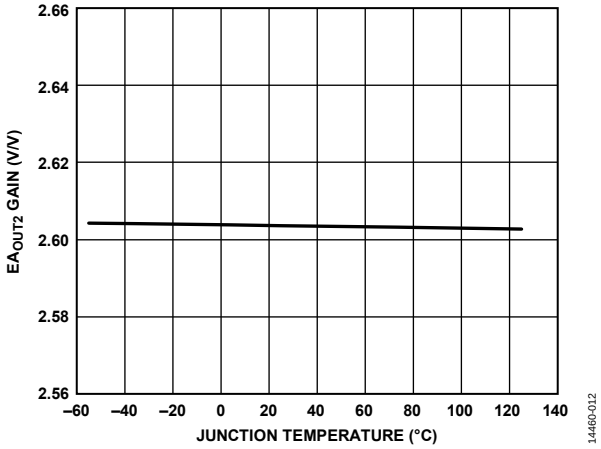

Figure 12. EA_{OUT2} Gain vs. Junction Temperature

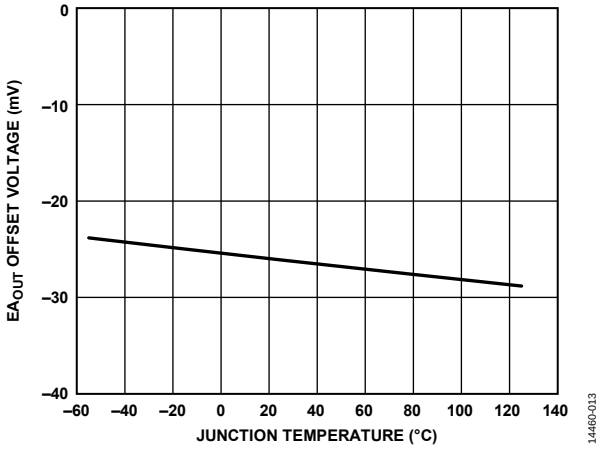

Figure 13. EA_{OUT} Offset Voltage vs. Junction Temperature

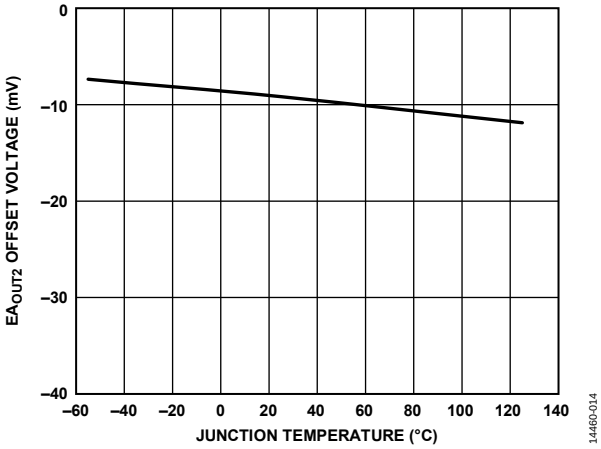

Figure 14. EA_{OUT2} Offset Voltage vs. Junction Temperature

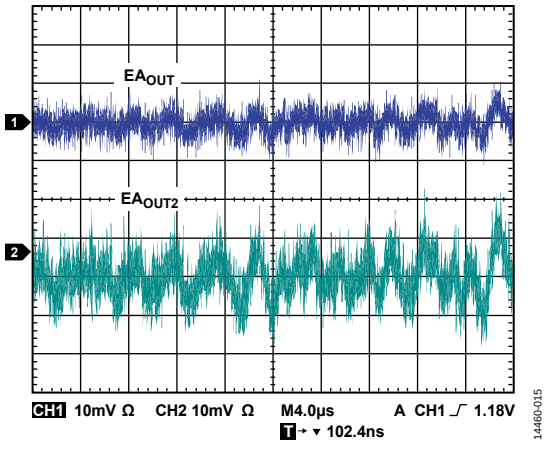

Figure 15. Output Noise with Test Circuit 1 (10 mV/DIV), Channel 1 = EA_{OUT}, Channel 2 = EA_{OUT2}

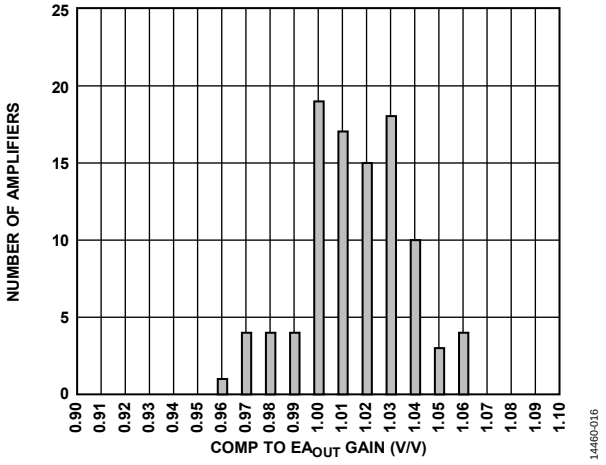

Figure 16. COMP to EA_{OUT} Gain Distribution at 25°C

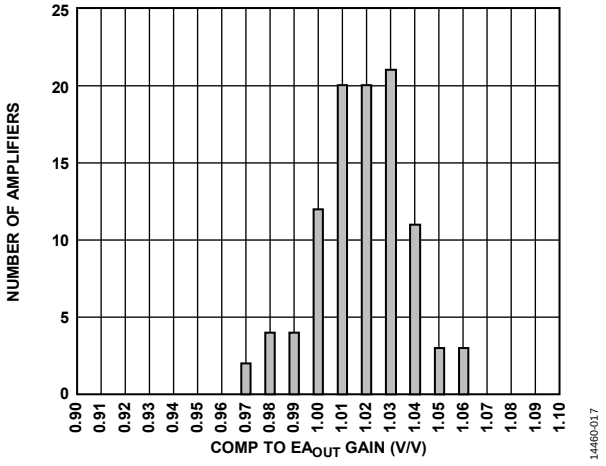

Figure 17. COMP to EA_{OUT} Gain Distribution at 125°C

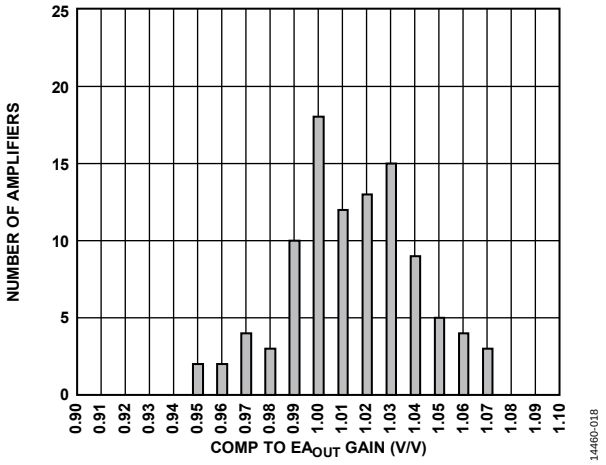

Figure 18. COMP to EA_{OUT} Gain Distribution at −55°C

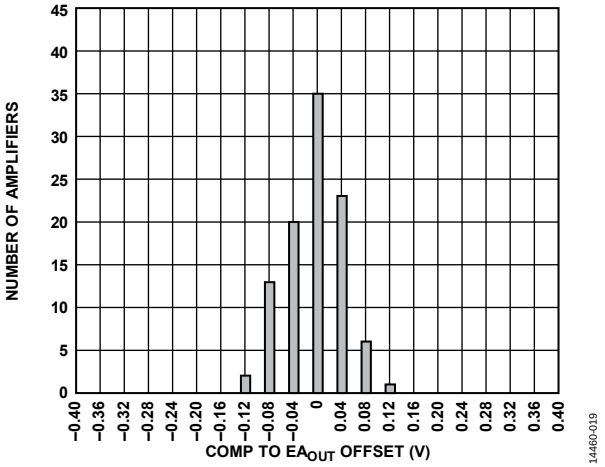

Figure 19. COMP to EA_{OUT} Offset Distribution at 25°C

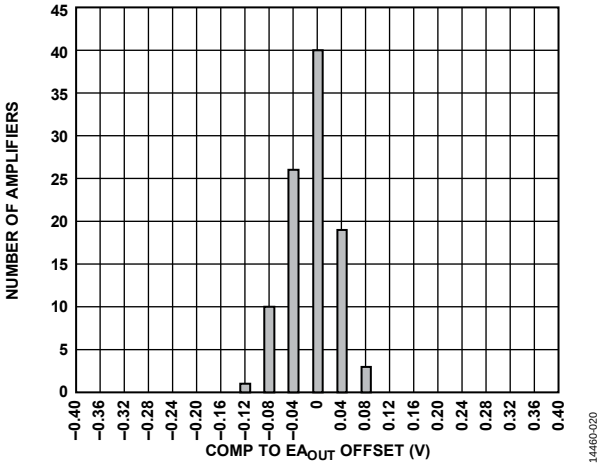

Figure 20. COMP to EA_{OUT} Offset Distribution at 125°C

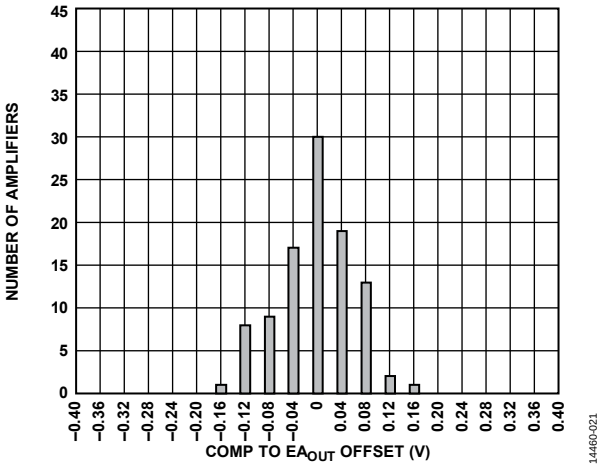

Figure 21. COMP to EA_{OUT} Offset Distribution at −55°C

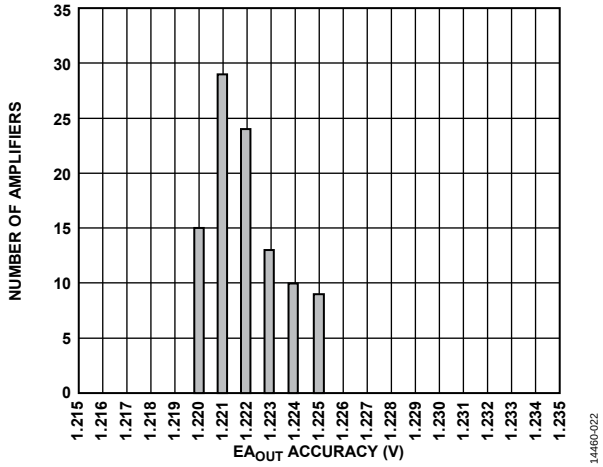

Figure 22. EA_{OUT} Accuracy Distribution at 25°C

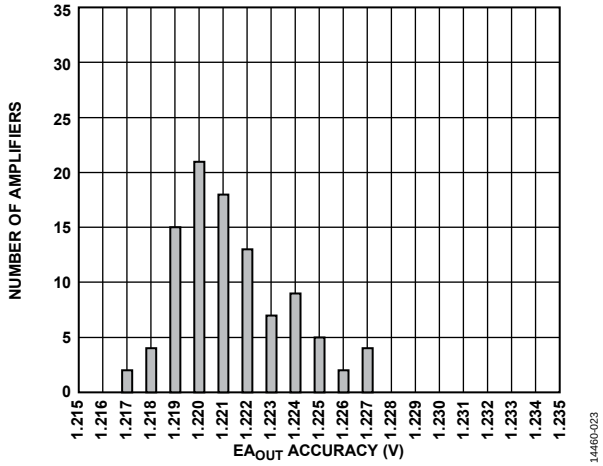

Figure 23. EA_{OUT} Accuracy Distribution at 125°C

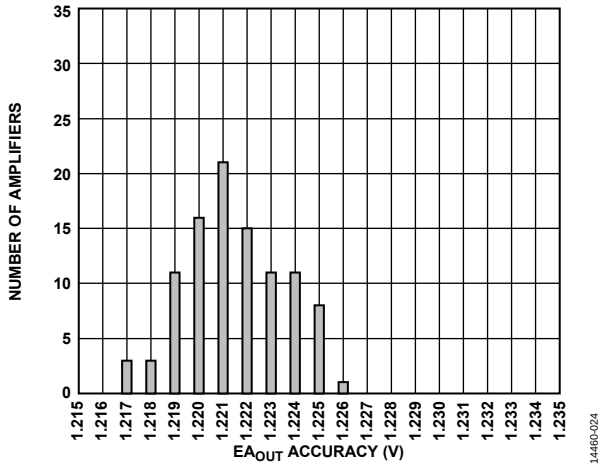

Figure 24. EA_{OUT} Accuracy Distribution at −55°C

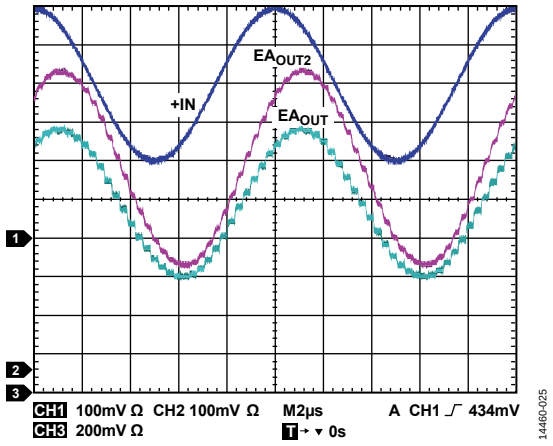

Figure 25. Output 100 kHz Signal with Test Circuit 3, Channel 1 = +IN, Channel 2 = EA_{OUT}, Channel 3 = EA_{OUT2}

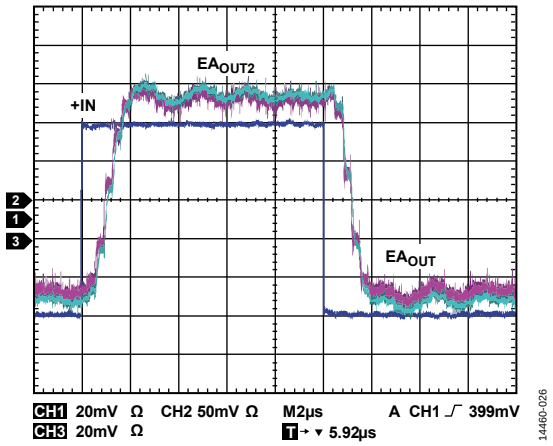

Figure 26. Output Square Wave Response with Test Circuit 3, Channel 1 = +IN, Channel 2 = EA_{OUT}, Channel 3 = EA_{OUT2}

TEST CIRCUITS

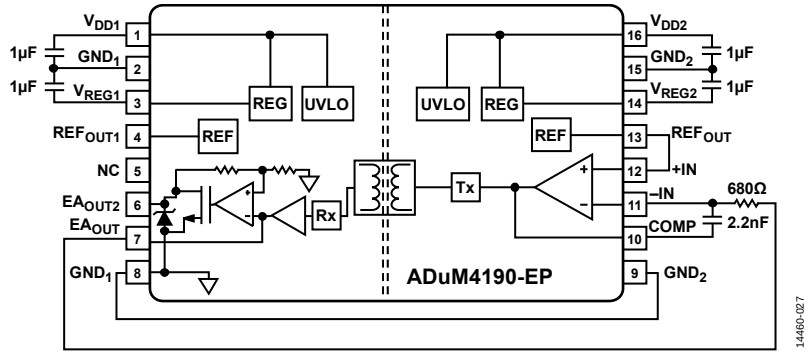

Figure 27. Accuracy Circuit Using EA_{OUT}

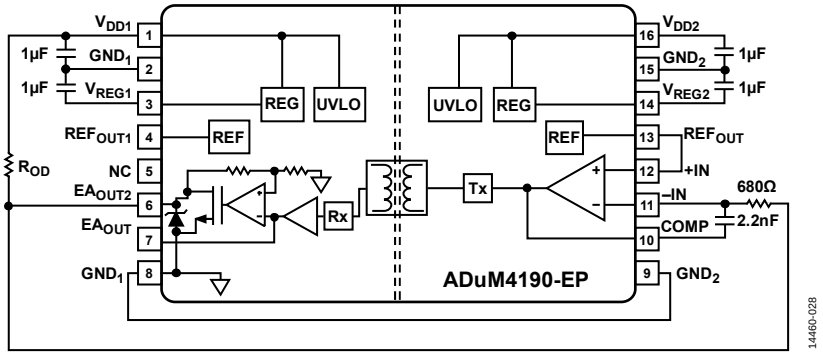

Figure 28. Accuracy Circuit Using EA_{OUT2}

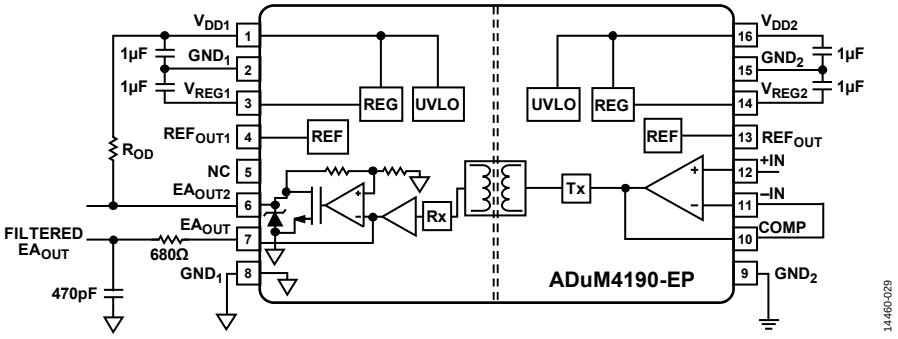

Figure 29. Isolated Amplifier Circuit

OUTLINE DIMENSIONS

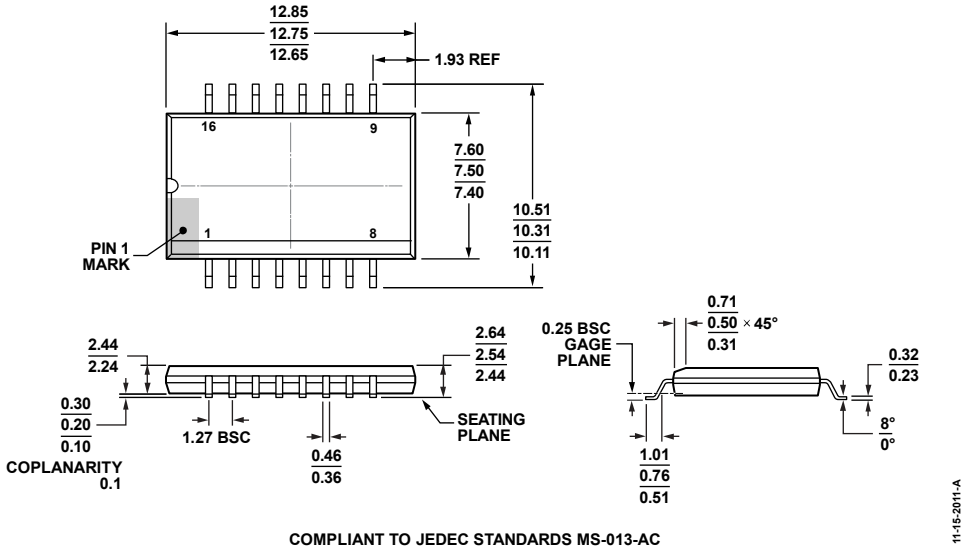

Figure 30. 16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-16-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Typical Bandwidth (kHz)	Package Description	Package Option
ADuM4190TRIZ-EP	−55°C to +125°C	400	16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-16-2
ADuM4190TRIZ-EP-RL	−55°C to +125°C	400	16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-16-2

[1] Z = RoHS Compliant Part.

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