ADSP-21369 EZ-KIT Lite®
Evaluation System Manual

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Analog Devices, Inc.
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ANALOG DEVICES

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Regulatory Compliance

The ADSP-21369 EZ-KIT Lite is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADSP-21369 EZ-KIT Lite has been certified to comply with the essential requirements of the European EMC directive 2004/108/EC and therefore carries the "**CE**" mark.

The ADSP-21369 EZ-KIT Lite has been appended to Analog Devices, Inc. EMC Technical File (EMC TF) referenced **DSPTOOLS1**, issue 2 dated June 4, 2008 and was declared CE compliant by an appointed Notified Body (No.0673) as listed below.

Notified Body Statement of Compliance: Z600ANA1.025

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The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

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PREFACE

Thank you for purchasing the ADSP-21369 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for SHARC® processors.

SHARC processors are based on a 32-bit super Harvard architecture that includes a unique memory architecture comprised of two large on-chip, dual-ported SRAM blocks coupled with a sophisticated I/O processor, which gives a SHARC processor the bandwidth for sustained high-speed computations. SHARC processors represents today's de facto standard for floating-point processing, targeted toward premium audio applications.

The evaluation system is designed to be used in conjunction with the CrossCore® Embedded Studio (CCES) and VisualDSP++® development environments to test capabilities of the ADSP-21369 SHARC processors. The development environment aids advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-21369 assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-21369 processor from a personal computer (PC) is achieved through a USB port or an external JTAG emulator. The USB interface provides unrestricted access to the ADSP-21369 processor and

evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to http://www.analog.com/dsp/tools.

The ADSP-21369 EZ-KIT Lite provides example programs to demonstrate the product capabilities.

Product Overview

The board features:

- Analog Devices ADSP-21369 SHARC processor
  - 256-pin SBGA package
  - 400 MHz core clock speed
- Synchronous dynamic random access memory (SDRAM)
  - 1M x 32-bit x 4 banks
- Synchronous random access memory (SRAM)
  - 512K bit x 8-bit
- Flash memory
  - 1M x 8-bit
- Serial peripheral interface (SPI) flash memory
  - 2M bit

- Analog audio interface
    - AD1835A codec
    - 4 x 2 RCA phono jack for 4 channels of stereo output
    - 2 x 1 RCA phono jack for 1 channel of stereo input
    - 3.5 mm headphone jack for 1 channel stereo output
- Digital audio interface
    - RCA phono jack output
    - RCA phono jack input
- Universal asynchronous receiver/transmitter (UART)
    - ADM3202 RS-232 driver/receiver
    - DB9 female connector
- National Instruments Educational Laboratory Virtual Instrumentation Suite (ELVIS) Interface
    - LabVIEW™-based virtual instruments
    - Multifunction data acquisition device
    - Bench-top workstation and prototype board
- LEDs
    - Eleven LEDs: one power (green), one board reset (red), one USB monitor (amber), and eight general-purpose (amber)

- Push buttons
    - Five push buttons: one reset, two connected to DAI, and two connected to the FLAG pins of the processor
- Expansion interface (Type A)
    - Parallel port, FLAG pins, DPI, DAI
- Other features
    - JTAG ICE 14-pin header
    - Test points for processor current measurement
    - DPI header
    - DAI header

Please visit www.analog.com/21369EZkit for additional information, including CCES support.

The EZ-KIT Lite board has a total of 1 MB of parallel flash memory and 2M bit of SPI flash memory. Flash memories can store user-specific boot code and allow the board to run as a stand-alone unit. For more information, see "External Memory" on page 1-11 and "Boot Mode and Clock Ratio Select Switch (SW2)" on page 2-10. The board also has 512 KB of SRAM and 16 MB of SDRAM, which can be used at runtime.

The DAI port of the processor is connected to the AD1835A audio codec, Sony/Philips Digital Interface (S/PDIF), and an external phase lock loop (PLL). The DAI interface facilitates development of digital and analog audio signal-processing applications. See "Analog Audio" on page 1-14 and "S/PDIF Coax Connectors (J7 and J8)" on page 2-24 for more information.

The DPI port of the processor is connected to the UART and SPI interfaces. The UART interface can connect to a standard RS-232 connector, while the SPI connects to 2M bit of serial flash memory.

Additionally, the EZ-KIT Lite board provides access to all of the processor's peripheral ports. Access is provided in the form of a three-connector expansion interface. See "Expansion Interface" on page 2-7 for details.

Purpose of This Manual

The *ADSP-21369 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-21369 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided for reference.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set.

Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts that describe your target architecture. For the locations of these documents, see "Related Documents".

Programmers who are unfamiliar with CCES or VisualDSP++ should refer to the online help and user's manuals.

Manual Contents

The manual consists of:

- Chapter 1, "Using the ADSP-21369 EZ-KIT Lite" on page 1-1
  Describes EZ-KIT Lite operation from a programmer's perspective and provides an easy-to-access memory map.
- Chapter 2, "ADSP-21369 EZ-KIT Lite Hardware Reference" on page 2-1
  Provides information on the EZ-KIT Lite hardware components
- Appendix A, "ADSP-21369 EZ-KIT Lite Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, "ADSP-21369 EZ-KIT Lite Schematic" on page B-1
  Provides the resources to allow board-level debugging or to use as a reference guide. Appendix B is part of the online help.

What's New in This Manual

This is revision 2.4 of the *ADSP-21369 EZ-KIT Lite Evaluation System Manual*. The manual has been updated to include CCES information. Additional changes include the following.

- Updated Bill of Materials, Appendix A, "ADSP-21369 EZ-KIT Lite Bill Of Materials".
- Updated ADSP-21369 EZ-KIT Lite Schematic, Appendix B, "ADSP-21369 EZ-KIT Lite Schematic".
- Modifications and corrections based on errata reports against the previous manual revision have been made.

For the latest version of this manual, please refer to the Analog Devices Web site.

Technical Support

You can reach Analog Devices processors and DSP technical support in the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:
  `http://ez.analog.com/community/dsp`
- Submit your questions to technical support directly at:
  `http://www.analog.com/support`
- E-mail your questions about processors, DSPs, and tools development software from **CrossCore Embedded Studio** or **VisualDSP++**:

  Choose **Help > Email Support**. This creates an e-mail to `processor.tools.support@analog.com` and automatically attaches your **CrossCore Embedded Studio** or **VisualDSP++** version information and `license.dat` file.
- E-mail your questions about processors and processor applications to:
  `processor.support@analog.com` or
  `processor.china@analog.com` (Greater China support)
- In the **USA only**, call **1-800-ANALOGD** (1-800-262-5643)
- Contact your Analog Devices sales office or authorized distributor. Locate one at:
  `www.analog.com/adi-sales`

- Send questions by mail to:
  Processors and DSP Technical Support
  Analog Devices, Inc.
  Three Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

The ADSP-21369 EZ-KIT Lite evaluation system supports Analog Devices ADSP-21369 SHARC processors.

Product Information

Product information can be obtained from the Analog Devices Web site and the online help system.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, myAnalog is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information

about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. myAnalog provides access to books, application notes, data sheets, code examples, and more.

Visit myAnalog (found on the Analog Devices home page) to sign up. If you are a registered user, just log on. Your user name is your e-mail address.

EngineerZone

EngineerZone is a technical support forum from Analog Devices. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

Related Documents

For additional information about the product, refer to the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-21367/ADSP-21368/ADSP-21369 SHARC Processors Data Sheet	General functional description, pinout, and timing of the processor
ADSP-2137x SHARC Processor Hardware Reference (Includes ADSP-21367, ADSP-21368, ADSP-21369, ADSP-21371, ADSP-21375)	Description of the internal processor architecture, registers, and all peripheral functions
SHARC Processor Programming Reference	Description of all allowed processor assembly instructions

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the development environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.

Example	Description
.SECTION	Commands, directives, keywords, and feature names are in text with letter gothic font.
filename	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

1 USING THE ADSP-21369 EZ-KIT LITE

This chapter provides information to assist you with development of programs for the ADSP-21369 EZ-KIT Lite evaluation system.

The information appears in the following sections.

- "Package Contents" on page 1-2
  Lists the items contained in your EZ-KIT Lite package.
- "Default Configuration" on page 1-3
  Shows the default configuration of the EZ-KIT Lite board.
- "CCES Install and Session Startup" on page 1-4
  Instructs how to start a new or open an existing EZ-KIT Lite session using CCES.
- "VisualDSP++ Install and Session Startup" on page 1-8
  Instructs how to start a new or open an existing EZ-KIT Lite session using VisualDSP++.
- "CCES Evaluation License" on page 1-10
  Describes the CCES demo license shipped with the EZ-KIT Lite.
- "VisualDSP++ Evaluation License" on page 1-11
  Describes the VisualDSP++ demo license shipped with the EZ-KIT Lite.
- "External Memory" on page 1-11
  Describes the memory map of the EZ-KIT Lite; describes how to access external memory.

- "ELVIS Interface" on page 1-13
  Describes the on-board National Instruments Educational Laboratory Virtual Instrumentation Suite (NI ELVIS) interface.
- "Analog Audio" on page 1-14
  Describes how to set up and communicate with the on-board audio codec.
- "LEDs and Push Buttons" on page 1-15
  Describes the board's general-purpose I/O pins and buttons.
- "Example Programs" on page 1-17
  Provides information about example programs included in the evaluation system.
- "Board Design Database" on page 1-17
  Highlights the available technical resources for the design, layout, fabrication, and assembly of the EZ-KIT Lite.

For information on the graphical user interface, including the boot loading, target options, and other facilities of the EZ-KIT Lite system, refer to the online help.

For detailed information on how to program the ADSP-21369 SHARC processor, refer to the documents referenced in "Related Documents".

Package Contents

Your ADSP-21369 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-21369 EZ-KIT Lite board
- Universal 7V DC power supply
- USB 2.0 cable

- 3.5 mm stereo headphones
- 6-foot RCA audio cable
- 6-foot 3.5 mm/RCA x 2 Y-cable

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-21369 EZ-KIT Lite board is designed to run outside your personal computer as a standalone unit. You do not have to open your computer case.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components. Figure 1-1 shows the default jumper settings, DIP switch, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before continuing.

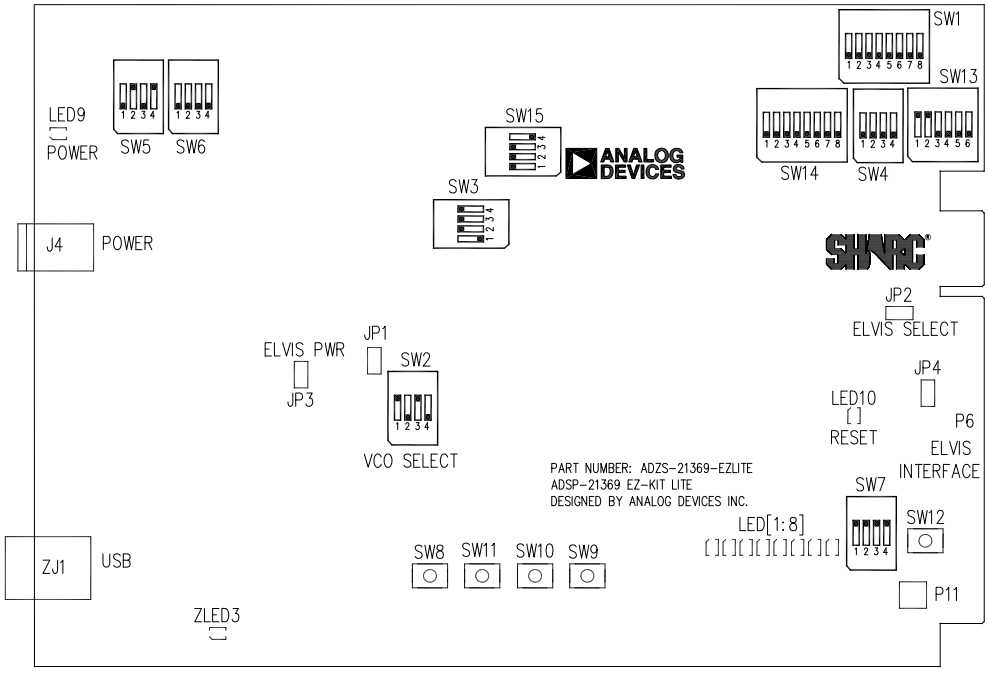

Figure 1-1. EZ-KIT Lite Hardware Setup

CCES Install and Session Startup

For information about CCES and to download the software, go to www.analog.com/CCES. A link for the ADSP-21369 EZ-KIT Lite Board Support Package (BSP) for CCES can be found at http://www.analog.com/SHARC/EZKits.

Follow these instructions to ensure correct operation of the product software and hardware.

Step 1: Connect the EZ-KIT Lite board to a personal computer (PC) running CCES using one of two options: an Analog Devices emulator or via the debug agent.

Using an Emulator:

1. Plug one side of the USB cable into the USB connector of the emulator. Plug the other side into a USB port of the PC running CCES.
2. Attach the emulator to the header connector ZP4 (labeled JTAG) on the EZ-KIT Lite board.

Using the on-board Debug Agent:

1. Plug one side of the USB cable into the USB connector of the debug agent ZP1 (labeled USB).
2. Plug the other side of the cable into a USB port of the PC running CCES.

Step 2: Attach the provided cord and appropriate plug to the 5V power adaptor.

1. Plug the jack-end of the power adaptor into the power connector J4 (labeled 7.5V) on the EZ-KIT Lite board.
2. Plug the other side of the power adaptor into a power outlet. The power LED (labeled LED9) is lit green when power is applied to the board.
3. Power the emulator (if used). Plug the jack-end of the assembled power adaptor into the emulator and plug the other side of the power adaptor into a power outlet. The enable/power indicator is lit green when power is applied.

Step 3 (if connected through the debug agent): Verify that the yellow USB monitor LED (labeled ZLED3)and the green power LED (labeled ZLED4) on the debug agent are both on. This signifies that the board is communicating properly with the host PC and ready to run CCES.

Session Startup

It is assumed that the CrossCore Embedded Studio software is installed and running on your PC.

Note: If you connect the board or emulator first (before installing CCES) to the PC, the Windows driver wizard may not find the board drivers.

1. Navigate to the CCES environment via the **Start** menu.

   Note that CCES is not connected to the target board.

2. Use the system configuration utility to connect to the EZ-KIT Lite board.

   If a debug configuration exists already, select the appropriate configuration and click **Apply and Debug** or **Debug**. Go to step 8.

   To create a debug configuration, do one of the following:

   - Click the down arrow next to the little bug icon, select **Debug Configurations**
   - Choose **Run > Debug Configurations**.

   The **Debug Configuration** dialog box appears.

3. Select **CrossCore Embedded Studio Application** and click  (**New launch configuration**).

   The **Select Processor** page of the **Session Wizard** appears.

4. Ensure **Blackfin** is selected in **Processor family**. In **Processor type**, select **ADSP-21369**. Click **Next**.

   The **Select Connection Type** page of the **Session Wizard** appears.

5. Select one of the following:
   - For standalone debug agent connections, **EZ-KIT Lite** and click **Next**.
   - For emulator connections, **Emulator** and click **Next**.

   The **Select Platform** page of the **Session Wizard** appears.
6. Do one of the following:
   - For standalone debug agent connections, ensure that the selected platform is **ADSP-21369 EZ-KIT** Lite via Debug Agent.
   - For emulator connections, choose the type of emulator that is connected to the board.
7. Click **Finish** to close the wizard.

   The new debug configuration is created and added to the program(s) to load list.
8. In the **Program(s) to load** section, choose the program to load when connecting to the board. If not loading any program upon connection to the target, do not make any changes.

   Note that while connected to the target, there is no way to choose a program to download. To load a program once connected, terminate the session.

To delete a configuration, go to the **Debug Configurations** dialog box and select the configuration to delete. Click ✖ and choose **Yes** when asked if you wish to delete the selected launch configuration. Then **Close** the dialog box.

To disconnect from the target board, click the terminate button (red box) or choose **Run > Terminate**.

To delete a session, choose **Target > Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

VisualDSP++ Install and Session Startup

For information about VisualDSP++ and to download the software, go to www.analog.com/VisualDSP.

1. Plug the provided power supply into J4 on the EZ-KIT Lite board. Visually verify that the green power LED (LED9) is on.
2. Verify that the red reset LED (LED10) goes on for a moment and then goes off, and, finally, LED1 through LED8 are sequentially blinking.
3. Connect one end of the USB cable to an available full speed USB port on your PC and the other end to ZJ1 on the ADSP-21369 EZ-KIT Lite board.
4. Verify that the yellow USB monitor LED (ZLED3, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.

Session Startup

1. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the **Start > Programs** menu. The main window appears. Note that VisualDSP++ does not connect to any session. Skip the rest of this step to step 2.

   If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and

force VisualDSP++ to start a new session by pressing and holding down the **Ctrl** key while starting VisualDSP++. Do not release the **Ctrl** key until the **Session Wizard** appears on the screen. Go to step 3.

2. To connect to a new EZ-KIT Lite session, start **Session Wizard** by selecting one of the following.
   - From the **Session** menu, **New Session**.
   - From the **Session** menu, **Session List**. Then click **New Session** from the **Session List** dialog box.
   - From the **Session** menu, **Connect to Target**.
3. The **Select Processor** page of the wizard appears on the screen. Ensure **SHARC** is selected in **Processor family**. In **Choose a target processor**, select **ADSP-21369**. Click **Next**.
4. The **Select Connection Type** page of the wizard appears on the screen. Select **EZ-KIT Lite** and click **Next**.
5. The **Select Platform** page of the wizard appears on the screen. Ensure that the selected platform is **ADSP-21369 EZ-KIT Lite via Debug Agent**. Specify your own **Session name** for your session or accept the default name.

   The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and open a new session.

   Click **Next**.

6. The **Finish** page of the wizard appears on the screen. The page displays your selections. Check the selections. If you are not satisfied, click **Back** to make changes; otherwise, click **Finish**. VisualDSP++ creates the new session and connects to the EZ-KIT Lite. Once connected, the main window's title is changed to include the session name set in step 5.

To disconnect from a session, click the disconnect button  or select **Session > Disconnect from Target**.

To delete a session, select **Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

CCES Evaluation License

The ADSP-21369 EZ-KIT Lite software is part of the Board Support Package (BSP) for the SHARC ADSP-2136x family. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for 90 days after activation. Once the evaluation period ends, the evaluation license becomes permanently disabled. If the evaluation license is installed but not activated, it allows 10 days of unrestricted use and then becomes disabled. The license can be re-enabled by activation.

An evaluation license can be upgraded to a full license. Licenses can be purchased from:

- Analog Devices directly. Call (800) 262-5645 or 781-937-2384 or go to:
  http://www.analog.com/buyonline.
- Analog Devices, Inc. local sales office or authorized distributor. To locate one, go to:
  http://www.analog.com/salesdir/continent.asp.

The EZ-KIT Lite hardware must be connected and powered up to use CCES with a valid evaluation or full license.

VisualDSP++ Evaluation License

The ADSP-21369 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

1. VisualDSP++ allows a connection to the ADSP-21369 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.
2. The linker restricts a user program to 7281 words of memory for code space with no restrictions for data space.

To avoid errors when opening VisualDSP++, the EZ-KIT Lite hardware must be connected and powered up. This is true for using VisualDSP++ with a valid evaluation or full license.

External Memory

The EZ-KIT Lite contains four types of memory: parallel flash (1 MB), SPI flash (2M bit), SRAM (512K bit), and SDRAM (128M bit). Flash memories can store user-specific boot code and allow the board to run as a stand-alone unit. For more information on how to select a boot device for the processor, see "Boot Mode and Clock Ratio Select Switch (SW2)" on page 2-10.

Table 1-1 provides start and end addresses of the on-board external memories.

Table 1-1. EZ-KIT Lite Evaluation Board External Memory

Start Address	End Address	Content
0x0020 0000	0x0027 FFFF	SRAM memory ($\overline{\text{MS0}}$)
0x0400 0000	0x040F FFFF	Flash memory ($\overline{\text{MS1}}$)
0x0800 0000	0x083F 0000	SDRAM memory ($\overline{\text{MS2}}$)
0x0C00 0000 0x0C00 0000	0x0CFF FFFF 0x0FFF FFFF	Unused chip select ($\overline{\text{MS3}}$) for non-SDRAM addresses Unused chip select ($\overline{\text{MS3}}$) for SDRAM addresses

Parallel flash memory, SDRAM, and SRAM are connected to the external memory of the processor. To access SRAM and flash memories, use memory addressing via the respective memory bank or use the DMA controller.

SDRAM memory is connected to the SDRAM controller of the processor. A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory accesses. Care must be taken when configuring the SDRAM control registers. For more information regarding the setup of the SDRAM controller, refer to the *ADSP-2137x SHARC Processor Hardware Reference (Includes ADSP-21367, ADSP-21368, ADSP-21369, ADSP-21371, ADSP-21375)*.

An example program is included in the EZ-KIT Lite installation directory to demonstrate the controller setup.

SPI flash memory is connected to the SPI port of the processor; SPI flash designates:

- DPI pin 5 (DPI5) as a chip select
- DPI pin 3 (DPI3) as the SPI clock

- DPI pin 1 (DPI1) as the MOSI
- DPI pin 2 (DPI2) as the MISO

By default, the DPI is set up for the SPI flash, and any required changes to the SPI flash can be made by modifying the DPI of the processor. An example program is included in the EZ-KIT Lite installation directory to demonstrate the SPI flash memory reads and writes.

Asynchronous SRAM memory and parallel flash memory are connected to the asynchronous memory controller of the processor. Each of their respective memory banks can be programmed independently with different timing parameters. For more information on changing wait states to speed up or slow down the asynchronous controller and other setup information, refer to the *ADSP-2137x SHARC Processor Hardware Reference (Includes ADSP-21367, ADSP-21368, ADSP-21369, ADSP-21371, ADSP-21375)*.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate flash memory reads and writes.

ELVIS Interface

The ADSP-21369 EZ-KIT Lite board contains the National Instruments Educational Laboratory Virtual Instrumentation Suite interface. The interface features the DC voltage and current measurement modules, oscilloscope and bode analyzer modules, function generator, arbitrary waveform generator, and digital I/O.

The ELVIS interface is a LabVIEW-based design and prototype environment for university science and engineering laboratories. The ELVIS interface consists of LabVIEW-based virtual instruments, a multifunction data acquisition (DAQ) device, and a custom-designed bench-top workstation and prototype board. This combination provides a ready-to-use suite of instruments found in most educational laboratories. Because the

interface is based on LabVIEW and provides complete data acquisition and prototyping capabilities, the system is ideal for academic coursework that range from lower-division classes to advanced project-based curriculums.

For more information on ELVIS and example demonstration programs, visit National Instruments Web site at www.ni.com.

Analog Audio

The AD1835A device is a high-performance, single-chip codec featuring four stereo digital-to-analog converters (DACs) for audio output and one stereo analog-to-digital converters (ADCs) for audio input. The codec can input and output data with a sample rate of up to 96 kHz on all channels. A 192 kHz sample rate can be used with one of the DAC channels.

The processor is interfaced with the AD1835A codec via the DAI port. The DAI pins can be configured to transfer serial data from the codec in either time-division multiplexed (TDM) or 2-wire interface mode (TWI). For more information on the AD1835A connection to the DAI, see "DAI Interface" on page 2-4.

The master input clock (MCLK) for the AD1835A codec can be generated by the on-board 12.288 MHz oscillator or supplied by one of the DAI pins of the processor. Using a DAI pin to generate the MCLK, as opposed to the on-board oscillator, allows synchronization of multiple devices in the system. This is done on the EZ-KIT Lite when data is coming from the Sony/Philips Digital Interface (S/PDIF) receiver and being output through the codec. The S/PDIF MCLK is routed to the AD1835A's MCLK in the processor's signal routing unit (SRU). It is possible to disable the on-board audio oscillator from driving the audio codec and the processor's input pin. For instructions on how to configure the clock, refer to "Codec Setup Switch (SW3)" on page 2-11.

The AD1835A codec can be configured as a master or a slave, depending on the DIP switch settings. In master mode, the codec drives the serial port clock and frame sync signals to the processor. In slave mode, the processor must generate and drive all of the serial port clock and frame sync signals. For more information, refer to "Codec Setup Switch (SW3)" on page 2-11.

The internal configuration registers of the codec are configured using the SPI port of the processor. The DPI pin 4 (DPI4 register) is used as the select for the device. For information on how to configure the multichannel codec, refer to the product data sheet at www.analog.com/AD1835A.

The RCA connector (J10) is used to input analog audio. When using an electret microphone on this connector, configure switch SW4 according to the instructions in "Electret Microphone Select Switch (SW4)" on page 2-12. The four output channels connect to the RCA connector (J5). Channel 4 of the codec connects to the headphone jack (J9). For more information, see "Connectors" on page 2-21.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate how to configure and use the board's analog audio interface.

LEDs and Push Buttons

The EZ-KIT Lite has eight general-purpose user LEDs and four general-purpose push buttons.

Two general-purpose push buttons are attached to the FLAG pins of the processor, while the other two are attached to the DAI pins. All of the push buttons are connected to the processor through a DIP switch (SW7). The DIP switch can disconnect the processor pins connected to the push buttons. See "Push Button Enable Switch (SW7)" on page 2-13 for

instructions on how to disable a push button from driving its corresponding processor pin.

The state of the push buttons connected to the FLAG pins can be determined by reading the FLAG register. The push buttons connected to the DAI pins must be configured as interrupts. It is necessary to set up an interrupt routine to determine each pin's state. Table 1-2 shows the push button and processor connections. Refer to the related example program shipped with the EZ-KIT Lite for more information.

Table 1-2. Push Button Connections

Push Button Label	Push Button Reference Designator	Processor Pin
PB1	SW8	FLAG1/$\overline{\text{IRQ1}}$
PB2	SW11	FLAG0/$\overline{\text{IRQ0}}$
PB3	SW10	DAI19
PB4	SW9	DAI20

Table 1-3 summarizes the LED connections to the processor. To use the LEDs connected to the DAI or DPI pins, configure the respective registers of the processor. For more information, refer to the *ADSP-2137x SHARC Processor Hardware Reference (Includes ADSP-21367, ADSP-21368, ADSP-21369, ADSP-21371, ADSP-21375)*.

Table 1-3. LED Connections

LED Reference Designator	Processor Pin
LED1	DPI6
LED2	DPI7
LED3	DPI8
LED4	DPI13
LED5	DPI14
LED6	DAI15

Table 1-3. LED Connections (Cont'd)

LED Reference Designator	Processor Pin
LED7	DAI16
LED8	FLAG3/TMREXP/$\overline{\text{MS3}}$

An example program is included in the EZ-KIT Lite installation directory to demonstrate functionality of the LEDs and push buttons.

Example Programs

Example programs are provided with the ADSP-21369 EZ-KIT Lite to demonstrate various capabilities of the product. The programs are included in the product installation kit and can be found in the `Examples` folder of the installation. Refer to a readme file provided with each example for more information.

CCES users are encouraged to use the example browser to find examples included with the EZ-KIT Lite Board Support Package.

Board Design Database

A `.zip` file containing all of the electronic information required for the design, layout, fabrication and assembly of the product is available for download from the Analog Devices board design database at: `http://www.analog.com/sharc-board-design-database`.

2 ADSP-21369 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-21369 EZ-KIT Lite board.

The following topics are covered.

- "System Architecture" on page 2-2
  Describes the ADSP-21369 board configuration and explains how the board components interface with the processor.
- "Switches" on page 2-9
  Shows the locations and describes the on-board switches.
- "LEDs and Push Buttons" on page 2-15
  Shows the locations and describes the on-board LEDs and push buttons.
- "Jumpers" on page 2-18
  Shows the locations and describes the on-board configuration jumpers.
- "Connectors" on page 2-21
  Shows the locations and provides part numbers for the on-board connectors. In addition, the manufacturer and part number information is provided for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board (Figure 2-1).

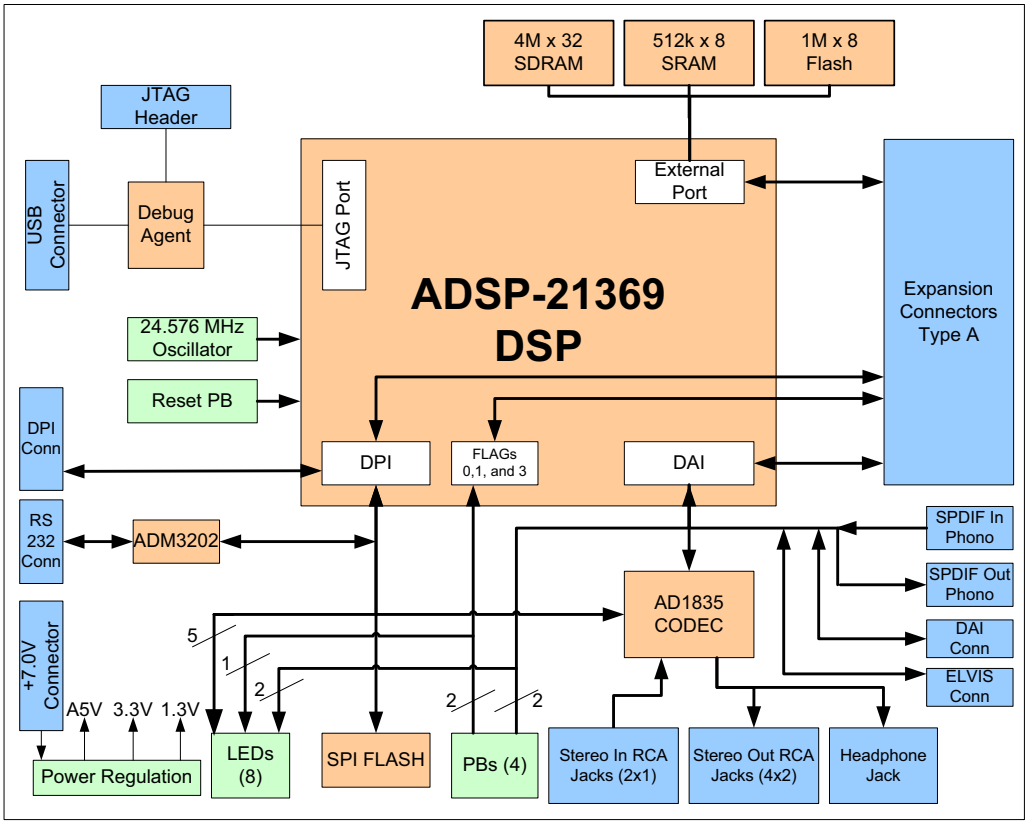

Figure 2-1. System Architecture Block Diagram

The EZ-KIT Lite is designed to demonstrate the ADSP-21369 processor capabilities. The processor core is powered at 1.3V, and the I/O is powered at 3.3V.

The CLKIN pin of the processor connects to a 24.576 MHz oscillator. The core frequency of the processor is derived by multiplying the frequency at the CLKIN pin by a value determined by the state of the processor pins CLKCFG1 and CLKCFG0. The value at these pins is determined by the state of switch SW2 state (see "Boot Mode and Clock Ratio Select Switch (SW2)" on page 2-10). By default, the EZ-KIT Lite provides a core frequency of 393.216 MHz. It is possible to change the speed of the processor by changing the value of the PMCTL register.

The SW2 switch also configures the boot mode of the processor. The EZ-KIT Lite is capable of EPROM/flash boot and SPI boot. By default, the EZ-KIT Lite boots from flash memory. For details, see "Boot Mode and Clock Ratio Select Switch (SW2)" on page 2-10.

External Port

The external port of the ADSP-21369 processor consists of a 24-bit address bus, 32-bit data memory bus, and control lines. The control lines are used to select, read, and write to external memory devices.

The external port connects to an 8-bit parallel flash memory, an 8-bit SRAM memory, and a 32-bit SDRAM memory. See "External Memory" on page 1-11 for more information about accessing flash memory and SDRAM memory.

All of the external port signals are available externally via the expansion interface connectors (J1–3). The pinout of the connectors can be found in "ADSP-21369 EZ-KIT Lite Schematic" on page B-1.

DAI Interface

The digital application interface (DAI) pins are connected to the signal routing unit (SRU) of the processor. The SRU is a flexible routing system, providing a large system of signal flows within the processor. In general, the SRU allows to route the DAI pins to different internal peripherals in various combinations.

The DAI pins are connected to the AD1835A audio codec, a 26-pin header, two RCA connectors, audio oscillator output, an external phase lock loop (PLL) circuit, two LEDs, and two push buttons. Figure 2-2 illustrates the EZ-KIT Lite's connections to the DAI.

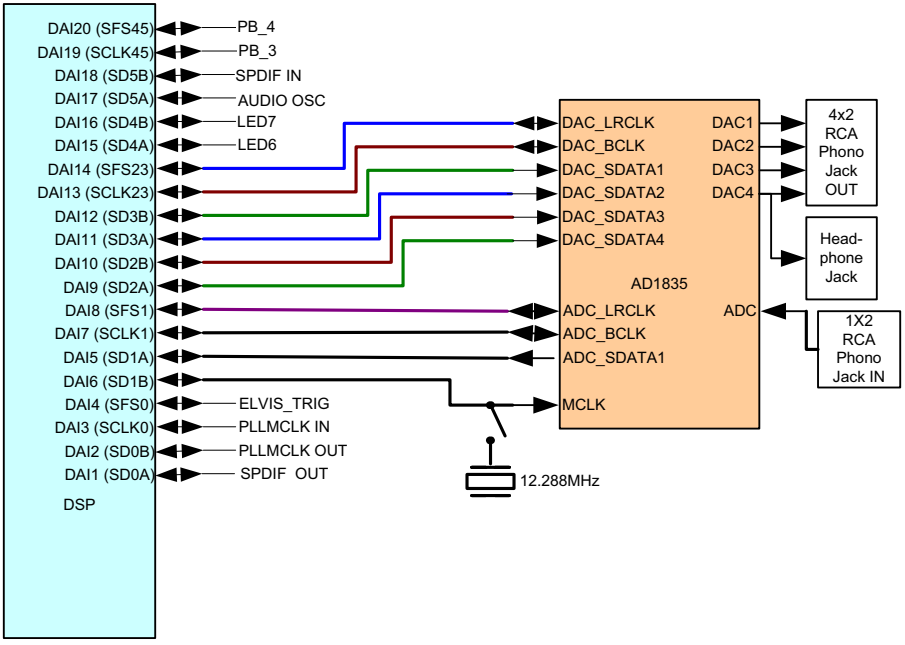

Figure 2-2. DAI Connections Block Diagram

To use the DAI for a different purpose, disable any signal driving the DAI pin with a switch (see "Codec Setup Switch (SW3)" on page 2-11). In addition, SW3 enables flexible routing of the 12.288 MHz audio oscillator's output signal. By default, the SW3 signal is used as the master clock (MCLK) for the AD1835A codec.

All of the DAI signals are available externally via the expansion interface connectors (J1–3) and 0.1" spaced header (P4). The pinout of the connectors can be found in "ADSP-21369 EZ-KIT Lite Schematic" on page B-1.

DPI Interface

The digital peripheral interface (DPI) pins are connected to a second signal routing unit of the processor (SRU2). The SRU2 unit, similar to the SRU, is a flexible routing system, providing a large system of signal flows within the processor. In general, the SRU2 can route the DPI pins to different internal peripherals in various combinations.

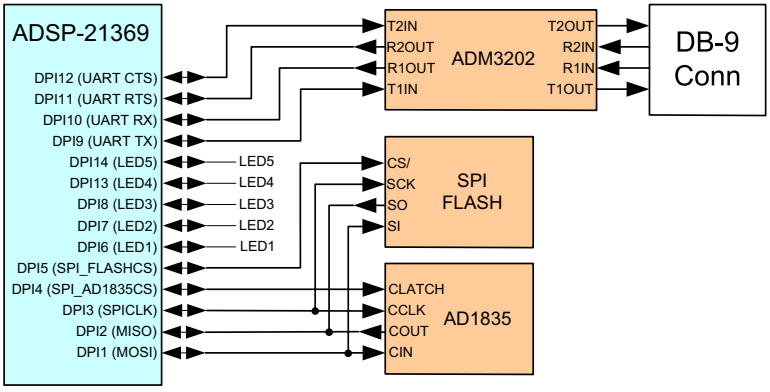

Figure 2-3. DPI Connections Block Diagram

The DPI pins are connected to the SPI flash memory, SPI of the AD1835A codec, a UART, a 20-pin header, and five LEDs. Figure 2-3 illustrates the EZ-KIT Lite's connections to the DPI.

To use the DPI for a different purpose, disable any signal driving a DPI pin with a switch (see "UART Enable Switch (SW5)" on page 2-12). Any DPI pin connected to a LED can be used without having to disconnect the pin. You can, however, see the respective LED turn ON and OFF when the signal is used elsewhere on the board.

All of the DPI signals are available externally via the expansion interface connectors (J1–3) and 0.1" spaced header (P3). The pinout of the connectors can be found in "ADSP-21369 EZ-KIT Lite Schematic" on page B-1.

FLAG Pins

The processor has four general-purpose I/O flag pins. Table 2-1 describes the flag pin connections.

Table 2-1. I/O FLAG Pins

Processor FLAG Pin	EZ-KIT Lite Function
FLAG0	Push button (SW2) input
FLAG1	Push button (SW2) input
FLAG2	SDRAM chip select
FLAG3	LED8

For information on how to disable a push button from driving its corresponding flag pin, see "Push Button Enable Switch (SW7)" on page 2-13.

The FLAG signals are available externally via the expansion interface connectors (J1–3). The pinout of the connectors can be found in "ADSP-21369 EZ-KIT Lite Schematic" on page B-1.

External PLL

The ADSP-21369 EZ-KIT Lite contains an external phase lock loop to help generate a faster and more stable master input clock, MCLK. The PLL uses DAI pin 3 as an input clock from the ADSP-21369 processor. The new clock generated by PLL connects to the processor via DAI pin 2.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate how to configure and use the board's external PLL.

Expansion Interface

The expansion interface consists of three 90-pin connectors. Table 2-2 shows the interfaces each connector provides. For the exact pinout of the connectors, refer to "ADSP-21369 EZ-KIT Lite Schematic" on page B-1. The mechanical dimensions of the connectors can be obtained from Technical Support.

Table 2-2. Expansion Interface Connectors

Connector	Interfaces
J1	5V, ADDR23-0, DATA31-0
J2	3.3V, FLAG3-0, DAIP20-1, DPI14-1, SDRAM control signals
J3	5V, 3.3V, reset, parallel port control signals

Limits to the current and interface speed must be taken into consideration when using the expansion interface. The maximum current limit is dependent on the capabilities of the used regulator. Additional circuitry also can add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the internal and external memory of the processor through a 6-pin interface. The JTAG emulation port of the processor also connects to the USB debugging interface. When an emulator connects to the board at ZP4, the USB debugging interface is disabled. This is not a standard connection of the JTAG interface.

For information about the standard connection of the interface, see *EE-68* published on the Analog Devices Web site. For more information about the JTAG connector, see "JTAG Header (ZP4)" on page 2-25. To learn more about available SHARC emulators, go to http://www.analog.com/processors/tools/sharc.

Switches

This section describes operation of the on-board switches. The switch locations and default settings are shown in Figure 2-4.

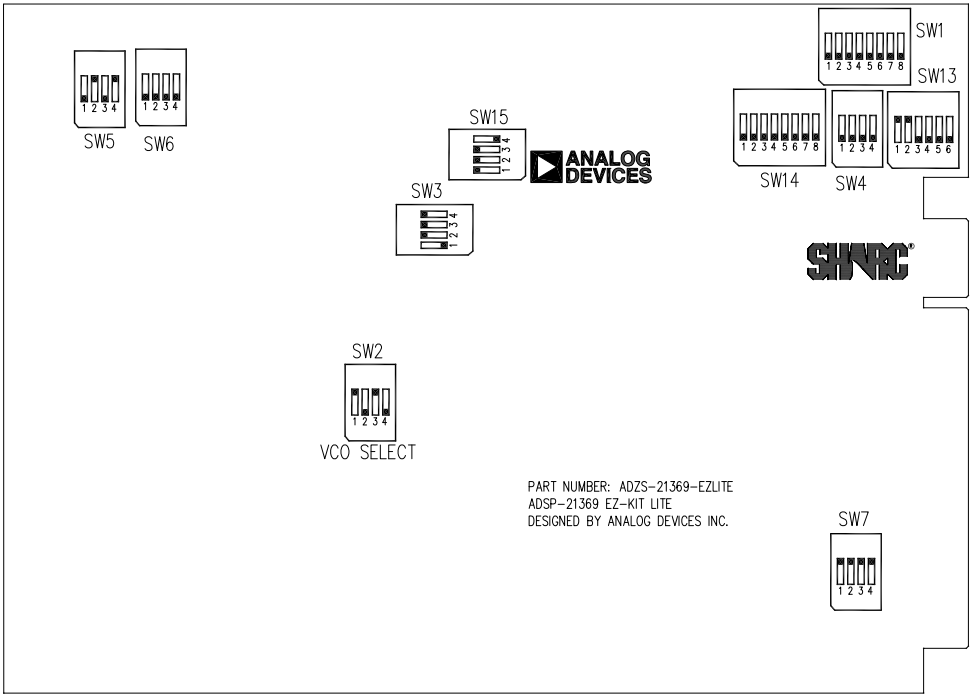

Figure 2-4. Switch Locations and Default Settings

Boot Mode and Clock Ratio Select Switch (SW2)

The SW2 switch sets the boot mode and clock multiplier ratio of the processor. Table 2-3 shows how to set up the boot mode using SW2 positions 1 and 2. By default, the EZ-KIT Lite boots in external port mode from flash memory.

Table 2-3. Boot Mode Configuration Switch (SW2)

BOOTCFG0 Pin (Position 1)	BOOTCFG1 Pin (Position 2)	Boot Mode
ON	ON	SPI slave boot
ON	**OFF**	**Parallel flash boot (default)**
OFF	ON	SPI master boot
OFF	OFF	Reserved

Table 2-4 shows how to set up the clock multiply ratio using SW2 positions 3 and 4. By default, the processor increases the clock multiply ratio by sixteen, setting the core clock to 393.216 MHz.

Table 2-4. Core Clock Rate Configuration

CLKCFG0 (Position 3)	CLKCFG1 (Position 4)	Core to CLKIN Ratio
ON	ON	6:1
ON	**OFF**	**16:1 (default)**
OFF	ON	32:1
OFF	OFF	Reserved

The core clock frequency can be increased or decreased via software by writing to the PMCTL register. For more information on changing the core clock frequency and other setup information, refer to the *ADSP-2137x SHARC Processor Hardware Reference (Includes ADSP-21367, ADSP-21368, ADSP-21369, ADSP-21371, ADSP-21375)*.

Codec Setup Switch (SW3)

The codec setup switch (SW3) can be used to change the routing of some signals going to the AD1835A codec and to set up the communication protocol of the codec.

SW3 positions 1 and 2 determine the clock routing for the audio oscillator to the codec and to the processor. Figure 2-5 illustrates how the switch positions 1 and 2 connect on the board. In the default position, route the DAI_P17 pin to DAI_P6 (in software) to clock the AD1835A codec.

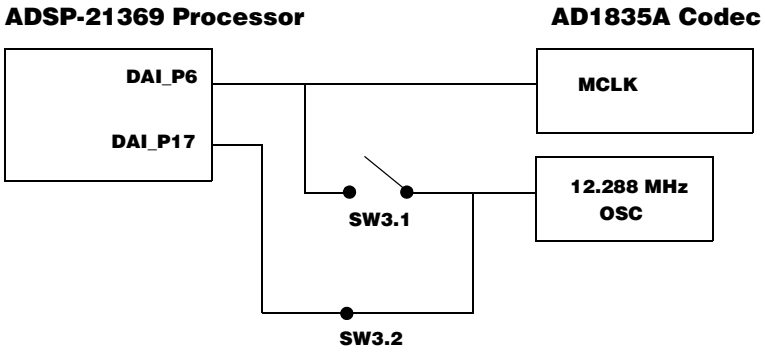

Figure 2-5. Audio Clock Routing

SW3 position 3 determines if the AD1835A device is a master or a slave. If the AD1835A is a master, the device's serial interface generates the frame sync and clock signals necessary to transfer data. When the device is a slave, the processor must generate the frame sync and clock signals. By default, position 3 is ON, and the AD1835A codec generates the control signals.

SW3 position 4 disconnects the AD1835A codec's ADC_DATA pin from the DAI. This is useful when the DAI is connected to another device.

Electret Microphone Select Switch (SW4)

To connect an electret microphone to audio input, place all positions of SW4 ON. The default switch position is all OFF. When SW4 is all ON, a DC offset of 2.5V is added to the signal, and gain of the input amplifiers is changed from 1x to 10x.

UART Enable Switch (SW5)

The UART enable switch (SW5) disconnects the UART signals from the DPI pins of the processor. When SW5 is OFF, its associated DPI signal (see Table 2-5) can be used on the expansion interface.

Table 2-5. UART Enable Switch (SW5)

Switch Position	EZ-KIT Lite Signal	Processor Signal
1 (**OFF**[1])	CTS	DPI12
2 (**ON**)	RX	DPI10
3 (**OFF**)	RTS	DPI11
4 (**ON**)	T2IN tied to R2OUT	N/A

1 Bold typeface denotes the default setting.

Loopback Test Switches (SW6 and SW14)

The loopback test switch (SW6) is located at the top left side of the board. The second loopback test switch, SW14, is located at the top right side of the board. These switches are used for testing only; all switch positions should remain OFF.

Push Button Enable Switch (SW7)

The push button enable switch (SW7) disconnects the push buttons from the respective processor pins. This allows the signals to be used elsewhere on the board. Table 2-6 shows switch SW7 connections. By default, all positions of SW7 are ON, and the push buttons function as designed.

Table 2-6. Push Button Enable Switch (SW7)

Switch Position	Push Button Label	Push Button Reference Designator	Processor Pin
1	PB1	SW8	FLAG1/$\overline{\text{IRQ}}$
2	PB2	SW11	FLAG0/$\overline{\text{IRQ0}}$
3	PB3	SW10	DAI19
4	PB4	SW9	DAI20

SPI Disable Switch (SW15)

The SPI interface switch (SW15) disables the SPI chip select lines connected to SPI flash memory and AD1835A audio codec. The switch allows you to re-use the same pins on the SPI interface and expansion interface. By default, SW15 positions 1–3 are ON and position 4 is OFF unless any of the SPI interface signals are used on the expansion connector or via an EZ-Extender®.

ELVIS Oscilloscope Configuration Switch (SW1)

The oscilloscope configuration switch (SW1) determines which audio circuit signals connect to channels A and B of the oscilloscope. The switch is used only when the board is connected to the Educational Laboratory Virtual Instrumentation Suite (ELVIS) station (see “ELVIS Interface” on page 1-13).

Each channel must have only one signal selected at a time, as described in Table 2-7.

Table 2-7. Oscilloscope Configuration Switch (SW1)

Channel	Switch Position	Audio Circuit Signal
A	1 (**OFF**[1])	AMP_LEFT_IN
A	2 (**OFF**)	AMP_RIGHT_IN
A	3 (**OFF**)	LEFT_OUT
A	4 (**OFF**)	RIGHT_OUT
B	5 (**OFF**)	AMP_LEFT_IN
B	6 (**OFF**)	AMP_RIGHT_IN
B	7 (**OFF**)	LEFT_OUT
B	8 (**OFF**)	RIGHT_OUT

1 Bold typeface denotes the default settings.

ELVIS Function Generator Configuration Switch (SW13)

The function generator configuration switch (SW13) controls which signals connect to the left and right input signals of the audio interface. The SW13 switch is used only when the board is connected to the ELVIS station (see "ELVIS Interface" on page 1-13). Each channel must have only one signal selected at a time, as described in Table 2-8.

Table 2-8. ELVIS Function Generator Configuration Switch (SW13)

Channel	Switch Position	Audio Signal
AMP_LEFT_IN	1 (**ON**[1])	LEFT_IN
AMP_RIGHT_IN	2 (**ON**)	RIGHT_IN
AMP_LEFT_IN	3 (**OFF**)	DAC0

Table 2-8. ELVIS Function Generator Configuration Switch (SW13) (Cont'd)

Channel	Switch Position	Audio Signal
AMP_RIGHT_IN	4 (**OFF**)	DAC1
AMP_LEFT_IN	5 (**OFF**)	FUNCT_OUT
AMP_RIGHT_IN	6 (**OFF**)	FUNCT_OUT

1 Bold typeface denotes the default settings.

LEDs and Push Buttons

This section describes the on-board LEDs and push buttons. The LED and push button locations are shown in Figure 2-6.

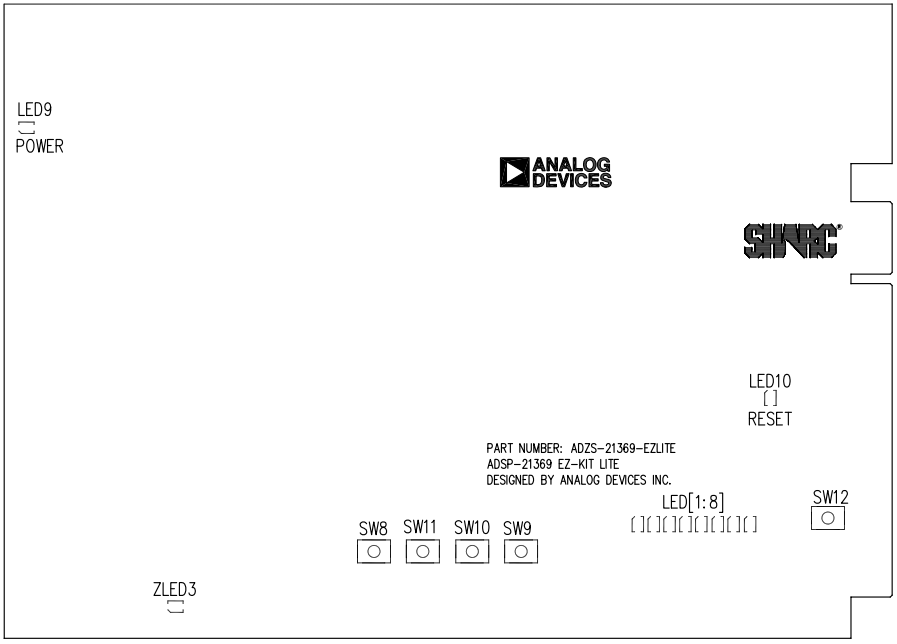

Figure 2-6. LED and Push Button Locations

General Purpose LEDs (LED1–8)

There are eight general-purpose LEDs on the board. Five LEDs are connected to the DPI interface, two LEDs are connected to the DAI interface, and one LED is connected to FLAG3 of the processor. "LEDs and Push Buttons" on page 1-15 summarizes the LED connections. To use an LED connected to the DAI or DPI, program its respective register on the processor. For more information on how to program the registers, refer to the *ADSP-2137x SHARC Processor Hardware Reference (Includes ADSP-21367, ADSP-21368, ADSP-21369, ADSP-21371, ADSP-21375)*.

Power LED (LED9)

When LED9 is lit (green), it indicates that power is being supplied to the board properly.

Reset LEDs (LED10)

When LED10 is lit (red), a master reset of all the major ICs is active.

USB Monitor LED (ZLED3)

The USB monitor LED (ZLED3) indicates that USB communication has been initialized successfully, and you can connect to the processor using an EZ-KIT Lite session. Once the USB cable is plugged into the board, it takes approximately 15 seconds for the USB monitor LED to light. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver.

When the development software is actively communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.

Push Buttons (SW8–11)

Four push buttons (SW8–11) are provided for general-purpose user input. Two push buttons are connected to the FLAG pins of the processor, while the other two are connected to the DAI of the processor. The push buttons are active high and, when pressed, send a high (1) to the processor. Refer to "LEDs and Push Buttons" on page 1-15 for more information. The push button enable switch (SW7) is capable of disconnecting the push buttons from the corresponding processor pins. Refer to "Push Button Enable Switch (SW7)" on page 2-13 for more information.

The push buttons and corresponding processor signals are summarized in Table 2-9.

Table 2-9. Push Button Connections

Push Button Label	Push Button Reference Designator	Processor Pin
PB1	SW8	FLAG1/$\overline{\text{IRQ1}}$
PB2	SW11	FLAG0/$\overline{\text{IRQ0}}$
PB3	SW10	DAI19
PB4	SW9	DAI20

Board Reset Push Button (SW12)

The RESET push button (SW12) resets all of the ICs on the board. The only exception is the USB interface chip (U4). The chip is not reset when the push button is pressed after the USB cable has been plugged in and communication initialized correctly with the PC. After USB communication has been initialized, the only way to reset the USB is by powering down the board.

Jumpers

This section describes functionality of the configuration jumpers. The jumper locations are shown in Figure 2-7.

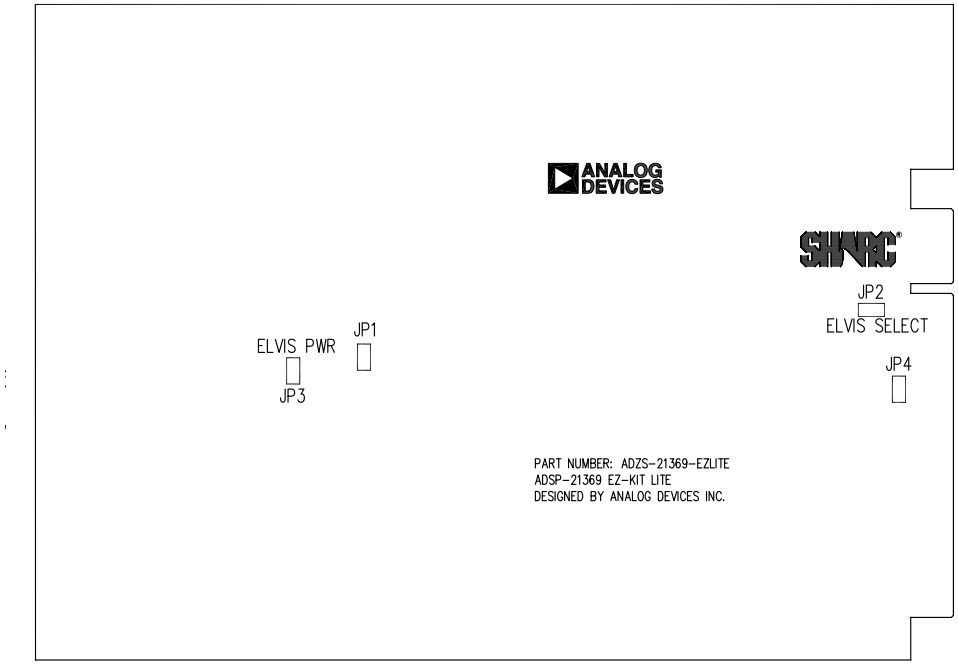

Figure 2-7. Jumper Locations

VCO Select Jumper (JP1)

The voltage-controlled oscillator (VCO) select jumper (JP1) configures the frequency selection of the on-board external PLL (U39). When JP1 is installed, the VCO output frequency is multiplied by a factor of 1.0. Conversely, when uninstalled, the VCO output frequency is multiplied by a factor of 0.5 or divided in half. The jumper settings are shown in Table 2-10.

Table 2-10. VCO Select Jumper (JP1)

JP1 Setting	Mode
OFF	**VCO output frequency x ½ (default)**
ON	VCO output frequency x 1.0

ELVIS Select Jumper (JP2)

The ELVIS select jumper (JP2) configures the EZ-KIT Lite's connection to an ELVIS station (see "ELVIS Interface" on page 1-13). When JP2 is installed, the connections to the push buttons and LED are re-directed to the ELVIS station instead of the processor. The jumper settings are shown in Table 2-11.

Table 2-11. ELVIS Select Jumper (JP2)

JP2 Setting	Mode
OFF	**Not connected to an ELVIS station (default)**
ON	Connected to an ELVIS station

ELVIS Voltage Selection Jumper (JP3)

The ELVIS voltage selection jumper (JP3) is used to select the power source for the EZ-KIT Lite. In a standard mode of operation, the board receives its power from an external power supply. When JP3 is installed, the board is powered from an ELVIS station, and no external power supply is required. The jumper settings are shown in Table 2-12.

Table 2-12. ELVIS Voltage Selection Jumper (JP3)

JP3 Setting	Mode
OFF	**Powered from an external power supply (default)**
ON	Powered from an ELVIS station

The external power supply must be disconnected from the board when JP3 is installed to avoid potential damage to the EZ-KIT Lite board and ELVIS unit.

ELVIS Programmable Flag Jumper (JP4)

The ELVIS programmable flag jumper (JP4) connects the ADSP-21369 processor's DAI4 pin to the ELVIS trigger pin. When JP4 is installed, DAI4 connects to the ELVIS TRIG1_2 pin directly. Conversely, when JP4 is uninstalled, DAIP4 is disconnected and can be used for another non-ELVIS operation. The jumper settings are shown in Table 2-13.

Table 2-13. ELVIS Select Jumper (JP4)

JP4 Setting	Mode
OFF	**DAI4 disconnected from the ELVIS TRIG pin (default)**
ON	DAI4 connected to the ELVIS TRIG pin

Connectors

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in Figure 2-8.

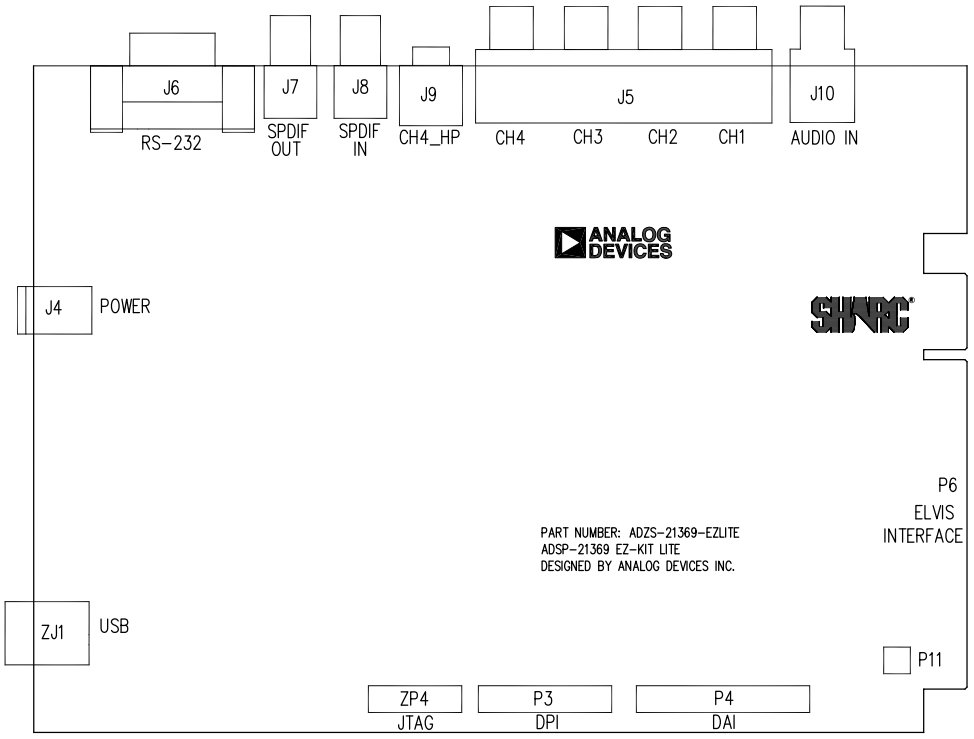

Figure 2-8. Connector Locations

Expansion Interface Connectors (J1–3)

Three board-to-board connectors (J1–3) provide signals for most peripheral interfaces of the processor. The connectors are located at the bottom of the board. For more information about the expansion interface, see "Expansion Interface" on page 2-7. For the connectors availability and pricing, contact Samtec.

Part Description	Manufacturer	Part Number
90-position 0.05" spacing, SMT	SAMTEC	SFC-145-T2-F-D-A
Mating Connectors		
90-position 0.05" spacing (through hole)	SAMTEC	TFM-145-x1 series
90-position 0.05" spacing (surface mount)	SAMTEC	TFM-145-x2 series
90-position 0.05" spacing (low cost)	SAMTEC	TFC-145 series

Audio In RCA Connector (J10)

Part Description	Manufacturer	Part Number
Two-channel right angle RCA jack	SWITCHCRAFT	PJRAS1X2S02
Mating Cable		
Two-channel RCA interconnect cable	MONSTER CABLE	BI100-1M

Audio Out RCA Connector (J5)

Part Description	Manufacturer	Part Number
Four-channel right angle RCA jack	SWITCHCRAFT	PJRAS4X2U01
Mating Cable		
Two-channel RCA interconnect cable	MONSTER CABLE	BI100-1M

Headphone Out Jack (J9)

Part Description	Manufacturer	Part Number
3.5 mm stereo jack	A/D ELECTRONICS	ST-323-5

Power Jack (J4)

The power connector (J4) provides all of the power necessary to operate the EZ-KIT Lite board.

Part Description	Manufacturer	Part Number
2.5 mm power jack	SWITCHCRAFT DIGI-KEY	RAPC712X-ND
Mating Power Supply (shipped with EZ-KIT Lite)		
7V power supply	CUI INC.	DMS070214-P6P-SZ

The power connector supplies DC power to the EZ-KIT Lite board. Table 2-14 shows the power supply specifications.

Table 2-14. Power Supply Specifications

Terminal	Connection
Center pin	+7 VDC@2.14A
Outer ring	GND

RS-232 Connector (J6)

Part Description	Manufacturer	Part Number
DB9, female, right angle	AMP/TYCO	5745781-4
Mating Cable		
Cable DB9M to DB9F 6 feet	DIGI-KEY	45-0308-0000-ND

S/PDIF Coax Connectors (J7 and J8)

Part Description	Manufacturer	Part Number
Coaxial	SWITCHCRAFT	PJRAN1X1U01
Mating Cable		
Two-channel RCA interconnect cable	MONSTER CABLE	BI100-1M

DPI Header (P3)

The DPI connector (P3) provides access to all of the DPI signals in the from of a .1" spacing header. When using the header to access the DPI pins of the processor, ensure that signals, which normally drive the DPI pins, are disabled. For more information, see "DPI Interface" on page 2-5.

Part Description	Manufacturer	Part Number
20-pin IDC header	FCI	68737-420HLF

DAI Header (P4)

The DAI connector (P4) provides access to all of the DAI signals in the from of a .1" spacing header. When using the header to access the DAI pins of the processor, ensure that signals, which normally drive the DAI pins, are disabled. Refer to "Codec Setup Switch (SW3)" on page 2-11 for more information on how to disable signals already being driven from elsewhere on the EZ-KIT Lite.

Part Description	Manufacturer	Part Number
26-pin IDC header	BERG	4102-T08-13LF

JTAG Header (ZP4)

The JTAG header (ZP4) is the connecting point for a JTAG in-circuit emulator pod. When an emulator connects to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

Part Description	Manufacturer	Part Number
14-pin IDC header	FCI	68737-414HLF

A ADSP-21369 EZ-KIT LITE BILL OF MATERIALS

The bill of materials corresponds to "ADSP-21369 EZ-KIT Lite Schematic" on page B-1.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	1	74LVC14A SOIC14	U40	TI	74LVC14AD
2	1	IDT74FCT3244 APY SSOP20	U37	IDT	IDT74FCT3244APYG
3	1	12.288MHZ OSC003	U1	EPSON	SG-8002CA MP
4	1	LT1765 SOIC8	VR1	LINEAR TECH	LT1765ES8#PBF
5	1	MT48LC4M32 B2 TSOP86	U36	DIGI-KEY	557-1196-1-ND
6	1	GTL2002 TSSOP8	U39	NPX	GTL2002DP,118
7	1	IS61LV5128AL TSOP44	U30	ISSI	IS61LV5128AL-10TLI
8	2	SN74LVC1G08 SOT23-5	U16,U18	TI	SN74LVC1G08DBVR
9	1	SN74LVC1G08 SOT23-5	U17	TI	SN74LVC1G08DBVR

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
10	1	TLC2932 TSSOP14	U38	TI	TLC2932IPWG4
11	1	24.576MHZ OSC003	U28	EPSON	SG-8002CA MP
12	1	21369 AM29LV081B "U35"	U35	AND	AM29LV081-120ED
13	1	SN65LVDS2D SOIC8	U2	NATIONAL SEMI	DS90LV018ATM
14	1	FDC658P SOT23-6	U3	FAIRCHILD	FDC658P
15	1	21369 M25P20 “U29”	U29	NUMONYX	M25P20-VMN6TP
16	1	SI7601DN ICS010	U45	VISHAY	SI7601DN-T1-GE3
17	1	ADM708SARZ SOIC8	U23	ANALOG DEVICES	ADM708SARZ
18	1	AD8532ARZ SOIC8	U19	ANALOG DEVICES	AD8532ARZ
19	2	ADP3336ARM Z MSOP8	VR3-VR4	ANALOG DEVICES	ADP3336ARMZ-REEL7
20	1	ADM3202ARN Z SOIC16	U32	ANALOG DEVICES	ADM3202ARNZ
21	8	AD8606ARZ SOIC8	U8-U15	ANALOG DEVICES	AD8606ARZ
22	1	AD1835AASZ MQFP52	U31	ANALOG DEVICES	AD1835AASZ

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
23	2	AD623ARMZ USOIC8	U5-U6	ANALOG DEVICES	AD623ARMZ
24	2	AD820ARZ SOIC8	U33-U34	ANALOG DEVICES	AD820ARZ
25	1	ADSP-21369 SBGA256	U44	ANALOG DEVICES	ADSP-21369KBPZ-3A
26	2	ADG774ABRQ Z QSOP16	U24-U25	ANALOG DEVICES	ADG774ABRQZ
27	2	ADP1864AUJZ SOT23-6	VR2,VR5	ANALOG DEVICES	ADP1864AUJZ-R7
28	1	PWR 2.5MM_JACK CON005	J4	SWITCH-CRAFT	RAPC712X
29	1	RCA 4X2 CON011	J5	SWITCH-CRAFT	PJRAS4X2U01X
30	2	RCA 1X1 CON012	J7-J8	SWITCH-CRAFT	PJRAN1X1U01X
31	5	MOMENTARY SWT013	SW8-SW12	PANASONIC	EVQ-PAD04M
32	3	.05 45X2 CON019	J1-J3	SAMTEC	SFC-145-T2-F-D-A
33	2	DIP8 SWT016	SW1,SW14	C&K	TDA08H0SB1
34	1	DIP6 SWT017	SW13	CTS	218-6LPST
35	7	DIP4 SWT018	SW2-SW7,SW15	ITT	TDA04HOSB1
36	1	DB9 9PIN DB9F	J6	TYCO	5747844-4

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
37	1	RCA RCA_1X2 CON031	J10	SWITCH-CRAFT	PJRAS1X2S02X
38	4	IDC 2X1 IDC2X1	JP1-JP4	FCI	90726-402HLF
39	1	IDC 10X2 IDC10X2	P3	BURG-FCI	54102-T08-10LF
40	1	IDC 2X2 IDC2X2	P11	FCI	68737-404HLF
41	1	3.5MM STEREO_JACK CON001	J9	DIGI-KEY	CP1-3525NG-ND
42	1	IDC 13X2 IDC13X2	P4	BERG	54102-T08-13LF
43	1	5A RESE-TABLE FUS005	F1	MOUSER	650-RGEF500
44	8	YELLOW LED001	LED1-LED8	DIGI-KEY	P512TR-ND
45	10	0.22UF 25V 10% 0805	C77,C91-C92,C118-C119,C152-C154,C185-C186	AVX	08053C224KAT2A
46	2	0.1UF 50V 10% 0805	C172,C216	AVX	08055C104KAT
47	2	2.2UF 35V 10% B	CT6,CT8	AVX	TAJB225K035R
48	5	600 100MHZ 200MA 0603	FER1-FER5	DIGI-KEY	490-1014-2-ND

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
49	1	2A S2A DO-214AA	D4	VISHAY	S2A-E3
50	4	1UF 16V 10% 0805	C204,C207-C209	DIGI-KEY	399-1284-2-ND
51	1	10UF 25V +80%/-20% 1210	C215	DIGI-KEY	587-1393-2-ND
52	2	68UF 25V 20% CAP003	CT1-CT2	PANASONIC	EEE-FC1E680P
53	1	2A SL22 DO-214AA	D1	VISHAY	SL22-E3/52T
54	1	0 1/8W 5% 0805	R14	VISHAY	CRCW08050000Z0EA
55	1	190 100MHZ 5A FER002	FER7	MURATA	DLW5BSN191SQ2
56	20	10UF 6.3V 10% 0805	C23-C24,C57-C58,C84-C85,C111-C114,C144-C147,C151,C162-C163,C176,C205-C206	AVX	08056D106KAT2A
57	3	6.04K 1/10W 1% 0805	R28-R30	DIGI-KEY	311-6.04KCRCT-ND
58	1	4.7UF 6.3V 10% 0805	C225	AVX	08056D475KAT2A
59	7	0.1UF 10V 10% 0402	C3,C75-C76,C168-C171	AVX	0402ZD104KAT2A
60	1	0.1UF 10V 10% 0402	C1	AVX	0402ZD104KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
61	89	0.01UF 16V 10% 0402	C4-C22,C25-C56,C59-C74,C78-C83,C173-C175,C177-C178,C183,C188,C190-C196,C201-C202	AVX	0402YC103KAT2A
62	1	0.01UF 16V 10% 0402	C184	AVX	0402YC103KAT2A
63	22	10K 1/16W 5% 0402	R5,R19-R23,R25-R26,R32-R34,R132,R152-R156,R161-R162,R173-R175	VISHAY	CRCW040210K0FKED
64	1	10K 1/16W 5% 0402	R24	VISHAY	CRCW040210K0FKED
65	3	4.7K 1/16W 5% 0402	R4,R180,R202	VISHAY	CRCW04024K70JNED
66	9	0 1/16W 5% 0402	R1-R3,R7-R9,R107,R121,R138	PANASONIC	ERJ-2GE0R00X
67	2	22 1/10W 5% 0402	R124,R133	DIGI-KEY	P22JTR-ND
68	2	33 1/16W 5% 0402	R6,R27	VISHAY	CRCW040233R0JNEA
69	1	1.5UH 20% IND003	L2	COIL CRAFT	DO1608C-152MLC
70	1	100MA CMDSH-3 SOD-323	D2	CENTRAL SEMI	CMDSH-3-E3
71	1	0.18UF 25V 10% 0805	C218	AVX	08053C184KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
72	1	100UF 10V 10% C	CT3	AVX	TPSC107K010R0075
73	2	64.9K 1/10W 1% 0805	R190,R194	VISHAY	CRCW080564K9FKEA
74	2	210.0K 1/4W 1% 0805	R191,R193	VISHAY	CRCW0805210KFKEA
75	1	107.0 1/10W 1% 0805	R128	DIGI-KEY	311-107CRTR-ND
76	1	249.0 1/10W 1% 0805	R127	DIGI-KEY	311-249CRTR-ND
77	2	0.1UF 16V 10% 0603	C187,C189	AVX	0603YC104KAT2A
78	1	1UF 16V 10% 0603	C179	DIG01	399-5090-2-ND
79	2	4.7UF 25V 20% 0805	C217,C220	AVX	0805ZD475KAT2A
80	2	68PF 50V 5% 0603	C93,C223	AVX	06035A680JAT2A
81	8	330PF 50V 5% 0603	C95,C101,C107,C116,C123,C129,C134,C142	AVX	06035A331JAT2A
82	2	470PF 50V 5% 0603	C90,C222	AVX	06033A471JAT2A
83	1	330 1/10W 5% 0603	R139	DIG01	541-330GTR-ND
84	10	330 1/10W 5% 0603	R163-R164,R168-R172,R176-R178	DIG01	541-330GTR-ND

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
85	8	0.0 1/10W 1% 0603	R12,R31,R126,R143, R184,R186,R192,R200	PHYCOMP	232270296001L
86	4	10 1/10W 5% 0603	R157-R160	VISHAY	CRCW060310R0JNEA
87	3	10.0K 1/16W 1% 0603	R125,R142,R148	DALE	CRCW060310K0FKEA
88	1	75.0K 1/16W 1% 0603	R131	VISHAY	CRCW060375K0FKEA
89	1	200.0K 1/16W 1% 0603	R134	VISHAY	CRCW0603200KFKEA
90	1	25.5K 1/16W 1% 0603	R150	DIGI-KEY	311-25.5KHRTR-ND
91	1	51.1K 1/16W 1% 0603	R198	VISHAY	CRCW060351K1FKEA
92	4	237.0 1/10W 1% 0603	R108-R109,R122-R123	DIGI-KEY	311-237HRTR-ND
93	2	750.0K 1/10W 1% 0603	R110,R116	DIGI-KEY	311-750KHRTR-ND
94	11	11.0K 1/10W 1% 0603	R39-R40,R50,R58,R73,R81,R86,R97,R102, R115,R144	DIGI-KEY	311-11.0KHRTR-ND
95	20	5.49K 1/10W 1% 0603	R37,R41-R42,R48,R51,R56,R59,R67,R72,R75,R80,R83-R84,R87, R96,R99,R103-R104, R113-R114	DIGI-KEY	311-5.49KHRTR-ND
96	9	3.32K 1/10W 1% 0603	R36,R43,R49,R57,R74,R82,R85,R94,R130	DIGI-KEY	311-3.32KHRTR-ND

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
97	8	1.65K 1/10W 1% 0603	R44,R52,R60,R64,R71,R79,R88,R95	DIGI-KEY	311-1.65KHRTR-ND
98	10	49.9K 1/10W 1% 0603	R46,R55,R63,R66,R68,R76,R91-R92,R119-R120	DIGI-KEY	311-49.9KHRTR-ND
99	8	604.0 1/10W 1% 0603	R45,R54,R62,R65,R69,R77,R90,R93	NIC COMPONENTS	NRC06F6040TRF
100	2	90.9K 1/10W 1% 0603	R146,R151	DIGI-KEY	311-90.9KHRTR-ND
101	1	0.1 1/10W 1% 0603	R149	PANASONIC	ERJ-3RSFR10V
102	3	10.0K 1/10W 1% 0603	R145,R147,R182	DIGI-KEY	311-10.0KHRTR-ND
103	4	5.76K 1/10W 1% 0603	R111-R112,R117-R118	DIGI-KEY	311-5.76KHRTR-ND
104	12	100PF 50V 5% 0603	C94,C99,C105,C117,C125,C131-C132,C140,C155,C161,C166-C167	AVX	06035A101JAT2A
105	5	1000PF 50V 5% 0603	C2,C156-C157,C164-C165	PANASONIC	ECJ-1VC1H102J
106	1	47.5K 1/10W 1% 0603	R183	DIGI-KEY	311-47.5KHRTR-ND
107	8	220PF 50V 5% 0603	C89,C97,C103,C109,C121,C127,C136,C139	PANASONIC	ECJ-1VC1H221J

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
108	12	680PF 50V 5% 0603	C96,C102,C108,C115,C122,C128,C135,C141,C148-C149,C158,C160	MURATA	GRM1885C1H681JA01D
109	9	2200PF 50V 5% 0603	C88,C98,C104,C110,C120,C126,C137-C138,C219	KEMET	C0603C222J5RACTU
110	1	33.0 1/10W 1% 0603	R195	DIGI-KEY	311-33.0HRTR-ND
111	8	2.74K 1/10W 1% 0603	R38,R47,R53,R61,R70,R78,R89,R98	DIGI-KEY	311-2.74KHRTR-ND
112	1	75.0 1/10W 1% 0603	R141	DALE	CRCW060375R0FKEA
113	4	1UF 6.3V 20% 0402	C197-C200	PANASONIC	ECJ-0EB0J105M
114	2	100 1/16W 5% 0402	R136-R137	DIGI-KEY	311-100JRTR-ND
115	4	100 1/16W 5% 0402	R165-R167,R179	DIGI-KEY	311-100JRTR-ND
116	1	0.027UF 25V 5% 0603	C181	AVX	06033C273JAT2A
117	2	0.27UF 16V 20% 0603	C180,C182	AVX	0603YG274ZAT2A
118	2	2.05K 1/16W 1% 0402	R100-R101	VISHAY	CRCW04022K05FKED
119	1	15.0K 1/16W 1% 0603	R140	DIGI-KEY	311-15.0KHRTR-ND

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
120	1	232.0 1/16W 1% 0603	R129	DIGI-KEY	311-232HRTR-ND
121	2	301.0 1/16W 1% 0603	R105-R106	DIGI-KEY	311-301HRTR-ND
122	2	24.9K 1/10W 1% 0603	R11,R196	DIGI-KEY	311-24.9KHTR-ND
123	1	47UF 6.3V 10% B	CT5	NIC COMPO-NENTS	NTC-T476K6.3TRBF
124	1	511.0 1/16W 1% 0402	R135	DIGI-KEY	311-511LCT-ND
125	1	0.05 1/2W 1% 1206	R13	SEI	CSF 1/2 0.05 1%R
126	2	10UF 16V 10% 1210	C100,C224	AVX	1210YD106KAT2A
127	1	GREEN LED001	LED9	PANASONIC	LN1361CTR
128	1	RED LED001	LED10	PANASONIC	LN1261CTR
129	2	1000PF 50V 5% 1206	C213-C214	AVX	12065A102JAT2A
130	1	255.0K 1/10W 1% 0603	R16	VISHAY	CRCW06032553FK
131	2	80.6K 1/10W 1% 0603	R15,R197	VISHAY	CRCW060380K6FKEA
132	1	6.8UH 25% IND009	L3	DIGI-KEY	308-1328-1-ND

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
133	1	4A SSB43L DO-214AA	D5	VISHAY	SSB43L
134	5	5A MBRS540T3G SMC	D3,D6-D7,D13-D14	ON SEMI	MBRS540T3G
135	1	2.5UH 30% IND013	L1	COILCRAFT	MSS1038-252NL_
136	1	470UF 2.5V 20% D2E	CT7	SANYO	2R5TPE470MF
137	3	30A GSOT05 SOT23-3	D9-D11	VISHAY	GSOT05-GS08
138	1	30A GSOT03 SOT23-3	D12	VISHAY	GSOT03-GS08
139	1	7A VESD01-02V-GS08 SOD-523	D8	VISHAY	VESD01-02V-GS08
140	2	0.03 1/2W 1% 1206	R199,R201	SEI	CSF 1/2 0.03 1%R

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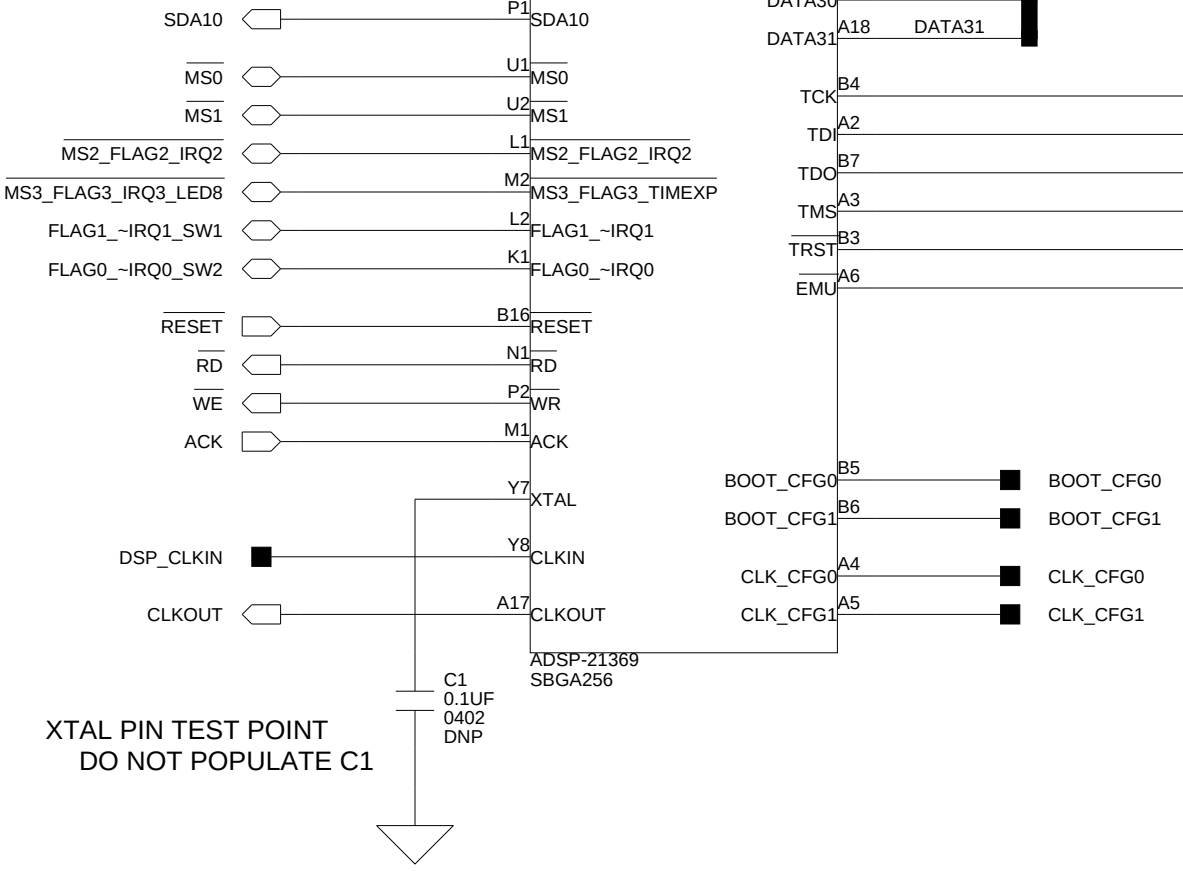
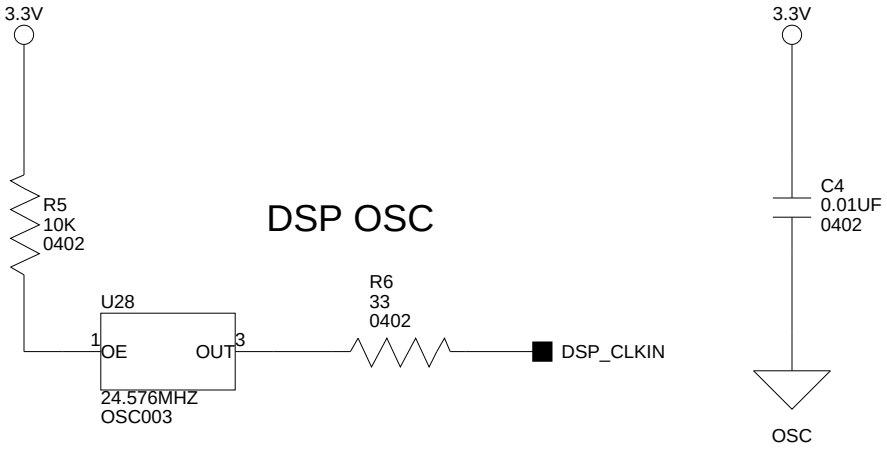
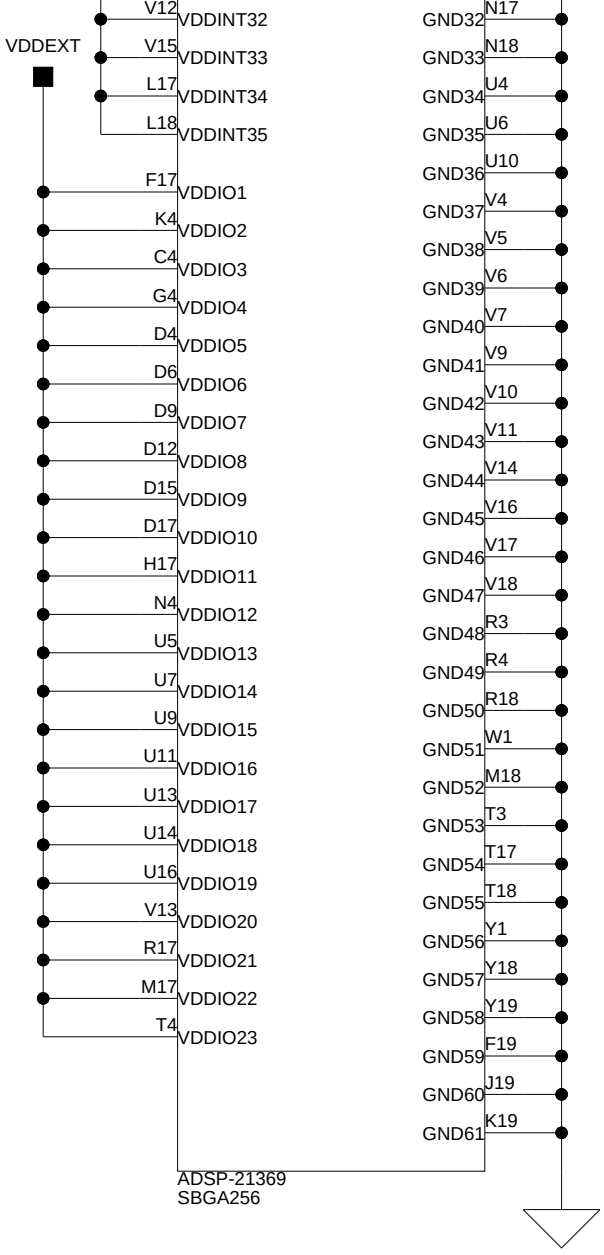

SDA10
P1
SDA10
MS0
U1
MS0
MS1
U2
MS1
MS2_FLAG2_IRQ2
L1
MS2_FLAG2_IRQ2
MS3_FLAG3_IRQ3_LED8
M2
MS3_FLAG3_TIMEXP
FLAG1_~IRQ1_SW1
L2
FLAG1_~IRQ1
FLAG0_~IRQ0_SW2
K1
FLAG0_~IRQ0
RESET
B16
RESET
RD
N1
RD
WE
P2
WR
ACK
M1
ACK
Y7
XTAL
DSP_CLKIN
Y8
CLKIN
CLKOUT
A17
CLKOUT
ADSP-21369
SBGA256
C1
0.1UF
0402
DNP
XTAL PIN TEST POINT
DO NOT POPULATE C1
DATA30
DATA31
A18
DATA31
TCK
B4
TDI
A2
TDO
B7
TMS
A3
TRST
B3
EMU
A6
BOOT_CFG0
B5
BOOT_CFG0
BOOT_CFG1
B6
BOOT_CFG1
CLK_CFG0
A4
CLK_CFG0
CLK_CFG1
A5
CLK_CFG1


3.3V
R5
10K
0402
DSP OSC
U28
1
OE
OUT
3
24.576MHZ
OSC003
R6
33
0402
DSP_CLKIN
3.3V
C4
0.01UF
0402
OSC



DA_EMULAT

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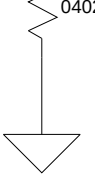
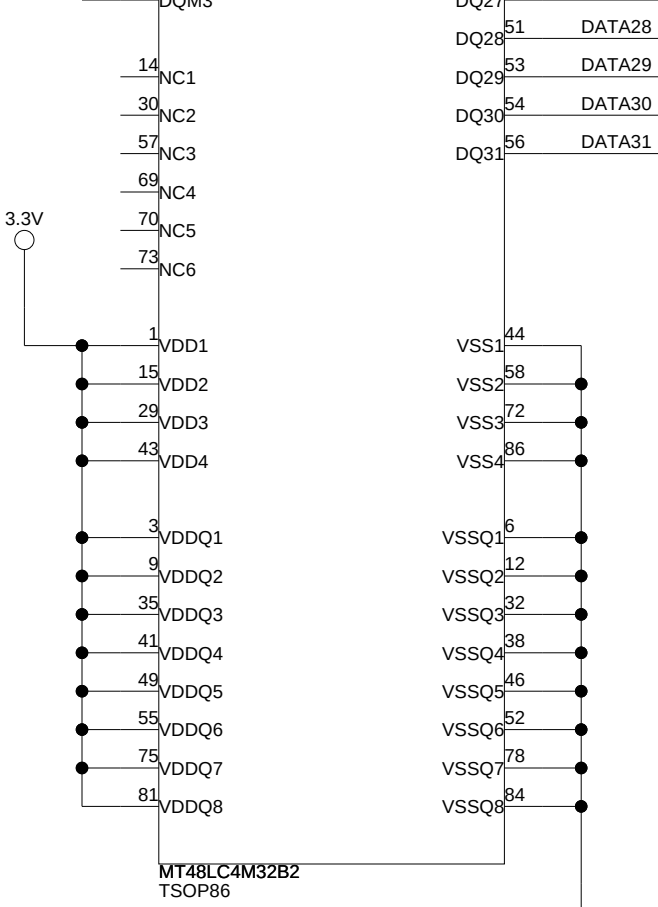
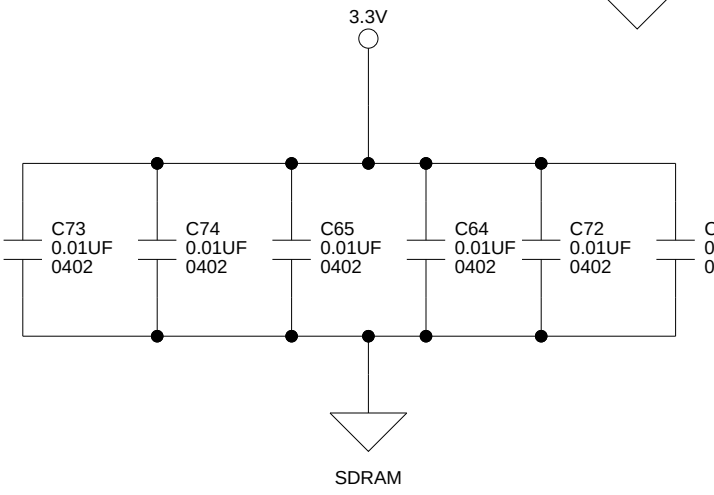
4

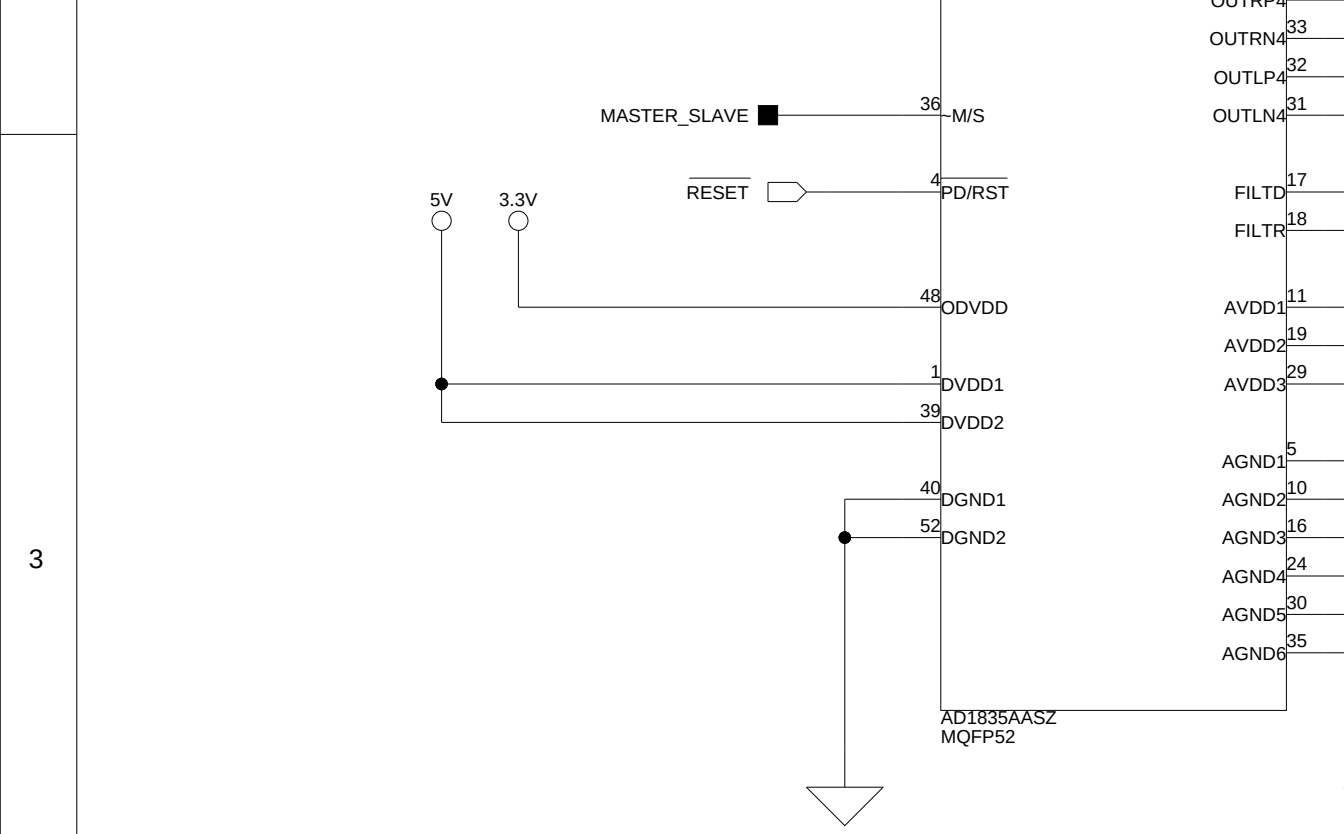
A

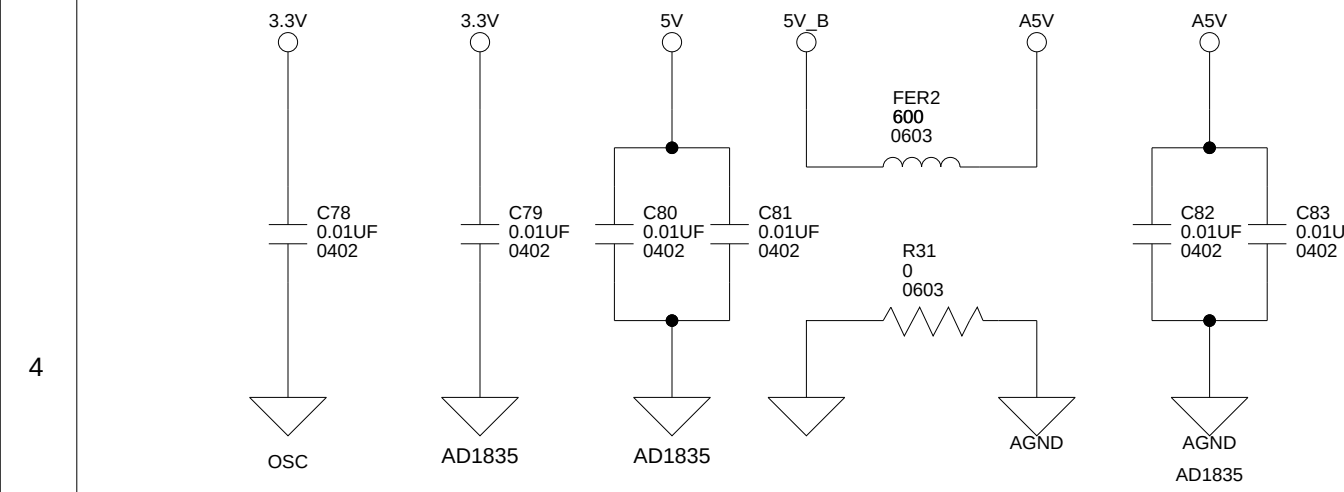


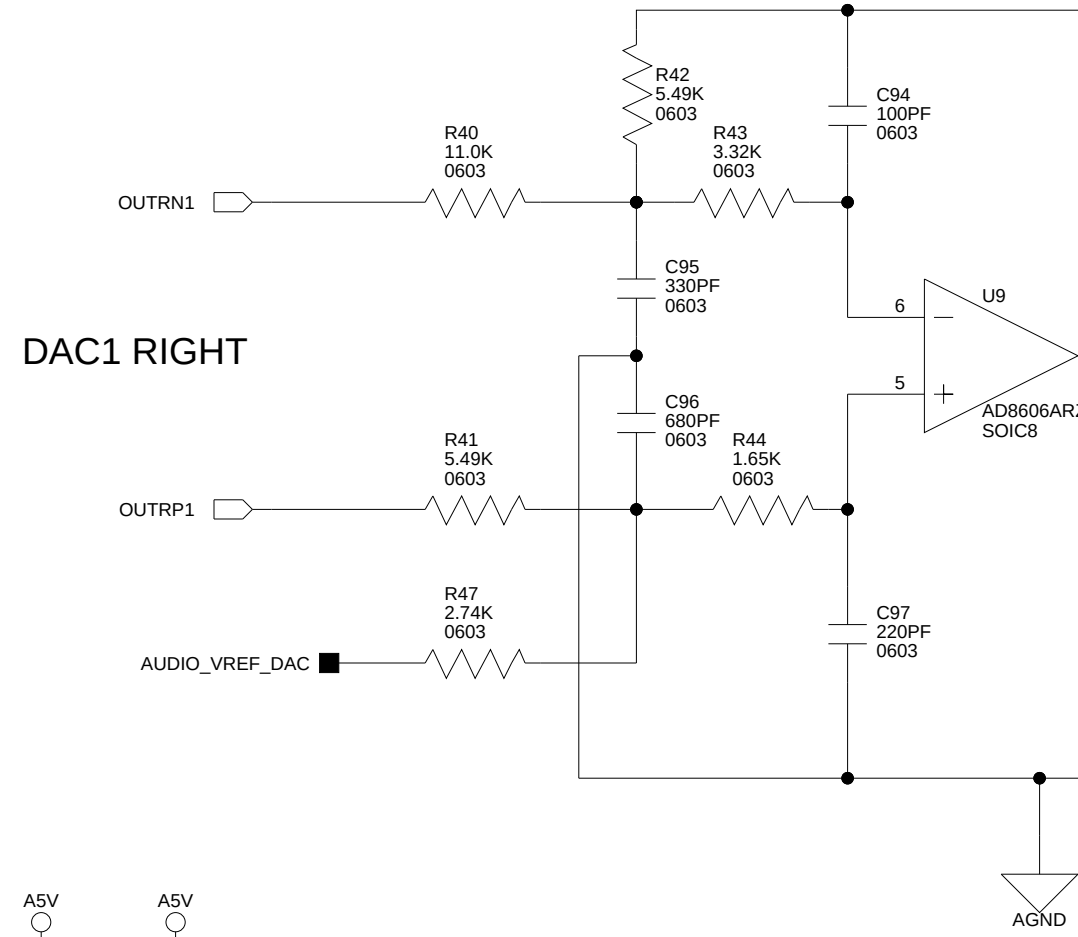
DQM signals are either tied to GND or driven by processor's FLAG pin. This is SDRAM device specific and the requirement is specified in SDRAM datasheets

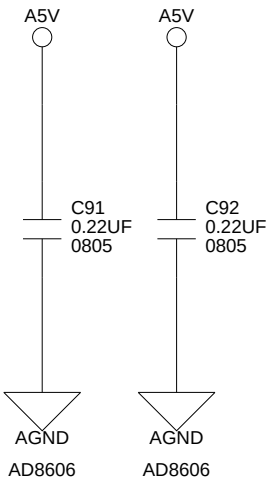





OUTRP4
OUTRN4
33
OUTLP4
32
OUTLN4
31
MASTER_SLAVE
36
M/S
RESET
4
PD/RST
FILTD
17
FILTR
18
5V
3.3V
48
ODVDD
AVDD1
11
AVDD2
19
AVDD3
29
1
DVDD1
39
DVDD2
AGND1
5
AGND2
10
AGND3
16
AGND4
24
AGND5
30
AGND6
35
40
DGND1
52
DGND2
AD1835AASZ
MQFP52


3.3V
C78
0.01UF
0402
OSC
3.3V
C79
0.01UF
0402
AD1835
5V
C80
0.01UF
0402
C81
0.01UF
0402
AD1835
5V_B
A5V
FER2
600
0603
R31
0
0603
AGND
A5V
C82
0.01UF
0402
C83
0.01U
0402
AGND
AD1835

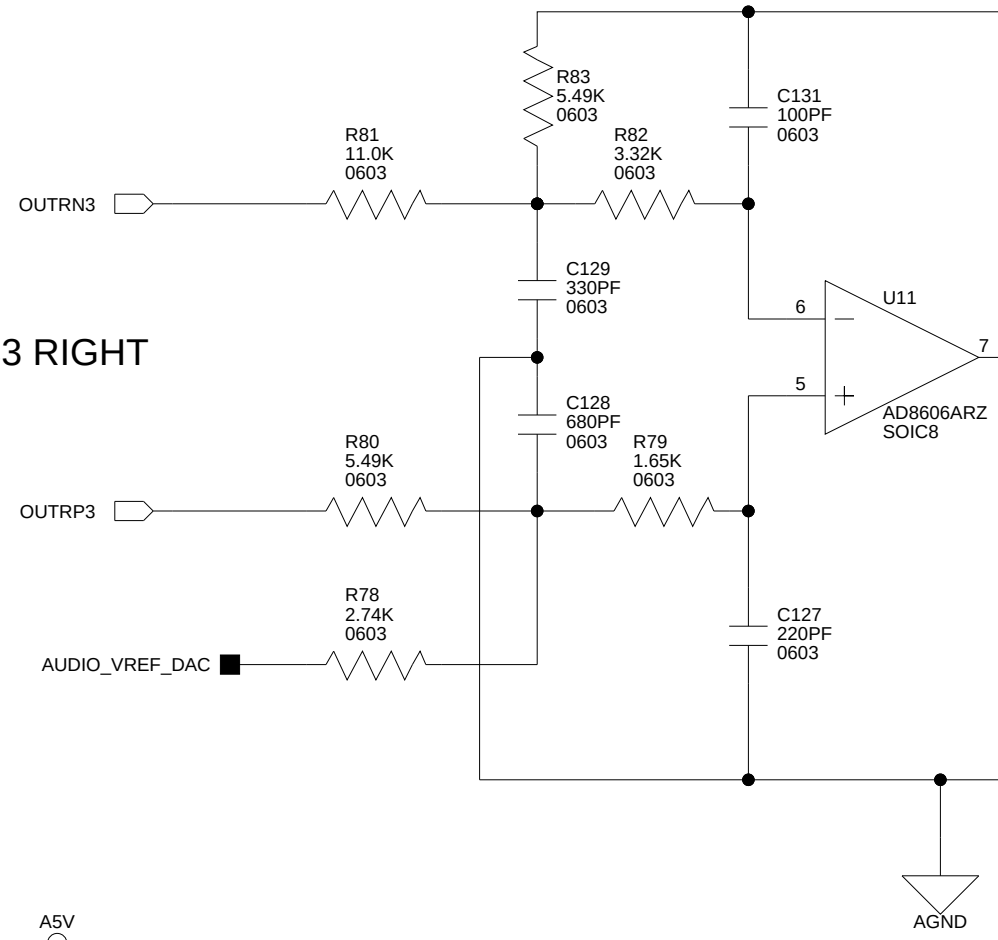

DAC1 RIGHT
R42
5.49K
0603
C94
100PF
0603
R40
11.0K
0603
R43
3.32K
0603
OUTRN1
C95
330PF
0603
U9
6
5
AD8606AR
SOIC8
C96
680PF
0603
R41
5.49K
0603
R44
1.65K
0603
OUTRP1
R47
2.74K
0603
C97
220PF
0603
AUDIO_VREF_DAC
AGND

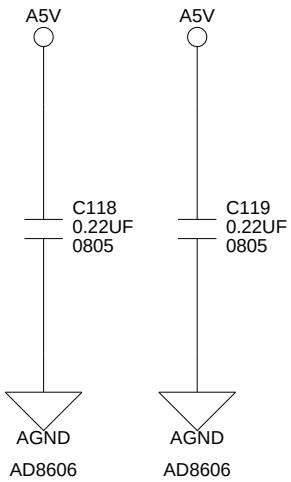

A5V
A5V
C91
0.22UF
0805
C92
0.22UF
0805
AGND
AGND
AD8606
AD8606

3

4

A

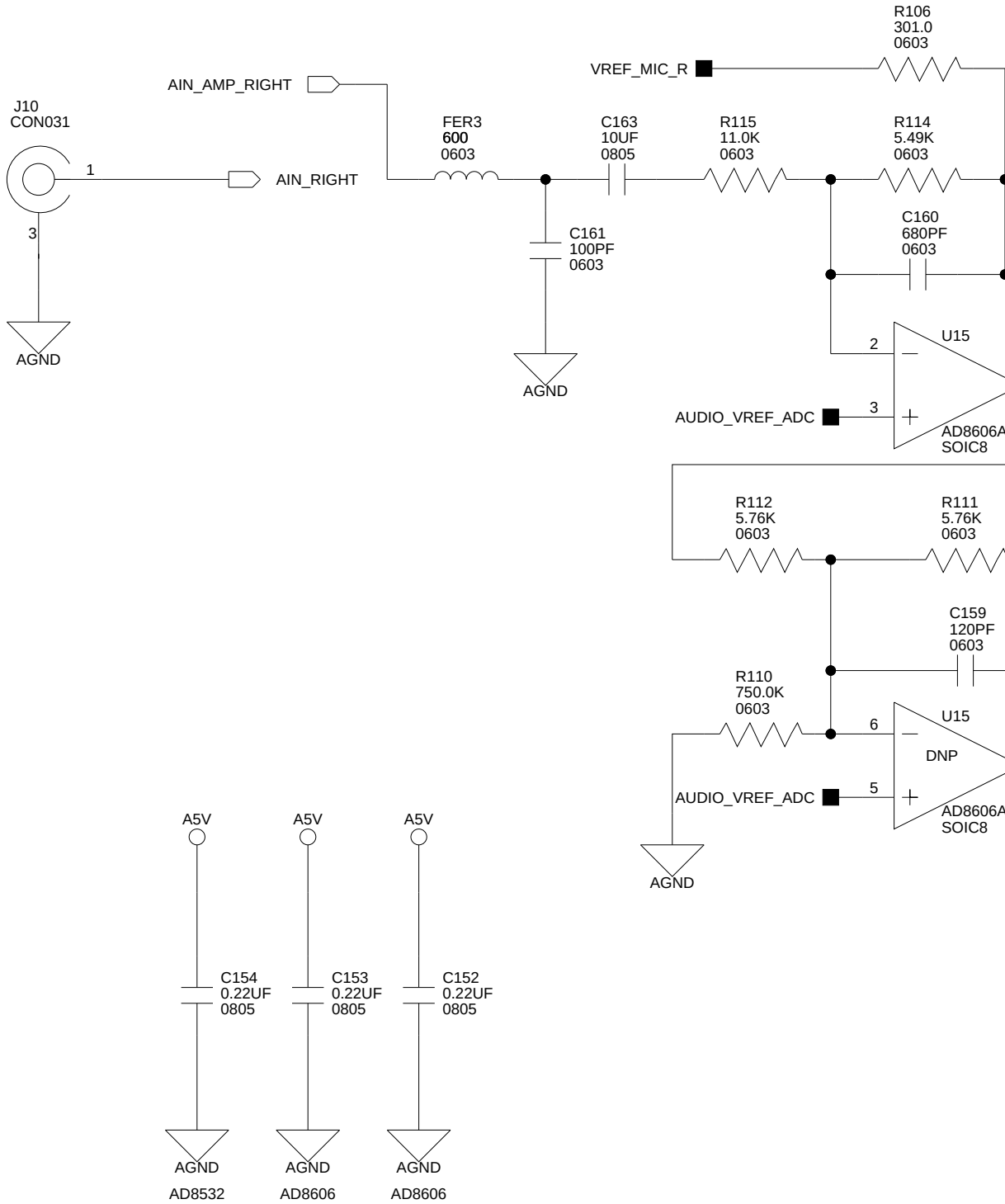

DAC3 RIGHT
R83
5.49K
0603
C131
100PF
0603
R81
11.0K
0603
R82
3.32K
0603
OUTRN3
C129
330PF
0603
U11
6
7
5
C128
680PF
0603
AD8606ARZ
SOIC8
R80
5.49K
0603
R79
1.65K
0603
OUTRP3
R78
2.74K
0603
C127
220PF
0603
AUDIO_VREF_DAC
AGND


A5V
A5V
C118
0.22UF
0805
C119
0.22UF
0805
AGND
AGND
AD8606
AD8606

3

4

A


R106
301.0
0603
VREF_MIC_R
AIN_AMP_RIGHT
J10
CON031
1
AIN_RIGHT
3
AGND
FER3
600
0603
C163
10UF
0805
R115
11.0K
0603
R114
5.49K
0603
C161
100PF
0603
AGND
C160
680PF
0603
U15
2
3
AUDIO_VREF_ADC
AD8606A
SOIC8
R112
5.76K
0603
R111
5.76K
0603
C159
120PF
0603
R110
750.0K
0603
6
5
U15
DNP
AUDIO_VREF_ADC
AD8606A
SOIC8
AGND
A5V
A5V
A5V
C154
0.22UF
0805
C153
0.22UF
0805
C152
0.22UF
0805
AGND
AGND
AGND
AD8532
AD8606
AD8606

3

4

A

65LVDS2D

DAIP1_SPDIF_OUT

U16
SN74LVC1G08
SOT23-5

U17
SN74LVC1G08
SOT23-5
DNP

C172
0.1UF
0805

3.3V
C174
0.01UF
0402
SN74LVC1G08

3.3V
C184
0.01UF
0402
DNP
SN74LVC1G08

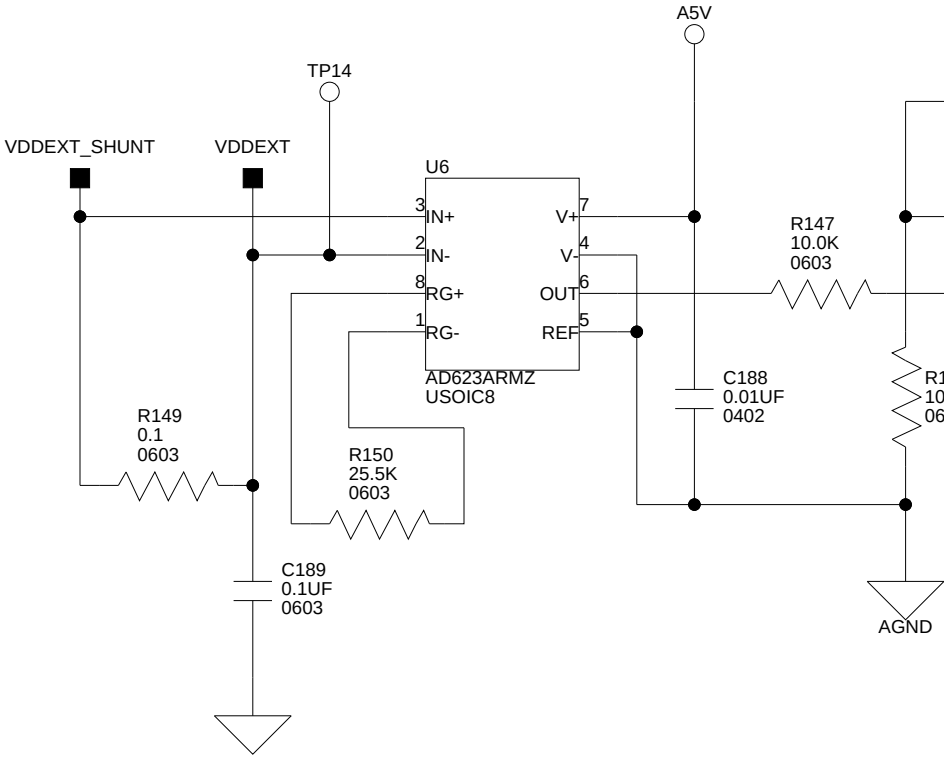
Loopback Test Switc
(Default= All OFF)
For Test Purposes On

SW6
SPDIF_COAX_IN
RX_IN
DIP4
SWT018

3

4

A

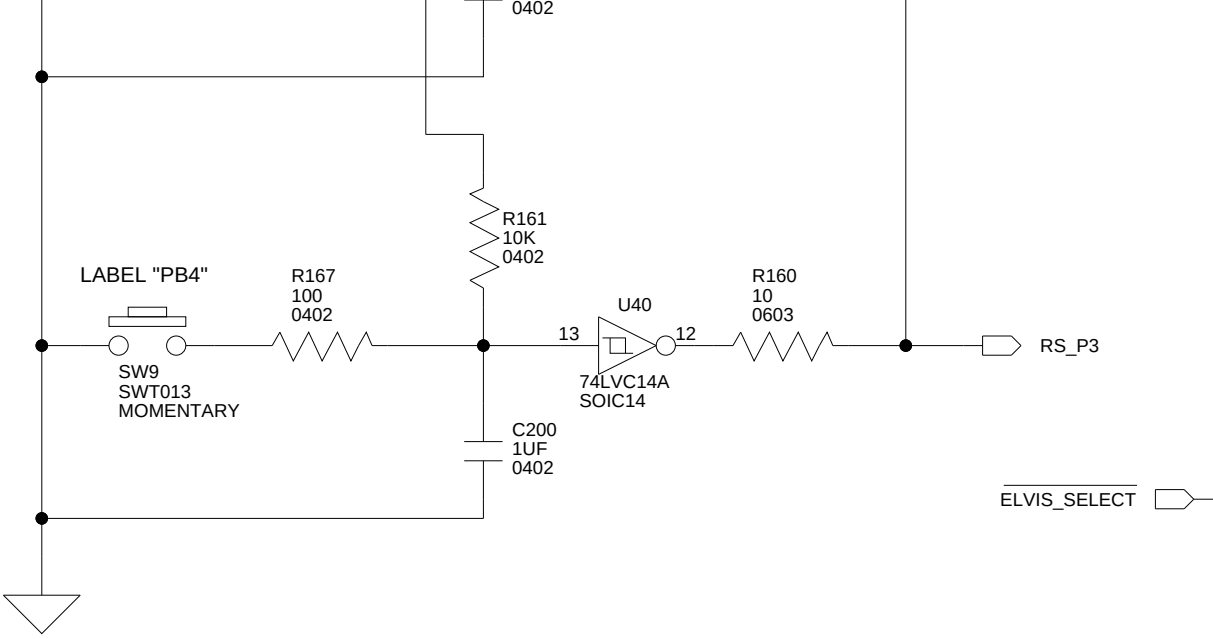


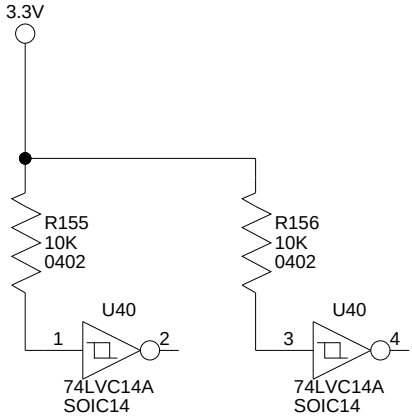
DSP IO CURRE

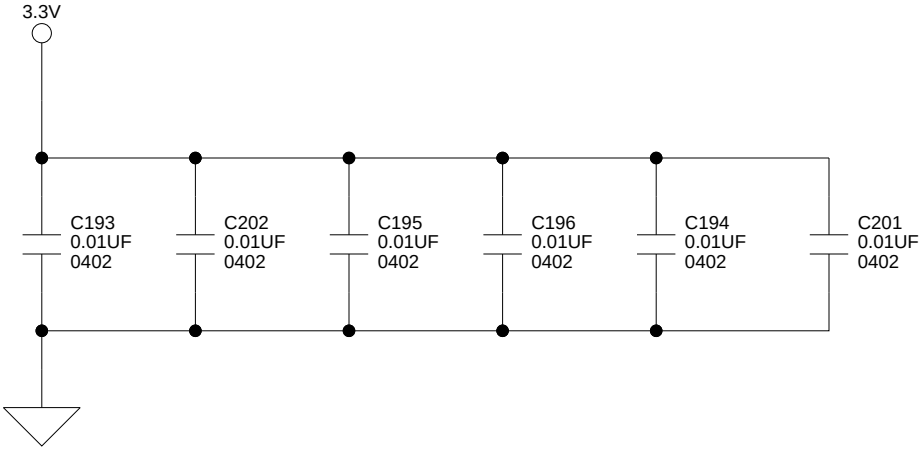
3

4

A





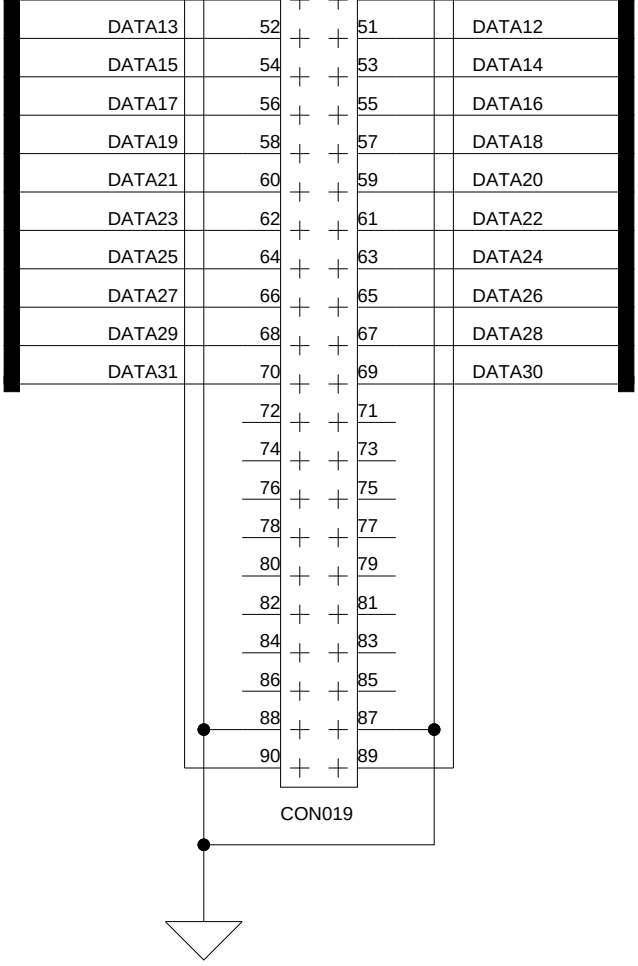


74LVC14A ADM708 IDT74FCT3244 ADG774A ADG774A SN74LVC1G08

3

4

A



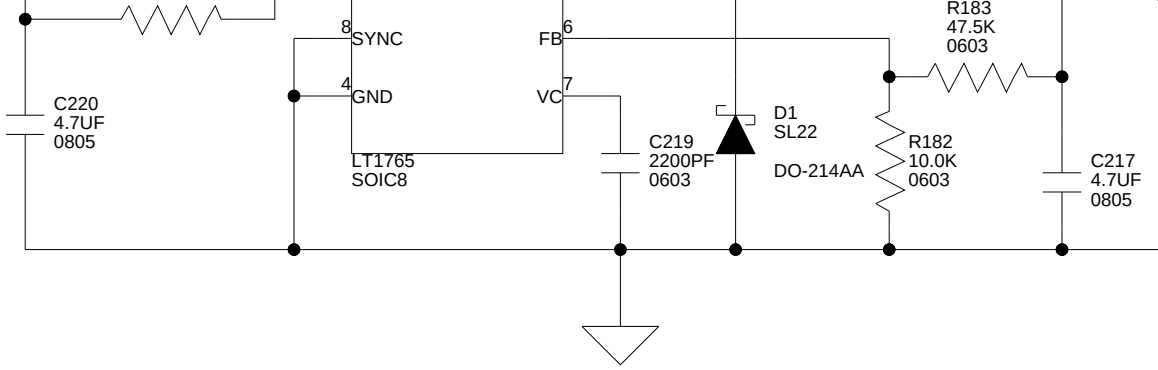
DAIP2_PLLMCLK_OUT
DAIP4_ELVIS_TRIG
DAIP6_AD1835_MCLK
DAIP8_ADC_LRCLK
DAIP10_DAC_D3
DAIP12_DAC_D1
DAIP14_DAC_LRCLK
DAIP16_LED7
DAIP18_SPDIF_IN
DAIP20_SW4
FLAG1_~IRQ1_SW1
DPI2_MISO
DPI4_SPI_AD1835_CS
DPI6_LED1

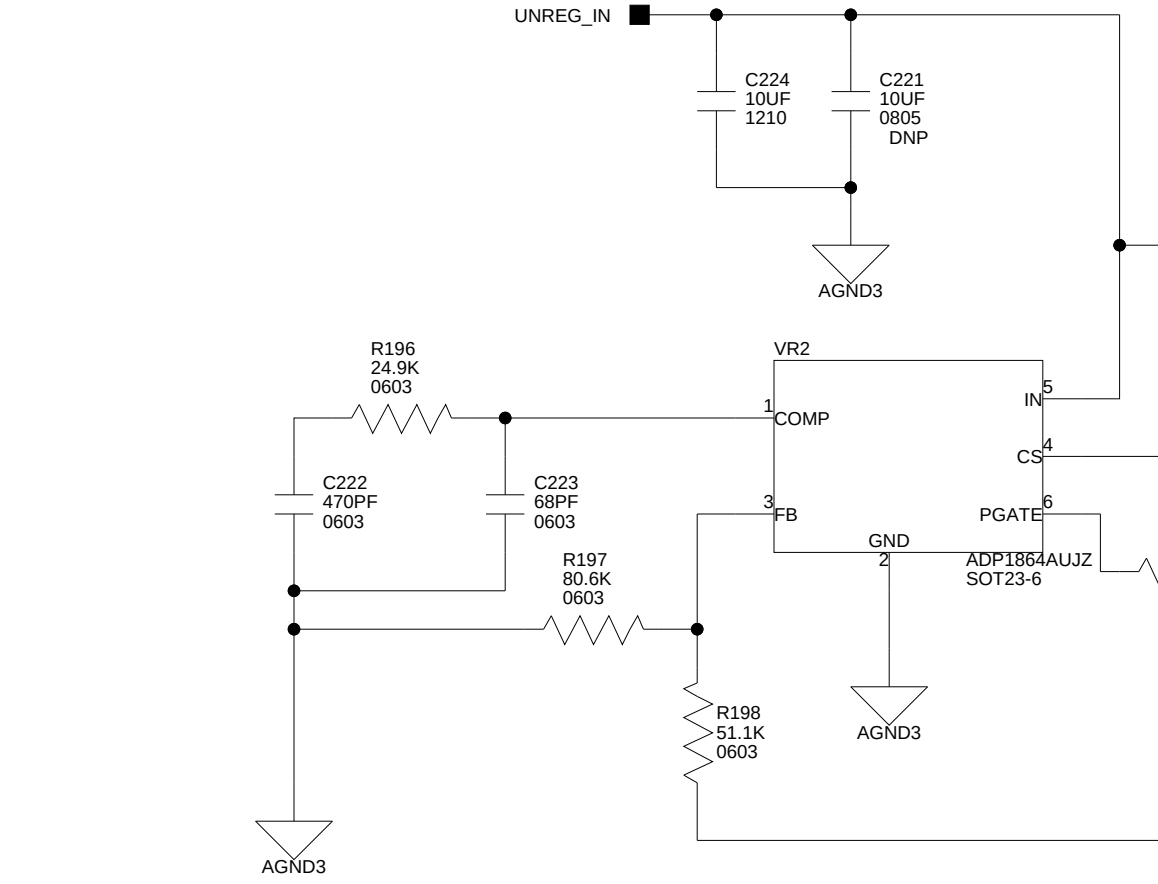
DPI8_LED3
DPI10_UART0_RX
DPI12_UART0_CTS
DPI14_LED5

3

4

A


R183
47.5K
0603
C220
4.7UF
0805
8
SYNC
4
GND
LT1765
SOIC8
FB
6
VC
7
C219
2200PF
0603
D1
SL22
DO-214AA
R182
10.0K
0603
C217
4.7UF
0805


UNREG_IN
C224
10UF
1210
C221
10UF
0805
DNP
AGND3
R196
24.9K
0603
VR2
1
COMP
IN
5
CS
4
C222
470PF
0603
C223
68PF
0603
3
FB
PGATE
6
GND
2
ADP1864AUJZ
SOT23-6
R197
80.6K
0603
R198
51.1K
0603
AGND3
AGND3

3

4

A

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