ADSP-BF527 EZ-KIT Lite®
Evaluation System Manual

Revision 1.7, July 2012

Part Number
82-000208-01

Analog Devices, Inc.
One Technology Way
Norwood, Mass. 02062-9106

ANALOG DEVICES

Copyright Information

Printed in the USA.

Disclaimer

Trademark and Service Mark Notice

Regulatory Compliance

The ADSP-BF527 EZ-KIT Lite is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADSP-BF527 EZ-KIT Lite has been certified to comply with the essential requirements of the European EMC directive 2004/108/EC and therefore carries the "**CE**" mark.

The ADSP-BF527 EZ-KIT Lite has been appended to Analog Devices, Inc. EMC Technical File (EMC TF) referenced **DSPTOOLS1**, issue 2 dated June 4, 2008 and was declared CE compliant by an appointed Notified Body (No.0673) as listed below.

Notified Body Statement of Compliance: Z600ANA2.030 dated June 4, 2008.

Issued by: Technology International (Europe) Limited
60 Shrivenham Hundred Business Park
Shrivenham, Swindon, SN6 8TY, UK

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

CONTENTS

Contents

PREFACE

Thank you for purchasing the ADSP-BF527 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for Blackfin® processors.

Blackfin processors embody a type of embedded processor designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications. They deliver breakthrough signal-processing performance and power efficiency within a reduced instruction set computing (RISC) programming model.

Blackfin processors support a media instruction set computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics. Blackfin processors deliver signal-processing performance in a microprocessor-like environment.

Based on the Micro Signal Architecture (MSA), Blackfin processors combine a 32-bit RISC instruction set, dual 16-bit multiply accumulate (MAC) DSP functionality, and eight-bit video processing performance that had previously been the exclusive domain of very-long instruction word (VLIW) media processors.

The evaluation board is designed to be used in conjunction with the CrossCore® Embedded Studio (CCES) and VisualDSP++® development environments to test capabilities of the ADSP-BF523/BF525/BF527 Blackfin processors. The development environment facilitates advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-BF527 assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the processor from a personal computer (PC) is achieved through a USB port or an external JTAG emulator. The USB interface provides unrestricted access to the ADSP-BF527 processor and evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to http://www.analog.com/dsp/tools.

The ADSP-BF527 EZ-KIT Lite provides example programs to demonstrate the evaluation board capabilities.

Product Overview

The board features:

- Analog Devices ADSP-BF527 Blackfin processor
    - Core performance up to 600 MHz
    - External bus performance up to 133 MHz
    - 289-pin 0.5 mm pitch mini-BGA package
    - 25 MHz oscillator
- Synchronous dynamic random access memory (SDRAM)
    - Micron MT48LC32M16A2TG – 64 MB (8M x 16 bits x 4 banks)
- Parallel flash memory
    - ST Micro M29W320EB – 32 Mb (2M x 16 bits)
- NAND flash memory
    - Numonyx NAND04 – 4 Gb
- SPI flash memory
    - ST Micro M25P16 – 16 Mb
- Internal audio codec
    - Low-power audio codec
    - One stereo `LINE OUT` jack
    - One input `MIC` jack
    - One input stereo `LINE IN` jack

- TFT LCD display with touchscreen
    - Sharp LQ035Q1DH02 320 x 240 3.5” touchscreen LCD
    - Analog Devices AD7879-1 four-wire touchscreen controller
- Ethernet interface
    - SMSC LAN8700 PHY device
    - 10-BaseT and 100-BaseTX Ethernet controller
    - Auto-MDIX
- Keypad
    - Analog Devices ADP5520 keypad controller
    - ACT components – 4 x 4 keypad assembly
- Thumbwheel
    - CTS Corp rotary encoder
- Universal asynchronous receiver/transmitter (UART)
    - ADM3202 RS-232 line driver/receiver
    - DB9 female connector
- LEDs
    - Ten LEDs: one power (green), one board reset (red), three general-purpose (yellow), one USB monitor (amber), PHY link (yellow), PHY activity (green), keypad controller (red), and FPGA done (yellow)

- Push buttons
    - Three push buttons: one reset, two programmable flags with debounce logic
- Expansion interface
    - Provides access to all ADSP-BF527 processor signals
- Other features
    - JTAG ICE 14-pin header
    - USB OTG connector
    - HOST interface connector
    - Power measurement jumpers
    - PPI IDC connector
    - SPORT0 and SPORT1 IDC connectors
    - TWI, SPI, timers, and UART0 IDC connectors

For information about the hardware components of the EZ-KIT Lite, refer to "ADSP-BF527 EZ-KIT Lite Hardware Reference" on page 2-1.

Purpose of This Manual

The *ADSP-BF527 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF527 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference guide for future designs.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set.

Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts that describe your target architecture. For the locations of these documents, see "Related Documents".

Programmers who are unfamiliar with CCES or VisualDSP++ should refer to the online help and user's manuals.

Manual Contents

The manual consists of:

- Chapter 1, "Using the ADSP-BF527 EZ-KIT Lite" on page 1-1
  Describes EZ-KIT Lite operation from a programmer's perspective and provides a simplified memory map.
- Chapter 2, "ADSP-BF527 EZ-KIT Lite Hardware Reference" on page 2-1
  Provides information on the EZ-KIT Lite hardware components.
- Appendix A, "ADSP-BF527 EZ-KIT Lite Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1
  Provides the resources for board-level debugging, can be used as a reference guide. Appendix B is part of the online help.

What's New in This Manual

This is revision 1.7 of the *ADSP-BF527 EZ-KIT Lite Evaluation System Manual*. The manual has been updated to include CCES information. In addition, modifications and corrections based on errata reports against the previous manual revision have been made.

For the latest version of this manual, please refer to the Analog Devices Web site.

Technical Support

You can reach Analog Devices processors and DSP technical support in the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:
  `http://ez.analog.com/community/dsp`
- Submit your questions to technical support directly at:
  `http://www.analog.com/support`
- E-mail your questions about processors, DSPs, and tools development software from **CrossCore Embedded Studio** or **VisualDSP++**:

  Choose **Help > Email Support**. This creates an e-mail to `processor.tools.support@analog.com` and automatically attaches your **CrossCore Embedded Studio** or **VisualDSP++** version information and `license.dat` file.
- E-mail your questions about processors and processor applications to:
  `processor.support@analog.com` or
  `processor.china@analog.com` (Greater China support)

- In the **USA only**, call **1-800-ANALOGD** (1-800-262-5643)
- Contact your Analog Devices sales office or authorized distributor. Locate one at:
  www.analog.com/adi-sales
- Send questions by mail to:
  Processors and DSP Technical Support
  Analog Devices, Inc.
  Three Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

This evaluation system supports Analog Devices ADSP-BF527 Blackfin embedded processors. Functionality of the ADSP-BF523 and ADSP-BF525 processors can be evaluated using the same product because the processors have many similarities.

Product Information

Product information can be obtained from the Analog Devices Web site and the online help system.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, myAnalog is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. myAnalog provides access to books, application notes, data sheets, code examples, and more.

Visit myAnalog (found on the Analog Devices home page) to sign up. If you are a registered user, just log on. Your user name is your e-mail address.

EngineerZone

EngineerZone is a technical support forum from Analog Devices. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

Related Documents

For additional information about the product, refer to the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-BF522/ADSP-BF523/ADSP-BF524/ ADSP-BF525/ADSP-BF526/ADSP-BF527 Blackfin Embedded Processor Data Sheet	General functional description, pinout, and timing of the processor
ADSP-BF2x Blackfin Processor Hardware Reference	Description of the internal processor architecture and all register functions
Blackfin Processor Programming Reference	Description of all allowed processor assembly instructions

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the development environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

1 USING THE ADSP-BF527 EZ-KIT LITE

This chapter provides information to assist you with development of programs for the ADSP-BF527 EZ-KIT Lite evaluation system.

The following topics are covered.

For information about the graphical user interface, including the boot loading, target options, and other facilities of the EZ-KIT Lite system, refer to the online help.

For more detailed information about the ADSP-BF527 Blackfin processor, see documents referred to at "Related Documents".

Package Contents

Your ADSP-BF527 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-BF527 EZ-KIT Lite board
- Universal 7.0V DC power supply
- Ethernet patch cable
- Three 3.5 mm male-to-male audio cables
- 3.5 mm headphones
- USB A-B male cable for USB debug agent
- 5-in-1cable and connectors for USB on-the-go (OTG) applications
- Ethernet loopback connector

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-BF527 EZ-KIT Lite board is designed to run outside your personal computer as a standalone unit. You do not have to open your computer case.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which can damage some components. Figure 1-1 shows the default jumper settings, switches, connector locations, and LEDs used in installation. Confirm that your board is in the default configuration before using the board.

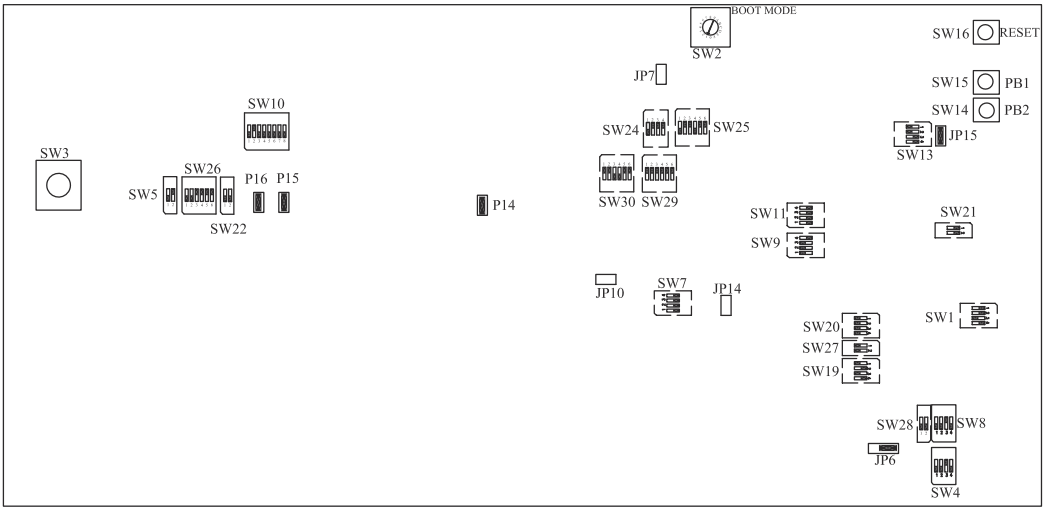


Figure 1-1. EZ-KIT Lite Hardware Setup

CCES Install and Session Startup

For information about CCES and to download the software, go to www.analog.com/CCES. A link for the ADSP-BF527 EZ-KIT Lite Board Support Package (BSP) for CCES can be found at http://www.analog.com/Blackfin/EZKits.

Follow these instructions to ensure correct operation of the product software and hardware.

Step 1: Connect the EZ-KIT Lite board to a personal computer (PC) running CCES using one of two options: an Analog Devices emulator or via the debug agent.

Using an Emulator:

1. Plug one side of the USB cable into the USB connector of the emulator. Plug the other side into a USB port of the PC running CCES.
2. Attach the emulator to the header connector ZP4 (labeled JTAG) on the EZ-KIT Lite board.

Using the on-board Debug Agent:

1. Plug one side of the USB cable into the USB connector of the debug agent ZJ1 (labeled USB).
2. Plug the other side of the cable into a USB port of the PC running CCES.

Step 2: Attach the provided cord and appropriate plug to the power adaptor.

1. Plug the jack-end of the power adaptor into the power connector J6 (labeled 7.0V) on the EZ-KIT Lite board.
2. Plug the other side of the power adaptor into a power outlet. The power LED (labeled LED4) is lit green when power is applied to the board.
3. Power the emulator (if used). Plug the jack-end of the assembled power adaptor into the emulator and plug the other side of the power adaptor into a power outlet. The enable/power is lit green when power is applied.

Step 3 (if connected through the debug agent): Verify that the yellow USB monitor LED (labeled ZLED3) on the debug agent is on. This signifies that the board is communicating properly with the host PC and ready to run CCES.

Session Startup

It is assumed that the CrossCore Embedded Studio software is installed and running on your PC.

Note: If you connect the board or emulator first (before installing CCES) to the PC, the Windows driver wizard may not find the board drivers.

1. Navigate to the CCES environment via the **Start** menu.

   Note that CCES is not connected to the target board.

2. Use the system configuration utility to connect to the EZ-KIT Lite board.

   If a debug configuration exists already, select the appropriate configuration and click **Apply and Debug** or **Debug**. Go to step 8.

   To create a debug configuration, do one of the following:

   - Click the down arrow next to the little bug icon, select **Debug Configurations**
   - Choose **Run > Debug Configurations**.

   The **Debug Configuration** dialog box appears.

3. Select **CrossCore Embedded Studio Application** and click  (**New launch configuration**).

   The **Select Processor** page of the **Session Wizard** appears.

4. Ensure **Blackfin** is selected in **Processor family**. In **Processor type**, select **ADSP-BF527**. Click **Next**.

   The **Select Connection Type** page of the **Session Wizard** appears.

5. Select one of the following:

   - For standalone debug agent connections, **EZ-KIT Lite** and click **Next**.
   - For emulator connections, **Emulator** and click **Next**.

   The **Select Platform** page of the **Session Wizard** appears.

6. Do one of the following:

   - For standalone debug agent connections, ensure that the selected platform is **ADSP-BF527 EZ-KIT** Lite via Debug Agent.
   - For emulator connections, choose the type of emulator that is connected to the board.

7. Click **Finish** to close the wizard.

   The new debug configuration is created and added to the program(s) to load list.

8. In the **Program(s) to load** section, choose the program to load when connecting to the board. If not loading any program upon connection to the target, do not make any changes.

Note that while connected to the target, there is no way to choose a program to download. To load a program once connected, terminate the session.

To delete a configuration, go to the **Debug Configurations** dialog box and select the configuration to delete. Click  and choose **Yes** when asked if you wish to delete the selected launch configuration. Then **Close** the dialog box.

To disconnect from the target board, click the terminate button (red box) or choose **Run** > **Terminate**.

To delete a session, choose **Target** > **Session** > **Session List**. Select the session name from the list and click **Delete**. Click **OK**.

VisualDSP++ Install and Session Startup

For information about VisualDSP++ and to download the software, go to www.analog.com/VisualDSP.

There are two USB interfaces on the ADSP-BF527 EZ-KIT Lite. Be sure to use the debugger's interface (ZJ1) when connecting your computer to the board with provided USB cable. The other USB interface (labelled USB-OTG, P1) is for applications use.

1. Verify that the yellow USB monitor LED (ZLED3, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the **Start** > **Programs** menu. The main window appears. Note that VisualDSP++ does not connect to any session. Skip the rest of this step to step 3.

If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and force VisualDSP++ to start a new session by pressing and holding down the **Ctrl** key while starting VisualDSP++. Do not release the **Ctrl** key until the **Session Wizard** appears on the screen. Go to step 4.

3. To connect to a new EZ-KIT Lite session, start **Session Wizard** by selecting one of the following.
    - From the **Session** menu, **New Session**.
    - From the **Session** menu, **Session List**. Then click **New Session** from the **Session List** dialog box.
    - From the **Session** menu, **Connect to Target**.
4. The **Select Processor** page of the wizard appears on the screen. Ensure **Blackfin** is selected in **Processor family**. In **Choose a target processor**, select **ADSP-BF527**. Click **Next**.
5. The **Select Connection Type** page of the wizard appears on the screen. Select **EZ-KIT Lite** and click **Next**.
6. The **Select Platform** page of the wizard appears on the screen. Ensure that the selected platform is **ADSP-BF527 EZ-KIT Lite via Debug Agent**. Specify your own **Session name** for the session or accept the default name.

    The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and open a new session and click **Next.**

7. The **Finish** page of the wizard appears on the screen. The page displays your selections. Check the selections. If you are not satisfied, click **Back** to make changes; otherwise, click **Finish**. VisualDSP++ creates the new session and connects to the EZ-KIT Lite. Once connected, the main window's title is changed to include the session name set in step 6.

To disconnect from a session, click the disconnect button  or select **Session > Disconnect from Target**.

To delete a session, select **Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

CCES Evaluation License

The ADSP-BF527 EZ-KIT Lite software is part of the Board Support Package (BSP) for the Blackfin ADSP-BF52x family. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for 90 days after activation. Once the evaluation period ends, the evaluation license becomes permanently disabled. If the evaluation license is installed but not activated, it allows 10 days of unrestricted use and then becomes disabled. The license can be re-enabled by activation.

An evaluation license can be upgraded to a full license. Licenses can be purchased from:

- Analog Devices directly. Call (800) 262-5645 or 781-937-2384 or go to:
  http://www.analog.com/buyonline.
- Analog Devices, Inc. local sales office or authorized distributor. To locate one, go to:
  http://www.analog.com/salesdir/continent.asp.

The EZ-KIT Lite hardware must be connected and powered up to use CCES with a valid evaluation or full license.

VisualDSP++ Evaluation License

The ADSP-BF527 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ restricts a connection to the ADSP-BF527 EZ-KIT Lite via the USB debug agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a user program to 20 KB of memory for code space with no restrictions for data space.

To avoid errors when opening VisualDSP++, the EZ-KIT Lite hardware must be connected and powered up. This is true for using VisualDSP++ with a valid evaluation or full license.

Lockbox Key Security Features

Blackfin processors feature Lockbox® secure technology: hardware-enabled code security and content protection for one-time programmable (OTP) memory. Customers purchasing Blackfin processors can program their own customer public key in OTP.

The ADSP-BF527 EZ-KIT Lites are evaluation boards with the Lockbox key pre-programmed and publicly documented—the burden of key generation and OTP programming of public keys is removed from the customer. Customers can still program other areas of OTP memory on the ADSP-BF527 EZ-KIT Lite. Analog Devices publicly document the EZ-KIT Lite's public and private key pair for customer evaluation and

support of the Lockbox feature, all while avoiding any keys information exchange. As a result, there is no confidentiality associated with the Lockbox key on EZ-KIT Lites.

To demonstrate Lockbox features using an EZ-KIT Lite, you must use the keys that are provided pre-programmed on your EZ-KIT Lite.

Use the EZ-KIT Lite key pair to generate a demo and then provide the keys to the demo users. Note that the EZ-KIT Lite cannot be used to secure any confidential information. If you wish to create a demo with confidential keys, you must build your own Blackfin board and personalize it with your own keys.

Memory Map

The ADSP-BF527 processor has internal static random access memory (SRAM) used for instructions or data storage. See Table 1-1. The internal memory details can be found in the *ADSP-BF2x Blackfin Processor Hardware Reference.*

The ADSP-BF527 EZ-KIT Lite board includes four types of external memory: synchronous dynamic random access memory (SDRAM), serial peripheral interconnect (SPI), parallel flash, and NAND flash. See Table 1-2. For more information about a specific memory type, go the respective section in this chapter.

Table 1-1. EZ-KIT Lite Internal Memory Map

Start Address	Content
0xEF00 0000	BOOT ROM (32K BYTE)
0xEF00 8000 0xFEB0 0000 0xFEB2 0000 0xFF40 0000 0xFF40 4000 0xFF40 8000 0xFF50 0000 0xFF50 4000 0xFF50 8000 0xFF60 0000 0xFF60 4000 0xFF60 8000 0xFF60 C000 0xFF61 0000 0xFF61 4000 0xFF70 0000 0xFF70 1000	Reserved
0xFF80 0000	L1 DATA BANKA SRAM (16K BYTE)
0xFF80 4000	L1 DATA BANKA SRAM/CACHE (16K BYTE)
0xFF80 8000	Reserved
0xFF90 0000	L1 DATA BANKB SRAM (16K BYTE)
0xFF90 4000	L1 DATA BANKB SRAM/CACHE (16K BYTE)
0xFF90 8000	Reserved
0xFFA0 0000	L1 INSTRUCTION BANKA LOWER SRAM (16K BYTE)
0xFFA0 4000	L1 INSTRUCTION BANKA UPPER SRAM (16K BYTE)
0xFFA0 8000	L1 INSTRUCTION BANKB LOWER SRAM (16 BYTE)
0xFFA0 C000	Reserved
0xFFA1 0000	L1 INSTRUCTION SRAM/CACHE (16K BYTE)

Table 1-1. EZ-KIT Lite Internal Memory Map (Cont'd)

Start Address	Content
0xFFA1 4000 0xFFA1 8000 0xFFA1 C000 0xFFA2 0000 0xFFA2 4000	Reserved
0xFFB0 0000	L1 SCRATCHPAD SRAM (4K BYTE)
0xFFB0 1000	Reserved
0xFFC0 0000	SYSTEM MMR REGISTERS
0xFFE0 0000	CORE MMR REGISTERS

Table 1-2. EZ-KIT Lite External Memory Map

Start Address	End Address	Content
0x0000 0000	0x03FF FFFF	SDRAM bank 0 (SDRAM)
0x2000 0000	0x200F FFFF	ASYNC memory bank 0 (flash)
0x2010 0000	0x201F FFFF	ASYNC memory bank 1 (flash)
0x2020 0000	0x202F FFFF	ASYNC memory bank 2 (flash)
0x2030 0000	0x203F FFFF	ASYNC memory bank 3 (flash)
0x2040 0000	0xEEFF FFFF	Reserved

SDRAM Interface

The ADSP-BF527 processor connects to a 64 MB Micron MT48LC32M16A2TG-75 chip through the external bus interface unit (EBIU). The SDRAM chip can operate at a maximum clock frequency of 133 MHz.

With a CCES or VisualDSP++ session running and connected to the EZ-KIT Lite board via the USB debug agent, SDRAM registers are configured automatically with values listed in Table 1-3 each time the processor is reset. The values are used whenever SDRAM is accessed through the debugger (for example, when viewing memory windows or loading a program).

To disable the automatic setting of the SDRAM registers, do one of the following:

- CCES users, choose **Target > Settings > Target Options** and clear the **Use XML reset values** check box.
- VisualDSP++ users, choose **Settings > Target Options** and clear the **Use XML reset values** check box.

Table 1-3. SDRAM Default Settings With a 133 MHz SCLK

Register	Value	Function
pEBIU_SDRRC	0x0407	Calculated with SCLK = 133 MHz fSCLK = 133 MHz tREF = 64 ms NRA = 8192 row addresses tRAS = 6 clock cycles tRP = 2 clock cycles RDIV = 0x407

Table 1-3. SDRAM Default Settings With a 133 MHz SCLK (Cont'd)

Register	Value	Function
pEBIU_SDBCTL	0x0025	EBCAW = 10 bits EBSZ = 64M byte EBE = enabled
pEBIU_SDGCTL	0x0091998d	TSCSR = 45 degrees C EMREN = disabled FBBRW = disabled PSSE = enables SDRAM powerup sequence on next SDRAM access PSM = precharge, 8 BCBR refresh cycles, mode register set PUPSD = no extra delay added before first precharge command TWR = 2 cycles TRCD = 3 cycles TRP = 3 cycles TRAS = 6 cycles PASR = all 4 banks refreshed CL = CAS latency 3 cycles SCTLE = CLOUT disabled

Table 1-4 shows the PLL register settings using a 400 MHz CCLK and 133 MHz SCLK. The PLL_CTL and PLL_DIV registers are initialized in the user code to achieve maximum performance.

Table 1-4. PLL Register Settings

Register	SCLK = 133 MHz CCLK = 400 MHz
PLL_CTL	16
PLL_DIV	3

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the SDRAM interface. For more information on how to initialize the registers after a reset, search the online help for "reset values".

Parallel Flash Memory Interface

The parallel flash memory interface of the ADSP-BF527 EZ-KIT Lite contains a 4 MB (2M x 16 bits) ST Micro M29W320EB chip. Flash memory is connected to the 16-bit data bus and address lines 1 through 19. Chip enable is decoded by using AMS0–3 select lines through NAND and AND gates. The address range for flash memory is 0x2000 0000 to 0x203F FFFF.

Flash memory is pre-loaded with boot code for the blink, LCD images, and power-on-self test (POST) programs. For more information, refer to "Power-On-Self Test" on page 1-30.

By default, the EZ-KIT Lite boots from the 16-bit parallel flash memory. The processor boots from flash memory if the boot mode select switch (SW2) is set to a position of 1; see "Boot Mode Select Switch (SW2)" on page 2-11.

Flash memory code can be modified. For instructions, refer to the online help and example program included in the EZ-KIT Lite installation directory.

NAND Flash Interface

The ADSP-BF527 processor is equipped with an internal NAND flash controller, which allows the 4 Gbit ST Micro's NAND04 device to be attached gluelessly to the processor. NAND flash is attached via the processor's specific NAND flash control and data lines. NAND flash shares pins with the Ethernet PHY, host connector, and expansion interface.

The NAND chip enable signal (NDCE#_HOSTD10) can be disconnected from NAND flash by turning SW11.4 (switch 11 position 4) OFF. This ensures that the NAND will not be driving data when HOSTD10 changes state. See "Rotary NAND Enable Switch (SW11)" on page 2-16 for more information.

The Ethernet PHY (U14) must be disabled in order for NAND flash to function properly. This is accomplished by setting SW1 to OFF, OFF, ON, OFF.

For more information about the NAND04 device, refer to the Numonyx Web site at http://www.numonyx.com.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the NAND flash interface.

SPI Interface

The ADSP-BF527 processor has one serial peripheral interface (SPI) port with multiple chip select lines. The SPI port connects directly to serial flash memory, LCD, audio codec, and expansion interface.

Serial flash memory is a 16 Mb ST Micro M25P16 device, which is selected using the SPISEL1 line of the processor. SPI flash memory is pre-loaded with boot code for the blink and POST programs. For more information, refer to "Power-On-Self Test" on page 1-30. By default, the EZ-KIT Lite boots from the 16-bit flash parallel memory. SPI flash can be selected as the boot source by setting the boot mode select switch (SW2) to position 3; see "Boot Mode Select Switch (SW2)" on page 2-11.

SPI flash code can be modified. For instructions, refer to the online help and example program included in the EZ-KIT Lite installation directory.

By default, the audio codec is set up to use the SPISEL5 signal as the SPI chip select when configuring the codec. The chip select is shared with the HOSTD9 signal. For more information, refer to "Audio Interface" on page 1-23.

By default, the LCD is setup to use SPISEL7. The LCD optionally can use SPISEL1 or SPISEL5 by setting SW25 appropriately. For more information, refer to "LCD/KPAD CTL Switch (SW25)" on page 2-20.

PPI Interface

The ADSP-BF527 processor provides a parallel peripheral interface (PPI), supporting data widths up to 16 bits. The PPI interface provides three multiplexed frame syncs, a dedicated clock input, and 16 data lines. The EZ-KIT Lite uses an eight-bit data connection to the TFT LCD module. The full PPI port is accessible on the PPI connector P8 and expansion interface.

The PPI signals are connected to multi-function pins; the upper eight data bit signals are configured for the rotary, SPI, UART1, and LED0 interfaces.

The PPI interface is set up to drive the LCD through a complex programmable logic device (CPLD). The CPLD has a 15 MHz oscillator input and drives PPICLK at 5 MHz, 10 MHz or 15 MHz, depending on the LCD display mode chosen. For more information, refer to the "LCD Module Interface" on page 1-19.

The source of the PPI clock can be configured by software via the PPI_SEL signal. The signal connects to the processor's flag pin PG12 by setting SW13 position 4 ON. Flag pin PG12 is shared with the HOSTACK_LED2 signal. When the clock select line is used, HOSTACK and LED2 are not available. The PPISEL signal does not need to be driven if the default CPLD clock is used; PPISEL is driven when the expansion interface is used as the clocking source. Refer to "GPIO Enable Switch (SW13)" on page 2-17 for more information.

LCD Module Interface

The EZ-KIT Lite features a Sharp LQ035Q1DH02 TFT LCD module with touchscreen overlay. This is a 3.5" landscape display with a resolution of 320 x 240 pixels and a color depth of 16 bits. By default, the interface is an RGB-888 serial parallel interface, eight bits of red, followed by eight bits of green, and then eight bits of blue.

To configure the PPI interface, refer to the LCD software example found in the Examples folder of the installation.

The configuration values are obtained from the timing characteristics section of the Sharp LQ035Q1DH02 data sheet.

The LCD interface setup is flexible and allows three data formats: RGB888 (24 bits per pixel), RGB565 (16 bits per pixel), and 16-bit pass through mode. All LCD signals are input from the processor into a Xilinx CPLD (XC95144XL), and the CPLD drives the LCD inputs. By default, switch SW26 is used to interface the LCD module in RGB888 mode.

The other two LCD modes are RGB565, where each pixel is represented by two bytes, and 16-bit pass through, where all 16 bits of the PPI data bus are connected to the CPLD and passed to the LCD. To run RGB565 or 16-bit pass through mode, configure the processor's PPI appropriately. For more information about setting up the LCD interface mode, see "Mode Switch (SW26)" on page 2-21.

When setting up the LCD module in 16-bit pass through mode, ensure PPI data signals PPID15–8 are not used elsewhere on the board because these processor pins are multiplexed with other functionality. Switches SW29 and SW30 disconnect the PPI data lines from the CPLD: turn SW29 all ON and SW30 positions 1 and 2 ON to disconnect PPID15–8 from the CPLD. See "CPLD D8–13 Switch (SW29)" on page 2-22 and "CPLD 14–15/DCE ENB Switch (SW30)" on page 2-22 for more information.

The LCD reset is selectable between the board's $\overline{\text{RESET}}$ signal and GPIO controllable signal HOSTWR#_LED1 (PG11). By default, the LCD reset is connected to the board's $\overline{\text{RESET}}$ signal. See "LCD Reset Switch (SW5)" on page 2-13 for more information.

The verilog source code for the CPLD can be found in the reference resource zip file in the Examples folder of the installation.

The LCD module can be disconnected from PPI by setting Enable2 to high. Refer to "Mode Switch (SW26)" on page 2-21 for more information.

Touchscreen Interface

The AD7879-1 touchscreen controller (U37) is connected to the 2-wire interface (TWI) of the processor. Switch SW22 sets the default I^2C address to 0101111. The AD7879_1_PENIRQ interrupt signal comes from one of the three signals connected to the SW24 switch. The default is LED0. To use two other signals for the touch pad interrupt, set SW24 appropriately. Refer to "Touchpad INT Switch (SW24)" on page 2-20 for more information.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to set up and access the touchscreen interface.

Keypad Interface

The ADP5520 keypad controller is used for keypad functions and connected to the TWI interface of the processor. By default, the keypad interrupt (NINT) is set up to the KEYIRQ signal on the PF9 port pin. To use two other signals for the keypad interrupt, set SW25 accordingly. Refer to "LCD/KPAD CTL Switch (SW25)" on page 2-20 for more information.

The I^2C address of the keypad controller is 0110101. A red LED (LED8) can be used as a general-purpose status LED. LED8 is connected to the ILED pin of the ADP5520 controller (U35).

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the keypad interface.

Rotary Encoder Interface

The ADSP-BF527 processor has a built-in, up-down counter interface with support for a rotary encoder. The three-wire rotary encoder interface connects to the rotary switch (SW3) and expansion interface connector. The rotary encoder can be turned clockwise for the up function, counter clockwise for the down function, or can be used as a push button for clearing the counter.

The rotary switch is a two-bit quadrature (Gray code) counter with detent, meaning that both the down signal (CDG) and up signal (CUD) will toggle when the count register increases on a rotation to the right. Upon rotating to the left, both CDG and CUD will toggle, and the over all count decreases.

If the processor pins are needed for the expansion interface, disconnect the rotary encoder switch via the four-position rotary NAND enable switch (SW11). For more information, see "Rotary NAND Enable Switch (SW11)" on page 2-16.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the rotary encoder interface.

Ethernet Interface

The ADSP-BF527 processor has an integrated Ethernet MAC with media independent interface (MII) and reduced media independent interface (RMII), which connects to an external PHY. The EZ-KIT Lite provides a SMSC LAN8700 RMII Ethernet PHY with Auto-MDIX, fully compliant with IEEE 802.2/802.2u standards. The SMSC LAN8700 chip supports 10BASE-T and 100BASE-TX operations. The part is attached gluelessly to the processor.

The Ethernet signals are shared with NAND flash. By default, Ethernet is turned off (SW1 OFF, OFF, ON, OFF). See "ETH Enable Switch (SW1)" on

page 2-10 for more information. It is important not to run code that accesses the NAND while using the Ethernet interface.

The Ethernet mode is set by the SW9 switch and defaults to all capable, auto negotiation with settings OFF, OFF, OFF, ON. See "ETH Mode Flash CS Switch (SW9)" on page 2-14 for more information.

The Ethernet chip is pre-loaded with a MAC address for the EZ-KIT Lite. The MAC address is stored in the public one-time programmable (OTP) memory of the processor and can be found on a sticker on the bottom side of the EZ-KIT Lite.

The PHY portion of the Ethernet chip is connected to a Pulse HX1188 (U26) magnetics, then to a standard RJ-45 Ethernet connector (J9). For more information, see "Ethernet Connector (J9)" on page 2-30.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate how to use the Ethernet interface.

Audio Interface

The audio interface of the EZ-KIT Lite consists of an internal low-power stereo codec with an integrated headphone driver and its associated passive components. There are two inputs, stereo line in, and mono microphone as well as two outputs, headphone, and stereo line out. The codec has integrated stereo analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) and requires minimal external circuitry.

The codec is connected to the ADSP-BF527 processor via the processor's serial port 0A (alternate). The SPORT0A port is disconnected from the codec by turning SW20 all OFF and SW27 positions 1 and 2 OFF. This allows SPORT0A to be used on the expansion interface.

The TFS0A signal is shared with the Ethernet and host connectors, as well as the RMIIMDINT# and HOSTCE# signals. SW21 allows this signal to be disconnected from the host connector by setting position 1 OFF, and STAMP

connectors position 2 OFF. To connect signal TFS0A_RMIIMDINT#_HOSTCE# to either interface, turn the corresponding switch position ON. Refer to "TFS0A/HOSTCE Enable Switch (SW21)" on page 2-19 for more information.

The control interface for the codec is selectable by the SW8 and SW19 switches between the TWI and SPI. By default, the board is in SPI mode, which is set up by the SW19 switch (ON, OFF, ON, OFF) and SW8 switch (positions 3 ON and 4 OFF). To select TWI mode, turn SW8 positions 3 OFF and 4 ON, as well as SW19 OFF, ON, OFF, ON. Refer to "Mic/HP LPBK Audio Mode Switch (SW8)" on page 2-14 and "SPI/TWI Switch (SW19)" on page 2-19 for more information.

Switch SW28 can be used to tie the LEFT_IN channel to LEFT_OUT and the RIGHT_IN channel to RIGHT_OUT, respectively. See "Line In-Out LPBK Switch (SW28)" on page 2-22 for more information.

Mic gain is selectable through the SW4 switch, with values of 14 dB, 0 dB, or –6 dB, by turning ON position 1, 2, or 3 respectively. All other positions must be OFF to achieve the desired gain. Refer to "MIC Gain Switch (SW4)" on page 2-12 for more information.

Microphone bias is provided through a low-noise reference voltage. A jumper on position 2 and 3 of JP6 connects the MICBIAS signal to the audio jack. Placing the jumper on positions 1 and 2 of JP6 connects the bias directly to the mic signal. Refer to "MIC Select Jumper (JP6)" on page 2-23 for more information.

J7 and J8 are 3.5 mm connectors for the audio portion of the board. J7 connects the mic on the top portion and line-in on the bottom. J8 connects the headphone on the top portion and line-out on the bottom. If there is no 3.5 mm cable plugged into the bottom of J7 or J8, the LINEIN to LINOUT signals are looped back inside the connector, as long as SW23 positions 3 and 4 are ON.

For testing purposes, SW8 positions 1 and 2 allow the MICIN signal to be connected to either the left or right headphone. Do not connect both left

and right to the MICIN signal at the same time—only position 1 or 2 of SW8 should be ON at the same time. Refer to "Mic/HP LPBK Audio Mode Switch (SW8)" on page 2-14 for more information.

For more information, see "Dual Audio Connectors (J7–8)" on page 2-30.

The EZ-KIT Lite is shipped with a headphone and multiple 3.5 mm cables, which allow you to run the example programs provided in the EZ-KIT Lite installation directory and learn about the audio interface.

USB OTG Interface

The ADSP-BF527 processor has a built-in, high-speed USB on-the-go (OTG) interface and integrated PHY. The interface is connected to a 24 MHz clock (U12), has a surge protector, and can be configured as a host or a device. When in device mode, the USB 5V regulator (VR3) and FET switch (U28) are turned OFF. When in host mode, the USB 5V regulator and FET are turned ON and can supply 5V at 500 mA.

The control mechanism to turn the two devices on and off are via the PG13 flag pin of the processor and must be connected on the board to signal USB_VRSEL through switch SW13. By default, USB_VRSEL is held low or a logic 0 via a pull-down resistor, and both devices are turned off. To use host mode and provide 5V to a device, turn SW13 position 2 OFF and position 3 ON. This disables push button 2. Note that signal USB_VRSEL is shared with HOSTADDR. By default, positions 2 and 3 of SW13 are ON and OFF, which shut off the VR3 regulator and U28 FET. For more information, see "GPIO Enable Switch (SW13)" on page 2-17.

The USB OTG interface has a mini-AB connector (P1); cables that plug into P1 are shipped with the EZ-KIT Lite.

Use example programs in the EZ-KIT Lite installation directory to learn about the ADSP-BF527 processor's device and host modes. For more

information about the USB interface, refer to the *ADSP-BF52x Blackfin Processor Hardware Reference*.

UART Interface

The ADSP-BF527 processor has two built-in universal asynchronous receiver transmitters (UARTs). UART1–0 share the processor pins with other peripherals on the EZ-KIT Lite.

UART1 has full RS-232 functionality via the Analog Devices 3.3V ADM3202 line driver and receiver (U25). The UART can be disconnected from the ADM3202 device by turning all positions of SW10 OFF. When using UART1, SW10 position 8 should be OFF. Turning this switch provides UART data loopback and should be ON only when running the POST program. If signals RTS and CTS are needed for flow control, the UART1CTS_LCDSPICS_Z port pin PF10 can be configured as a GPIO for CTS. The HWAIT port pin PG0 can be used for RTS by setting up the pin accordingly. See "UART Enable Switch (SW10)" on page 2-15 for more information.

UART1 signals are connected to the ADM3202 device through the CPLD 14–15/DCE enable switch (SW30). To connect TX and RX signals, turn SW30 positions 3 and 4 ON. Additionally, a flow control can be added by connecting SW30 positions 5 and 6 ON. Refer to "CPLD 14–15/DCE ENB Switch (SW30)" on page 2-22 for more information.

UART0 and UART1 are connected to the expansion interface. UART0 of the processor also is available via a STAMP connector (P5). See "UART0 Connector (P5)" on page 2-31.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate UART and RS-232 operations.

For more information about the UART interface, refer to the *ADSP-BF52x Blackfin Processor Hardware Reference*.

RTC Interface

The ADSP-BF527 processor has a real-time clock (RTC) and a watchlog timer. Typically the RTC interface is used to implement a real-time watchlog or life counter of the time elapsed since the last system reset. The EZ-KIT Lite is equipped with a Sanyo (CR2430) lithium coin 3V battery supplying 280 mAh. The 3V battery and 3.3V supply of the board are connected to the `RTC` power pin of the processor. When the EZ-KIT Lite is powered, the RTC circuit uses the board power to supply voltage to the `RTC` pin. When the EZ-KIT Lite is not powered, the RTC circuit uses the lithium battery to maintain the power to the `RTC` pin. After removing the mylar, the battery will last for about one year with the EZ-KIT Lite unpowered.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate the RTC features.

The EZ-KIT Lite is shipped with a protective Mylar sheet placed between the coin battery and positive pin of the battery holder. Please remember to remove the Mylar sheet before trying to use RTC functionality of the processor.

For more information on the RTC and watchdog timer, refer to the *ADSP-BF52x Blackfin Processor Hardware Reference*.

LEDs and Push Buttons

The EZ-KIT Lite provides two push buttons and three LEDs for general-purpose I/O.

The three LEDs, labeled `LED1` through `LED3`, are accessed via the `PF8`, `PG11`, and `PG12` pins of the processor, respectively. For information on how to program the pins, refer to the *ADSP-BF52x Blackfin Processor Hardware Reference*.

LED0 is shared with a touchscreen controller interrupt and PPI data pin 8. LED1 is shared with the HOSTWR# signal, keypad controller interrupt, touchscreen controller interrupt, and LCD reset. LED2 is shared with the HOSTACK signal. The LED1 signal can be used for the LCD reset by turning SW5 positions 1 ON and 2 OFF. LED2 is shared with HOSTACK and PPI_SEL functionality. Refer to "LCD Reset Switch (SW5)" on page 2-13, "Touchpad INT Switch (SW24)" on page 2-20, "LCD/KPAD CTL Switch (SW25)" on page 2-20, and "GPIO Enable Switch (SW13)" on page 2-17 for configuration options.

The two general-purpose push buttons are labeled PB1 and PB2. The status of each individual button can be read through programmable flag inputs, PG0 and PG13. The flag reads 1 when a corresponding switch is being pressed. When the switch is released, the flag reads 0. A connection between the push button and processor input is established through the SW13 DIP switch.

Push button 1 is shared with HWAIT. Push button 2 is shared with HOSTADDR and also can be connected to USB_VRSEL by setting SW13 position 2 OFF and position 3 ON. USB_VRSEL allows the USB OTG to power an external USB device with 5V. See "USB OTG Interface" on page 1-25 and "GPIO Enable Switch (SW13)" on page 2-17 for more information.

An example program is included in the EZ-KIT Lite installation directory to demonstrate functionality of the LEDs and push buttons.

JTAG Interface

The JTAG emulation port allows an emulator to access the processor's internal and external memory through a six-pin interface. The JTAG emulator port of the processor can be accessed via the on-board USB debug agent or with an external emulator via the JTAG connector (ZP4). When an external emulator connects to the board, the on-board USB debug agent is disabled. See "JTAG Connector (ZP4)" on page 2-35 for more information.

For more information about emulators, contact Analog Devices or go to: http://www.analog.com/processors/tools/blackfin.

Expansion Interface

The expansion interface consists of three 90-pin connectors (J1–3). These connectors contain a majority of the ADSP-BF527 processor's signals. For the pinout of the connectors, go to "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1. The expansion interface allows an EZ-Extender® or a custom-design daughter board to be tested across various hardware platforms. The mechanical dimensions of the expansion connectors can be obtained by contacting Technical Support.

Analog Devices offers many EZ-Extender products. For more information about EZ-Extenders, visit the Analog Devices Web site at: http://www.analog.com/processors/tools/blackfin.

Limits to current and interface speed must be taken into consideration when using the expansion interface. Current for the expansion interface is sourced from the EZ-KIT Lite; therefore, the current should be limited to 1A for both the 5V and 3.3V planes. If more current is required, then a separate power connector and a regulator must be designed on a daughter card. Additional circuitry can add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

Power Measurements

Several locations are provided for measuring the current draw from various power planes. Precision 0.05 ohm shunt resistors are available on the VDDINT, VDDEXT, and VDDMEM pins. For current draw measuments, the associated jumper (P14, P15, or P16) should be removed. Once the jumper is

removed, voltage across the resistor can be measured using an oscilloscope. Once voltage is measured, current can be calculated by dividing the voltage by 0.05. For the highest accuracy, a differential probe should be used for measuring the voltage across the resistor.

For more information, see "VDDINT Power Jumper (P14)", "VDDEXT Power Jumper (P15)", and "VDDMEM Power Jumper (P16)" on page 2-25.

Power-On-Self Test

The power-on-self program (POST) tests all EZ-KIT Lite peripherals and validates functionality as well as connectivity to the processor. Once assembled, each EZ-KIT Lite is fully tested for an extended period of time with a POST. All EZ-KIT Lites are shipped with the POST preloaded into parallel flash (U5) and SPI flash (U8) memories. The POST is executed by resetting the board and pressing the proper push button(s). The POST also can be used for reference for a custom software design or hardware troubleshooting.

When running the POST, you may need to place switches and jumpers in specific test modes. In some instances, such as Ethernet, you may need to plug in an Ethernet loopback connector (provided with the EZ-KIT Lite) to run the POST. The user LEDs (LED1–3) convey whether the specific tests have passed or failed.

Note that the source code for the POST program is included in the EZ-KIT Lite installation directory along with the readme file, which describes how the board is configured to run POST.

The POST program is only available when using VisualDSP++.

Example Programs

Example programs are provided with the ADSP-BF527 EZ-KIT Lite to demonstrate various capabilities of the product. The programs are included in the product installation kit and can be found in the `Examples` folder of the installation. Refer to a readme file provided with each example for more information.

CCES users are encouraged to use the example browser to find examples included with the EZ-KIT Lite Board Support Package.

Board Design Database

A `.zip` file containing all of the electronic information required for the design, layout, fabrication and assembly of the product is available for download from the Analog Devices board design database at: `http://www.analog.com/board-design-database`.

2 ADSP-BF527 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF527 EZ-KIT Lite board.

The following topics are covered.

- "System Architecture" on page 2-2
  Describes the ADSP-BF527 EZ-KIT Lite board configuration and explains how the board components interface with the processor.
- "Programmable Flags" on page 2-3
  Shows the locations and describes the programming flags (PFs).
- "Push Buttons and Switches" on page 2-10
  Shows the locations and describes the on-board push buttons and switches.
- "Jumpers" on page 2-23
  Shows the locations and describes the on-board configuration jumpers.
- "LEDs" on page 2-26
  Shows the locations and describes the on-board LEDs.
- "Connectors" on page 2-28
  Shows the locations and provides part numbers for the on-board connectors. In addition, the manufacturer and part number information is provided for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board (Figure 2-1).

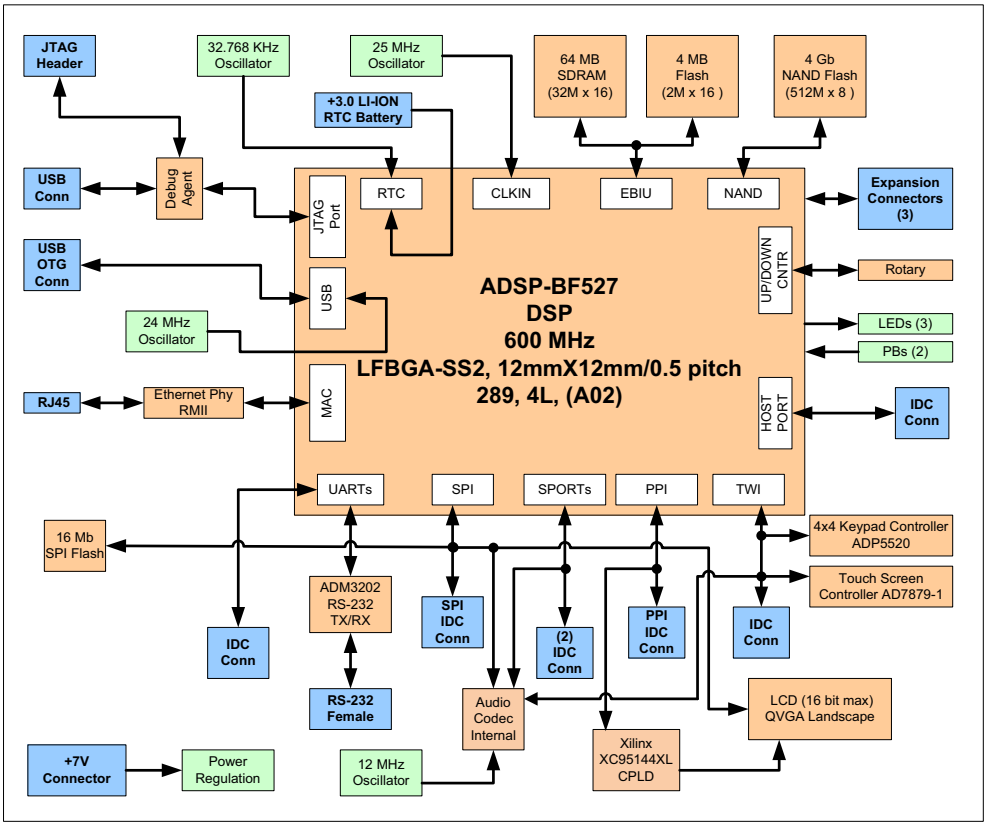


Figure 2-1. System Architecture

The EZ-KIT Lite is designed to demonstrate the ADSP-BF527 processor capabilities. The processor has an I/O voltage of 3.3V. The core voltage of the processor is controlled by the internal voltage regulator.

The core voltage and clock rate can be set on the fly by the processor. The input clock is 25 MHz. A 32.768 kHz crystal supplies the real-time clock (RTC) inputs of the processor. The default boot mode for the processor is external parallel flash boot. See "Boot Mode Select Switch (SW2)" on page 2-11 for information on how to change the default boot mode.

Programmable Flags

The processor has 50 general-purpose input/output (GPIO) signals spread across four ports (PF, PG, PH, and PJ). The pins are multi-functional and depend on the ADSP-BF527 processor setup. The following tables show how the programmable flag pins are used on the EZ-KIT Lite.

- PF programmable flag pins in Table 2-1
- PG programmable flag pins in Table 2-2
- PH programmable flag pins in Table 2-3
- PJ programmable flag pins in Table 2-4

Table 2-1. PF Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PF0	PPID0/DR0PRI/ND_D0A	Default: LCD via CPLD. Expansion interface via J1.72. PPI connector via P8.8.
PF1	PPID1/RFS0/ND_D1A	Default: LCD via CPLD. Expansion interface via J1.73. PPI connector via P8.9.
PF2	PPID2/RSCLK0/ND_D2	Default: LCD via CPLD. Expansion interface via J1.74. PPI connector via P8.10.
PF3	PPID3/DT0PRI/ND_D3A	Default: LCD via CPLD. Expansion interface via J1.75. PPI connector via P8.11.

Table 2-1. PF Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PF4	PPID4/TFS0/ND_D4A/ TACLK0	Default: LCD via CPLD. Expansion interface via J2.43. PPI connector via P8.12.
PF5	PPID5/TSCLK0/ND_D5A/ TACLK1	Default: LCD via CPLD. Expansion interface via J2.44. PPI connector via P8.13.
PF6	PPID6/DT0SEC/ND_D6A/ TACI0	Default: LCD via CPLD. Expansion interface via J2.45. PPI connector via P8.14.
PF7	PPID7/DR0SEC/ND_D7A/ TACI1	Default: LCD via CPLD. Expansion interface via J2.46. PPI connector via P8.15.
PF8	PPID8/DR1PRI	Default: LED1. LCD via CPLD, SW29, and JP15. Touchscreen interrupt via SW24.1 and JP15. Expansion interface via J1.79, J2.29, and J2.47. Via a quick switch U30 and JP15 to the following connectors: SPORT0 P6.25, SPORT1 P7.8, SPI P9.14, TWI P10.10, and PPI P8.24.
PF9	PPID9/RSCLK1/SPISEL6#	Default: KEYIRQ# (U35) via SW25.4. LCD via CPLD and SW29. Expansion interface via J2.48 and J2.33. Via a quick switch U38 to SPORT1 connector P7.16 and PPI connector P8.17.
PF10	PPID10/PRFS1/SPISEL7#	Default: $\overline{\text{LCD\_SPICS}}$ via SW25.1. LCD via CPLD and SW29. CTS UART1 U25 via SW10.3 and SW30. Expansion interface via J2.31 and J2.49. Via a quick switch U38 to SPORT1 connector P7.7 and PPI connector P8.18.
PF11	PPID11/TFS1/CZM	Default: CZM rotary (SW3) via SW11.3. LCD via CPLD and SW29. Expansion interface via J2.32 and J2.50. Via a quick switch U30 to PPI connector P8.19 and SPORT1 connector P7.11.

Table 2-1. PF Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PF12	PPID12/DT1PRI/ SPISEL2#/CDG	Default: CDG rotary (SW3) via SW11.2. LCD via CPLD and SW29. Expansion interface via J2.30 and J2.51. Via a quick switch U31 to the following connectors: SPI P9.9, SPORT1 P7.14 and P7.19, PPI P8.20 and P8.26, SPORT0 P6.19.
PF13	PPID13/TSCLK1/ SPISEL3#/CUD	Default: CUD rotary (SW3) via SW11.1. LCD via CPLD and SW29. Expansion interface via J2.34 and J2.52. Via a quick switch U30 to the following connectors: SPORT1 P7.6 and P7.21, SPORT0 P6.21, PPI P8.21 and P8.25, SPI P9.12.
PF14	PPID14/DT1SEC/UART1TX	Default: UART1 (U25) TX via SW30. LCD via CPLD and SW30. Expansion interface via J2.28, J2.53, J2.55, J3.8. Via a quick switch U38 to SPORT1 connector P7.12, and PPI connector P8.22.
PF15	PPID15/DR1SEC/UART1RX/TACI3	Default: UART1 (U25) RX via SW10.2 and SW30. LCD via CPLD and SW30. Expansion interface via J2.27, J2.54, J2.56, J3.7, SPORT1 connector P7.10, and PPI connector P8.23

Table 2-2. PG Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PG0	HWAIT	Default: PB1 via SW13.1. UART1 RTS (HWAIT) via SW10.1 and SW30, host connector P13.12, and expansion interface J1.84.
PG1	SPISS#/SPISEL1#	Default: SPI flash (U8) CS via SW9.4. LCD CS via SW25.2, expansion interface J2.11, via quick switch U31 to the following connectors: SPI P9.10, PPI P8.27, SPORT0 P6.17, and SPORT1 P7.17.

Table 2-2. PG Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PG2	SPISCK	Default: SPI flash (U8), codec (U2) via SW19, and LCD. Expansion interface J2.9, via quick switch U31 to the following connectors: SPI P9.8, SPORT0 P6.22, SPORT1 P7.22, and PPI P8.34.
PG3	SPIMISO/DR0SECA	Default: SPI flash (U8) and LCD. Via a quick switch (U31) to the following connectors: SPI P9.6, SPORT0 P6.10 and P6.20, SPORT1 P7.20, and PPI P8.32, and expansion interface J2.12, J2.35.
PG4	SPIMOSI/DT0SECA	Default: SPI flash (U8), codec (U2) via SW19, and LCD. Via a quick switch (U31) to the following connectors: SPORT0 P6.12 and P6.18, SPORT1 P7.18, SPI P9.5, PPI P8.30, and expansion interface J2.10, J2.36.
PG5	TMR1/PPIFS2/TFS0A	Default: LCD via CPLD. PPI connector P8.33, expansion interface J2.24.
PG6	DT0PRIA/TMR2/PPIFS3	Default: SPORT0 audio codec (U2) via SW20.2. Via JP14 to PPI connector P8.29 and SPORT0 connector P6.14. Expansion interface via J2.38, J2.23.
PG7	TMR3/DR0PRIA/UART0TX	Default: SPORT0 audio codec (U2) via SW20.3. Via a quick switch (U34) to the following connectors: UART0 P5.6, SPORT0 P6.8 and P6.28, SPORT1 P7.28, timers P11.6, and expansion interface J2.37, J3.6.
PG8	TMR4/RFS0A/UART0RX/ TACI4	Default: SPORT0 audio codec (U2) via SW20.4. Via a quick switch (U34) to the following connectors: SPORT0 P6.7 and P6.30, SPORT1 P7.30, timers P11.8, UART0 P5.10, and expansion interface J2.39, J3.5.
PG9	TMR5/RSCLK0A/TACI5	Default: SPORT0 audio codec (U2) via SW23.2. Via a quick switch (U34) to the following connectors: SPORT0 P6.32 and P6.16, SPORT1 P7.32, timers P11.10, and expansion interface J2.41.
PG10	TMR6/TSCLK0A/TACI6	Default: SPORT0 audio codec (U2) via SW23.1. SPORT0 connector P6.6, expansion interface J2.42.

Table 2-2. PG Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PG11	TMR7/HOST_WR#	Default: LED2. Keypad interrupt via SW25.5, touchscreen interrupt via SW24.2, LCD reset via SW5.1. Host connector P13.4, via a quick switch to the following connectors: SPORT0 P6.27, UART0 P5.3, SPORT1 P7.29, TWI P10.9, timers P11.3, SPI P9.15, and expansion interface J1.80.
PG12	DMAR1/UART1TXA/ HOST_ACK	Default: LED3. PPI_SEL via SW13.4, host connector P13.10, via a quick switch (U30) to the following connectors: UART0 P5.5, timers P11.5, TWI P10.12, SPORT0 P6.29, SPORT1 P7.31, SPI P9.16, and expansion interface J1.81.
PG13	DMAR0/UART1RXA/ HOST_ADDR/TACI2	Default: PB2 via SW13.2. OTG USB_VRSEL via SW13.3 ON and SW13.2 OFF, host connector P13.8, and expansion interface J1.85.
PG14	TSCLK0A/MDC/HOST_RD#	Default: host connector P13.6. MDIO PHY (U14) via SW1.2, expansion interface J3.41.
PG15	TFS0A/MIIPHYINT#/ RMIIMDINT#/HOST_CE#	Default: SPORT0 audio codec (U2) via SW20.1. RMIIMDINT# PHY (U14), host connector P13.6, SPORT0 connector P6.11, and expansion interface J2.40, J3.31.

Table 2-3. PH Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PH0	ND_D0/MIICRS/ RMIICRSDV/HOST_D0	Default: NAND Data 0 (U4). RMII carrier sense/receive data valid (U14.36), host connector data 0 (P13.31), and expansion interface (J3.40).
PH1	ND_D1/ERXER/HOST_D1	Default: NAND Data 1 (U4). PHY receive error (U14.21), host connector data 1 (P13.29), expansion interface (J3.39).

Table 2-3. PH Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PH2	ND_D2/MDIO/HOST_D2	Default: NAND Data 2 (U4). PHY management bus MDIO via SW1.1, host connector data 2 (P13.27), and expansion interface (J3.42).
PH3	ND_D3/ETXEN/HOST_D3	Default: NAND Data 3 (U4). PHY transmit enable (U14.6), host connector data 3 (P13.25), and expansion interface (J3.15).
PH4	ND_D4/MIITXCLK/ RMIIREF_CLK/ HOST_D4	Default: NAND Data 4 (U4). PHY RMII ref clock (U14.14) via SW1.3 OFF, oscillator output U24, host connector data 4 (P13.23), and expansion interface (J3.16).
PH5	ND_D5/ETXD0/HOST_D5	Default: NAND Data 5 (U4). PHY RMII transmit data 0 (U14.23), host connector data 5 (P13.21), and expansion interface (J3.11).
PH6	ND_D6/ERXD0/HOST_D6	Default: NAND Data 6 (U4). PHY RMII receive data 0 (U14.18), PHY mode via SW9.3, host connector data 6 (P13.19), and expansion interface (J3.33).
PH7	ND_D7/ETXD1/HOST_D7	Default: NAND Data 7 (U4). PHY RMII transmit data 1 (U14.24), host connector data 7 (P13.17), and expansion interface (J3.12).
PH8	SPISEL4#/ERXD1/ HOST_D8/TACLK2	Default: NAND Data 7 (U4). PHY RMII transmit data 1 (U14.24), keypad/touch-screen chip select via SW18.2, host connector data 8 (P13.17), and expansion interface (J3.12).
PH9	SPISEL5#/ETXD2/ HOST_D9/TACLK3	Default: SPI SEL5 audio codec U2. Host connector data 9 (P13.13), expansion interface (J3.13).
PH10	ND_CE#_ERXD2/HOST_D10	Default: NAND chip enable via SW11.4 ON. Host connector data 10 (P13.17), expansion interface (J3.35).
PH11	ND_WE/ETXD3/HOST_D11	Default: NAND write enable (U4). Host connector data 11 (P13.9), expansion interface (J3.14).

Table 2-3. PH Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PH12	ND_RE/ERXD3/HOST_D12	Default: NAND output enable (U4). Host connector data 12 (P13.7), expansion interface (J3.36).
PH13	ND_BUSY/ERXCLK/ HOST_D13	Default: NAND busy (U4). Host connector data 13 (P13.5), expansion interface (J3.38).
PH14	ND_CLE/ERXDV/HOST_D14	Default: NAND command latch enable (U4). Host connector data 14 (P13.3), expansion interface (J3.37).
PH15	ND_ALE/COL/HOST_D15	Default: NAND address latch enable (U4). Host connector data 15 (P13.1), expansion interface (J3.32).

Table 2-4. PJ Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PJ0	PPIFS1/TMR0	Default: LCD via CPLD. PPI connector (P8.31), expansion interface (J2.25).
PJ1	PPICLK/TMRCLK	Default: LCD via CPLD. Output of switch (U20), PPI connector (P8.6), and expansion interface (J1.71).
PJ2	SCL	Default: touchscreen (U37). Codec via SW19.4, expansion interface (J2.57), the following connectors via a quick switch (U31): TWI (P10.5), PPI (P8.38), SPORT0 (P6.26), and SPORT1 (P7.26).
PJ3	SDA	Default: touchscreen (U37). Codec via SW19.4, expansion interface (J2.58), the following connectors via a quick switch (U31): TWI (P10.6), PPI (P8.36), SPORT0 (P6.24), and SPORT1 (P7.24).

Push Buttons and Switches

This section describes operation of the push buttons and switches. The push button and switch locations are shown in Figure 2-2.

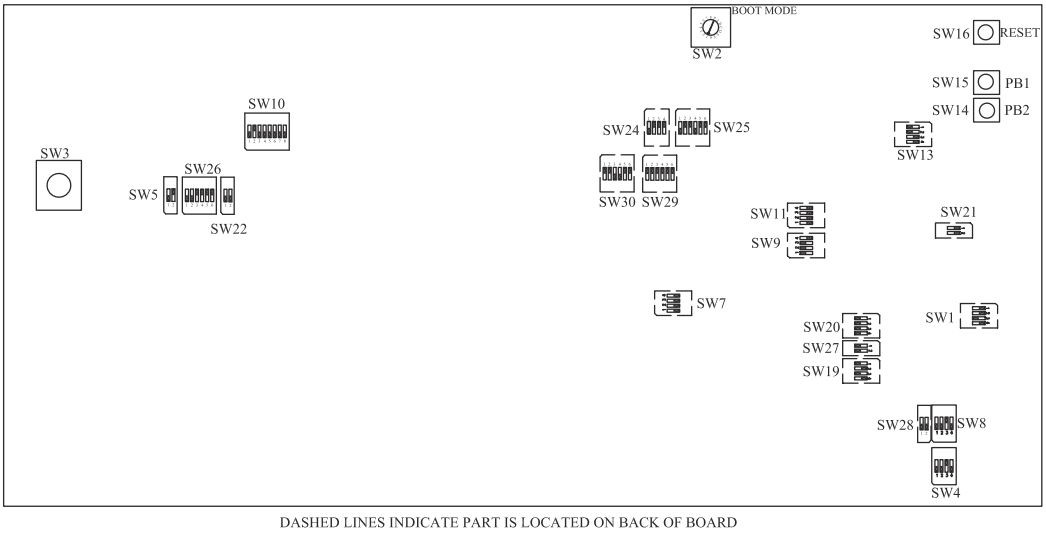


Figure 2-2. Push Button and Switch Locations

ETH Enable Switch (SW1)

The Ethernet enable switch (SW1) allows the Ethernet to operate. Ethernet and NAND flash share the same lines and cannot operate at the same time. By default, SW1 is OFF, OFF, ON, OFF (see Table 2-5). Ethernet is enabled by setting the switch to ON, ON, OFF, ON. SW1 positions 1 and 2 connect the management bus (MDIO and MDC). SW1 position 3 enables the 50 MHz RMII clock. SW1 position 4 holds the PHY in reset (set to OFF) or connects the PHY reset to the EZ-KIT Lite reset (set to ON).

Table 2-5. ETH Enable Switch (SW1)

SW1 Switch Setting	Ethernet Mode
OFF, OFF, ON, OFF	**OFF (default)**
ON, ON, OFF, ON	ON

Boot Mode Select Switch (SW2)

The rotary switch (SW2) determines the boot mode of the processor. Table 2-6 shows the available boot mode settings. By default, the ADSP-BF527 processor boots from the on-board parallel flash memory.

The selected position of SW2 is marked by the notch down the entire rotating portion of the switch, not the small arrow.

Table 2-6. Boot Mode Select Switch (SW2)

SW2 Position	Processor Boot Mode
0	Reserved
1	**Boot from 8-bit external flash memory (default)**
2	Boot from 16-bit asynchronous FIFO
3	Boot from serial SPI memory
4	Boot from SPI host device
5	Boot from serial TWI memory
6	Boot from TWI host
7	Boot from UART0 host
8	Boot from UART1 host
9	Reserved
A	Boot from SDRAM
B	Reserved
C	Boot from 8-bit NAND flash PORTF
D	Boot from 8-bit NAND flash PORTH

Table 2-6. Boot Mode Select Switch (SW2) (Cont'd)

SW2 Position	Processor Boot Mode
E	Boot from 16-bit host DMA
F	Boot from 8-bit host DMA

Rotary Encoder With Momentary Switch (SW3)

The rotary encoder (SW3) can be turned clockwise for an up count or counter-clockwise for a down count. The encoder also features a momentary switch, activated by pushing down the switch and setting the counter to zero. The rotary encoder is a two-bit quadrature (Gray code) encoder. Refer to the "Rotary Counter" section in the *ADSP-BF52x Hardware Reference Manual* for additional information about interfacing with the rotary encoder.

The rotary encoder can be disconnected from the processor by setting the rotary enable switch SW11 positions 1, 2 and 3 to OFF. See "Rotary NAND Enable Switch (SW11)" on page 2-16 for more information.

MIC Gain Switch (SW4)

The microphone gain switch (SW4) sets the gain of the MIC signal, which is connected to the top 3.5 mm jack (J7). The gain can be set to 14 dB, 0 dB, or –6 dB by turning position 1, 2 or 3 of the switch ON (see Table 2-7). When the corresponding position for the desired gain is ON, the remaining positions should be OFF. Refer to "Audio Interface" on page 1-23 for more information about the audio codec.

Table 2-7. MIC Gain Switch (SW4)

Gain	SW4 Switch Settings
5 (14 dB)	ON, OFF, OFF, OFF
1 (0 dB)	OFF, ON, OFF, OFF

Table 2-7. MIC Gain Switch (SW4) (Cont'd)

Gain	SW4 Switch Settings
0.5 (–6 dB)	**OFF, OFF, ON, OFF (default)**
Unused	OFF, OFF, OFF, OFF

LCD Reset Switch (SW5)

The LCD reset switch (SW5) in default mode connects the general $\overline{\text{RESET}}$ line to the $\overline{\text{LCD\_RESET}}$ line. By default, SW5.2 is ON. When SW5.1 is set to ON, $\overline{\text{LCD\_RESET}}$ comes from HOSTWR#_LED1 (see Table 2-8).

Table 2-8. LCD Reset Switch (SW5)

SW5 Position (Default)	From	To	Function
1 (OFF)	Processor (U2, PG11)	LCD RESET	Resets the LCD through the processor's PG11 pin
2 (ON)	Main reset (U27)	LCD RESET	Reset the LCD through the main reset

Flash Enable Switch (SW7)

The flash enable switch (SW7) disconnects $\overline{\text{AMS}}$ signals from flash memory, allowing other devices to utilize the signals via the expansion interface. For each switch listed in Table 2-9 that is turned OFF, the size of available flash memory is reduced by 1 MB.

Table 2-9. Flash Enable Switch (SW7)

SW7 Switch Position (Default)	Processor Signal
1 (ON)	$\overline{\text{AMS0}}$
2 (ON)	$\overline{\text{AMS1}}$

Table 2-9. Flash Enable Switch (SW7) (Cont'd)

SW7 Switch Position (Default)	Processor Signal
3 (ON)	$\overline{\text{AMS2}}$
4 (ON)	$\overline{\text{AMS3}}$

Mic/HP LPBK Audio Mode Switch (SW8)

The audio mode select switch SW8 places the EZ-KIT Lite in loopback mode to test signal/circuit continuity and functionality (see "Power-On-Self Test" on page 1-30).

SW8 positions 1 and 2 connect the MICIN signal to the headphone left and right outputs for audio loopback. Do not turn SW8 positions 1 and 2 ON at the same time.

SW8 positions 3 and 4 select the control interface for the audio codec. SW8 position 3 ON and 4 OFF select SPI interface, while position 3 OFF and position 4 ON select TWI mode. The SW8 default settings are OFF, OFF, ON, OFF. See "SPI/TWI Switch (SW19)" on page 2-19 for more information.

ETH Mode Flash CS Switch (SW9)

The Ethernet mode flash CS switch (SW9) sets the bootstrapping options for the LAN8700 RMII PHY chip (U14). Table 2-10 shows the SW9 default as well as the alternate switch settings.

SW9 position 4 disconnects SPISEL1 from the SPI flash chip (U8). Setting SW9 position 4 OFF is useful when using SPISEL1 on the expansion interface at connector J2 pin 11. By default, SW9 position 4 is ON.

Table 2-10. ETH Mode Flash CS Switch (SW9)

SW9 Switch Setting	MODE[2:0] Setting	Mode Definitions
OFF, OFF, OFF	**111**	**All capable, auto negotiation (default)**
OFF, OFF, ON	110	Power down mode
OFF, ON, OFF	101	Repeater mode, auto negotiation
OFF, ON, ON	100	100Base-TX half duplex advertised, auto negotiation
ON, OFF, OFF	011	100Base-TX full duplex
ON, OFF, ON	010	100Base-TX half duplex
ON, ON, OFF	001	10Base-T full duplex
ON, ON, ON	000	10Base-T half duplex

UART Enable Switch (SW10)

The UART enable switch (SW10) disconnects UART1 signals from the GPIO pins of the processor (see Table 2-11). When SW10 is OFF, its associated GPIO signals can be used for other functions. By default, SW10 is OFF, ON, OFF, OFF, OFF, OFF, OFF, OFF. Flow control is not implemented in POST programs, so SW10 positions 1 and 3 are OFF. Refer to the ADM3202 data sheet for more information about the UART interface.

Table 2-11. UART Enable Switch (SW10)

POS	From	To	Default	Alternate Function
SW10.1	HWAIT_PUSHBUTTON1 (PG0) (U2)	T2IN in U25	OFF	Ties URT1RTS to T2IN
SW10.2	UART1RX (PF15) (U2)	U25	ON	Disconnects UART1RX
SW10.3	UART1CTS_LCDSPICS (PF10) (U2)	R2OUT in U25	OFF	CTS flow control signal
SW10.4	R2OUT	T2IN in U25	OFF	Loopback of CTS to RTS

Table 2-11. UART Enable Switch (SW10) (Cont'd)

POS	From	To	Default	Alternate Function
SW10.5	R2OUT	SOFT_RESET	OFF	Soft resets the processor through UART
SW10.6	Pin 7 in J4	R2IN in U25	OFF	Ties pin 7 in J4 to R2IN
SW10.7	Pins 1, 4, 6 in J4	R2IN in U25	OFF	Ties pins 1, 4, 6 in J4 to R2IN
SW10.8	UART1TX	UART1RX	OFF	Loopback of TX to RX

Rotary NAND Enable Switch (SW11)

The rotary NAND enable switch (SW11) disconnects the rotary encoder signals from the GPIO pins of the processor. When SW11 is OFF, its associated GPIO signals can be used on the host interface (see Table 2-12). Position 4 of SW11 disconnects the chip enable for NAND flash memory (U4).

Table 2-12. Rotary NAND Enable Switch (SW11)

SW11 Position (Default)	From	To	Alternate Function/OFF Mode
1 (ON)	Encoder (SW3)	Processor (U2, PF13)	Expansion interface (J2.34, J2.52) STAMP buffer (U34)
2 (ON)	Encoder (SW3)	Processor (U2, PF12)	CS audio codec (U2), CS keypad/touch controller (U16), expansion interface (J2.30, J2.51), STAMP buffer (U30)
3 (ON)	Encoder (SW3)	Processor (U2, PF11)	Expansion interface (J2.32, J2.50), STAMP buffer (U34)
4 (ON)	Processor (U2, PH10)	NAND (U4)	Host connector (P13.11), expansion interface (J3.35)

GPIO Enable Switch (SW13)

The general-purpose input/output (GPIO) switch (SW13) disconnects the associated push buttons and LED circuits from the GPIO pins of the processor and allows the signals to be used for other functions. Depending on the switch configuration, the signals can be used as PPI clock select, keypad_busy, or OTG host mode 5V select (see Table 2-13).

Table 2-13. GPIO Enable Switch (SW13)

SW13 Position (Default)	From	To	Function
1 (ON)	Push button 1	Processor (U2, PG0)	ON (PB1), OFF (UART1 CTS U25, host connector P13.12, keypad busy SW13.8, expansion interface J1.84)
2 (ON)	Push button 2	Processor (U2, PG13)	ON (PB2), OFF (host connector P13.8, OTG voltage select SW13.7, expansion interface J1.85)
3 (OFF)	OTG PWR (VR3, U28)	Processor (U2, PG13)	OFF (host connector P13.8, expansion interface J1.85), ON (PB2 SW13.11, OTG power VR3, U28)
4 (OFF)	Processor (U2, PG12)	PPI CLK (U20)	OFF (LED2, host connector P13.10, expansion interface J1.81, STAMP buffer U34), ON (PPI CLK U20)

To select an on-board or external PPI clock through software, set SW13 position 4 ON. Drive the PG12 programmable flag to low (0) to connect an external expansion interface clock. Drive PG12 high to select the on-board PPI oscillator. By default, SW13 position 4 is OFF, and the PPI clock source is on-board.

The USB_VRSEL signal is used to provide 5V to a device connected over the USB OTG interface when running in host mode. Signal USB_VRSEL is connected by setting SW13 position 2 OFF and position 3 ON. Then the PG13 programmable flag pin of the processor can be used to control the 5V regulator (VR3). Refer to "USB OTG Interface" on page 1-25 for more information.

Programmable Flag Push Buttons (SW14–15)

Two momentary push buttons (SW14–15) are provided for general-purpose user input. The push buttons are connected to the PG0 and PG13 GPIO pins of the processor. The push buttons are active high and, when pressed, send a high (1) to the processor. The GPIO enable switch (SW13) disconnects the push buttons from the corresponding PB signal. Refer to "GPIO Enable Switch (SW13)" on page 2-17 for more information.

Reset Push Button (SW16)

The reset push button (SW16) resets the following ICs.

- Processor (U2), parallel flash (U5), PHY (U14) if SW1 position 4 is ON
- LCD (P12) if SW5 position 1 is OFF and 2 is ON
- CPLD (U34)

The reset push button does not reset the following ICs.

- SDRAM (U7), NAND flash (U4), SPI flash (U8)
- Audio codec (U2), keypad controller (U35), touchscreen controller (U37)
- UART1 (U25)

The reset push button does not reset the debug agent once it has been connected to a PC. The USB chip is not reset when the push button is pressed after the USB cable has been plugged in and communication with the PC has been initialized correctly. After USB communication has been initialized, the only way to reset the USB chip is by powering down the board.

SPI/TWI Switch (SW19)

The SPI/TWI switch (SW19) selects the control interface for the audio codec. By default, SW19 is ON, OFF, ON, OFF (SPI interface is selected). TWI is selected by setting SW19 to OFF, ON, OFF, ON. See "Mic/HP LPBK Audio Mode Switch (SW8)" on page 2-14 for more information on how to set up the audio mode.

SPORT0A ENBL Switches (SW20 and SW27)

The SPORT0A enable switches (SW20 and SW27) connect the SPORT0A interface of the processor to the audio codec. When SPORT0A is needed at the expansion interface, turn SW20, SW27.1, and SW27.2 all OFF. By default, the switches are all ON.

TFS0A/HOSTCE Enable Switch (SW21)

The TFS0A/HOSTCE enable switch (SW21) disconnects the PG15 programmable flag signal TFS0A_RMIIMDINT#_HOSTCE# from SPORT0 (position 1) connector P6 pin 11 and host connector (position 2) P13 pin 6. By default, SW21 is OFF, OFF.

Touch ADD Switch (SW22)

The touchscreen address switch (SW22) sets the I^2C address of the AD7879-1 controller (U37) as shown in Table 2-14.

Table 2-14. AD7879-1 (U37) I^2C Address Options

SW22.1 Setting	SW22.2 Setting	I^2C Address
ON	ON	0101 100
ON	OFF	0101 101

Table 2-14. AD7879-1 (U37) I^2C Address Options (Cont'd)

SW22.1 Setting	SW22.2 Setting	I^2C Address
OFF	ON	0101 110
OFF	**OFF**	**0101 111 (default)**

Touchpad INT Switch (SW24)

The touchpad interrupt switch (SW24) selects a GPIO signal as the AD7879-1 controller's (U37) interrupt signal. The signal options are:

- LED0 (PF8) on position 1
- HOSTWR#_LED1 (PG11) on position 2
- SPISEL5#_HOSTD9 (PH9) on position 3

Position 4 is not connected to any signals. By default, SW24 is ON, OFF, OFF, OFF.

LCD/KPAD CTL Switch (SW25)

The LCD/keypad control switch (SW25) selects the LCD SPI chip select and interrupt line signals for the ADP5520 keypad controller (U35).

The signal options for the LCD SPI chip select are:

- UART1CTS_LCDSPICS (PF10) on position 1
- $\overline{\text{SPISEL1}}$ (PG1) on position 2
- SPISEL5#_HOSTD9 (PH9) on position 3.

The signal options for the keypad interrupt are:

- KEYIRQ# (PF9) on position 4
- HOSTWR#_LED1 (PG11) on position 5
- SPISEL5#_HOSTD9 (PH9) on position 6.

By default, SW25 is ON, OFF, OFF, ON, OFF, OFF.

Check other board settings before making a selection for this switch. Many signals are multiplexed with other functions and may cause a conflict if not handled appropriately.

Mode Switch (SW26)

The mode switch (SW26) selects the mode between the LCD and CPLD interfaces. See Table 2-15.

Table 2-15. LCD Mode Interface Select Switch (SW26)

SW26 Positions 2, 1	Mode Definition
ON, ON	16-bit PPI pass through
ON, OFF	16-bit PPI pass through
OFF, ON	RGB565 input mMode 16BPP
OFF, OFF	**RGB888 input mode 24BPP (default)**

SW26 positions 3, 4, and 5 are not used and available for future use. SW26 position 6 enables a PPI data buffer between the processor and LCD (active low). By default, SW26 is OFF, OFF, ON, ON, ON, ON.

Line In-Out LPBK Switch (SW28)

The line in/out loopback switch (SW28) disconnects LINEIN audio signals from LINEOUT (the signals are no longer looped back). The loopback also can be broken by plugging a cable into the bottom of the J7 or J8 connector. SW28 is ON when a POST example is running.

CPLD D8–13 Switch (SW29)

The CPLD D8–13 switch (SW29) connects PPI data lines 8–13 to the CPLD. By default, SW29 is all OFF.

CPLD 14–15/DCE ENB Switch (SW30)

The CPLD 14–15/DCE enable switch (SW30) disconnects the processor's signals from the EZ-KIT Lite's peripherals:

- Positions 1 and 2 disconnect PPI data lines 14-15 from the CPLD.
- Positions 3 and 4 disconnect UART1TX and UART1RX signals from the DCE (UART) interface.
- Positions 5 and 6 disconnect flow control signals from the DCE (UART) interface.

By default, SW30 is OFF, OFF, ON, ON, OFF, OFF.

Jumpers

This section describes functionality of the configuration jumpers. Figure 2-3 shows the jumper locations.

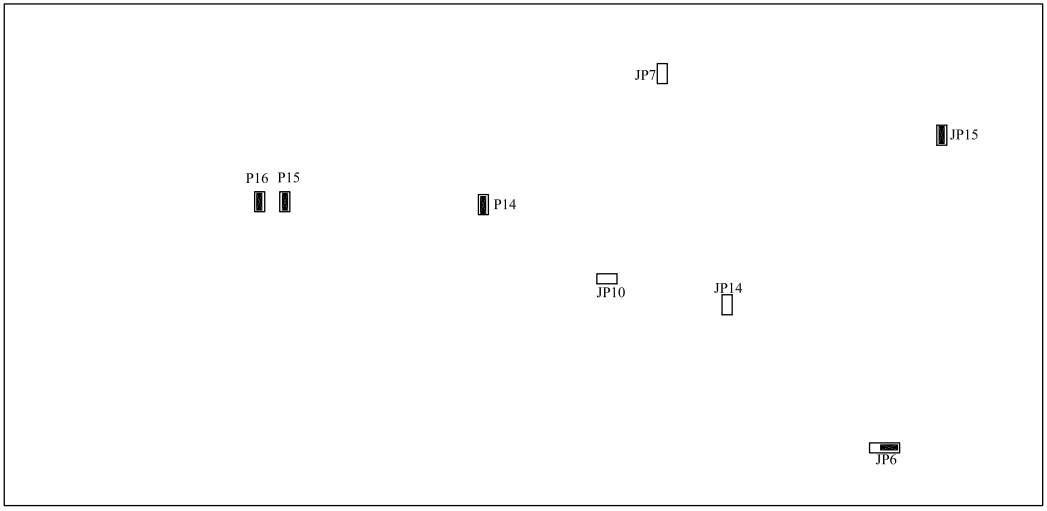


Figure 2-3. Configuration Jumper Locations

MIC Select Jumper (JP6)

The MIC select jumper (JP6) connects the MICBIAS signal to the MICIN (JP6 on 1 and 2) or the 3.5 mm connector J7 pin 3 (JP6 on 2 and 3). By default, JP6 is installed on 2 and 3.

STAMP Enable Jumper (JP7)

STAMP connectors have a number of nets connected by enabling quick switches at locations U30, U31, and U38. When installed, the STAMP enable jumper (JP7) enables the quick switches. Table 2-16 lists the

signals that are connected when JP7 is installed. By default. JP7 is uninstalled.

Table 2-16. STAMP Enable Jumper (JP7)

STAMP Signals Connected through Quick Switches U30–31, U38	
SCL	DROPRIA
SDA	RFSOA
SPISCK	CZM
SPISEL1	CUD
SPISEL2#_CDG	LED0
SPIMISO	HOSTWR#_LED1
SPIMOSI	HOSTACK_LED2
RSCLKOA	KEYIRQ#, UART1CTS_LCDSPICS, UART1TX

Flash WP Jumper (JP10)

The flash WP jumper (JP10) is used to write-protect block 70 of the parallel flash chip. Block 70 contains 64 KB of configuration data at address range 0x203 F0000–0x203 FFFFF. When the jumper is installed on JP10, and the parallel flash driver from Analog Devices is used, block 70 is read-only. By default, JP10 is not installed.

STP ENB Enable Jumper (JP14)

The stamp enable jumper (JP14) connects the DT0PRIA_PPIFS3 signal to the STAMP interface connectors. By default, JP14 is uninstalled.

LED0 OFF Jumper (JP15)

The LED0 OFF jumper (JP15) disconnects the LED0 signal from the following switches: SW24, SW29, and a quick switch U38.

VDDINT Power Jumper (P14)

The VDDINT power jumper (P14) is used to measure the core voltage and current supplied to the processor core. By default, P14 is ON, and the power flows through the two-pin IDC header. To measure power, remove the jumper and measure voltage across the 0.05 ohm resistor. Once voltage is measured, the power can be calculated. For more information, refer to "Power Measurements" on page 1-29.

VDDEXT Power Jumper (P15)

The VDDEXT power jumper (P15) is used to measure the processor's I/O voltage and current. By default, JP15 is ON, and the power flows through the two-pin IDC header. To measure power, remove the jumper and measure voltage across the 0.05 ohm resistor. Once voltage is measured, the power can be calculated.

VDDMEM Power Jumper (P16)

The VDDMEM power jumper (P16) is used to measure the voltage and current supplied to the memory interface of the processor. By default, P16 is ON, and the power flows through the two-pin IDC header. To measure power, remove the jumper and measure voltage across the 0.05 ohm resistor. Once voltage is measured, the power can be calculated.

LEDs

This section describes the on-board LEDs. Figure 2-4 shows the LED locations.

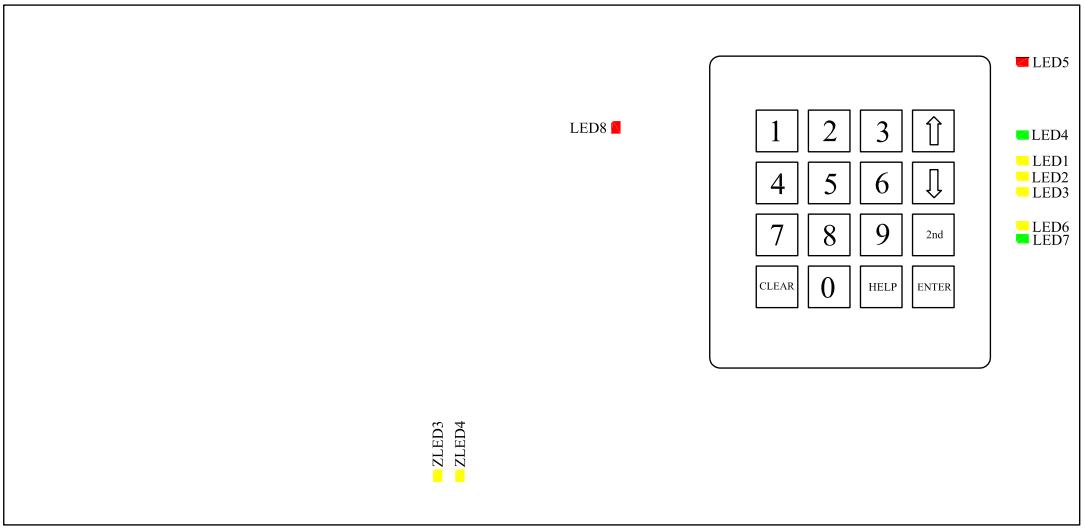


Figure 2-4. LED Locations

User LEDs (LED1–3)

Three LEDs are connected to the three general-purpose I/O pins of the processor (see Table 2-17). The LEDs are active high and are lit by writing a `1` to the correct `PF` signal.

Table 2-17. User LEDs

LED Reference Designator	Processor Programmable Flag Pin
LED1	PF8
LED2	PG11
LED3	PG12

Power LED (LED4)

When LED4 is lit (green), it indicates that power is being properly supplied to the board.

Reset LED (LED5)

When LED5 is lit, it indicates that the master reset of all major ICs is active. The reset LED is controlled by the Analog Devices ADM708 supervisory reset circuit. You can assert the reset push button (SW16) to assert a master reset and to activate LED5. For more information, see "Reset Push Button (SW16)" on page 2-18.

Ethernet LEDs (LED6–7)

When LED6 is lit solid, it indicates that the SMSC LAN8700 chip (U14) detects a valid link. When transmit or receive activity is sensed, LED7 flashes as an activity indicator. For more information about LEDs, refer to the LAN8700 chip data sheet provided by the product manufacturer.

Keypad Current Sink LED (LED8)

LED8 can be used as a keypad current sink LED. It is programmable up to 14 mA and can be turned on and off. The sink current can be set up using LED1_CURRENT in register 0 x 14. The LED sink can be enabled with the LED1_EN register 0 x 11 in the ADP5520 keypad controller (U35). For details, refer to the ADP5520 data sheet.

Connectors

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in Figure 2-5.

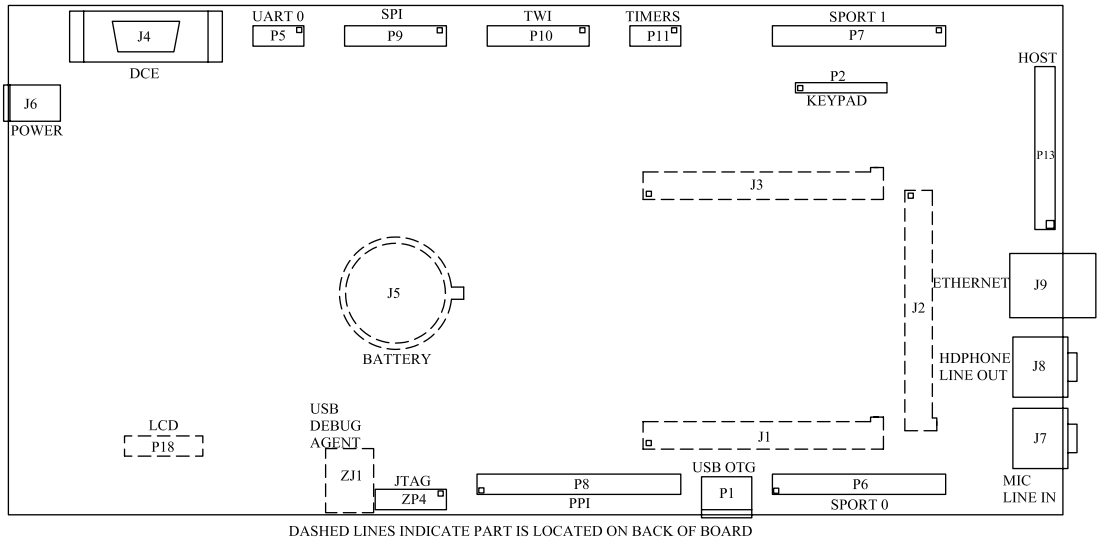


Figure 2-5. Connector Locations

Expansion Interface Connectors (J1–3)

Three board-to-board connector footprints provide signals for most of the processor's peripheral interfaces. The connectors are located at the bottom of the board. For more information, see "Expansion Interface" on page 1-29. For availability and pricing of the `J1–3` connectors, contact Samtec.

Part Description	Manufacturer	Part Number
90-position 0.05” spacing, SMT	SAMTEC	SFC-145-T2-F-D-A
Mating Connector		
90-position 0.05” spacing (through hole)	SAMTEC	TFM-145-x1 series
90-position 0.05” spacing (surface mount)	SAMTEC	TFM-145-x2 series
90-position 0.05” spacing (low cost)	SAMTEC	TFC-145 series

DCE (RS-232) Connector (J4)

Part Description	Manufacturer	Part Number
DB9, female, vertical mount	NORCOMP	191-009-213-L-571
Mating Cable		
2m female-to-female cable	DIGI-KEY	AE1020-ND

Battery Holder (J5)

Part Description	Manufacturer	Part Number
24 mm battery holder	KEYSTONE	105
Mating Battery (shipped with EZ-KIT Lite)		
3V 280MAH 24 mm LI-COIN	SANYO	CR2430

Power Connector (J6)

The power connector (J6) provides all of the power necessary to operate the EZ-KIT Lite board.

Part Description	Manufacturer	Part Number
2.5 mm power jack	SWITCHCRAFT	RAPC712X
Mating Power Supply (shipped with EZ-KIT Lite)		
7.0VDC@2.14A power supply	CUI INC	DMS070214-P6P-SZ

Dual Audio Connectors (J7–8)

Part Description	Manufacturer	Part Number
3.5 mm dual stereo jack	SWITCHCRAFT	35RAPC7JS
Mating Cable (shipped with EZ-KIT Lite)		
3.5 mm male/male 6' cable	RANDOM	10A3-01106
Mating Headphone (shipped with EZ-KIT Lite)		
3.5 mm stereo headphones	KOSS	151225 UR5

Ethernet Connector (J9)

Part Description	Manufacturer	Part Number
RJ-45 Ethernet jack	STEWART	SS-6488-NF
Mating Cable (shipped with EZ-KIT Lite)		
Cat 5E patch cable	RANDOM	PC10/100T-007

USB OTG Connector (P1)

The pinout of the P1 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
USB 5-pin mini AB	MOLEX	56579-0576
Mating Keypad (shipped with EZ-KIT Lite)		
5-in-1 USB 2.0 cable	JO-DAN INTERNAT	GXQU-06

Keypad Connector (P2)

Part Description	Manufacturer	Part Number
IDC header female	SAMTEC	SSW-109-01-TM-S
Mating Keypad (shipped with EZ-KIT Lite)		
4 x 4 keypad	ACT COMPONENTS	ACT-07-30008-000-R

UART0 Connector (P5)

The pinout of the P5 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-410HLF
Mating Connector		
IDC socket	DIGI-KEY	S4205-ND

SPORT0 Connector (P6)

The pinout of the P6 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-434HLF
Mating Connector		
IDC socket	DIGI-KEY	S4217-ND

SPORT1 Connector (P7)

The pinout of the P7 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-434HLF
Mating Connector		
IDC socket	DIGI-KEY	S4217-ND

PPI Connector (P8)

The pinout of the P8 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-440HLF
Mating Connector		
IDC socket	DIGI-KEY	S4220-ND

SPI Connector (P9)

The pinout of the P9 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-420HLF
Mating Connector		
IDC socket	DIGI-KEY	S4210-ND

TWI Connector (P10)

The pinout of the P10 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-420HLF
Mating Connector		
IDC socket	DIGI-KEY	S4210-ND

TIMERS Connector (P11)

The pinout of the P11 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-410HLF
Mating Connector		
IDC socket	DIGI-KEY	S4205-ND

Host Interface Connector (P13)

The pinout of the P13 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	SAMTEC	TSW-116-26-T-D
Mating Connector		
IDC socket	SAMTEC	TSW-116-01-T-D

CPLD JTAG Connector (P17)

The CPLD JTAG connector (P17) is not populated; CPLD code should not be altered for LCD operations.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-410HLF
Mating Connector		
IDC socket	DIGI-KEY	S4205-ND

LCD Data Connector (P18)

Part Description	Manufacturer	Part Number
FPC 67PIN CON063	KYOCERA ELCO	046281267212846+
Mating LCD Display Module (shipped with EZ-KIT Lite)		
3.5" TFT LCD with touchscreen	Sharp	LQ035Q1DH02

USB Debug Agent Connector (ZJ1)

The USB debug agent connector (ZJ1) is the connecting point for the JTAG USB debug agent interface. The JTAG header (ZP4) should not be used whenever ZJ1 and its mating cable are used to communicate to the processor via CCES or VisualDSP++.

JTAG Connector (ZP4)

The JTAG header (ZP4) is the connecting point for a JTAG in-circuit emulator pod. When an emulator connects to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

A ADSP-BF527 EZ-KIT LITE BILL OF MATERIALS

The bill of materials corresponds to "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	1	74LVC14A SOIC14	U17	TI	74LVC14AD
2	1	IDT74FCT3244APY SSOP20	U22	IDT	IDT74FCT3244APYG
3	1	SN74AHC1G00 SOT23-5	U6	TI	SN74AHC1G00DBVR
4	1	32.768KHZ OSC008	U1	EPSON	MC-156-32.7680KA-A0:ROHS
5	1	25MHZ OSC003	U3	EPSON	SG-8002CA MP
6	5	SN74LVC1G08 SOT23-5	U9-11,U29,U36	TI	SN74LVC1G08DBVR
7	1	FDS9431A SOIC8	U21	FAIRCHILD	FDS9431A
8	1	MT48LC32M16A2TG-75 TSOP54	U7	MICRON	MT48LC32M16A2P-75
9	2	SI4411DY SO-8	U18,U23	VISHAY	Si4411DY-T1-E3
10	1	HX1188 ICS007	U26	DIGI-KEY	553-1340-ND
11	1	24MHZ OSC003	U12	EPSON	SG-8002CA-MP

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
12	1	LAN8700 QFN36	U14	SMSC	LAN8700C-AEZG
13	1	BF527 M25P16 “U8”	U8	NUMONYX	M25P16-VMW6G
14	1	BF527 M29W320EB "U5"	U5	NUMONYX	M29W320EB70ZE6E
15	1	NAND04 TSOP48	U4	NUMONYX	NAND04GW3B2BN6E
16	1	MIC2025-1 SOIC8	U28	DIGI-KEY	576-1057-ND
17	1	12MHZ OSC003	U13	EPSON	SG-8002CA-MP
18	3	74CBTLV3244 TSSOP20	U30-31,U38	IDT	IDT74CBTLV3244PGG
19	1	15MHZ OSC003	U19	EPSON	SG-8002CA-MPT
20	1	BF527 XC95144XL U34	U34	XILINX	XC95144XL-10TQ100C
21	1	50MHZ OSC003	U24	DIGI-KEY	SG-8002CA-PCB-ND(50.000M)
22	1	ADM708SARZ SOIC8	U27	ANALOG DEVICES	ADM708SARZ
23	2	ADP3336ARMZ MSOP8	VR3-4	ANALOG DEVICES	ADP3336ARMZ-REEL7
24	1	ADG752BRTZ SOT23-6	U20	ANALOG DEVICES	ADG752BRTZ-REEL
25	1	ADM3202ARNZ SOIC16	U25	ANALOG DEVICES	ADM3202ARNZ
26	1	ADSPBF527KBCZENGC1 MBGA28	U2	ANALOG DEVICES	ADSP-BF527KBCZ-6C2

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
27	2	ADP1864AUJZ SOT23-6	VR1-2	ANALOG DEVICES	ADP1864AUJZ-R7
28	1	ADP5520 LFCSP_VQ24	U35	ANALOG DEVICES	ADP5520ACPZ-RL
29	1	AD7879-1 LFCSP16	U37	ANALOG DEVICES	AD7879-1ACPZ-RL
30	1	ADP1613 MSOP8	VR5	ANALOG DEVICES	ADP1613ARMZ-R7
31	1	PWR 2.5MM_JACK CON005	J6	SWITCH-CRAFT	RAPC712X
32	3	.05 45X2 CON019	J1-3	SAMTEC	SFC-145-T2-F-D-A
33	1	DIP8 SWT016	SW10	C&K	TDA08H0SB1
34	4	DIP6 SWT017	SW25-26,SW29-30	CTS	218-6LPST
35	10	DIP4 SWT018	SW1,SW4,SW7-9, SW11,SW13,SW19-20, SW24	ITT	TDA04HOSB1
36	1	DB9 9PIN CON038	J4	NORCOMP	191-009-213-L-571
37	5	DIP2 SWT020	SW5,SW21-22,SW27-28	C&K	CKN9064-ND
38	2	IDC 2X1 IDC2X1	JP7,JP10	FCI	90726-402HLF
39	3	IDC 2X1 IDC2X1	P14-16	FCI	90726-402HLF
40	1	IDC 3X1 IDC3X1	JP6	FCI	90726-403HLF
41	2	IDC 5X2 IDC5X2	P5,P11	FCI	68737-410HLF
42	2	IDC 10X2 IDC10X2	P9-10	BURG-FCI	54102-T08-10LF

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
43	2	IDC 17X2 IDC17X2	P6-7	BURG-FCI	54102-T08-17LF
44	1	IDC 20X2 IDC20X2	P8	BURG-FCI	54102-T08-20LF
45	4	IDC 2PIN_JUMPER _SHORT	SJ7-10	DIGI-KEY	S9001-ND
46	1	5A RESE-TABLE FUS005	F2	MOUSER	650-RGEF500
47	1	ROTARY SWT023	SW2	DIGI-KEY	563-1047-ND
48	1	ROTARY_ENC ODER SWT022	SW3	CTS	290UAB0R201B2
49	1	IDC 16x2 IDC16x2	P13	SAMTEC	TSW-116-26-T-D
50	1	USB_MINI-AB 5PIN CON052	P1	MOLEX	56579-0576
51	1	RJ45 8PIN CON_RJ45_12 P	J9	DIGI-KEY	380-1022-ND
52	3	MOMEN-TARY SWT024	SW14-16	PANASONIC	EVQ-Q2K03W
53	1	IDC 9X1 IDC9X1	P2	SAMTEC	SSW-109-01-TM-S
54	1	BATT_HOLDE R 24MM CON054	J5	KEYSTONE ELEC	105
55	1	FPC 67PIN CON063	P18	KYOCERA ELCO	046281267212846+
56	2	3.5MM DUAL_STERE O CON066	J7-8	SWITCH-CRAFT	35RAPC7JS

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
57	1	IDC 2PIN_JUMPER _SHORT	SJ13	DIGI-KEY	3M9414-ND
58	2	IDC 2X1 IDC2X1_2MM	JP14-15	SAMTEC	TMM-101-01-T-D
59	4	YELLOW LED001	LED1-3,LED6	DIGI-KEY	P512TR-ND
60	1	22PF 50V 5% 0805	C307	AVX	08055A220JAT
61	6	0.22UF 25V 10% 0805	C112,C283-287	AVX	08053C224KAT2A
62	1	0.1UF 50V 10% 0805	C277	AVX	08055C104KAT
63	4	10K 1/10W 5% 0805	R319-322	VISHAY	CRCW080510K0JNEA
64	2	100 1/10W 5% 0805	R122,R124	VISHAY	CRCW0805100RJNEA
65	15	600 100MHZ 200MA 0603	FER2-16	DIGI-KEY	490-1014-2-ND
66	3	600 100MHZ 500MA 1206	FER1,FER19-20	STEWARD	HZ1206B601R-10
67	5	1UF 16V 10% 0805	C92,C144,C148,C159, C178	KEMET	C0805C105K4RAC TU
68	1	10 1/10W 5% 0805	R64	VISHAY	CRCW080510R0FKEA
69	2	10UF 16V 20% CAP002	CT5,CT8	PANASONIC	EEE1CA100SR
70	1	10UH 20% IND001	L1	TDK	445-2014-1-ND
71	2	0 1/10W 5% 0805	R58,R188	VISHAY	CRCW08050000Z0EA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
72	1	190 100MHZ 5A FER002	FER17	MURATA	DLW5BSN191SQ2
73	2	1A ZHCS1000 SOT23-312	D7,D9	ZETEX	ZHCS1000TA
74	4	1UF 10V 10% 0805	C164-165,C302-303	AVX	0805ZC105KAT2A
75	11	10UF 6.3V 10% 0805	C7,C22,C33,C43,C52, C59,C68,C99,C101-102,C186	AVX	08056D106KAT2A
76	2	4.7UF 6.3V 10% 0805	C143,C171	AVX	08056D475KAT2A
77	48	0.1UF 10V 10% 0402	C12-19,C27-30,C38-41,C47-50,C56-57, C64-66,C78,C81,C83, C88,C98,C100,C103, C105,C111,C132, C135-136,C146,C157-158,C160-161,C249, C280,C300-301,C305, C308	AVX	0402ZD104KAT2A
78	76	0.01UF 16V 10% 0402	C2,C4-6,C8-11,C20-21,C23-26,C31-32, C34-37,C42,C44-46, C51,C53-55,C58,C60-63,C67,C69-77,C79-80,C82,C84-87,C90-91,C93,C97,C116-117, C121-127,C137-138, C155-156,C163,C166-168,C187-188,C248, C250,C306	AVX	0402YC103KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
79	69	10K 1/16W 5% 0402	R2-3,R11-14,R16-22, R24-27,R34,R53-55, R59,R65,R69-70,R73-76,R89,R91,R104-105, R107,R118-121,R125-126,R129-131,R140, R144,R157-158,R160, R164,R166,R169,R176-178,R196,R198,R213, R305,R318,R324-325, R329,R332-333,R335, R342-343,R345,R351	VISHAY	CRCW040210K0FKED
80	2	4.7K 1/16W 5% 0402	R23,R212	VISHAY	CRCW04024K70JNED
81	12	0 1/16W 5% 0402	R6-7,R110,R116,R149, R172,R192,R215,R302, R310,R336-337	PANASONIC	ERJ-2GE0R00X
82	2	1.2K 1/16W 5% 0402	R87-88	PANASONIC	ERJ-2GEJ122X
83	3	22 1/16W 5% 0402	R193-195	PANASONIC	ERJ-2GEJ220X
84	17	33 1/16W 5% 0402	R1,R8-10,R31,R46, R139,R167,R311,R344, R346-347,R350,R352-353,R356-357	VISHAY	CRCW040233R0JNEA
85	2	18PF 50V 5% 0805	C1,C3	AVX	08055A180JAT2A
86	3	100UF 10V 10% C	CT6,CT9-10	AVX	TPSC107K010R0075
87	1	150UF 10V 10% D	CT16	AVX	TPSD157K010R0050
88	10	2.2UF 10V 10% 0805	C288-290,C293-299	AVX	0805ZD225KAT2A
89	1	64.9K 1/10W 1% 0805	R145	VISHAY	CRCW080564K9FKEA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
90	1	210.0K 1/4W 1% 0805	R146	VISHAY	CRCW0805210KFKEA
91	2	1.5K 1/10W 5% 0603	R71-72	PANASONIC	ERJ-3GEYJ152V
92	3	0.1UF 16V 10% 0603	C169,C273-274	AVX	0603YC104KAT2A
93	3	1UF 16V 10% 0603	C96,C104,C109	KEMET	C0603C105K4PACTU
94	2	68PF 50V 5% 0603	C141,C183	AVX	06035A680JAT2A
95	1	4.7UF 6.3V 20% 0603	C131	PANASONIC	ECJ-1VB0J475M
96	2	470PF 50V 5% 0603	C140,C182	AVX	06033A471JAT2A
97	3	220UF 6.3V 20% D2E	CT1,CT7,CT11	SANYO	10TPE220ML
98	2	10K 1/10W 5% 0603	R314-315	VISHAY	CRCW060310K0JNEA
99	1	10M 1/10W 5% 0603	R15	VISHAY	CRCW060310M0FNEA
100	1	100K 1/10W 5% 0603	R317	VISHAY	CRCW0603100KJNEA
101	5	330 1/10W 5% 0603	R111-113,R115,R123	VISHAY	CRCW0603330RJNEA
102	1	1M 1/10W 5% 0603	R33	VISHAY	CRCW06031M00FNEA
103	7	0 1/10W 5% 0603	R102,R109,R133,R168, R308-309,R334	PHYCOMP	232270296001L
104	10	49.9 1/16W 1% 0603	R60-63,R78-80,R83-85	VISHAY	CRCW060349R9FNEA
105	2	10 1/10W 5% 0603	R127-128	VISHAY	CRCW060310R0JNEA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
106	8	100PF 50V 5% 0603	C260-267	PANASONIC	ECJ-1VC1H101J
107	1	12.4K 1/10W 1% 0603	R67	DIGI-KEY	311-12.4KHRTR-ND
108	2	75.0 1/10W 1% 0603	R81-82	DALE	CRCW060375R0FKEA
109	2	100 1/16W 5% 0402	R44-45	DIGI-KEY	311-100JRTR-ND
110	1	390PF 25V 5% 0603	C270	AVX	06033A391FAT2A
111	2	24.9K 1/10W 1% 0603	R98,R150	DIGI-KEY	311-24.9KHTR-ND
112	5	10UF 10V 10% 0805	C89,C94,C128,C170, C279	PANASONIC	ECJ-2FB1A106K
113	1	105.0K 1/16W 1% 0603	R137	PANASONIC	ERJ-3EKF1053V
114	4	0.05 1/2W 1% 1206	R134,R141-143	SEI	CSF 1/2 0.05 1%R
115	2	10UF 16V 10% 1210	C147,C184	AVX	1210YD106KAT2A
116	2	GREEN LED001	LED4,LED7	PANASONIC	LN1361CTR
117	2	RED LED001	LED5,LED8	PANASONIC	LN1261CTR
118	2	1000PF 50V 5% 1206	C179-180	AVX	12065A102JAT2A
119	1	255.0K 1/10W 1% 0603	R152	VISHAY	CRCW06032553FK
120	2	80.6K 1/10W 1% 0603	R99,R151	DIGI-KEY	311-80.6KHRCT-ND
121	4	5A MBRS540T3G SMC	D5,D10-12	ON SEMI	MBRS540T3G

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
122	3	15KV PGB1010603 0603	D2-4	LITTLEFUSE	PGB1010603MR
123	1	VARISTOR V5.5MLA 30A 0603	R37	LITTLEFUSE	V5.5MLA0603
124	1	THERM 0.5A 0.4 1206	R36	LITTLEFUSE	1206L050-C
125	1	20MA MA3X717E DIO005	D1	PANASONIC	MA3X717E
126	2	2.5UH 30% IND013	L2,L4	COILCRAFT	MSS1038-252NLB
127	2	330.0 1/16W 1% 0402	R68,R77	DIGI-KEY	541-330LCT-ND
128	5	47.0K 1/16W 1% 0402	R38-39,R50-52	ROHM	MCR01MZPF4702
129	3	1.0K 1/16W 1% 0402	R197,R199-200	PANASONIC	ERJ-2RKF1001X
130	2	1000PF 2000V 10% 1206	C133-134	AVX	1206GC102KAT1A
131	1	1UF 50V 10% 0603	C304	DIGI-KEY	587-1257-2-ND
132	1	10.0K 1/16W 1% 0402	R312	DIGI-KEY	541-10.0KLCT-ND
133	2	0.027 1/2W 1% 1206	R101,R103	SUSUMU	RL1632T-R027-F-N
134	4	5.6K 1/16W 0.5% 0402	R40-43	SUSUMU	RR0510P-562-D
135	1	680 1/16W 1% 0402	R47	BC COMPO-NENTS	2312 275 16801
136	1	90.9K 1/16W 5% 0402	R90	DIGI-KEY	541-90.9KLCT-ND

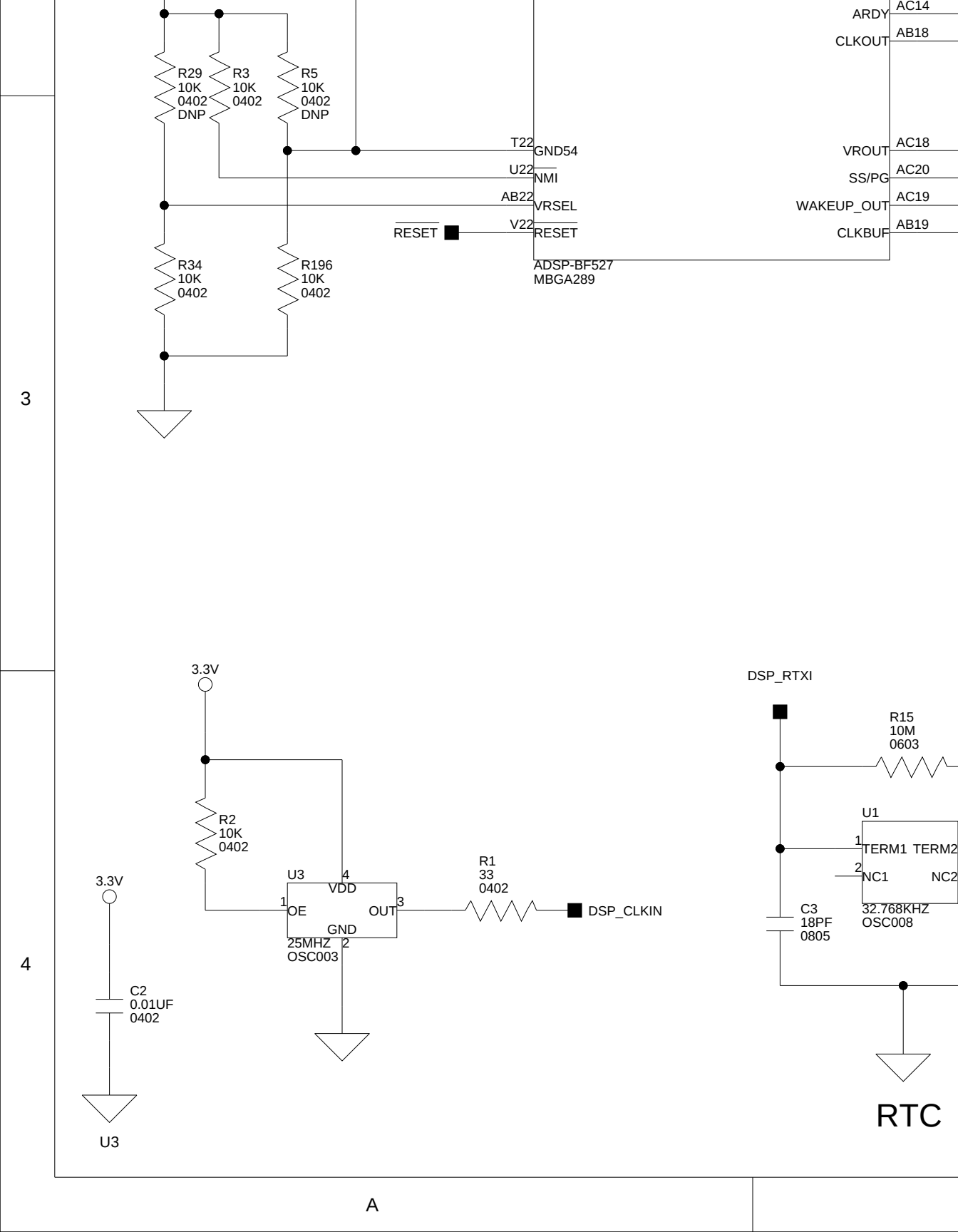
Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
137	1	40.2K 1/16W 5% 0402	R57	DIGI-KEY	541-40.2KLCT-ND
138	4	3.3UF 16V 10% 0805	C113,C118,C120,C129	DIGI-KEY	490-3337-2-ND
139	3	22UF 10V 10% 1210	C139,C142,C145	DIGI-KEY	490-1876-2-ND
140	1	95K 1/10W 1% 0603	R136	DIGI-KEY	311-95.3KHRTR-ND
141	5	15PF 50V 5% 0402	C119,C130,C197-199	DIGI-KEY	399-1014-2-ND
142	1	422K 1/10W 1% 0603	R100	PANASONIC	ERJ-3EKF4223V
143	1	15uH 20% IND015	L5	COILCRAFT	MSS4020-153ML
144	3	.5A B0540W SOD-123	D17-19	DIODES INC	B0540W-7-F
145	1	.5A BZT52C33S SOD-323	D20	DIODES INC	BZT52C33S-7-F
146	5	2.2UF 25V 10% 0805	C275-276,C278,C291-292	DIGI-KEY	490-3331-1-ND
147	11	33 1/16W 5% RNS003	RN2-12	PANASONIC	EXB-2HV330JV
148	2	33 1/32W 5% RNS005	RN13-14	PANASONIC	EXB-28V330JX
149	2	51.1 1/16W 1% 0402	R316,R348	DIGI-KEY	541-51.1LCT-ND
150	1	30A GSOT05 SOT23-3	D15	VISHAY	GSOT05-GS08
151	1	30A GSOT03 SOT23-3	D14	VISHAY	GSOT03-GS08

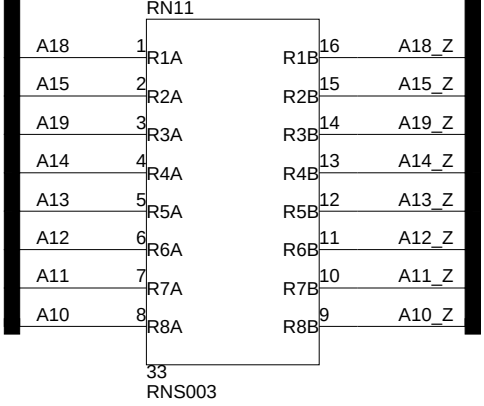
Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
152	1	40A ESD5Z2.5T1 SOD-523	D13	ON SEMI	ESD5Z2.5T1G
153	1	30A GSOT08 SOT23-3	D16	VISHAY	GSOT08-GS08

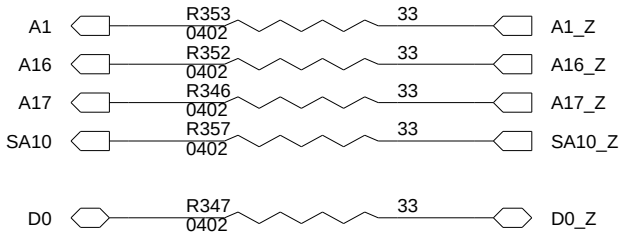
3

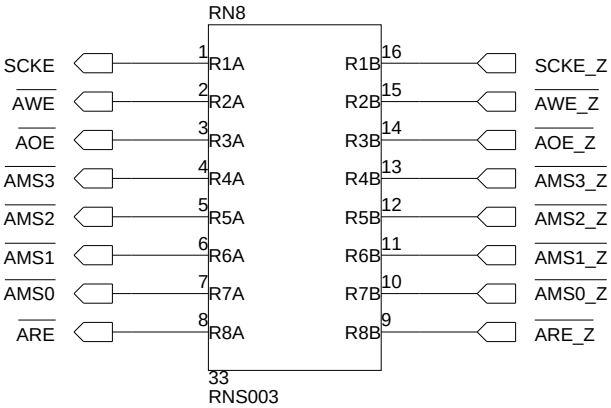
4

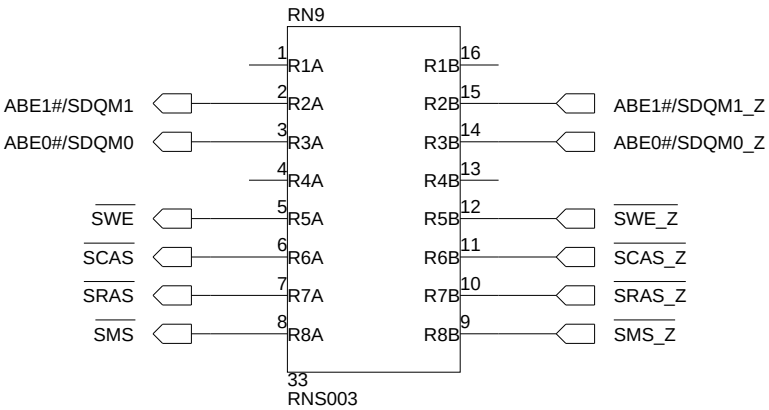
A


R29
10K
0402
DNP
R3
10K
0402
R5
10K
0402
DNP
R34
10K
0402
R196
10K
0402
T22
GND54
U22
NMI
AB22
VRSEL
V22
RESET
RESET
ADSP-BF527
MBGA289
AC14
ARDY
AB18
CLKOUT
AC18
VROUT
AC20
SS/PG
AC19
WAKEUP_OUT
AB19
CLKBUF
3.3V
R2
10K
0402
U3
4
VDD
1
OE
OUT
3
GND
2
25MHZ
OSC003
R1
33
0402
DSP_CLKIN
3.3V
C2
0.01UF
0402
U3
DSP_RTXI
R15
10M
0603
U1
1
TERM1
TERM2
2
NC1
NC2
C3
18PF
0805
32.768KHZ
OSC008
RTC









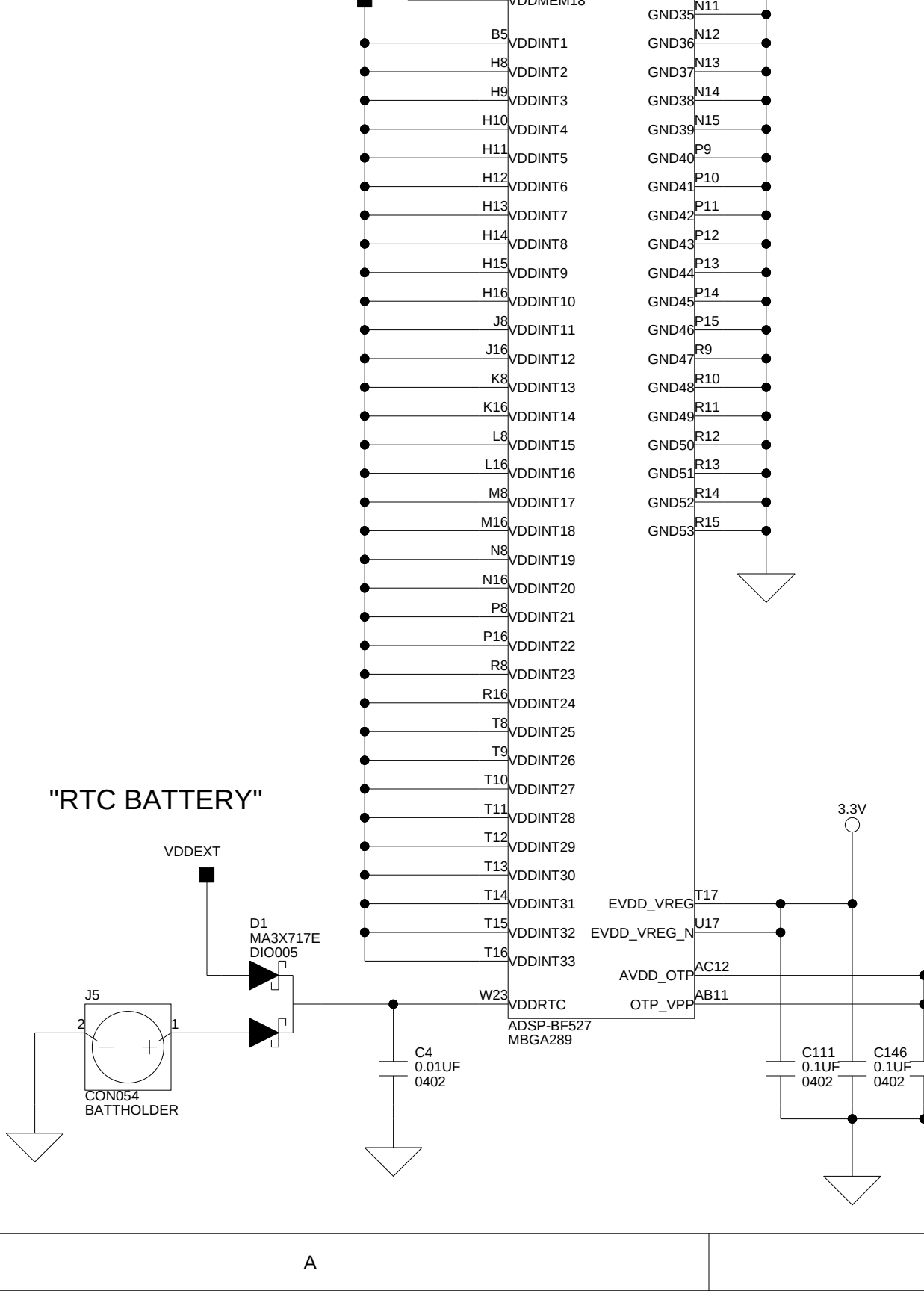
TFS0A_R

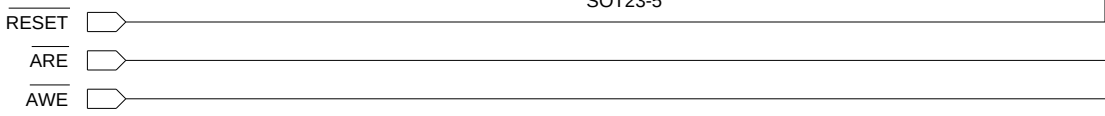
HOSTA

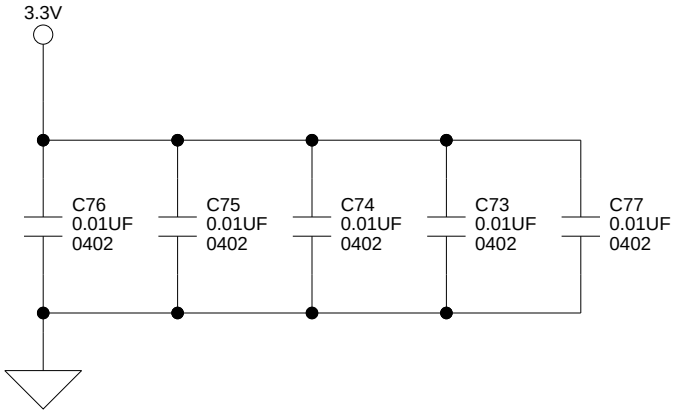
3

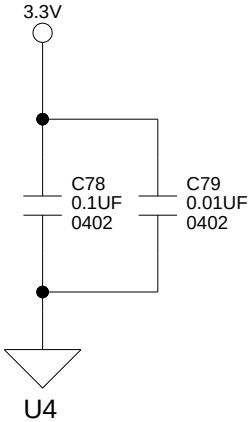
4

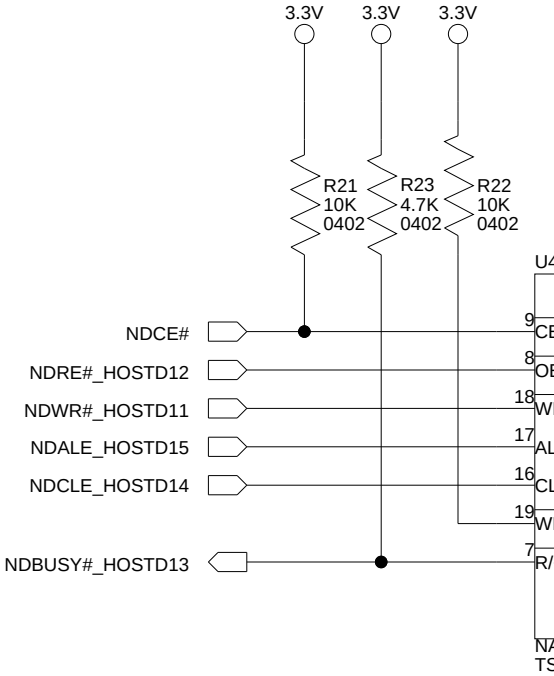
A

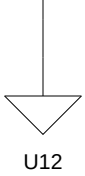

VDDMEM18
B5 VDDINT1
H8 VDDINT2
H9 VDDINT3
H10 VDDINT4
H11 VDDINT5
H12 VDDINT6
H13 VDDINT7
H14 VDDINT8
H15 VDDINT9
H16 VDDINT10
J8 VDDINT11
J16 VDDINT12
K8 VDDINT13
K16 VDDINT14
L8 VDDINT15
L16 VDDINT16
M8 VDDINT17
M16 VDDINT18
N8 VDDINT19
N16 VDDINT20
P8 VDDINT21
P16 VDDINT22
R8 VDDINT23
R16 VDDINT24
T8 VDDINT25
T9 VDDINT26
T10 VDDINT27
T11 VDDINT28
T12 VDDINT29
T13 VDDINT30
T14 VDDINT31
T15 VDDINT32
T16 VDDINT33
W23 VDDRTC
ADSP-BF527
MBGA289
GND35 N11
GND36 N12
GND37 N13
GND38 N14
GND39 N15
GND40 P9
GND41 P10
GND42 P11
GND43 P12
GND44 P13
GND45 P14
GND46 P15
GND47 R9
GND48 R10
GND49 R11
GND50 R12
GND51 R13
GND52 R14
GND53 R15
"RTC BATTERY"
VDDEXT
D1
MA3X717E
DIO005
J5
2
1
CON054
BATTHOLDER
C4
0.01UF
0402
EVDD_VREG T17
EVDD_VREG_N U17
AVDD_OTP AC12
OTP_VPP AB11
3.3V
C111
0.1UF
0402
C146
0.1UF
0402
3
4
A


2
4
SN74LVC1G08
SOT23-5
RESET
ARE
AWE


3.3V
C76
0.01UF
0402
C75
0.01UF
0402
C74
0.01UF
0402
C73
0.01UF
0402
C77
0.01UF
0402
U5, U6, U9, U10, U11


3.3V
C78
0.1UF
0402
C79
0.01UF
0402
U4

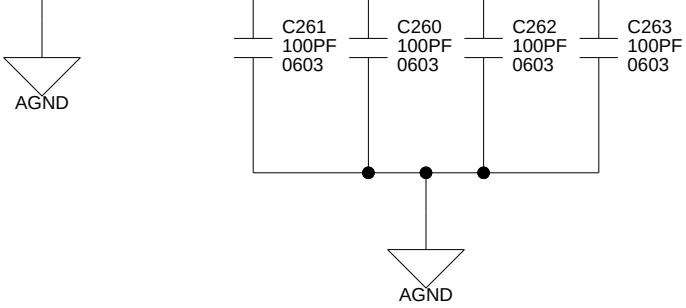

3.3V
3.3V
3.3V
R21
10K
0402
R23
4.7K
0402
R22
10K
0402
NDCE#
NDRE#_HOSTD12
NDWR#_HOSTD11
NDALE_HOSTD15
NDCLE_HOSTD14
NDBUSY#_HOSTD13

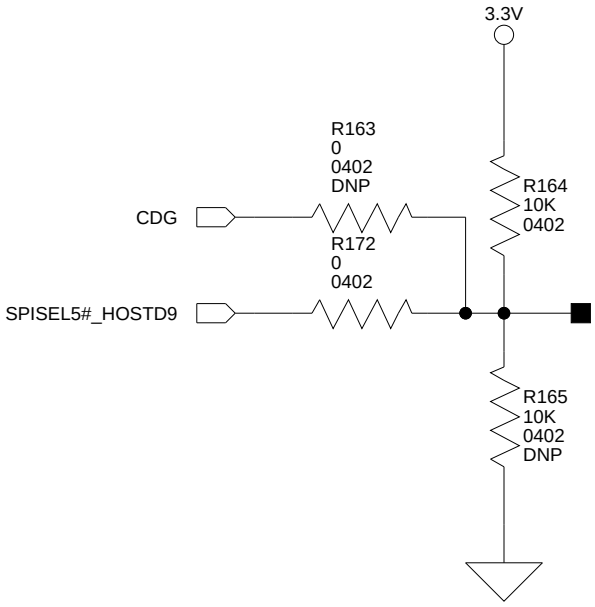


3

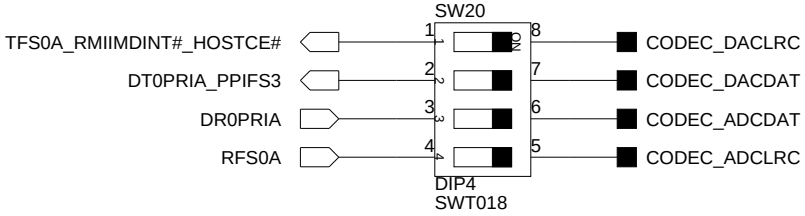
4

A

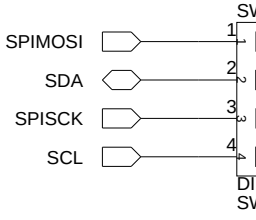




"SPORT"
"0A"
"ENBL"



"SPI



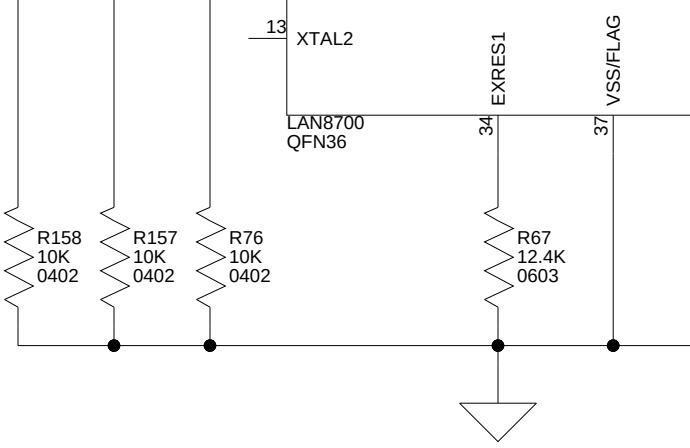
SW20 and SWXX disconnect DSP from AUDIO CODEC

AUDIO CODEC
SPI MODE:
TWI MODE:

3

4

A



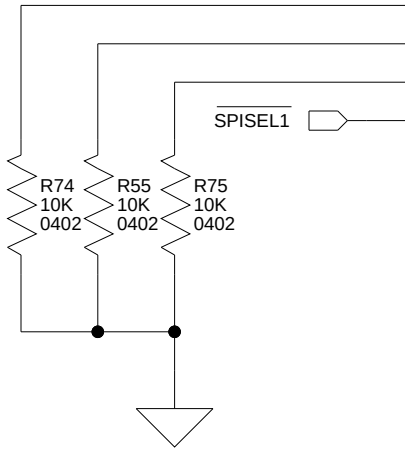
3

SW9: Ethernet Mode Select (SW9.1, SW9.2, SW9.3)

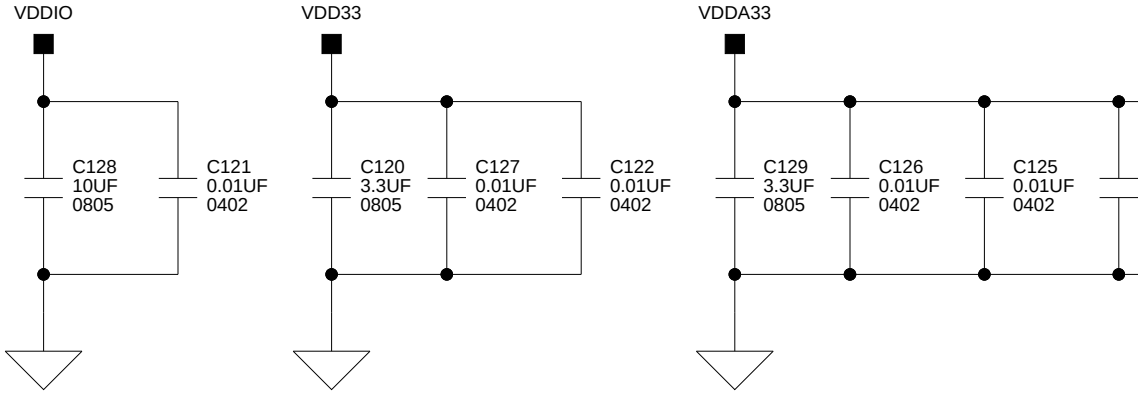
MODE[2:0]	MODE DEFINITIONS
111	All Capable, Auto Negotiation DEFAULT
110	Power Down Mode
101	Repeater Mode, Auto Negotiation
100	100Base-TX Half duplex Advertised, Auto Negotiaion
011	100Base-TX Full Duplex
010	100Base-TX Half Duplex
001	10Base-T Full Duplex
000	10Base-T Half Duplex

Internal LAN8700 pullups are used for mode pins

SW9.4 discconnects SPISEL1, for use on expansion interface (J2.11)

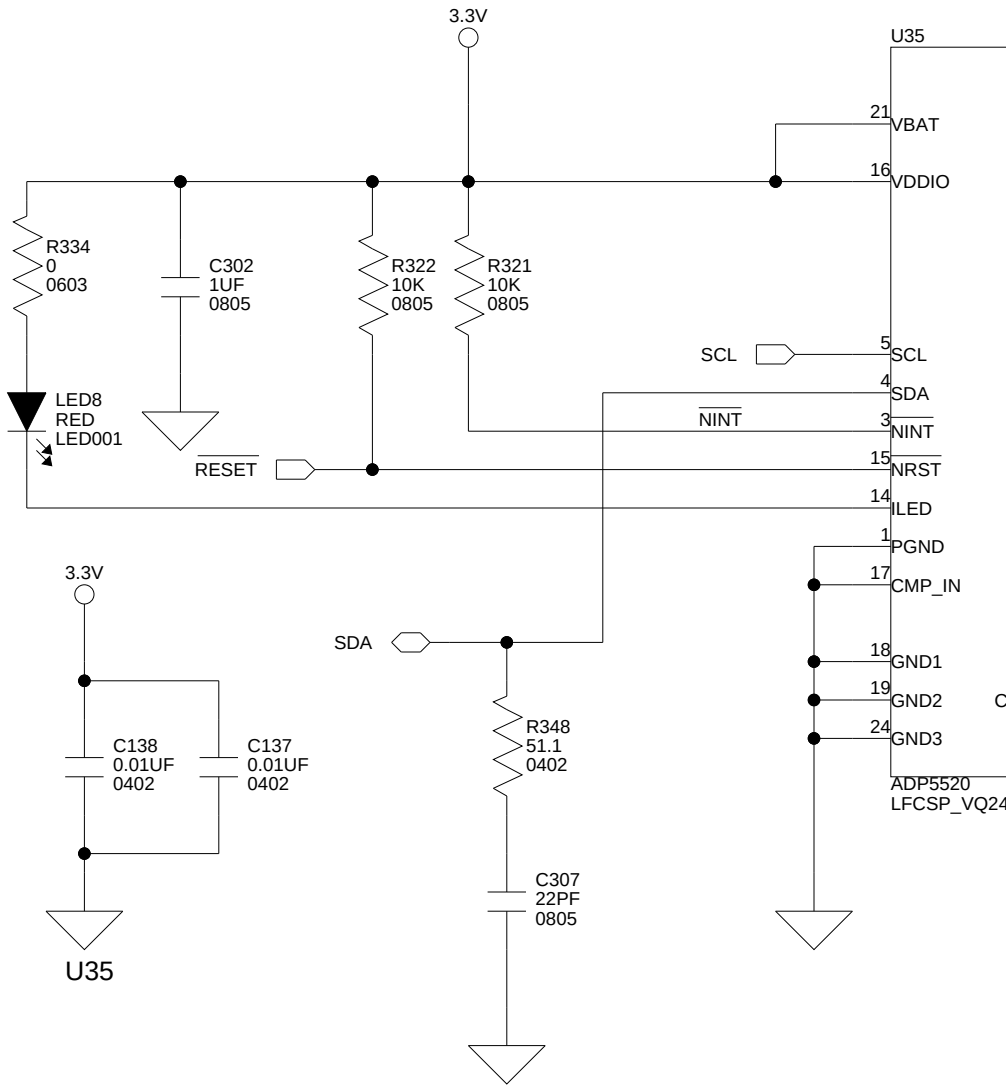


4



A

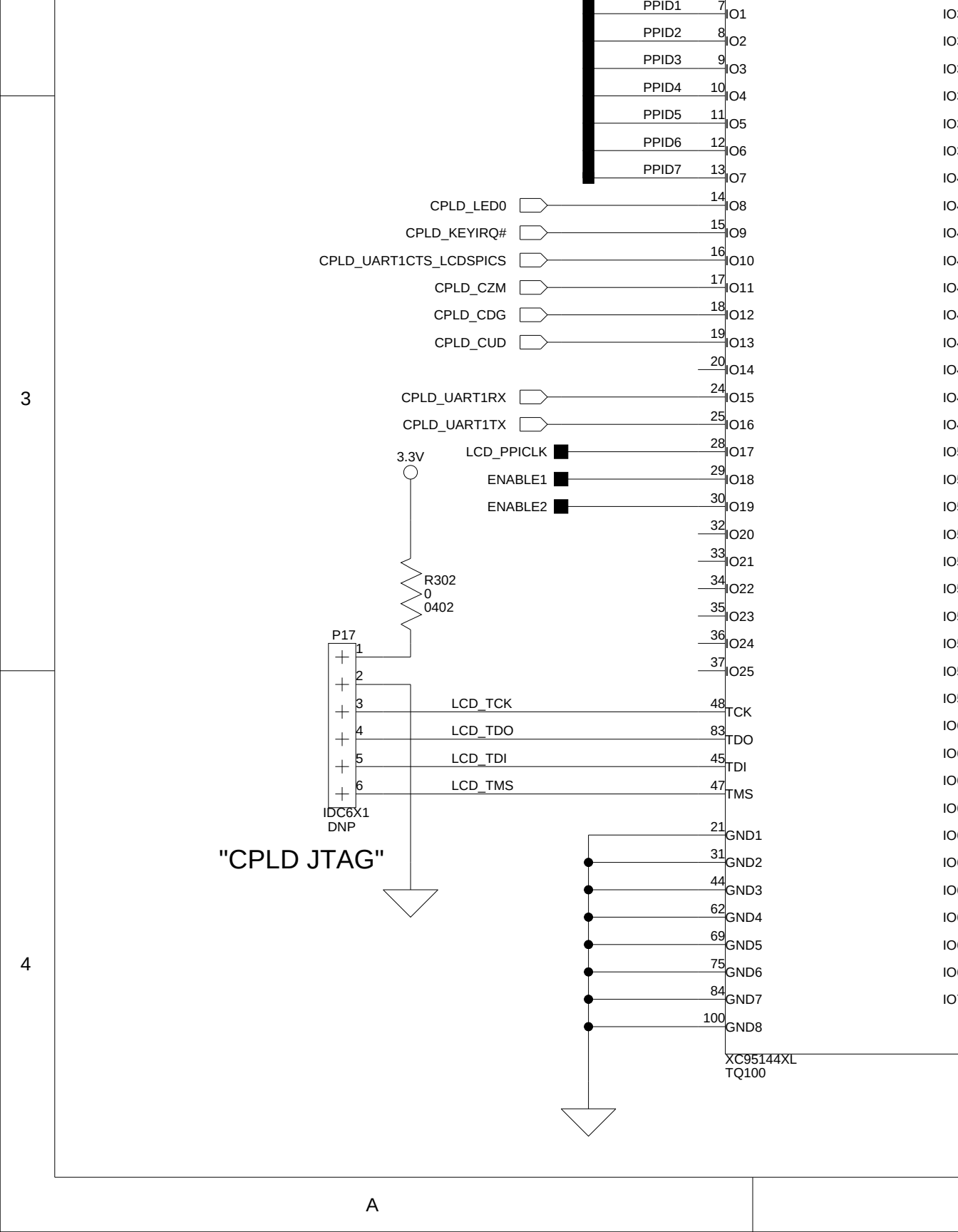
I2C address is

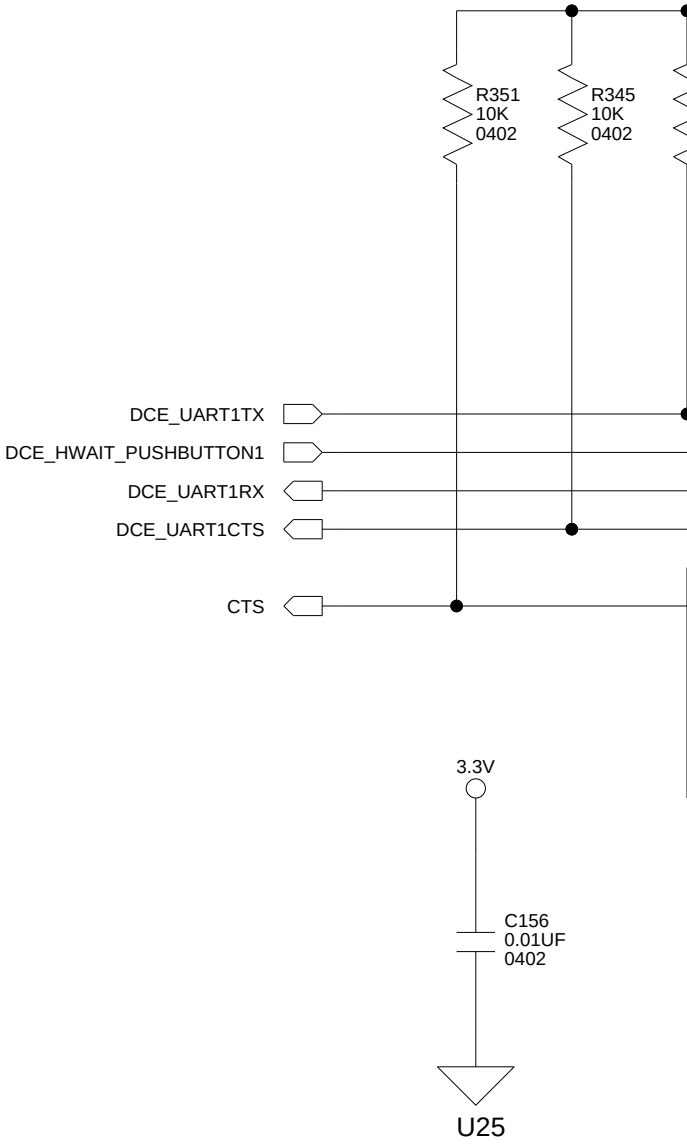


3

4

A


PPID1
PPID2
PPID3
PPID4
PPID5
PPID6
PPID7
CPLD_LED0
CPLD_KEYIRQ#
CPLD_UART1CTS_LCDSPICS
CPLD_CZM
CPLD_CDG
CPLD_CUD
CPLD_UART1RX
CPLD_UART1TX
LCD_PPICLK
ENABLE1
ENABLE2
3.3V
R302
0
0402
P17
IDC6X1
DNP
LCD_TCK
LCD_TDO
LCD_TDI
LCD_TMS
"CPLD JTAG"
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
IO14
IO15
IO16
IO17
IO18
IO19
IO20
IO21
IO22
IO23
IO24
IO25
TCK
TDO
TDI
TMS
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
XC95144XL
TQ100
3
4
A

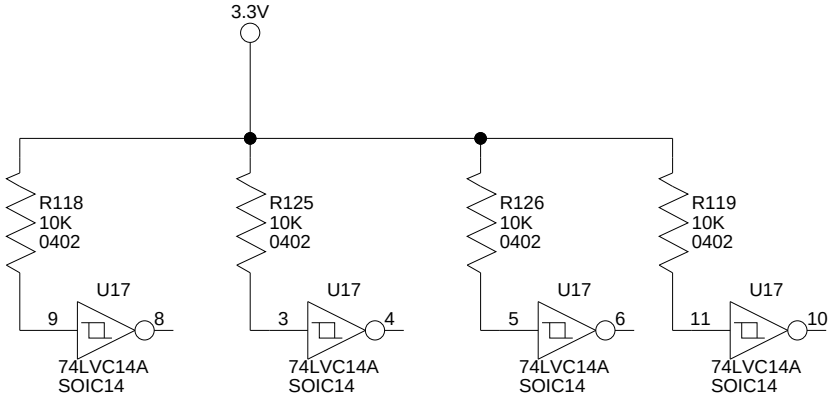

R351
10K
0402
R345
10K
0402
DCE_UART1TX
DCE_HWAIT_PUSHBUTTON1
DCE_UART1RX
DCE_UART1CTS
CTS
3.3V
C156
0.01UF
0402
U25

3

4

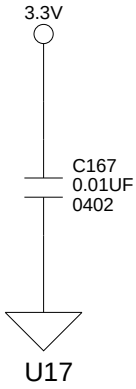
A

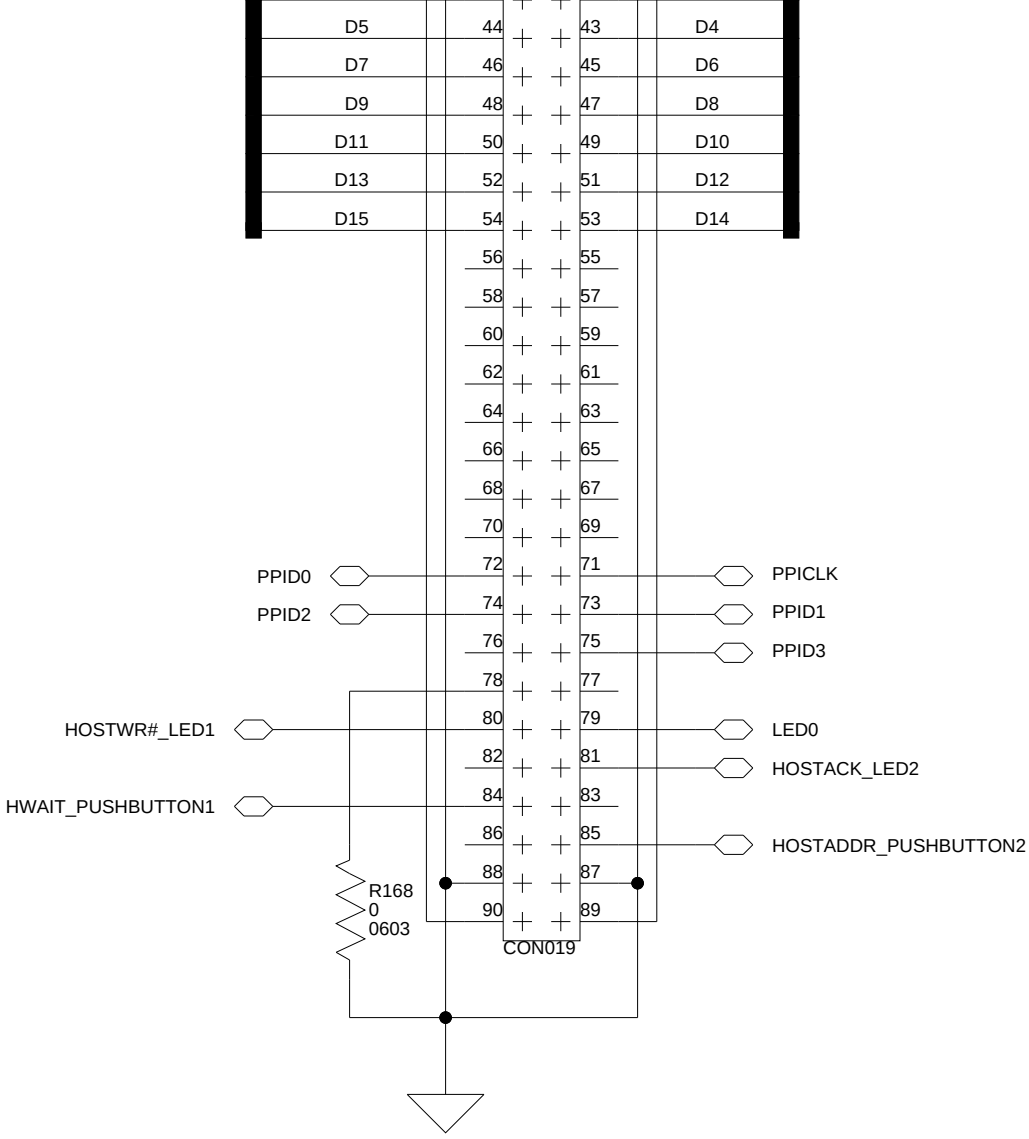
SW13.2	push button 2	DSP (U2, PG13)	ON	ON (PB2), OFF (HOST connector P13.
SW13.3	OTG PWR(VR3, U28)	DSP (U2, PG13)	OFF	OFF (HOST connector P13.8, Expansio
SW13.4	DSP(U2, PG12)	PPI CLK (U20)	OFF	OFF (LED2, Host connector P13.10, Ex



DA_SOFT_RESET

CTS

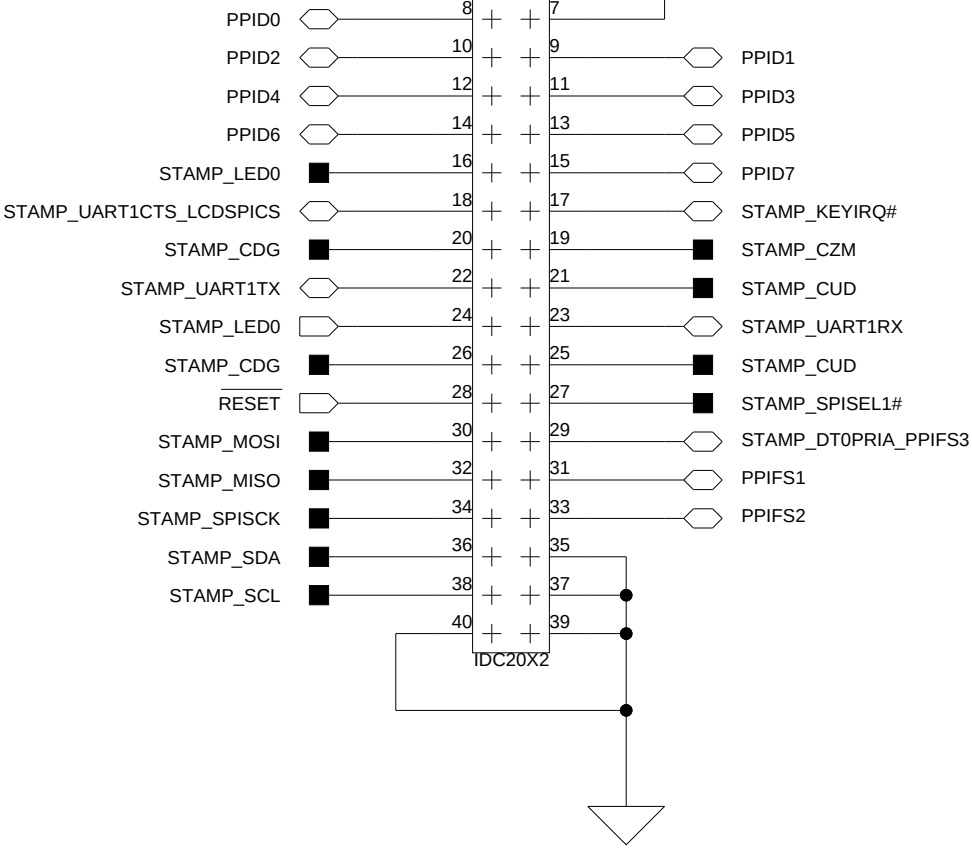



D5
D7
D9
D11
D13
D15
D4
D6
D8
D10
D12
D14
TSCLK0A
PPID5
PPID7
KEYIRQ#
CZM
CUD
UART1RX
UART1RX
SCL
ABE1#/SDQM1
ABE0#/SDQM0
AOE
AWE
SMS
ABE0#/SDQM0
SRAS
SA10
SWE
PPID0
PPID2
PPICLK
PPID1
PPID3
HOSTWR#_LED1
LED0
HOSTACK_LED2
HWAIT_PUSHBUTTON1
HOSTADDR_PUSHBUTTON2
R168
0
0603
CON019

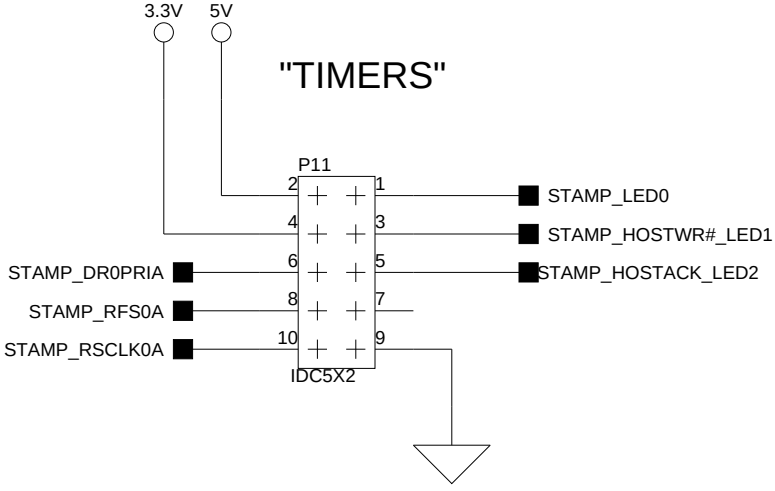
3

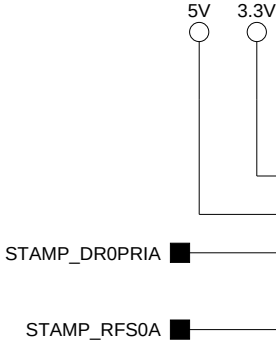
4

A


PPID0
PPID2
PPID4
PPID6
STAMP_LED0
STAMP_UART1CTS_LCDSPICS
STAMP_CDG
STAMP_UART1TX
STAMP_LED0
STAMP_CDG
RESET
STAMP_MOSI
STAMP_MISO
STAMP_SPISCK
STAMP_SDA
STAMP_SCL
8
10
12
14
16
18
20
22
24
26
28
30
32
34
36
38
40
7
9
11
13
15
17
19
21
23
25
27
29
31
33
35
37
39
IDC20X2
PPID1
PPID3
PPID5
PPID7
STAMP_KEYIRQ#
STAMP_CZM
STAMP_CUD
STAMP_UART1RX
STAMP_CUD
STAMP_SPISEL1#
STAMP_DT0PRIA_PPIFS3
PPIFS1
PPIFS2

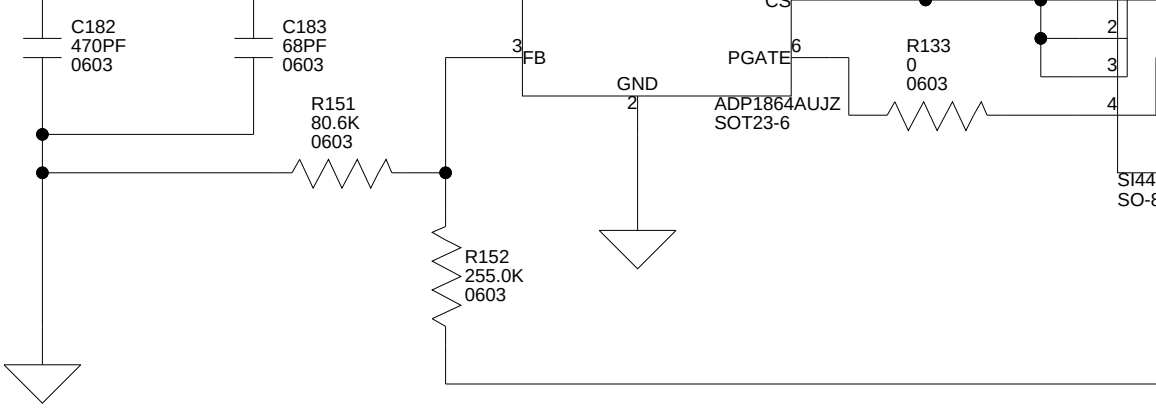
3

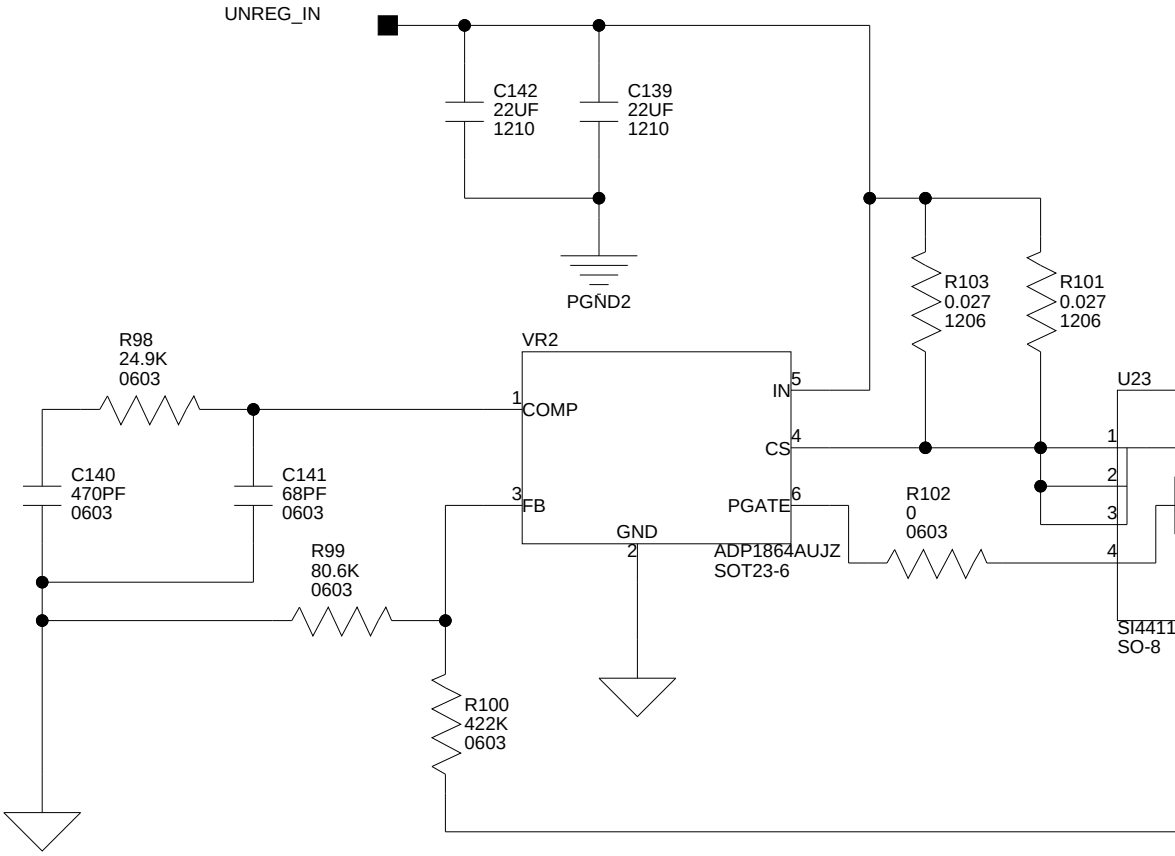

3.3V
5V
"TIMERS"
P11
2
4
6
8
10
1
3
5
7
9
IDC5X2
STAMP_LED0
STAMP_HOSTWR#_LED1
STAMP_HOSTACK_LED2
STAMP_DR0PRIA
STAMP_RFS0A
STAMP_RSCLK0A


5V
3.3V
STAMP_DR0PRIA
STAMP_RFS0A

4

A


C182
470PF
0603
C183
68PF
0603
R151
80.6K
0603
R152
255.0K
0603
FB
GND
PGATE
ADP1864AUJZ
SOT23-6
R133
0
0603
SI44
SO-8


UNREG_IN
C142
22UF
1210
C139
22UF
1210
PGND2
R103
0.027
1206
R101
0.027
1206
R98
24.9K
0603
VR2
COMP
C140
470PF
0603
C141
68PF
0603
FB
GND
R99
80.6K
0603
R100
422K
0603
IN
CS
PGATE
ADP1864AUJZ
SOT23-6
R102
0
0603
U23
SI4411
SO-8

3

4

A

I INDEX

K

L

M

N

O

P

R

S

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Development Boards & Kits - Other Processors ***category:***

Click to view products by Analog Devices ***manufacturer:***

Other Similar products are found below :

EVB-MEC1418MECC 20-101-1252 C29XPCIE-RDB CC-ACC-18M433 MAX1464EVKIT RTE510Y470TGB00000R RTK0EN0001D01001BZ MAXQ622-KIT# YR0K505231S000BE YR0K50571MS000BE YQB-R5F1057A-TB QB-R5F104PJ-TB CC-ACC-ETHMX OV-7604-C7-EVALUATION-BOARD SK-AD02-D62Q1747TB SK-BS01-D62Q1577TB ST7MDT1-EMU2 GROVE BASE KIT FOR RASPBERRY PI CAB M-M(40-17-RAINBOW) CY8CKIT-143A EK-MPC5744P KITAURIXTC234TFTTOBO1 ESP32-C3-DEVKITC-02 ENW89854AXKF ENWF9201AVEF QB-R5F104LE-TB LV18F V6 64-80-PIN TQFP MCU CARD EMPTY LV-24-33 V6 44-PIN TQFP MCU CARD EMPTY LV-24-33 V6 64-PIN TQFP MCU CARD EMPTY LV-24-33 V6 80-PIN TQFP 1 MCU CARD EMPTY 32X32 RGB LED MATRIX PANEL - 6MM PITCH 3.3 - 5 VTRANSLATOR READY FOR XMEGA CASING (WHITE) RELAY4 BOARD ETHERNET CONNECTOR RFID CARD 125KHZ - TAG RFID READER RFM12B-DEMO MAROON 3G CLICK (FOR EUROPE AND AUSTRALIA) MAX232 MAX3232 BOARD ARTY S7-50 THREE-AXIS ACCELEROMETER BOARD TINKERKIT HALL SENSOR TOUCHPANEL TOUCHPANEL CONTROLLER MIKROBOARD FOR AVR WITH ATMEGA128 MIKROBOARD FOR PSOC WITH CY8C27643 MIKROBUS CAPE