ADSP-BF538F EZ-KIT Lite®
Evaluation System Manual

Revision 1.3, July 2012

Part Number
82-000945-01

Analog Devices, Inc.
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ANALOG DEVICES

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Regulatory Compliance

The ADSP-BF538F EZ-KIT Lite is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADSP-BF538F EZ-KIT Lite has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC amended by 93/68/EEC and therefore carries the "**CE**" mark.

The ADSP-BF538F EZ-KIT Lite has been appended to Analog Devices, Inc. Technical Construction File (TCF) referenced '**DSPTOOLS1**' dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body as listed below.

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Shrivenham, Swindon, SN6 8TY, UK

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

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PREFACE

Thank you for purchasing the ADSP-BF538F EZ-KIT Lite®, Analog Devices, Inc. evaluation system for Blackfin® processors.

Blackfin processors embody a type of embedded processor designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications. They deliver breakthrough signal-processing performance and power efficiency within a reduced instruction set computing (RISC) programming model.

Blackfin processors support a media instruction set computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics. Blackfin processors deliver signal-processing performance in a microprocessor-like environment.

Based on the Micro Signal Architecture (MSA), Blackfin processors combine a 32-bit RISC instruction set, dual 16-bit multiply accumulate (MAC) DSP functionality, and 8-bit video processing performance that had previously been the exclusive domain of very-long instruction word (VLIW) media processors.

The evaluation board is designed to be used in conjunction with the CrossCore® Embedded Studio (CCES) and VisualDSP++® development environments to test the capabilities of the ADSP-BF538F Blackfin processors. The development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-BF538F assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-BF538F processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-BF538F processor and the evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to http://www.analog.com/dsp/tools.

The ADSP-BF538F EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

Product Overview

The board features:

- Analog Devices ADSP-BF538F processor
    - Core performance up to 600 MHz
    - External bus performance to 133 MHz
    - 182-pin mini-BGA package
    - 25 MHz crystal
- Synchronous dynamic random access memory (SDRAM)
    - MT48LC32M8 – 64 MB (8M x 8-bits x 4 banks) x 2 chips
- Flash memory
    - 4MB (2M x 16-bits)
- Analog audio interface
    - AD1871 96 kHz analog-to-digital codec (ADC)
    - AD1854 96 kHz digital-to-audio codec (DAC)
    - 1 input stereo jack
    - 1 output stereo jack

- Controller Area Network (CAN) interface
    - Philips TJA1041 high-speed CAN transceiver
- National Instruments Educational Laboratory Virtual Instrumentation Suite (ELVIS) interface
    - LabVIEW™-based virtual instruments
    - Multifunction data acquisition device
    - Bench-top workstation and prototype board
- Universal asynchronous receiver/transmitter (UART)
    - ADM3202 RS-232 line driver/receiver
    - DB9 female connector
- LEDs
    - 10 LEDs: 1 power (green), 1 board reset (red), 1 USB (red), 5 general-purpose (amber), and 1 USB monitor (amber)
- Push buttons
    - 5 push buttons: 1 reset, 4 programmable flags with debounce logic
- Expansion interface
    - All processor signals
- Other features
    - JTAG ICE 14-pin header

The EZ-KIT Lite board has flash memory with a total of 4 MB. Flash memory can be used to store user-specific boot code, allowing the board to run as a stand-alone unit. For more information, see “Flash Memory”

on page 1-15. The board also has 64 MB of SDRAM, which can be used by the user at runtime.

SPORT0 interfaces with the audio circuit, facilitating development of audio signal processing applications. SPORT0, SPORT1, and SPORT2 also interface to an off-board connector for communication with other serial devices. For more information, see "SPORT0 Interface" on page 2-4.

The UART of the processor connects to an RS-232 line driver and a DB9 female connector, providing an interface to a PC or other serial device.

Additionally, the EZ-KIT Lite board provides access to all of the processor's peripheral ports. Access is provided in the form of a three-connector expansion interface. For more information, see "Expansion Interface" on page 2-8.

Purpose of This Manual

The *ADSP-BF538F EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF538F EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set.

Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts that describe your

target architecture. For the locations of these documents, see “Related Documents”.

Programmers who are unfamiliar with CCES or VisualDSP++ should refer to the VisualDSP++ online help and user’s manuals.

Manual Contents

The manual consists of:

- Chapter 1, “Using the ADSP-BF538F EZ-KIT Lite” on page 1-1
  Describes EZ-KIT Lite functionality from a programmer’s perspective and provides an easy-to-access memory map.
- Chapter 2, “ADSP-BF538F EZ-KIT Lite Hardware Reference” on page 2-1
  Provides information on the EZ-KIT Lite hardware components.
- Appendix A, “ADSP-BF538F EZ-KIT Lite Bill of Materials” on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, “ADSP-BF538F EZ-KIT Lite Schematic” on page B-1
  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design. Appendix B is part of the online help.

What's New in This Manual

This is revision 1.3 of the *ADSP-BF538F EZ-KIT Lite Evaluation System Manual*. The manual has been updated to include CCES information. In addition, modifications and corrections based on errata reports against the previous manual revision have been made.

For the latest version of this manual, please refer to the Analog Devices Web site.

Technical Support

You can reach Analog Devices processors and DSP technical support in the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:
  `http://ez.analog.com/community/dsp`
- Submit your questions to technical support directly at:
  `http://www.analog.com/support`
- E-mail your questions about processors, DSPs, and tools development software from **CrossCore Embedded Studio** or **VisualDSP++**:

  Choose **Help > Email Support**. This creates an e-mail to `processor.tools.support@analog.com` and automatically attaches your **CrossCore Embedded Studio** or **VisualDSP++** version information and `license.dat` file.
- E-mail your questions about processors and processor applications to:
  `processor.support@analog.com` or
  `processor.china@analog.com` (Greater China support)

- In the **USA only**, call **1-800-ANALOGD** (1-800-262-5643)
- Contact your Analog Devices sales office or authorized distributor. Locate one at:
  www.analog.com/adi-sales
- Send questions by mail to:
  Processors and DSP Technical Support
  Analog Devices, Inc.
  Three Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

This evaluation system supports Analog Devices ADSP-BF538F Blackfin embedded processors.

Product Information

Product information can be obtained from the Analog Devices Web site and the online help system.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a

link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, myAnalog is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. myAnalog provides access to books, application notes, data sheets, code examples, and more.

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EngineerZone is a technical support forum from Analog Devices. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

Related Documents

For additional information about the product, refer to the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-BF538/ADSP-BF538F Blackfin Embedded Processor Data Sheet	General functional description, pinout, and timing of the processor
ADSP-BF538/ADSP-BF538F Blackfin Processor Hardware Reference	Description of internal processor architecture and all register functions
Blackfin Processor Programming Reference	Description of all allowed processor assembly instructions

If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, also refer to the documentation that accompanies the emulator.

Notation Conventions

Text conventions used in this manual are identified and described as follows. Additional conventions, which apply only to specific chapters, may appear throughout this document.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the development environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.

Example	Description
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
.SECTION	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

1 USING THE ADSP-BF538F EZ-KIT LITE

This chapter provides specific information to assist you with development of programs for the ADSP-BF538F EZ-KIT Lite evaluation system.

The information appears in the following sections.

- "SDRAM Interface" on page 1-13
  Defines the register values to configure the on-board SDRAM.
- "Flash Memory" on page 1-15
  Describes the internal and external flash memory.
- "CAN Interface" on page 1-15
  Describes the on-board Controller Area Network (CAN) interface.
- "ELVIS Interface" on page 1-16
  Describes the on-board National Instruments Educational Laboratory Virtual Instrumentation Suite (NI ELVIS) interface.
- "Audio Interface" on page 1-17
  Describes the on-board audio circuit.
- "LEDs and Push Buttons" on page 1-17
  Describes the board's general-purpose IO pins and buttons.
- "Board Design Database" on page 1-18
  Provides board design information.
- "Example Programs" on page 1-18
  Provides information about example programs included in the ADSP-BF538F EZ-KIT Lite evaluation system.

For information on the graphical user interface, including the boot loading, target options, and other facilities of the EZ-KIT Lite system, refer to the online help.

For more detailed information about programming the ADSP-BF538F Blackfin processor, see the documents referred to as "Related Documents".

Package Contents

Your ADSP-BF538F EZ-KIT Lite evaluation system package contains the following items.

- ADSP-BF538F EZ-KIT Lite board
- Universal 7V DC power supply
- 6-foot 3.5 mm male-to-male audio cable
- 3.5 mm headphones
- 10-foot USB 2.0 cable

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-BF538F EZ-KIT Lite board is designed to run outside your personal computer as a standalone unit.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components. Figure 1-1 shows the default jumper settings, switches, connector locations, and LEDs used in installation. Confirm that your board is in the default configuration before using the board.

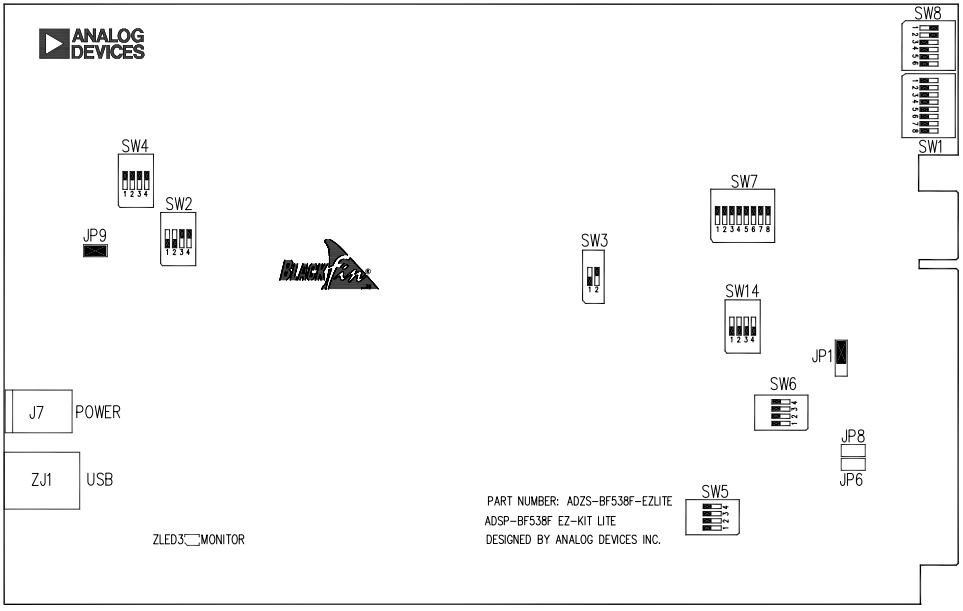

Figure 1-1. EZ-KIT Lite Hardware Setup

CCES Install and Session Startup

For information about CCES and to download the software, go to www.analog.com/CCES. A link for the ADSP-BF538F EZ-KIT Lite Board Support Package (BSP) for CCES can be found at http://www.analog.com/Blackfin/EZKits.

Follow these instructions to ensure correct operation of the product software and hardware.

Step 1: Connect the EZ-KIT Lite board to a personal computer (PC) running CCES using one of two options: an Analog Devices emulator or via the debug agent.

Using an Emulator:

1. Plug one side of the USB cable into the USB connector of the emulator. Plug the other side into a USB port of the PC running CCES.
2. Attach the emulator to the header connector ZP4 (labeled JTAG) on the EZ-KIT Lite board.

Using the on-board Debug Agent:

1. Plug one side of the USB cable into the USB connector of the debug agent ZP1.
2. Plug the other side of the cable into a USB port of the PC running CCES.

Step 2: Attach the provided cord and appropriate plug to the power adaptor.

1. Plug the jack-end of the power adaptor into the power connector J7 (labeled 7V) on the EZ-KIT Lite board.
2. Plug the other side of the power adaptor into a power outlet. The power LED (labeled LED7) is lit green when power is applied to the board.
3. Power the emulator (if used). Plug the jack-end of the assembled power adaptor into the emulator and plug the other side of the power adaptor into a power outlet. The enable/power is lit green when power is applied.

Step 3 (if connected through the debug agent): Verify that the yellow USB monitor LED (labeled ZLED3) on the debug agent is on. This signifies that the board is communicating properly with the host PC and ready to run CCES.

Session Startup

It is assumed that the CrossCore Embedded Studio software is installed and running on your PC.

Note: If you connect the board or emulator first (before installing CCES) to the PC, the Windows driver wizard may not find the board drivers.

1. Navigate to the CCES environment via the **Start** menu.

   Note that CCES is not connected to the target board.

2. Use the system configuration utility to connect to the EZ-KIT Lite board.

   If a debug configuration exists already, select the appropriate configuration and click **Apply and Debug** or **Debug**. Go to step 8.

   To create a debug configuration, do one of the following:

   - Click the down arrow next to the little bug icon, select **Debug Configurations**
   - Choose **Run > Debug Configurations**.

   The **Debug Configuration** dialog box appears.

3. Select **CrossCore Embedded Studio Application** and click  (**New launch configuration**).

   The **Select Processor** page of the **Session Wizard** appears.

4. Ensure **Blackfin** is selected in **Processor family**. In **Processor type**, select **ADSP-BF538F**. Click **Next**.

   The **Select Connection Type** page of the **Session Wizard** appears.

5. Select one of the following:
   - For standalone debug agent connections, **EZ-KIT Lite** and click **Next**.
   - For emulator connections, **Emulator** and click **Next**.

   The **Select Platform** page of the **Session Wizard** appears.
6. Do one of the following:
   - For standalone debug agent connections, ensure that the selected platform is **ADSP-BF538F EZ-KIT** Lite via Debug Agent.
   - For emulator connections, choose the type of emulator that is connected to the board.
7. Click **Finish** to close the wizard.

   The new debug configuration is created and added to the program(s) to load list.
8. In the **Program(s) to load** section, choose the program to load when connecting to the board. If not loading any program upon connection to the target, do not make any changes.

   Note that while connected to the target, there is no way to choose a program to download. To load a program once connected, terminate the session.

To delete a configuration, go to the **Debug Configurations** dialog box and select the configuration to delete. Click  and choose **Yes** when asked if you wish to delete the selected launch configuration. Then **Close** the dialog box.

To disconnect from the target board, click the terminate button (red box) or choose **Run > Terminate**.

To delete a session, choose **Target > Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

VisualDSP++ Install and Session Startup

For information about VisualDSP++ and to download the software, go to www.analog.com/VisualDSP.

1. Verify that the yellow USB monitor LED (ZLED3, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the **Start > Programs** menu.

   The main window appears. Note that VisualDSP++ does not connect to any session. Skip the rest of this step to step 3.

   If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and force VisualDSP++ to start a new session by pressing and holding down the **Ctrl** key while starting VisualDSP++. Do not release the **Ctrl** key until the **Session Wizard** appears on the screen. Go to step 4.

3. To connect to a new EZ-KIT Lite session, start **Session Wizard** by selecting one of the following.
    - From the **Session** menu, **New Session**.
    - From the **Session** menu, **Session List**. Then click **New Session** from the **Session List** dialog box.
    - From the **Session** menu, **Connect to Target**.
4. The **Select Processor** page of the wizard appears on the screen. Ensure **Blackfin** is selected in **Processor family**. In **Choose a target processor**, select **ADSP-BF538F**. Click **Next**.
5. The **Select Connection Type** page of the wizard appears on the screen. Select **EZ-KIT Lite** and click **Next**.
6. The **Select Platform** page of the wizard appears on the screen. In the **Select your platform** list, select **ADSP-BF538F EZ-KIT Lite via Debug Agent**. In **Session name**, highlight or specify the session name.

    The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and to open a new session.

    Click **Next**.
7. The **Finish** page of the wizard appears on the screen. The page displays your selections. If you are satisfied, click **Finish**. If not, click **Back** to make changes.

To disconnect from a session, click the disconnect button  or select **Session > Disconnect from Target**.

To delete a session, select **Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

CCES Evaluation License

The ADSP-BF538F EZ-KIT Lite software is part of the Board Support Package (BSP) for the Blackfin ADSP-BF53x family. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for 90 days after activation. Once the evaluation period ends, the evaluation license becomes permanently disabled. If the evaluation license is installed but not activated, it allows 10 days of unrestricted use and then becomes disabled. The license can be re-enabled by activation.

An evaluation license can be upgraded to a full license. Licenses can be purchased from:

- Analog Devices directly. Call (800) 262-5645 or 781-937-2384 or go to:
  `http://www.analog.com/buyonline`.
- Analog Devices, Inc. local sales office or authorized distributor. To locate one, go to:
  `http://www.analog.com/salesdir/continent.asp`.

The EZ-KIT Lite hardware must be connected and powered up to use CCES with a valid evaluation or full license.

VisualDSP++ Evaluation License

The ADSP-BF538F EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-BF538F EZ-KIT Lite via the USB debug agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a user's program to 20 KB of memory for code space with no restrictions for data space.

To avoid errors when opening VisualDSP++, the EZ-KIT Lite hardware must be connected and powered up. This is true for using VisualDSP++ with a valid evaluation or full license.

Memory Map

The ADSP-BF538F processor has internal SRAM that can be used for instruction or data storage. SRAM configuration details can be found in the *ADSP-BF538/ADSP-BF538F Blackfin Processor Hardware Reference*.

The ADSP-BF538F EZ-KIT Lite board includes two types of external memory: SDRAM and flash.

The size of SDRAM is 64 Mbytes (32M x 16-bit). The processor's memory select pin, $\overline{\text{SMS0}}$, is configured for SDRAM.

The size of the external flash memory is 4 Mbytes (2M x 16-bits), and the size of the internal flash memory is 1 Mbyte. The processor's asynchronous memory select pins ($\overline{\text{AMS3-0}}$) are configured for flash memory. Any of the $\overline{\text{AMS}}$ signals can be mapped to internal or external flash memory.

Table 1-1. EZ-KIT Lite Evaluation Board Memory Map

Start Address		End Address	Content
External Memory	0x0000 0000	0x03FF FFFF	SDRAM bank 0 (SDRAM). See "SDRAM Interface" on page 1-13.
	0x2000 0000	0x200F FFFF	ASYNC memory bank 0. See "Flash Memory" on page 1-15.
	0x2010 0000	0x201F FFFF	ASYNC memory bank 1. See "Flash Memory" on page 1-15.
	0x2020 0000	0x202F FFFF	ASYNC memory bank 2. See "Flash Memory" on page 1-15.
	0x2030 0000	0x203F FFFF	ASYNC memory bank 3. See "Flash Memory" on page 1-15.
	All other locations		Not used
Internal Memory	0xFF80 0000	0xFF80 3FFF	Data bank A SRAM 16 KB
	0xFF80 4000	0xFF80 7FFF	Data bank A SRAM/CACHE 16 KB
	0xFF90 0000	0xFF90 7FFF	Data bank B SRAM 16 KB
	0xFF90 4000	0xFF90 7FFF	Data bank B SRAM/CACHE 16 KB
	0xFFA0 0000	0xFFA0 7FFF	Instruction bank A SRAM 32 KB
	0xFFA1 0000	0xFFA1 3FFF	Instruction bank B SRAM 16 KB
	0xFFA0 8000	0xFFA0 BFFF	Instruction SRAM/CACHE 16 KB
	0xFFB0 0000	0xFFB0 0FFF	Scratch pad SRAM 4 KB
	0xFFC0 0000	0xFFDF FFFF	System MMRs 2 MB
	0xFFE0 0000	0xFFFF FFFF	Core MMRs 2 MB
	All other locations		Reserved

SDRAM Interface

The three SDRAM control registers must be initialized in order to use the MT48LC32M8A2 32M x 16 bits (64 MB) SDRAM memory. When you are in a CCES or VisualDSP++ session and connect to the EZ-KIT Lite board, the SDRAM registers are configured automatically through the debugger each time the processor is reset. The values in Table 1-2 are used whenever SDRAM bank 0 is accessed through the debugger (for example, when viewing memory windows or loading a program). The numbers were derived for maximum flexibility and work for a system clock frequency between 54 MHz and 133 MHz.

Table 1-2. EZ-KIT Lite Session SDRAM Default Settings[1]

Register	Value	Function
EBIU_SDGCTL	0x0091998D	Calculated with SCLK = 133 MHz 16-bit data path External buffering timing disabled t_{WR} = 2 SCLK cycles t_{RCD} = 3 SCLK cycles t_{RP} = 3 SCLK cycles t_{RAS} = 6 SCLK cycles pre-fetch disabled CAS latency = 3 SCLK cycles SCLK1 disabled
EBIU_SDBCTL	0x00000025	Bank 0 enabled Bank 0 size = 64 MB Bank 0 column address width = 10 bits
EBIU_SDRRC	0x000003A0	Calculated with SCLK = 54 MHz RDIV = 416 clock cycles

1 54 MHz <=SCLK <= 133 MHz.

To re-write the EBIU_SDGCTL register within the user code, first, place the chip in self-refresh (see the *ADSP-BF538/ADSP-BF538F Blackfin Processor Hardware Reference*). To disable the automatic setting of the registers, do one of the following:

- CCES users, choose **Target > Settings > Target Options** and clear the **Use XML reset values** check box.
- VisualDSP++ users, choose **Settings > Target Options** and clear the **Use XML reset values** check box.

For more information about the **Target Options** dialog box, see the online help.

Automatic configuration of SDRAM is not optimized for any SCLK frequency. Table 1-3 shows optimized configuration for the SDRAM registers using a 125 MHz and 133 MHz SCLK. Only the EBIU_SDRRC register needs to be modified in the user code to achieve maximum performance.

Table 1-3. SDRAM Optimum Settings

Register	SCLK = 133 MHz (CCLK = 400 MHz)	SCLK = 125 MHz (CCLK = 500 MHz)
EBIU_SDGCTL	0x0091 998D	0x0091 998D
EBIU_SDBCTL	0x0000 0025	0x0000 0025
EBIU_SDRRC	0x0000 0408	0x0000 03A0

An example program is included in the EZ-KIT Lite installation directory to demonstrate the SDRAM memory setup.

Flash Memory

The flash memory interface of the ADSP-BF538F EZ-KIT Lite can connect to an external 4 MB (2M x 16-bits) ST Micro M29W320EB device or the 1 MB internal flash memory. The size and connections of flash memory are controlled by the flash address range switch (SW6) and the flash chip enable (FCE) switch (SW14). See "Flash Enable Switch (SW6)" on page 2-11 and "FCE Enable Switch (SW14)" on page 2-12.

The default for the SW6 switch is all positions ON, which allows the user to have access to the full 4 MB of the external flash memory. The default for the SW14 switch is all positions OFF, which allows the user to have access to the full 4 MB of the external flash memory. Each $\overline{\text{AMS}}$ signal accounts for 1 MB of flash memory. The amount of available flash memory decreases as $\overline{\text{AMS}}$ signals are turned OFF.

Example code is provided in the EZ-KIT Lite installation directory to demonstrate how to program flash memory.

Table 1-4 shows a sample value for the asynchronous memory configuration register, EBIU_AMBCTL0.

Table 1-4. Asynchronous Memory Control Register Setting Example

Register	Value	Function
EBIU_AMBCTL0	0x7BB07BB0	Timing control for banks 1 and 0

CAN Interface

The Controller Area Network interface contains a Philips TJA1041 high-speed CAN transceiver. The PD9 programmable flag connects to the error and power-on indication output (ERR). The PC1 of the processor connects to the receive data output (RXD), and PC0 connects to the transmit data input (TXD).

The CAN interface can be disconnected from the processor by turning positions 1 though 4 of the SW2 switch OFF. When in the OFF position, the signals can be used elsewhere on the board. See "CAN Enable Switch (SW2)" on page 2-10 for more information.

The CAN interface contains two 4-position modular connectors (see "CAN Connectors (J5 and J11)" on page 2-21).

Example programs are included in the EZ-KIT Lite installation directory to demonstrate CAN circuit operation.

ELVIS Interface

This EZ-KIT Lite board contains the National Instruments ELVIS interface. The interface features the DC voltage and current measurement modules, oscilloscope and bode analyzer modules, function generator, arbitrary waveform generator, and digital IO.

The ELVIS interface is a NI LabVIEW-based design and prototype environment for university science and engineering laboratories. The ELVIS interface consists of the LabVIEW-based virtual instruments, a multifunction data acquisition (DAQ) device, and a custom-designed bench-top workstation and prototype board. This combination provides a ready-to-use suite of instruments found in most educational laboratories. Because the interface is based on the LabVIEW and provides complete data acquisition and prototyping capabilities, the system is ideal for academic coursework that range from lower-division classes to advanced project-based curriculums.

For more information on ELVIS and example demonstration programs, visit National Instruments Web site at www.ni.com.

Audio Interface

The audio circuit of the EZ-KIT Lite consists of an AD1871 analog-to-digital converter (ADC) and an AD1854 digital-to-analog converter (DAC). The audio circuit provides one channel of stereo input and one channel of stereo output via 3.5 mm stereo jacks. The SPORT0 interface of the processor is linked with the stereo audio data input and output pins of the audio circuit.

The frame sync and bit clocks are generated from the ADC and feed to the processor because the ADC is operating in master mode. The audio interface samples data at a 48 kHz sample rate. The serial data interface operates in 2-wire interface (TWI) mode and connects to SPORT0 of the processor.

The audio interface can be disconnected from the SPORT0 by turning positions 1 and 5 of the SW7 switch OFF. When in the OFF position, the SPORT0 signals can be used on the SPORT0 connector (P6) or on the expansion interface (see "SPORT0 and SPORT1 Connectors (P6 and P7)" on page 2-23 and "Audio Enable Switch (SW7)" on page 2-12 for more information).

Example programs are included in the EZ-KIT Lite installation directory to demonstrate audio circuit operation.

LEDs and Push Buttons

The EZ-KIT Lite provides four push buttons and five LEDs for general-purpose IO.

The five LEDs, labeled LED2 through LED6, are accessed via the PC5-9 processor pins. For information on how to program the pins, refer to the *ADSP-BF538/ADSP-BF538F Blackfin Processor Hardware Reference*.

The four general-purpose push button are labeled SW10 through SW13. A status of each individual button can be read through the processor's programmable flag inputs, PF0-3. The signal reads 1 when a corresponding switch is being pressed-on. When the switch is released, the signal reads 0. A connection between the push button and programmable flag input is established through the DIP switch, SW5. See "LEDs and Push Buttons" on page 2-17 for details.

An example program is included in the EZ-KIT Lite installation directory to demonstrate functionality of the LEDs and push buttons.

Board Design Database

A .zip file containing all of the electronic information required for the design, layout, fabrication and assembly of the product is available for download from the Analog Devices board design database at: http://www.analog.com/board-design-database.

Example Programs

Example programs are provided with the ADSP-BF538F EZ-KIT Lite to demonstrate various capabilities of the product. The programs are included in the product installation kit and can be found in the Examples folder of the installation. Refer to a readme file provided with each example for more information.

CCES users are encouraged to use the example browser to find examples included with the EZ-KIT Lite Board Support Package.

2 ADSP-BF538F EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF538F EZ-KIT Lite board. The following topics are covered.

- "System Architecture" on page 2-2
  Describes the ADSP-BF538F EZ-KIT Lite board configuration and explains how the board components interface with the processor.
- "Jumper and Switch Settings" on page 2-9
  Shows the locations and describes the configuration jumpers and switches.
- "LEDs and Push Buttons" on page 2-17
  Shows the locations and describes the LEDs and push buttons.
- "Connectors" on page 2-20
  Shows the locations and provides part numbers for the on-board connectors. In addition, the manufacturer and part number information is provided for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board.

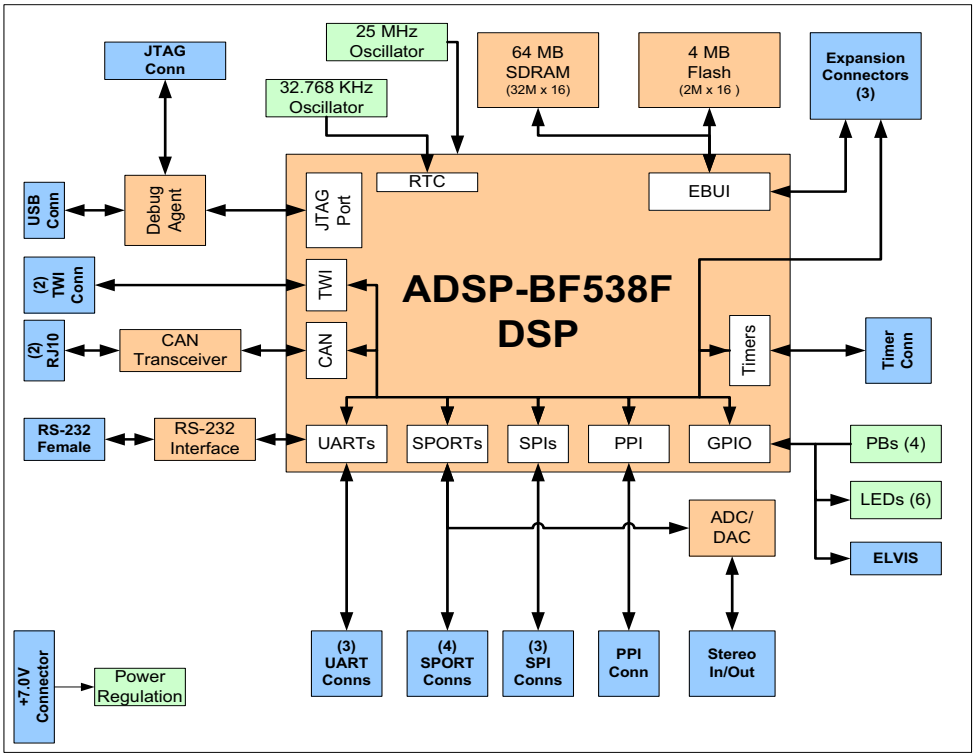

Figure 2-1. System Architecture

This EZ-KIT Lite is designed to demonstrate capabilities of the ADSP-BF538F Blackfin processor. The processor has an IO voltage of 3.3V. The core voltage of the processor is supplied by the internal voltage regulator.

The core voltage and the core clock rate can be set on the fly by the processor. The input clock is 25 MHz. A 32.768 kHz crystal supplies the real-time clock (RTC) inputs of the processor. The default boot mode for the processor is flash boot. See "Boot Mode Select Switch (SW3)" on page 2-13 for information about changing the default boot mode.

External Bus Interface Unit

The external bus interface unit (EBIU) connects external memory to the ADSP-BF538F processor. The unit includes a 16-bit wide data bus, an address bus, and a control bus. On the EZ-KIT Lite, the EBIU connects to the SDRAM, flash memory, and expansion interfaces.

The 64 Mbytes (32M x 16 bits) of SDRAM connect to the synchronous memory select 0 pin ($\overline{\text{SMS0}}$). Refer to "SDRAM Interface" on page 1-13 for information about SDRAM configuration. Note that SDRAM clock is the processor's clock out (CLK OUT), which must not exceed 133 MHz.

The flash memory device connects to the asynchronous memory select signals, $\overline{\text{AMS3}}$ through $\overline{\text{AMS0}}$. The device provides a total of 4 MB of external flash memory or 1 MB of internal flash memory. The processor can use flash memory for both booting and storing information during a standard mode of operation. Refer to "Flash Memory" on page 1-15 for details.

All of the address, data, and control signals are available externally via the expansion interface (J1-3). The pinout of these connectors can be found in "ADSP-BF538F EZ-KIT Lite Schematic" on page B-1.

SPORT0 Interface

SPORT0 connects to the audio circuit, SPORT0 connector (P6), and expansion interface. The audio circuit uses the primary data transmit and receive pins to input and output data from the audio input and outputs.

SPORT1 and SPORT2 of the processor connect to the SPORT connectors (P3 and P4) and expansion interface.

The pinout of the SPORT interface and expansion interface connectors can be found in "ADSP-BF538F EZ-KIT Lite Schematic" on page B-1.

SPI Interface

The serial peripheral interface (SPI) of the processor connects to the SPI connectors (P1, P2, and P9) and expansion interface.

UART Interface

The UART interface of the processor connects to the UART connectors (P12, P14, and P15) and expansion interface.

Programmable Flags

The processor has 53 general-purpose input/output (GPIO) signals spread across four ports (PC, PD, PE, and PF). The pins are multi-functional and depend on the processor setup. Table 2-1 shows how the programmable flag pins are used on the EZ-KIT Lite.

Table 2-1. Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PC0	CANTX	UART0 CTS/CAN transmit
PC1	CANRX	UART0 CTS/CAN receive
PC5		LED (LED2) or ELVIS_PF1. See "LED and Push Button Locations" on page 2-17 and "Push Button Enable Switch (SW5)" on page 2-11 for information on how to disable the push button.
PC6		LED (LED3) or ELVIS_PF2. See "LED and Push Button Locations" on page 2-17 and "Push Button Enable Switch (SW5)" on page 2-11 for information on how to disable the push button.
PC7		LED (LED4) or ELVIS_PF5. See "LED and Push Button Locations" on page 2-17 and "Push Button Enable Switch (SW5)" on page 2-11 for information on how to disable the push button.
PC8		LED (LED5) or ELVIS_PF6. See "LED and Push Button Locations" on page 2-17 and "Push Button Enable Switch (SW5)" on page 2-11 for information on how to disable the push button.
PC9		LED (LED6) or ELVIS_PF7. See "LEDs and Push Buttons" on page 1-17 and "Push Button Enable Switch (SW5)" on page 2-11 for information on how to disable the push button.
PD0	MOSI1	Not used
PD1	MISO1	Not used
PD2	SCK1	Not used
PD3	SPI1SS	Not used
PD4	SPI1SEL	AUDIO_RESET
PD5	MOSI2	Not used

Table 2-1. Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PD6	MISO2	Not used
PD7	SCK2	PPI_DIR_CTL (for AV-Extender)
PD8	SPI2SS	PPI_CLK_SEL (for AV-Extender)
PD9	SPI2SEL	CAN_ERR
PD10	RX1	Not used
PD11	TX1	Not used
PD12	RX2	Not used
PD13	TX2	Not used
PE0	RSCLK2	Not used
PE1	RFS2	Not used
PE2	DR2PRI	Not used
PE3	DR2SEC	Not used
PE4	TSCLK2	Not used
PE5	TFS2	Not used
PE6	DT2PRI	Not used
PE7	DT2SEC	Not used
PE8	RSCLK3	Not used
PE9	RFS3	Not used
PE10	DR3PRI	Not used
PE11	DR3SEC	Not used
PE12	TSCLK3	Not used
PE13	TFS3	Not used
PE14	DT3PRI	Not used
PE15	DT3SEC	Not used

Table 2-1. Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PF0	SPISS	Push button (SW13). See "Programmable Flag Push Buttons (SW10–13)" on page 2-18.
PF1	SPIOSEL1/TMRCLK	Push button (SW12). See "Programmable Flag Push Buttons (SW10–13)" on page 2-18.
PF2	SPIOSEL2	Push button (SW11). See "Programmable Flag Push Buttons (SW10–13)" on page 2-18.
PF3	PPI_FS3/SPIOSEL3	Push button (SW10). See "Programmable Flag Push Buttons (SW10–13)" on page 2-18.
PF4	PPI_D15/SPIOSEL4	Not used
PF5	PPI_D14/SPIOSEL5	Not used
PF6	PPI_D13/SPIOSEL6	Not used
PF7	PPI_D12/SPIOSEL7	Not used
PF8	PPI_D11	Not used
PF9	PPI_D10	Not used
PF10	PPI_D9	Not used
PF11	PPI_D8	Not used
PF12	PPI_D7	Not used
PF13	PPI_D6	Not used
PF14	PPI_D5	No used
PF15	PPI_D4	Not used

UART Port

The universal asynchronous receiver/transmitter (UART) port of the processor connects to the ADM3202 RS-232 line driver as well as to the expansion interface. The RS-232 line driver connects to the DB9 female connector, providing an interface to a PC and other serial devices.

Expansion Interface

The expansion interface consists of three 90-pin connectors. Table 2-2 shows the interfaces each connector provides. For the exact pinout of the connectors, refer to "ADSP-BF538F EZ-KIT Lite Schematic" on page B-1. The mechanical dimensions of the connectors can be obtained from Technical Support.

Analog Devices offers many EZ-Extender® products that plug on to the expansion interface. For more information on these products, visit the Analog Devices Web site at:
www.analog.com/processors/tools/blackfin.

Table 2-2. Expansion Interface Connectors

Connector	Interfaces
J1	5V, GND, address, data, PPI
J2	3.3V, GND, SPI, NMI, TMR2-0, SPORT0, SPORT1, PF15-0, EBUI control signals
J3	5V, 3.3V, GND, UART, flash IO, reset, audio control signals

Limits to the current and to the interface speed must be taken into consideration when using the expansion interface. The maximum current limit is dependent on the capabilities of the used regulator. Additional circuitry also can add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the processor's internal and external memory through a 6-pin interface. The JTAG emulation port of the processor connects also to the USB debugging interface. When an emulator connects to the board at ZP4, the USB debugging interface is disabled. See "JTAG Connector (ZP4)" on page 2-23 for more information about the connector.

To learn more about available emulators, go to: www.analog.com/processors/tools/blackfin.

Jumper and Switch Settings

The jumper and switch locations are shown in Figure 2-2.

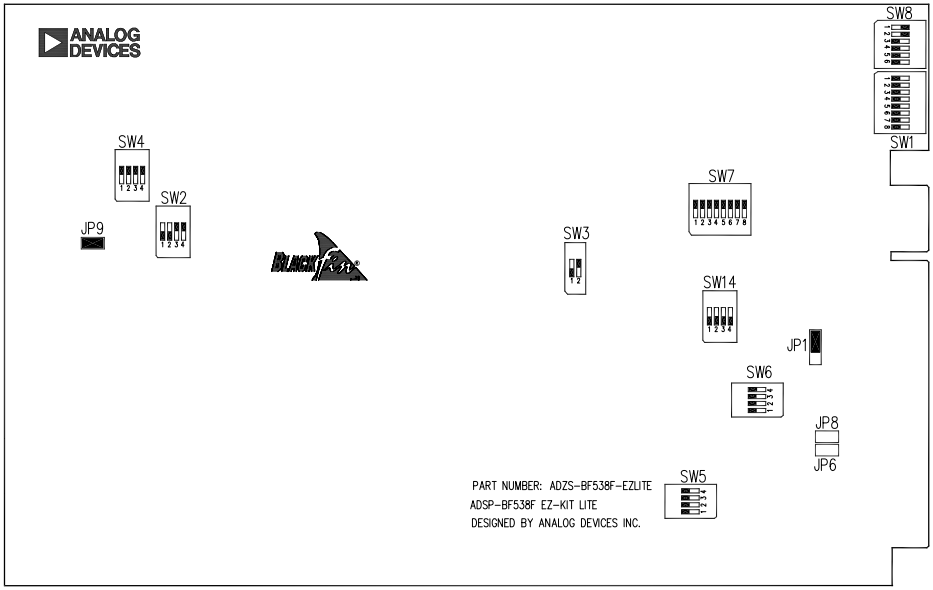

Figure 2-2. Jumper and Switch Locations

CAN Enable Switch (SW2)

The Controller Area Network (CAN) enable switch (SW2) disconnects CAN signals from the GPIO pins of the processor. When the SW2 switch is in the OFF position, the associated GPIO signals (see Table 2-3) can be used on the expansion interface.

Table 2-3. CAN Enable Switch (SW2)

CAN Signal	SW2 Switch Position (Default)	Processor Signal
ENABLE	1 (ON)	NU
STANDBY	2 (ON)	NU
ERROR	3 (ON)	PD9
RECEIVE DATA	4 (ON)	PC1

UART Enable Switch (SW4)

The UART enable switch (SW4) disconnects UART signals from the GPIO pins of the processor. When the switch is in the OFF position, the associated GPIO signals (see Table 2-4) can be used on the expansion interface.

Table 2-4. UART Enable Switch (SW4)

EZ-KIT Lite Signal	SW4 Switch Position (Default)	Processor Signal
CTS	1 (ON)	PC0
RX0	2 (ON)	NU
RTS	3 (ON)	PC1
LOOPBACK	4 (OFF)	NU

Push Button Enable Switch (SW5)

The push button enable switch (SW5) disconnects the associated signal and the push button circuit drivers from the GPIO pins of the processor. When the SW5 switch is in the OFF position, the GPIO signal (see Table 2-5) can be used on the expansion interface.

Table 2-5. Push Button Enable Switch (SW5)

Push Button	SW5 Switch Position (Default)	Processor Signal
PB1 (SW13)	1 (ON)	PF0
PB2 (SW12)	2 (ON)	PF1
PB3 (SW11)	3 (ON)	PF2
PB4 (SW10)	4 (ON)	PF3

Flash Enable Switch (SW6)

The flash enable switch (SW6) disconnects the $\overline{\text{AMS}}$ signals from the external flash memory, allowing other devices to utilize the signals via the expansion interface. For each switch listed in Table 2-6 that is turned OFF, the size of available flash memory is reduced by 1 MB.

Table 2-6. Flash Enable Switch (SW6)

Processor Signal	SW6 Switch Position (Default)
$\overline{\text{AMS0}}$	1 (ON)
$\overline{\text{AMS1}}$	2 (ON)
$\overline{\text{AMS2}}$	3 (ON)
$\overline{\text{AMS3}}$	4 (ON)

FCE Enable Switch (SW14)

The flash chip enable (FCE) switch (SW14) selects which $\overline{\text{AMS}}$ signals connect to the internal flash memory. Since the internal memory is 1 MB, only one $\overline{\text{AMS}}$ signal must be connected at a time. For each switch listed in Table 2-7 that is turned ON, the size of available flash memory is reduced by 1 MB.

Table 2-7. FCE Enable Switch (SW14)

Processor Signal	SW14 Switch Position (Default)
$\overline{\text{AMS0}}$	1 (OFF)
$\overline{\text{AMS1}}$	2 (OFF)
$\overline{\text{AMS2}}$	3 (OFF)
$\overline{\text{AMS3}}$	4 (OFF)

Audio Enable Switch (SW7)

The audio enable switch (SW7) disconnects the audio signals from the processor (positions 1–5) and determines how the clock for the audio circuit generates and connects (positions 6–8). Position 8 determines if the ADC is in master or slave mode. When in master mode (position 8 is ON), the ADC generates the clock. When in slave mode (position 8 is OFF), the processor generates the clock. Positions 6 and 7 connect together the transmit and receive clocks (see Table 2-8).

Table 2-8. Audio Enable Switch (SW7)

EZ-KIT Lite Signal	SW7 Switch Position (Default)	Processor Signal
DROPRI	1 (ON)	DROPRI
RSCLK0	2 (ON)	RSCLK0
RFS0	3 (ON)	RFS0
TSCLK0	4 (ON)	TSCLK0

Table 2-8. Audio Enable Switch (SW7) (Cont'd)

EZ-KIT Lite Signal	SW7 Switch Position (Default)	Processor Signal
TFS0	5 (ON)	TFS0
Clock loopback	6 (ON)	NU
FS loopback	7 (ON)	NU
ADC master/slave	8 (ON)	NU

Boot Mode Select Switch (SW3)

This switch (SW3) determines the boot mode of the processor. Table 2-9 shows the available boot mode settings. By default, the ADSP-BF538F processor boots from the on-board flash memory.

Table 2-9. Boot Mode Select Switch (SW3)

Position 1 BMODE0	Position 2 BMODE1	Boot Mode
ON	ON	Execute from 16-bit external memory
ON	OFF	Boot from 16-bit flash memory (default)
OFF	ON	Boot from SPI serial master
OFF	OFF	Boot from SPI serial slave
Note: For SW3, a switch position of "ON" applies logic low for the corresponding BMODE pin, and a switch position of "OFF" applies logic high for the corresponding BMODE pin.		

PPI Direction Control (JP1)

The PPI direction control jumper (JP1) is used when the board connects to a Blackfin AV EZ-Extender. JP1 allows the GPIO signal PD7 to control the direction of the PPI bus via a software flag. The default is positions 1 and 2. When connected to the extender, JP1 must be placed in positions 2 and 3.

UART Loop Jumper (JP9)

The UART loop jumper (JP9) is for looping the transmit and receive signals. The default is OFF.

ELVIS Oscilloscope Configuration Switch (SW1)

The oscilloscope configuration switch (SW1) determines which audio circuit signals connect to channels A and B of the oscilloscope. The switch is used when the board connects to the Educational Laboratory Virtual Instrumentation Suite (ELVIS) station (see "ELVIS Interface" on page 1-16). Each channel must have only one signal selected at a time (see Table 2-10).

Table 2-10. Oscilloscope Configuration Switch (SW1)

Channel	SW1 Switch Position (Default)	Audio Circuit Signal
A	1 (OFF)	AMP_LEFT_IN
A	2 (OFF)	AMP_RIGHT_IN
A	3 (OFF)	LEFT_OUT
A	4 (OFF)	RIGHT_OUT
B	5 (OFF	AMP_LEFT_IN
B	6 (OFF)	AMP_RIGHT_IN
B	7 (OFF)	LEFT_OUT
B	8 (OFF)	RIGHT_OUT

ELVIS Function Generator Configuration Switch (SW8)

The function generator configuration switch (SW8) controls signals connecting to the left and right input signals of the audio interface. The SW8 switch is used when the board connects to the ELVIS station (see "ELVIS Interface" on page 1-16). Each channel must have only one signal selected at a time, as described in Table 2-11.

Table 2-11. Function Generator Configuration Switch (SW8)

Channel	SW8 Switch Position (Default)	Audio Circuit Signal
AMP_LEFT_IN	1 (ON)	LEFT_IN
AMP_RIGHT_IN	2 (ON)	RIGHT_IN
AMP_LEFT_IN	3 (OFF)	DAC0
AMP_RIGHT_IN	4 (OFF)	DAC1
AMP_LEFT_IN	5 (OFF)	FUNCT_OUT
AMP_RIGHT_IN	6 (OFF)	FUNCT_OUT

ELVIS Voltage Selection Jumper (JP6)

The ELVIS voltage selection jumper (JP6) is used to select the power source for the EZ-KIT Lite. In a standard mode of operation, the board receives its power from an external power supply. When JP6 is installed, the board is powered from an ELVIS station, and no external power supply is required. The jumper setting is shown in Table 2-12.

Table 2-12. ELVIS Voltage Selection Jumper (JP6)

JP6 Setting	Mode
OFF	**Powered from an external power supply (default)**
ON	Powered from an ELVIS station

The external power supply must be disconnected from the board when JP6 is installed. Otherwise, the power supply can cause damage to the EZ-KIT Lite board and ELVIS unit.

ELVIS Select Jumper (JP8)

The ELVIS select jumper (JP8) configures the EZ-KIT Lite's connection to an ELVIS station (see "ELVIS Interface" on page 1-16). When JP8 is installed, the connections to the push buttons and LED are redirected to the ELVIS station, instead of the processor. The jumper setting is shown in Table 2-13.

Table 2-13. ELVIS Select Jumper (JP8)

JP8 Setting	Mode
OFF	**Not connected to an ELVIS station (default)**
ON	Connected to an ELVIS station

LEDs and Push Buttons

This section describes functionality of the LEDs and push buttons. Figure 2-3 shows the locations of the LEDs and push buttons.

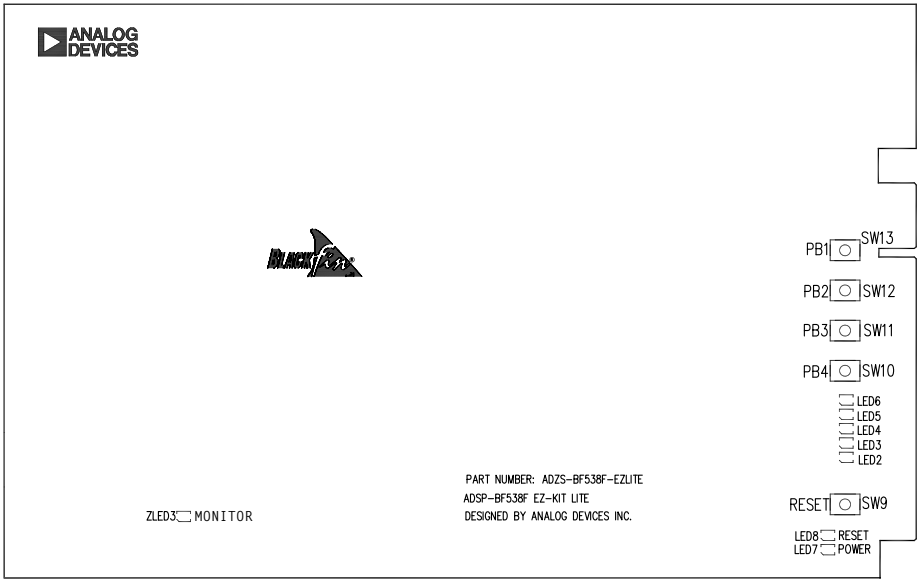

Figure 2-3. LED and Push Button Locations

Reset Push Button (SW9)

The RESET push button resets all of the ICs on the board. One exception is the USB interface chip. The chip is not being reset when the push button is pressed after the USB cable has been plugged in and communication with the PC has been initialized correctly. After USB communication has been initialized, the only way to reset the USB chip is by powering down the board.

Programmable Flag Push Buttons (SW10–13)

Four push buttons, SW10-13, are provided for general-purpose user input. The buttons connect to the PF0-3 programmable flag pins of the processor. The push buttons are active high and, when pressed, send a high (1) to the processor. Refer to "LEDs and Push Buttons" on page 1-17 for more information on how to use the flags to program the processor. The push button enable switch (SW5) is capable of disconnecting the push buttons from its corresponding PF signal (refer to "Push Button Enable Switch (SW5)" on page 2-11). The programmable flag signals and associated switches are shown in Table 2-14.

Table 2-14. Programmable Flag Switches

Processor Programmable Flag Pin	Push Button Reference Designator
PF0	SW13
PF1	SW12
PF2	SW11
PF3	SW10

Power LED (LED7)

When LED7 is lit (green), it indicates that power is being properly supplied to the board.

Reset LED (LED8)

When LED8 is lit, it indicates that the master reset of all the major ICs is active.

User LEDs (LED2–6)

Five LEDs connect to five general-purpose IO pins of the processor (see Table 2-15). The LEDs are active high and are lit by writing a 1 to the correct PC signal. Refer to "LEDs and Push Buttons" on page 1-17 for more information about how to use flash memory when programming the LEDs.

Table 2-15. User LEDs

LED Reference Designator	Processor Programmable Flag Pin
LED2	PC5
LED3	PC6
LED4	PC7
LED5	PC8
LED6	PC9

USB Monitor LED (ZLED3)

The USB monitor LED (ZLED3) indicates that USB communication has been initialized successfully, and you can connect to the processor using a CCES or VisualDSP++ EZ-KIT Lite session. This takes approximately 15 seconds. If the LED does not light, try cycling power on the board and/or re-installing the USB driver.

When CCES or VisualDSP++ is actively communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.

Connectors

This section describes the connector functionality and provides information about mating connectors. The connector locations are shown in Figure 2-4.

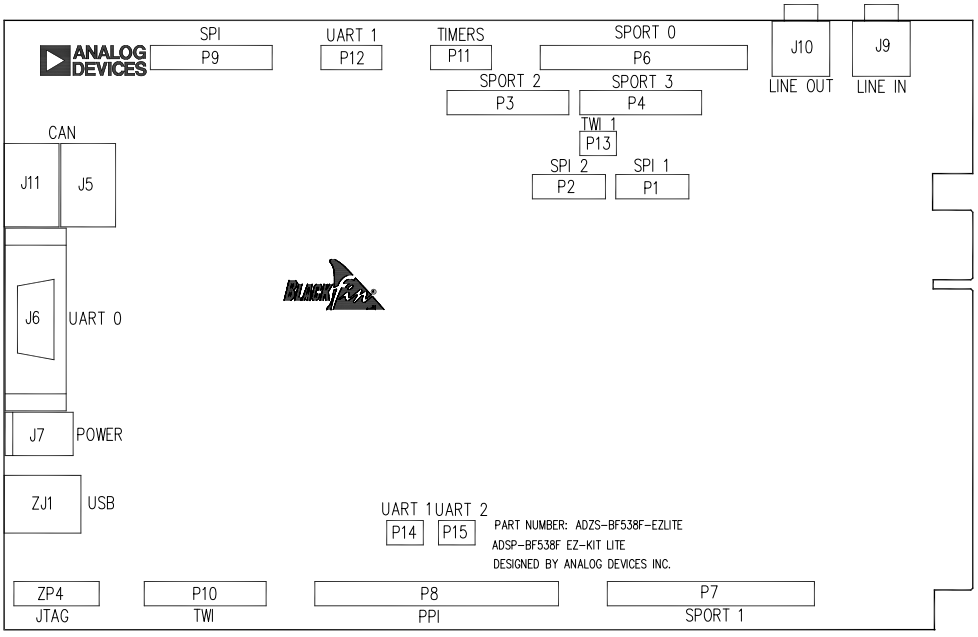

Figure 2-4. Connector Locations

Audio Connectors (J9 and J10)

Part Description	Manufacturer	Part Number
3.5 mm stereo jack	A/D ELECTRONICS	ST323-5
Mating Cable (shipped with EZ-KIT Lite)		
3.5 mm stereo interconnect cable	RANDOM	10A3-01106
3.5 mm headphones	KOSS	UR5

CAN Connectors (J5 and J11)

Part Description	Manufacturer	Part Number
Modular jack	AMP	5558872-1
Mating Cable		
4-conductor modular jack cable	L-COM	TSP3044

RS-232 Connector (J6)

Part Description	Manufacturer	Part Number
DB9, female, vertical mount	NORCOMP	191-009-213-L-571
Mating Cable		
2m female-to-female cable	DIGI-KEY	AE1020-ND

Power Connector (J7)

The power connector provides all of the power necessary to operate the EZ-KIT Lite board.

Part Description	Manufacturer	Part Number
2.5 mm power jack	SWITCHCRAFT	RAPC712X
Mating Power Supply (shipped with EZ-KIT Lite)		
7V power supply	CUI INC.	DMS070214-P6P-SZ

Expansion Interface Connectors (J1–3)

Three board-to-board connector footprints provide signals for most of the processor's peripheral interfaces. The connectors are located at the bottom of the board. For more information about the interface, see "Expansion Interface" on page 2-8. For the availability and pricing of the `J1`, `J12`, and `J3` connectors, contact Samtec.

Part Description	Manufacturer	Part Number
90-position 0.05" spacing, SMT	SAMTEC	SFC-145-T2-F-D-A
Mating Connector		
90-position 0.05" spacing (through hole)	SAMTEC	TFM-145-x1 series
90-position 0.05" spacing (surface mount)	SAMTEC	TFM-145-x2 series
90-position 0.05" spacing (low cost)	SAMTEC	TFC-145 series

JTAG Connector (ZP4)

The JTAG header is the connecting point for a JTAG in-circuit emulator pod. When an emulator connects to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

SPORT0 and SPORT1 Connectors (P6 and P7)

The pinout of the P6 and P7 connectors can be found in "ADSP-BF538F EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-434HLF
Mating Connector		
IDC socket	DIGI-KEY	S4217-ND

PPI Connector (P8)

The pinout of the P8 connector can be found in "ADSP-BF538F EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-440HLF
Mating Connector		
IDC socket	DIGI-KEY	S4220-ND

SPI Connector (P9)

The pinout of the P9 connector can be found in "ADSP-BF538F EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-420HLF
Mating Connector		
IDC socket	DIGI-KEY	S4210-ND

2-Wire Interface Connector (P10)

The pinout of the P10 connector can be found in "ADSP-BF538F EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-420HLF
Mating Connector		
IDC socket	DIGI-KEY	S4210-ND

TIMERS Connector (P11)

The pinout of the P11 connector can be found in "ADSP-BF538F EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-410HLF
Mating Connector		
IDC socket	DIGI-KEY	S4205-ND

UART1 Connector (P12)

The pinout of the P12 connector can be found in "ADSP-BF538F EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-410HLF
Mating Connector		
IDC socket	DIGI-KEY	S4205-ND

A ADSP-BF538F EZ-KIT LITE BILL OF MATERIALS

The bill of materials corresponds to "ADSP-BF538F EZ-KIT Lite Schematic" on page B-1.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	1	74LVC14A SOIC14	U37	TI	74LVC14AD
2	1	IDT74FCT3244APY SSOP20	U36	IDT	IDT74FCT3244APYG
3	1	SN74AHC1G00 SOT23-5	U39	TI	SN74AHC1G00DBVR
4	1	12.288MHZ OSC003	U4	DIGI-KEY	SG-8002CA-PCC-ND (12.288M)
5	1	32.768KHZ OSC008	Y2	EPSON	MC-156-32.7680KA-A0:ROHS
6	1	25MHZ OSC003	U51	DIGI-KEY	SG-8002CA-PCC-ND (25.00M)
7	5	SN74LVC1G08 SOT23-5	U22,U47-50	TI	SN74LVC1G08DBVR
8	2	MT48LC32M8A2 TSOP54	U15-16	MICRON	MT48LC32M8A2P-75
9	1	TJA1041 SOIC14	U21	PHILIPS	TJA1041T
10	1	FDS9431A SOIC8	U28	FAIRCHILD	FDS9431A
11	3	LMV722M SOIC8	U29-31	NATIONAL SEMI	LMV722MNOPB
12	1	LTC3727EUH-1 VQFN32	U20	LINEAR TECH	LTC3727EUH-1PBF

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
13	2	FDS6990AS SOIC8	U12-13	FAIRCHILD	FDS6990AS
14	1	BF538 M29W320EB "U24"	U24	ST MICRO	M29W320EB70ZE6E
15	1	ADM708SARZ SOIC8	U27	ANALOG DEVICES	ADM708SARZ
16	1	AD1854JRSZ SSOP28	U38	ANALOG DEVICES	AD1854JRSZ
17	1	AD1871YRSZ SSOP28	U33	ANALOG DEVICES	AD1871YRSZ
18	1	ADG752BRTZ SOT23-6	U6	ANALOG DEVICES	ADG752BRTZ-REEL
19	1	ADM3202ARNZ SOIC16	U32	ANALOG DEVICES	ADM3202ARNZ
20	2	AD623ARMZ USOIC8	U2-3	ANALOG DEVICES	AD623ARMZ
21	2	AD820ARZ SOIC8	U11,U23	ANALOG DEVICES	AD820ARZ
22	4	ADG774ABRQZ QSOP16	U54-57	ANALOG DEVICES	ADG774ABRQZ
23	1	ADSP-BF538F MBGA316	U1	ANALOG DEVICES	ADSP-BF538BBCZ-5F8
24	5	RUBBER FOOT	M1-5	MOUSER	517-SJ-5018BK
25	1	PWR2.5MM_JACK CON005	J7	SWITCH-CRAFT	RAPC712X
26	5	MOMENTARY SWT013	SW9-13	PANASONIC	EVQ-PAD04M
27	3	.05 45X2 CON019	J1-3	SAMTEC	SFC-145-T2-F-D-A
28	2	DIP8 SWT016	SW1,SW7	C&K	TDA08H0SB1
29	1	DIP6 SWT017	SW8	CTS	218-6LPST

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
30	5	DIP4 SWT018	SW2,SW4-6, SW14	ITT	TDA04HOSB1
31	1	DB9 9PIN CON038	J6	NORCOMP	191-009-213-L-571
32	2	RJ11 4PIN CON039	J5,J11	TYCO	5558872-1
33	1	DIP2 SWT020	SW3	C&K	TDA02H0SB1
34	3	IDC 2X1 IDC2X1	JP6,JP8-9	FCI	90726-402HLF
35	1	IDC 3X1 IDC3X1	JP1	FCI	90726-403HLF
36	2	IDC 5X2 IDC5X2	P11-12	FCI	68737-410HLF
37	1	IDC 7X2 IDC7X2	ZP4	FCI	68737-414HLF
38	4	IDC 10X2 IDC10X2	P3-4,P9-10	FCI	68737-420HLF
39	2	IDC 17X2 IDC17X2	P6-7	FCI	68737-434HLF
40	1	IDC 20X2 IDC20X2	P8	FCI	68737-440HLF
41	1	2.5A RESETABLE FUS001	F1	RAYCHEM	SMD250F-2
42	3	IDC 2PIN_JUMPER_ SHORT	SJ5-7	DIGI-KEY	S9001-ND
43	2	3.5MM STEREO_JACK CON001	J9-10	A/D ELEC-TRONICS	ST-323-5
44	3	IDC 3X2 IDC3X2	P13-15	SULLINS	GEC03DAAN
45	2	IDC 6X2 IDC6X2	P1-2	FCI	68737-412HLF
46	5	YELLOW LED001	LED2-6	PANASONIC	LN1461C
47	1	0.1UF 50V 10% 0805	C116	AVX	08055C104KAT

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
48	1	10UF 16V 10% C	CT7	AVX	TAJC106K016R
49	6	10K 1/10W 5% 0805	R69-74	VISHAY	CRCW080510K0JNEA
50	4	100 1/10W 5% 0805	R82,R100-101, R103	VISHAY	CRCW0805100RJNEA
51	4	600 100MHZ 200MA 0603	FER1-4	DIGI-KEY	490-1014-2-ND
52	1	2A S2A DO-214AA	D4	MICRO COMM	S2A-TP
53	2	68UF 25V 20% CAP003	CT1-2	PANASONIC	EEE-FC1E680P
54	1	10UH 20% IND001	L1	TDK	445-2014-1-ND
55	1	190 100MHZ 5A FER002	FER7	MURATA	DLW5BSN191SQ2
56	1	1A ZHCS1000 SOT23-312	D5	ZETEX	ZHCS1000TA pb-free
57	5	1UF 10V 10% 0805	C131,C210, C220-222	AVX	0805ZC105KAT2A
58	11	10UF 6.3V 10% 0805	C206-209, C212-218	AVX	080560106KAT2A
59	2	1000PF 10V 20% 0805	C119,C123	DIGI-KEY	311-1136-1-ND
60	13	0.1UF 10V 10% 0402	C55-57,C59-60, C111-115,C120, C126,C136	AVX	0402ZD104KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
61	71	0.01UF 16V 10% 0402	C1-27,C30-46, C91-93,C95-97, C103-104, C107-109,C132, C137,C141, C143-147, C202-205,C211, C225-227	AVX	0402YC103KAT2A
62	28	10K 1/16W 5% 0402	R2-3,R5,R7,R9, R12-16,R24-25, R77,R79-80, R84-85,R87-90, R162,R169, R171-172,R176, R179,R182,R216	VISHAY	CRCW040210K0FKED
63	1	4.7K 1/16W 5% 0402	R4	VISHAY	CRCW04024K70JNED
64	5	0 1/16W 5% 0402	R120-121,R163, R207,R215	PANASONIC	ERJ-2GE0R00X
65	4	1.2K 1/16W 5% 0402	R10,R67-68, R175	PANASONIC	ERJ-2GEJ122X
66	6	33 1/16W 5% 0402	R1,R8,R54, R75-76,R119	PANASONIC	ERJ-2GEJ330X
67	2	18PF 50V 5% 0805	C28-29	AVX	08055A180JAT2A
68	2	100MA CMDSH-3 SOD-323	D1-2	CENTRAL SEMI	CMDSH-3-E3
69	2	100UF 10V 10% C	CT3,CT5	KOA	TMC1ACTTE107K
70	2	1000PF 50V 5% 0402	C127-128	AVX	04025C102JAT2A
71	9	0.1UF 16V 10% 0603	C64,C72-74, C87-89,C125, C130	AVX	0603YC104KAT2A
72	2	33PF 50V 5% 0603	C118,C122	PANASONIC	ECJ-1VC1H330J

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
73	4	0.01UF 16V 10% 0603	C50-51,C62-63	AVX	0603YC103KAT2A
74	1	4.7UF 25V 20% 0805	C110	AVX	0805ZD475KAT2A
75	2	330PF 50V 5% 0603	C79,C84	AVX	06035A331JAT2A
76	4	10K 1/10W 5% 0603	R37,R53,R81, R99	VISHAY	CRCW060310K0JNEA
77	1	10M 1/10W 5% 0603	R11	VISHAY	CRCW060310M0FNEA
78	2	100K 1/10W 5% 0603	R20,R26	VISHAY	CRCW0603100KJNEA
79	8	330 1/10W 5% 0603	R83,R91-96,R98	VISHAY	CRCW0603330RJNEA
80	5	0 1/10W 5% 0603	R27,R113,R115, R118,R168	PHYCOMP	232270296001L
81	7	10 1/10W 5% 0603	R6,R55-57,R59, R62,R112	VISHAY	CRCW060310R0JNEA
82	2	10.0K 1/16W 1% 0603	R64,R102	DALE	CRCW060310K0FKEA
83	1	25.5K 1/16W 1% 0603	R104	DIGI-KEY	311-25.5KHRTR-ND
84	1	4700PF 16V 10% 0603	C90	DIGI-KEY	311-1083-2-ND
85	4	237.0 1/10W 1% 0603	R23,R29,R31, R33	DIGI-KEY	311-237HRTR-ND
86	2	750.0K 1/10W 1% 0603	R30,R32	DIGI-KEY	311-750KHRTR-ND
87	3	11.0K 1/10W 1% 0603	R39-40,R60	DIGI-KEY	311-11.0KHRTR-ND

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
88	4	5.49K 1/10W 1% 0603	R42-43,R46-47	DIGI-KEY	311-5.49KHRTR-ND
89	2	3.32K 1/10W 1% 0603	R44,R48	DIGI-KEY	311-3.32KHRTR-ND
90	2	1.65K 1/10W 1% 0603	R45,R49	DIGI-KEY	311-1.65KHRTR-ND
91	2	49.9K 1/10W 1% 0603	R38,R41	DIGI-KEY	311-49.9KHRTR-ND
92	2	604.0 1/10W 1% 0603	R50-51	DIGI-KEY	311-604HRTR-ND
93	2	90.9K 1/10W 1% 0603	R58,R63	DIGI-KEY	311-90.9KHRTR-ND
94	2	0.1 1/10W 1% 0603	R61,R148	PANASONIC	ERJ-3RSFR10V
95	2	10.0K 1/10W 1% 0603	R159-160	DIGI-KEY	311-10.0KHRTR-ND
96	8	5.76K 1/10W 1% 0603	R17-19,R21-22, R28,R34-35	DIGI-KEY	311-5.76KHRTR-ND
97	4	120PF 50V 5% 0603	C47-49,C71	AVX	06035A121JAT2A
98	12	100PF 50V 5% 0603	C52-54,C61, C65,C68,C75, C77,C81,C85, C94,C106	AVX	06035A101JAT2A
99	4	1000PF 50V 5% 0603	C66-67,C69-70	PANASONIC	ECJ-1VC1H102J
100	2	62.0 1/10W 1% 0603	R65-66	DIGI-KEY	311-62.0HRTR-ND
101	4	220PF 50V 5% 0603	C82,C86,C117, C124	PANASONIC	ECJ-1VC1H221J
102	2	680PF 50V 5% 0603	C80,C83	PANASONIC	ECJ-1VC1H681J

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
103	2	2200PF 50V 5% 0603	C76,C78	PANASONIC	ECJ-1VB1H222K
104	2	2.74K 1/10W 1% 0603	R36,R52	DIGI-KEY	311-2.74KHRTR-ND
105	2	15.0K 1/16W 1% 0603	R106-107	DIGI-KEY	311-15.0KHRTR-ND
106	2	27PF 50V 5% 0402	C121,C129	AVX	04025A270JAT2A
107	1	10UF 10V 10% 0805	C98	PANASONIC	ECJ-2FB1A106K
108	1	61.9K 1/16W 1% 0603	R111	PANASONIC	ERJ-3EKF6192V
109	1	105.0K 1/16W 1% 0603	R108	PANASONIC	ERJ-3EKF1053V
110	2	20.0K 1/16W 1% 0603	R109-110	PANASONIC	ERJ-3EKF2002V
111	2	8UH 20% IND008	L2-3	WURTH ELECTRON.	744392820
112	2	0.015 1W 1% 0815	R114,R116	SUSUMU	RL3720WT-015-F
113	2	10UF 16V 10% 1210	C58,C135	AVX	1210YD106KAT2A
114	1	GREEN LED001	LED7	PANASONIC	LN1361CTR
115	1	RED LED001	LED8	PANASONIC	LN1261CTR
116	2	150UF 6.3V 10% D	CT4,CT6	PANASONIC	EEFUE0J151R

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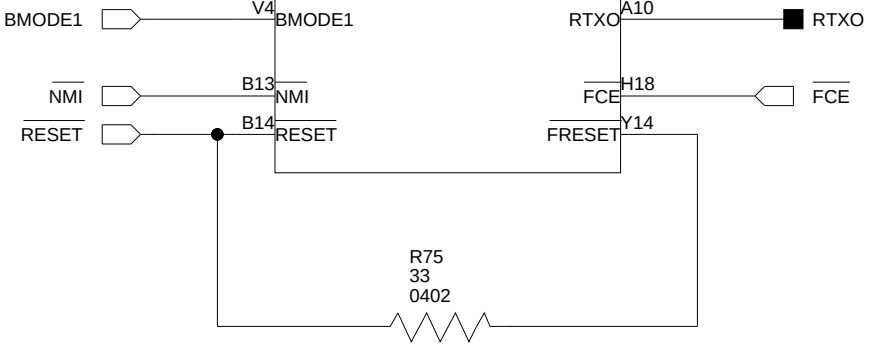
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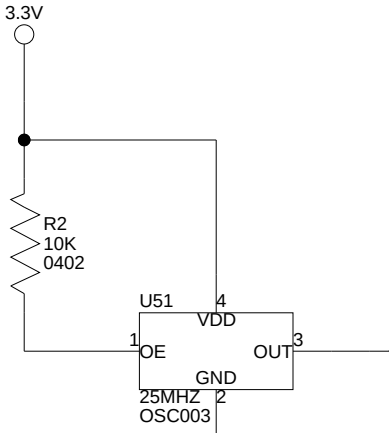
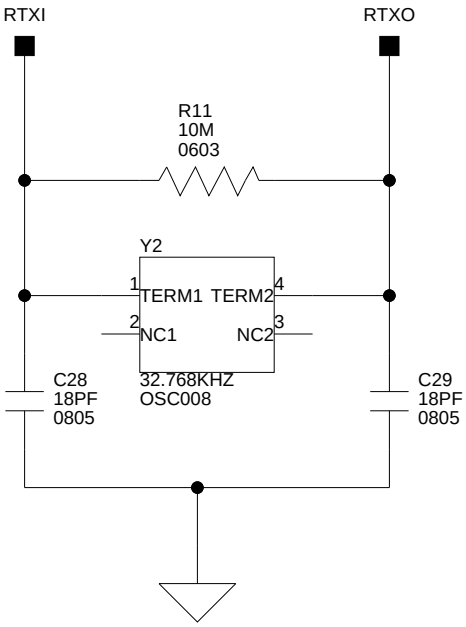
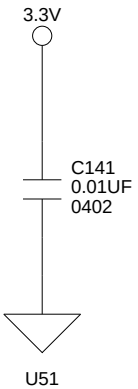
V4
BMODE1
RTXO
A10
RTXO
NMI
B13
NMI
FCE
H18
FCE
RESET
B14
RESET
FRESET
Y14
R75
33
0402


3.3V
R2
10K
0402
U51
4
VDD
1
OE
OUT
3
GND
25MHZ
2
OSC003


RTXI
RTXO
R11
10M
0603
Y2
1
TERM1
TERM2
4
2
NC1
NC2
3
C28
18PF
0805
32.768KHZ
OSC008
C29
18PF
0805


3.3V
C141
0.01UF
0402
U51

RTC

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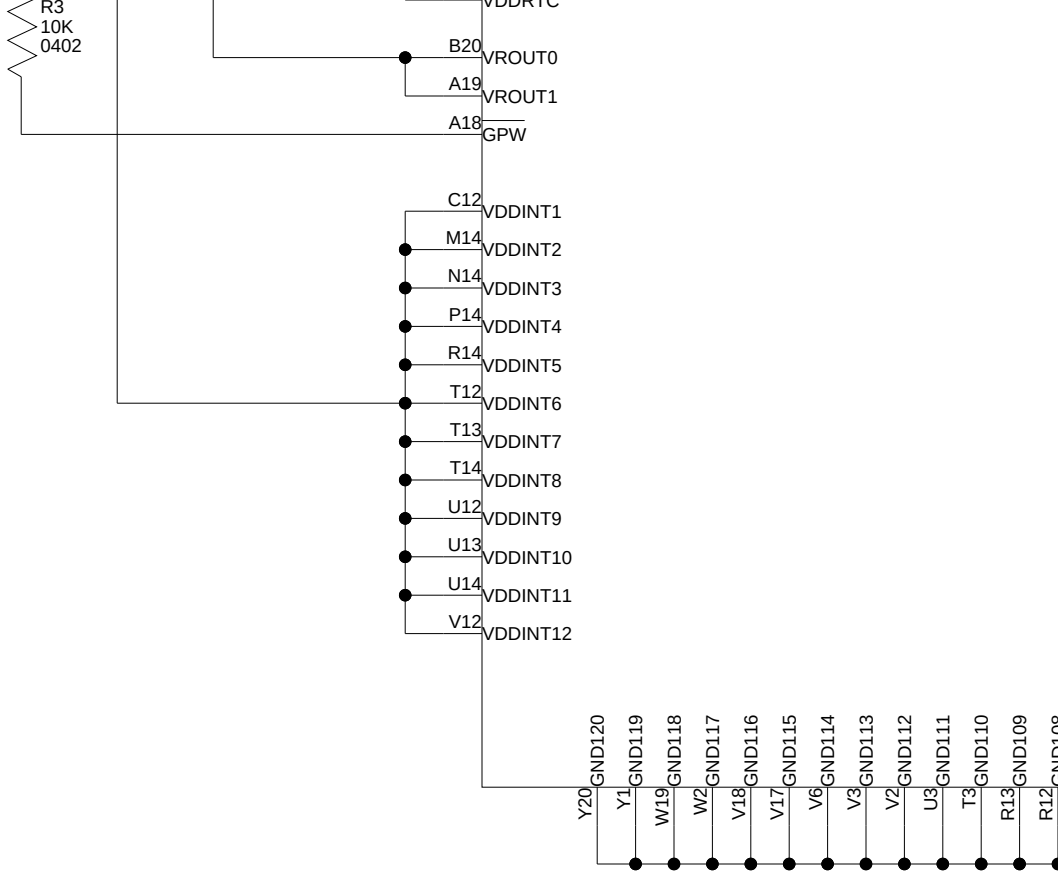
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10K
0402
VDDRTC
B20
VROUT0
A19
VROUT1
A18
GPW
C12
VDDINT1
M14
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N14
VDDINT3
P14
VDDINT4
R14
VDDINT5
T12
VDDINT6
T13
VDDINT7
T14
VDDINT8
U12
VDDINT9
U13
VDDINT10
U14
VDDINT11
V12
VDDINT12
Y20
GND120
Y1
GND119
W19
GND118
W2
GND117
V18
GND116
V17
GND115
V6
GND114
V3
GND113
V2
GND112
U3
GND111
T3
GND110
R13
GND109
R12

3

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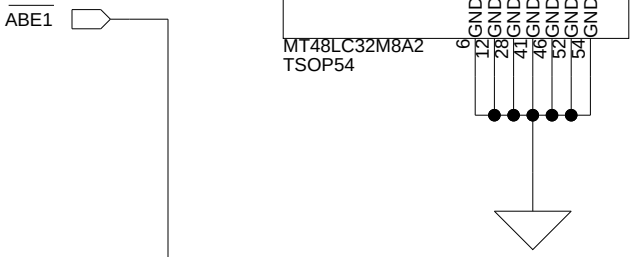
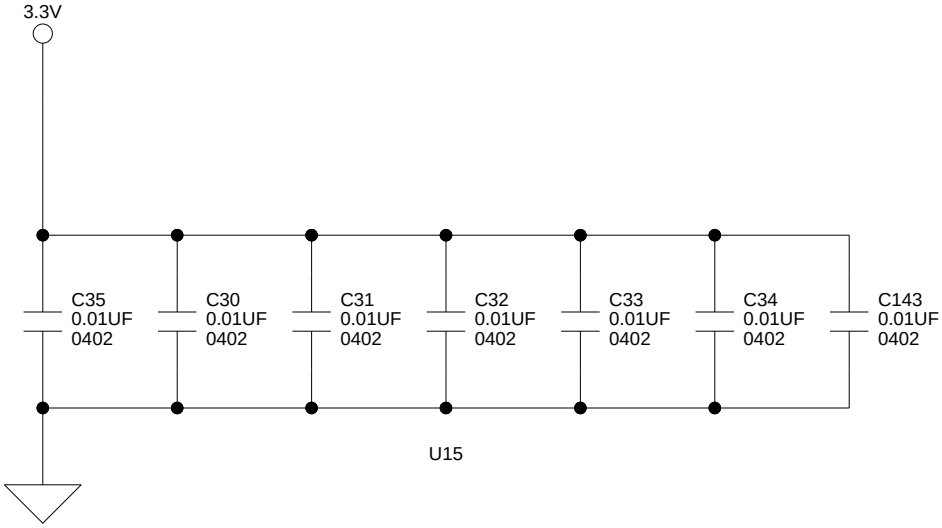
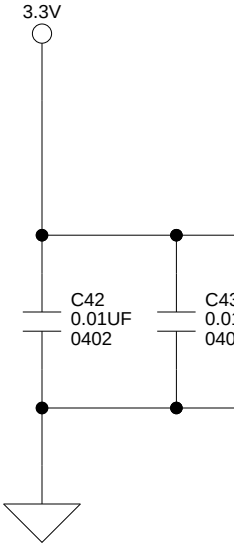


64 MB SDRAM
(8M x 8 x 4 banks) x 2 chips





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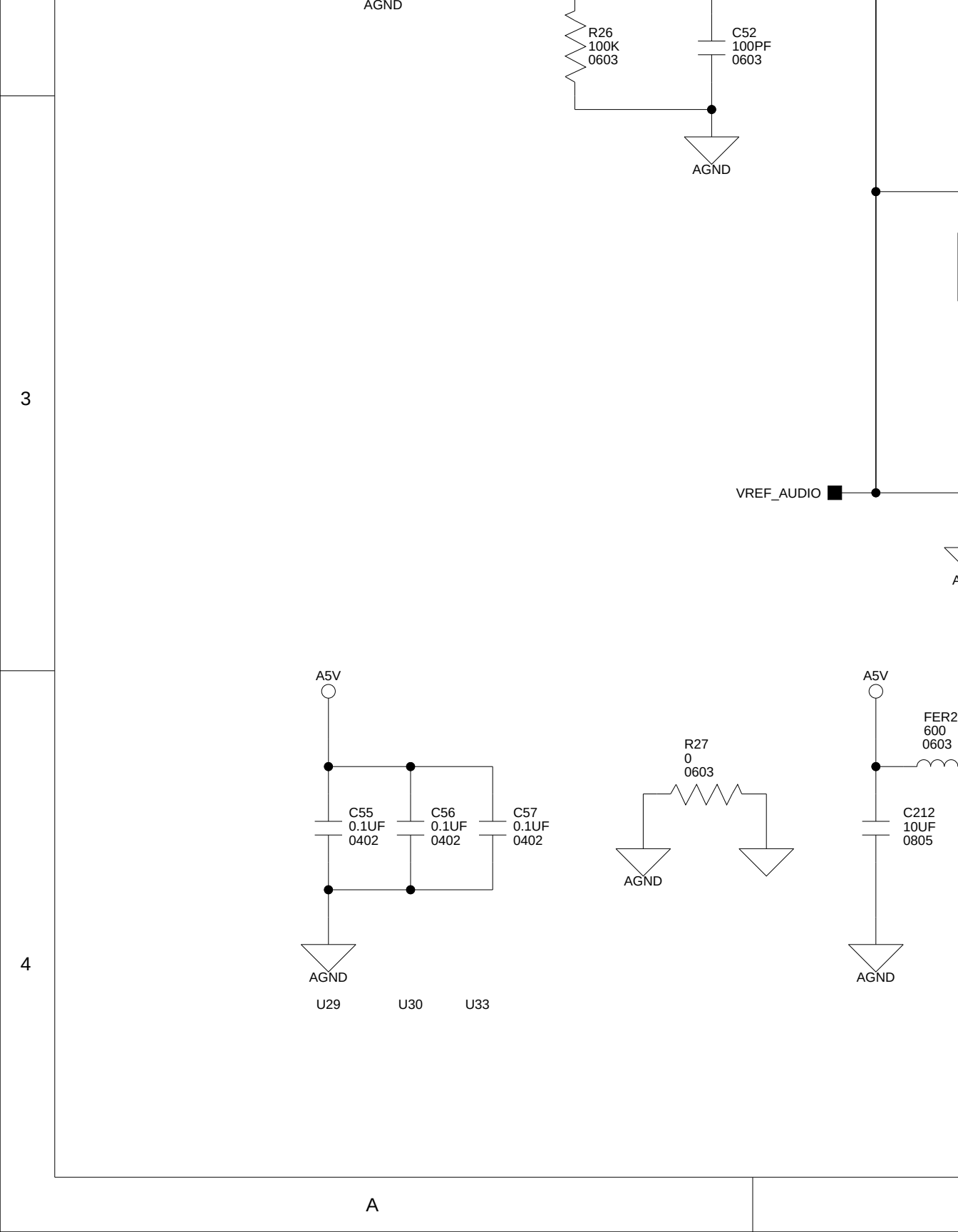
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100K
0603
C52
100PF
0603
AGND
VREF_AUDIO
A5V
C55
0.1UF
0402
C56
0.1UF
0402
C57
0.1UF
0402
AGND
U29
U30
U33
R27
0
0603
AGND
A5V
FER2
600
0603
C212
10UF
0805
AGND
3
4
A


R37
10K
0603
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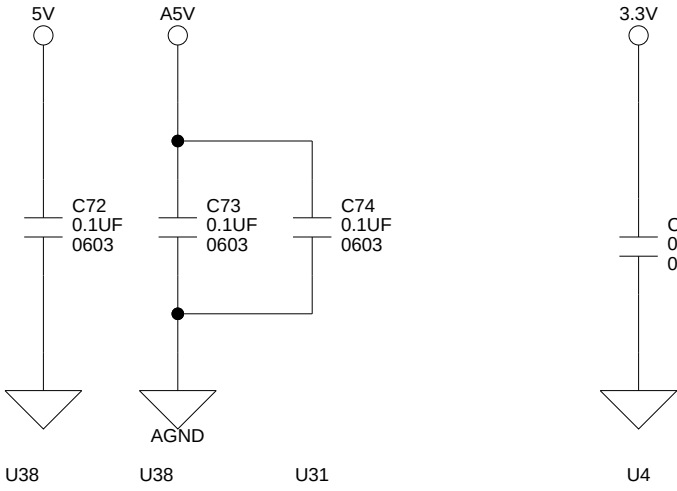
DEEMP
23
MUTE
21
IDPM0
20
IDPM1
AD185
SSOP2


5V
A5V
3.3V
C72
0.1UF
0603
C73
0.1UF
0603
C74
0.1UF
0603
AGND
U38
U38
U31
U4

3

4

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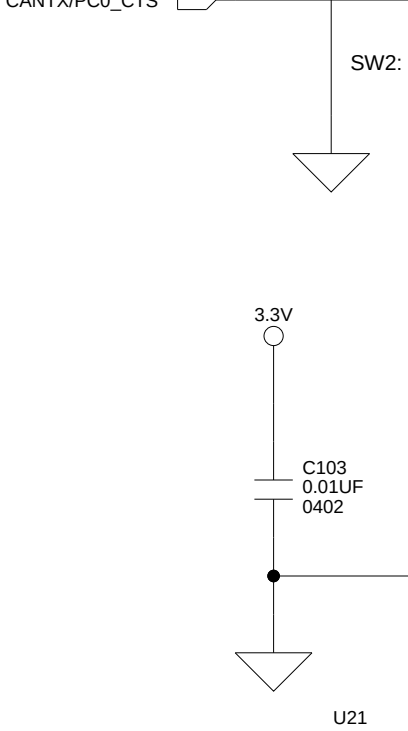

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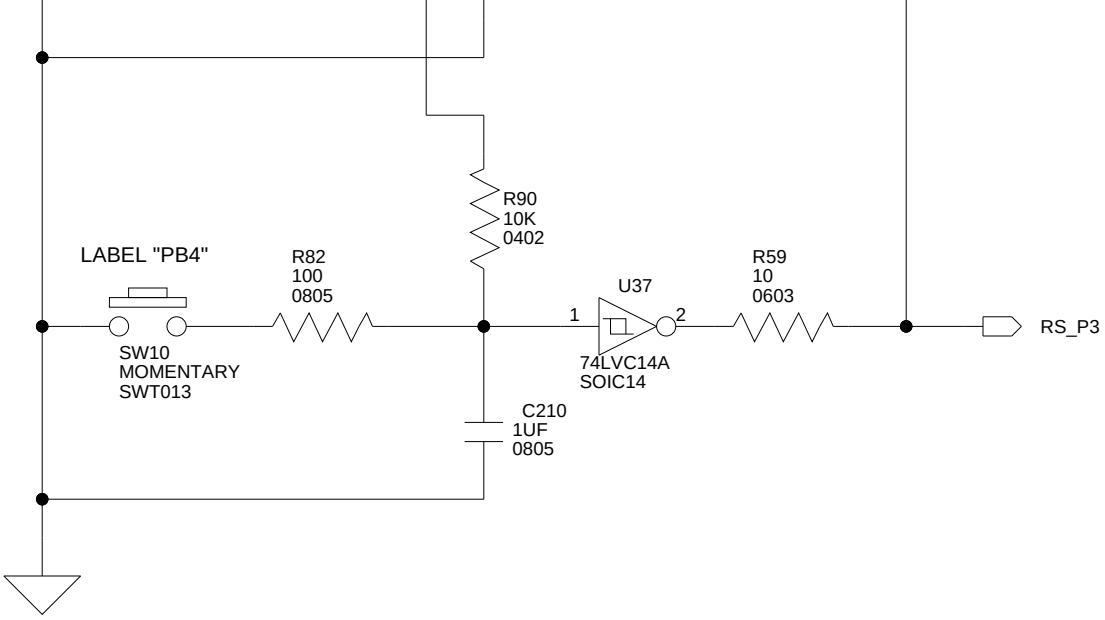

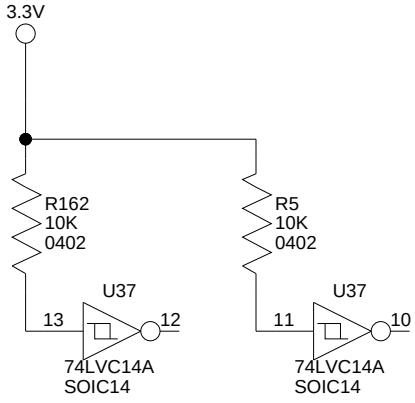

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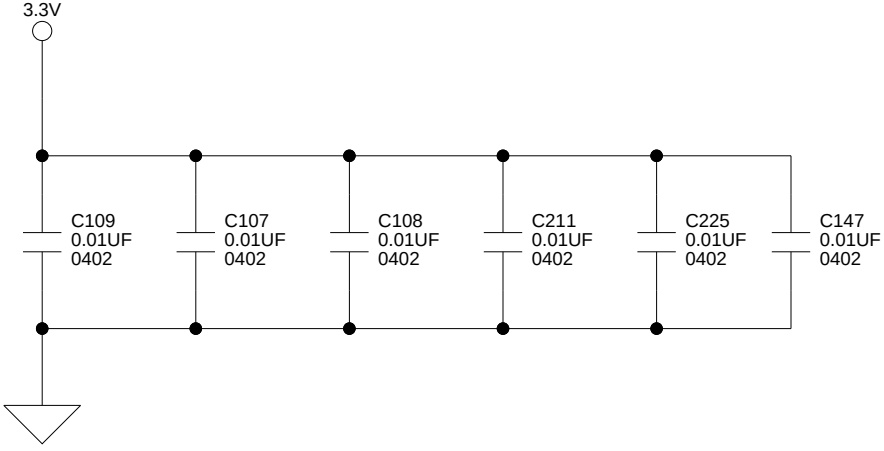

U37 U27 U36 U54 U55 U50

3

4

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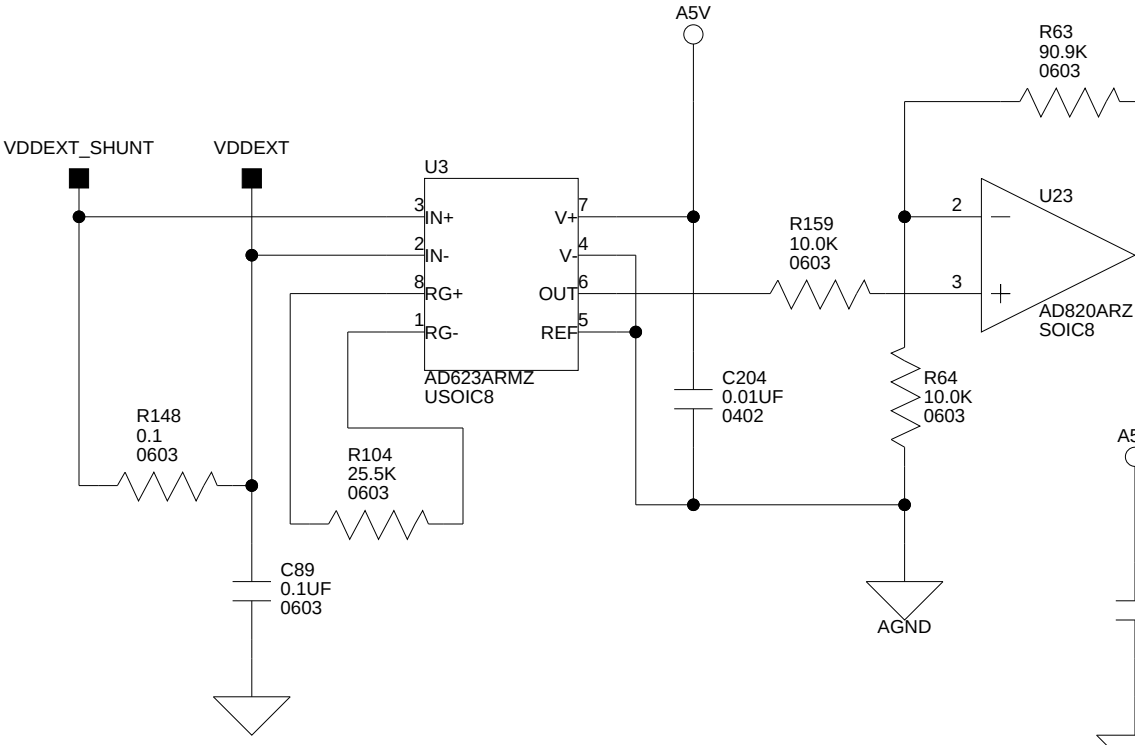
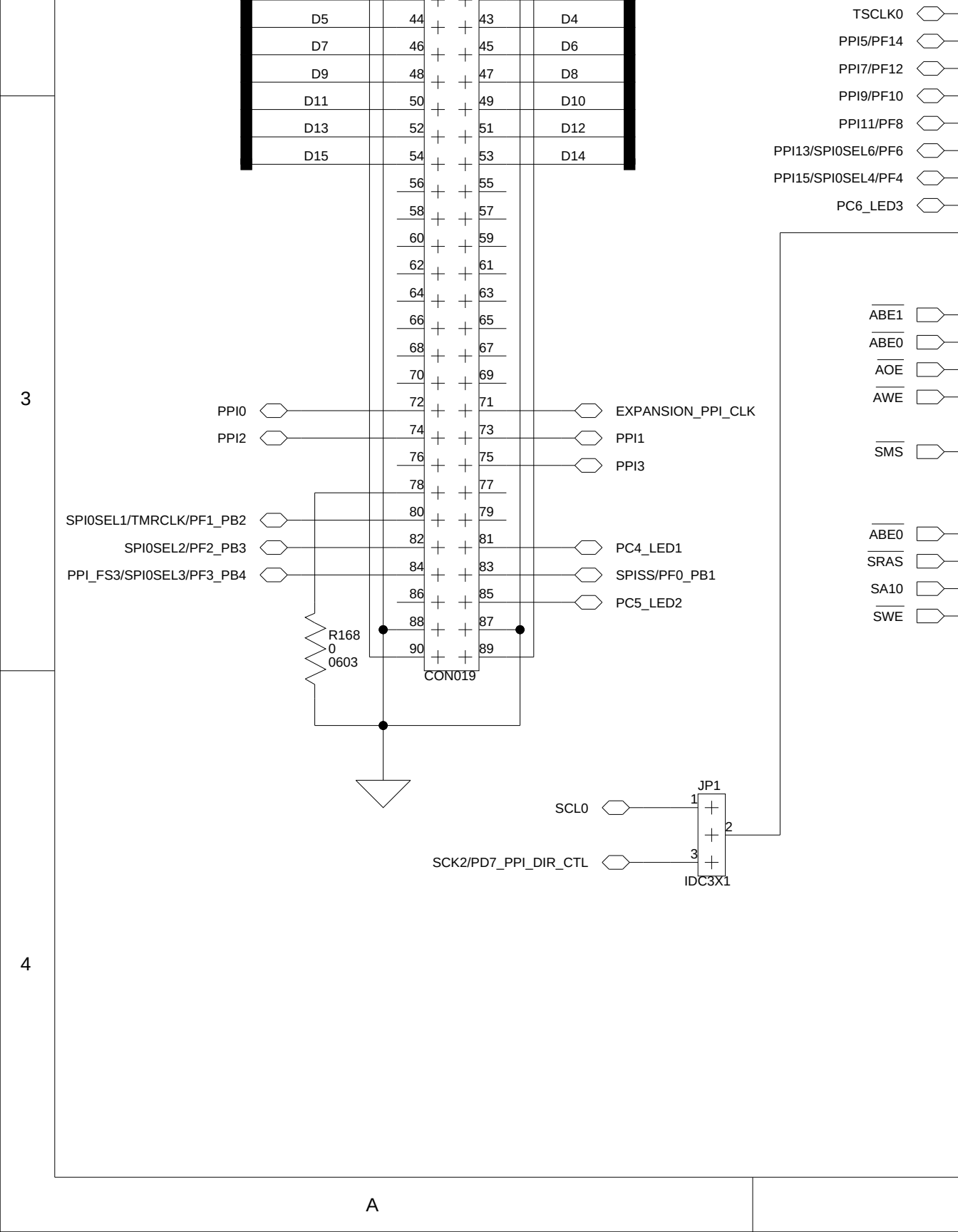


DSP IO CURRENT


D5
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D4
D7
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D6
D9
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47
D8
D11
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49
D10
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D12
D15
54
53
D14
56
55
58
57
60
59
62
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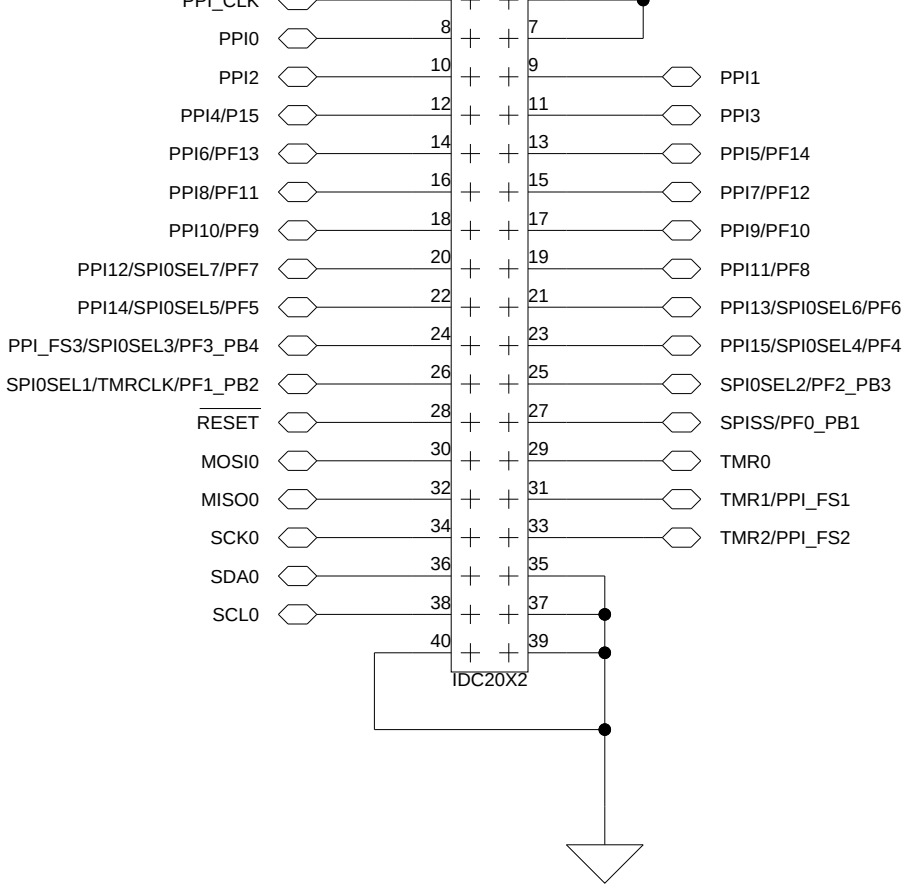
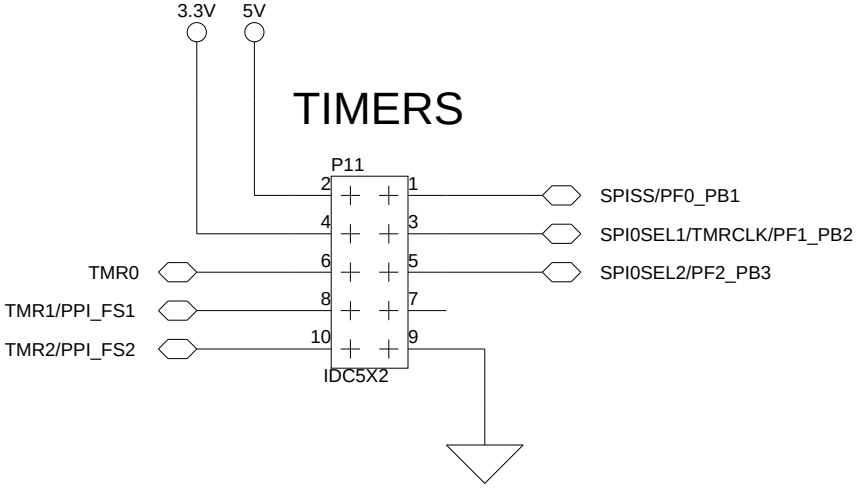
64
63
66
65
68
67
70
69
72
71
74
73
76
75
78
77
80
79
82
81
84
83
86
85
88
87
90
89
CON019
TSCLK0
PPI5/PF14
PPI7/PF12
PPI9/PF10
PPI11/PF8
PPI13/SPI0SEL6/PF6
PPI15/SPI0SEL4/PF4
PC6_LED3
ABE1
ABE0
AOE
AWE
SMS
ABE0
SRAS
SA10
SWE
PPI0
PPI2
EXPANSION_PPI_CLK
PPI1
PPI3
SPI0SEL1/TMRCLK/PF1_PB2
SPI0SEL2/PF2_PB3
PPI_FS3/SPI0SEL3/PF3_PB4
PC4_LED1
SPISS/PF0_PB1
PC5_LED2
R168
0
0603
JP1
SCL0
SCK2/PD7_PPI_DIR_CTL
1
2
3
IDC3X1
3
4
A

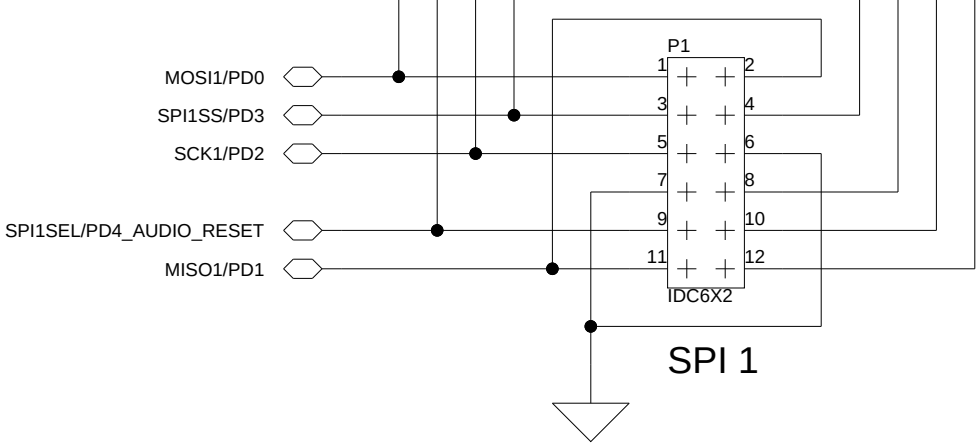

PPI_CLK
PPI0
PPI2
PPI4/P15
PPI6/PF13
PPI8/PF11
PPI10/PF9
PPI12/SPI0SEL7/PF7
PPI14/SPI0SEL5/PF5
PPI_FS3/SPI0SEL3/PF3_PB4
SPI0SEL1/TMRCLK/PF1_PB2
RESET
MOSI0
MISO0
SCK0
SDA0
SCL0
8
7
10
9
12
11
14
13
16
15
18
17
20
19
22
21
24
23
26
25
28
27
30
29
32
31
34
33
36
35
38
37
40
39
IDC20X2
PPI1
PPI3
PPI5/PF14
PPI7/PF12
PPI9/PF10
PPI11/PF8
PPI13/SPI0SEL6/PF6
PPI15/SPI0SEL4/PF4
SPI0SEL2/PF2_PB3
SPISS/PF0_PB1
TMR0
TMR1/PPI_FS1
TMR2/PPI_FS2


3.3V
5V
TIMERS
P11
2
1
4
3
6
5
8
7
10
9
IDC5X2
SPISS/PF0_PB1
SPI0SEL1/TMRCLK/PF1_PB2
SPI0SEL2/PF2_PB3
TMR0
TMR1/PPI_FS1
TMR2/PPI_FS2

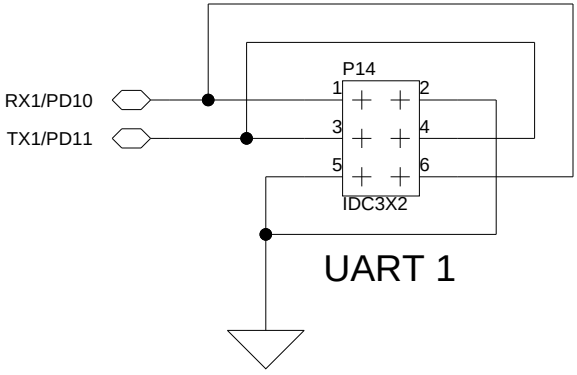
3

4

A



SPI 1

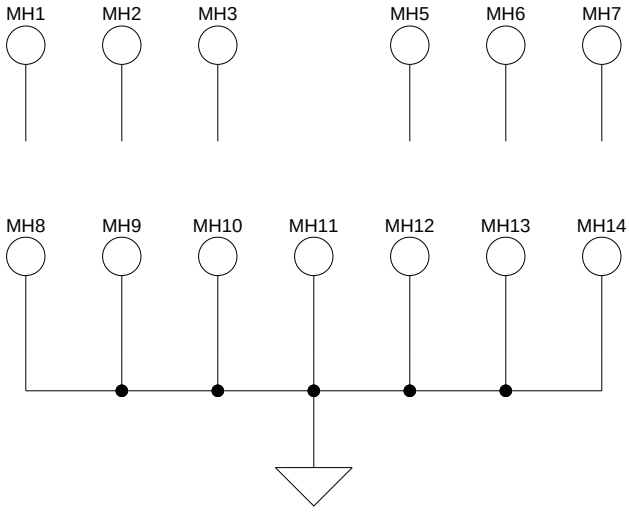


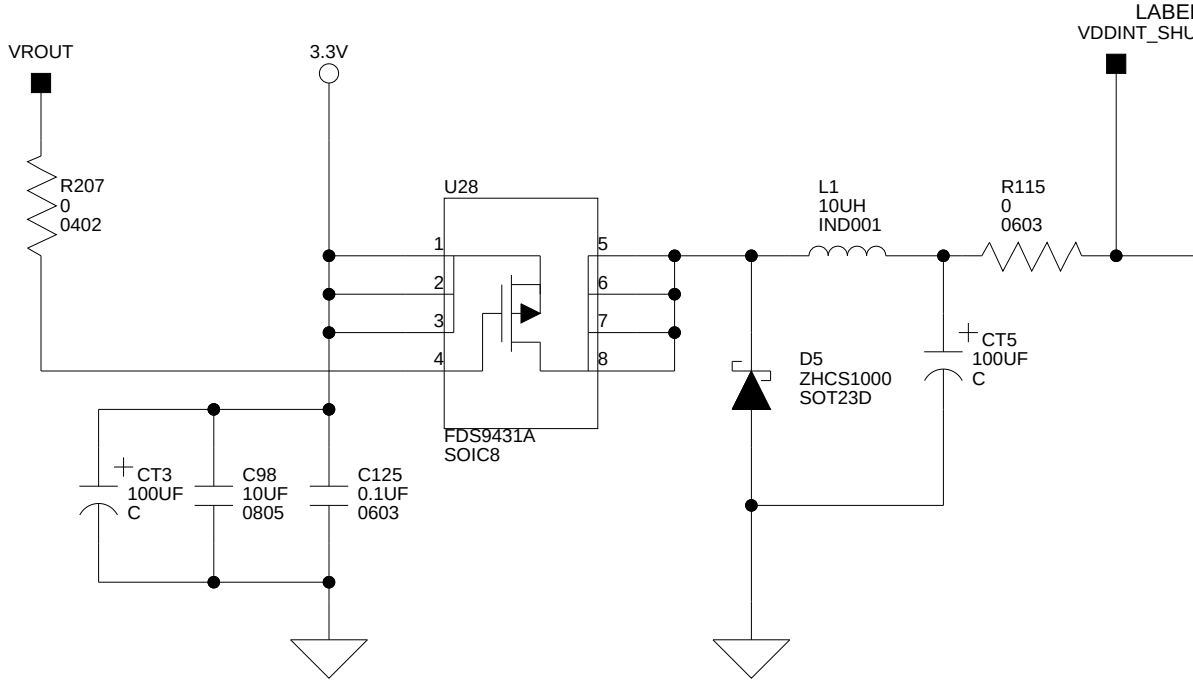
UART 1

3

4

A


MH1
MH2
MH3
MH5
MH6
MH7
MH8
MH9
MH10
MH11
MH12
MH13
MH14


VROUT
3.3V
LABE
VDDINT_SHU
R207
0
0402
U28
1
2
3
4
5
6
7
8
FDS9431A
SOIC8
L1
10UH
IND001
R115
0
0603
D5
ZHCS1000
SOT23D
CT5
100UF
C
CT3
100UF
C
C98
10UF
0805
C125
0.1UF
0603

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