ADSP-BF548 EZ-KIT Lite®
Evaluation System Manual

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Analog Devices, Inc.
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ANALOG DEVICES

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Regulatory Compliance

The ADSP-BF548 EZ-KIT Lite is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADSP-BF548 EZ-KIT Lite has been certified to comply with the essential requirements of the European EMC directive 2004/108/EC and therefore carries the "CE" mark.

The ADSP-BF548 EZ-KIT Lite has been appended to Analog Devices, Inc. EMC Technical File (EMC TF) referenced DSPTOOLS1, issue 2 dated June 4, 2008 and was declared CE compliant by an appointed Notified Body (No.0673) as listed below.

Notified Body Statement of Compliance: NB600ANA2.ABS dated June 4, 2008.

Issued by:

Technology International (Europe) Limited
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Shrivenham, Swindon, SN6 8TY, UK

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

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PREFACE

Thank you for purchasing the ADSP-BF548 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for Blackfin® processors.

Blackfin processors embody a type of embedded processor designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications. They deliver breakthrough signal-processing performance and power efficiency within a reduced instruction set computing (RISC) programming model.

Blackfin processors support a media instruction set computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics. Blackfin processors deliver signal-processing performance in a microprocessor-like environment.

Based on the Micro Signal Architecture (MSA), Blackfin processors combine a 32-bit RISC instruction set, dual 16-bit multiply accumulate (MAC) DSP functionality, and eight-bit video processing performance that had previously been the exclusive domain of very-long instruction word (VLIW) media processors.

The evaluation board is designed to be used in conjunction with the CrossCore® Embedded Studio (CCES) and VisualDSP++® development environments to test the ADSP-BF548 processor capabilities. The development environment facilitates advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-BF548 assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-BF548 processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-BF548 processor and the evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to http://www.analog.com/dsp/tools.

The ADSP-BF548 EZ-KIT Lite provides example programs to demonstrate the evaluation board capabilities.

Product Overview

The board features:

- Analog Devices ADSP-BF548 Blackfin processor
    - Core performance up to 600 MHz
    - External bus performance up to 133 MHz
    - 400-pin mini-BGA package
    - 25 MHz crystal
- Double data rate (DDR) synchronous dynamic random access memory (SDRAM)
    - Micron MT46V32M16 – 64 MB (8M x 16-bits x 4 banks)
- Burst flash memory
    - Intel PC28F128P33T85A – 16 MB (8M x 16-bits)
- NAND flash memory
    - ST Micro NAND02 – 2 Gb
- SPI flash memory
    - ST Micro M25P16 – 16 Mb
- Advanced technology attachment packet interface (ATAPI)
    - 80 GB HDD
- TFT LCD display with touchscreen
    - Sharp LQ043T1DG01 – 480 x 272, 4.3” touchscreen LCD
    - Analog Devices AD7877 – touchscreen controller

- Analog audio interface
    - Analog Devices AD1980 SoundMAX codec
    - 6 DAC channels for 5.1 surround
    - 1 input stereo MIC jack
    - 1 input stereo LINE IN jack
    - 1 output stereo LINE OUT/HEAD PHONE OUT jack
    - 1 output stereo SURROUND jack
    - 1 output center and LFE jack
- Ethernet interface
    - SMSC LAN9218 device
    - 10-BaseT and 100-BaseTX Ethernet controller
    - Integrated PHY and MAC
    - HP Auto-MDIX
- Keypad
    - ACT components – 4 x 4 keypad assembly
- Thumbwheel
    - CTS Corp rotary encoder
- Universal asynchronous receiver/transmitter (UART)
    - ADM3202 RS-232 line driver/receiver
    - DB9 female connector

- LEDs
    - 10 LEDs: 1 power (green), 1 board reset (red), 1 USB (red), 6 general-purpose (amber), and 1 USB monitor (amber)
- Push buttons
    - 5 push buttons: 1 reset, 4 programmable flags with debounce logic
- Expansion interface: all ADSP-BF548 processor signals
- Other features
    - JTAG ICE 14-pin header
    - USB OTG connector
    - `HOST` interface connector
    - Blackfin power measurement jumpers
    - `PPI1` IDC connector
    - `SPORT2` and `SPORT3` IDC connectors
    - TWI, SPI, timers, `UART3` IDC connectors

For information about the hardware components of the EZ-KIT Lite, refer to Chapter 2, "ADSP-BF548 EZ-KIT Lite Hardware Reference".

Purpose of This Manual

The *ADSP-BF548 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF548 EZ-KIT

Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

VisualDSP++ users should use this manual in conjunction with the *Getting Started with ADSP-BF548 EZ-KIT Lite*, which familiarizes users with the hardware capabilities of the evaluation system and demonstrates how to access these capabilities in the VisualDSP++ environment.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set.

Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts that describe your target architecture. For the locations of these documents, see "Related Documents".

Programmers who are unfamiliar with CCES or VisualDSP++ should refer to the online help and user's manuals.

Manual Contents

The manual consists of:

- Chapter 1, "Using the ADSP-BF548 EZ-KIT Lite" on page 1-1
  Describes EZ-KIT Lite functionality from a programmer's perspective and provides an easy-to-access memory map.
- Chapter 2, "ADSP-BF548 EZ-KIT Lite Hardware Reference" on page 2-1
  Provides information on the EZ-KIT Lite hardware components.

- Appendix A, "ADSP-BF548 EZ-KIT Lite Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, "ADSP-BF548 EZ-KIT Lite Schematic" on page B-1
  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design. Appendix B is part of the online help.

What's New in This Manual

This is revision 1.4 of the *ADSP-BF548 EZ-KIT Lite Evaluation System Manual*. The manual has been updated to include CCES information. In addition, modifications and corrections based on errata reports against the previous manual revision have been made.

For the latest version of this manual, please refer to the Analog Devices Web site.

Technical Support

You can reach Analog Devices processors and DSP technical support in the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:
  http://ez.analog.com/community/dsp
- Submit your questions to technical support directly at:
  http://www.analog.com/support

- E-mail your questions about processors, DSPs, and tools development software from **CrossCore Embedded Studio** or **VisualDSP++**:

  Choose **Help > Email Support**. This creates an e-mail to `processor.tools.support@analog.com` and automatically attaches your **CrossCore Embedded Studio** or **VisualDSP++** version information and `license.dat` file.

- E-mail your questions about processors and processor applications to:
  `processor.support@analog.com` or
  `processor.china@analog.com` (Greater China support)

- In the **USA only**, call **1-800-ANALOGD** (1-800-262-5643)

- Contact your Analog Devices sales office or authorized distributor. Locate one at:
  `www.analog.com/adi-sales`

- Send questions by mail to:
  Processors and DSP Technical Support
  Analog Devices, Inc.
  Three Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

This evaluation system supports Analog Devices ADSP-BF548 Blackfin embedded processors.

Product Information

Product information can be obtained from the Analog Devices Web site and the online help system.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, myAnalog is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. myAnalog provides access to books, application notes, data sheets, code examples, and more.

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EngineerZone

EngineerZone is a technical support forum from Analog Devices. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

Related Documents

For additional information about the product, refer to the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-BF542/BF544/BF547/BF548/BF549 Blackfin Embedded Processor Data Sheet	General functional description, pinout, and timing of the processor
ADSP-BF54x Blackfin Processor Hardware Reference	Description of the internal processor architecture and all register functions
Blackfin Processor Programming Reference	Description of all allowed processor assembly instructions

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the development environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

Notation Conventions

1 USING THE ADSP-BF548 EZ-KIT LITE

This chapter provides specific information to assist you with development of programs for the ADSP-BF548 EZ-KIT Lite evaluation system.

The following topics are covered.

For information about the graphical user interface, including the boot loading, target options, and other facilities of the EZ-KIT Lite system, refer to the online help.

For more detailed information about the ADSP-BF548 Blackfin processor, see documents referred to at "Related Documents".

Package Contents

Your ADSP-BF548 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-BF548 EZ-KIT Lite board
- Universal 7.5V DC power supply
- Secure digital (SD) memory card
- USB high-speed flash drive
- 7-foot Ethernet crossover cable
- 7-foot Ethernet patch cable
- Four 6-foot 3.5 mm male-to-male audio cables
- 3.5 mm headphones
- 10-foot USB A-B male cable for USB Debug Agent
- 5-in-1cable and connectors for USB on-the-go (OTG) applications
- Ethernet loopback connector
- CAN loopback cable

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-BF548 EZ-KIT Lite board is designed to run outside your personal computer as a standalone unit. You do not have to open your computer case.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which can damage some components. Figure 1-1 shows the default jumper settings, switches, connector locations, and LEDs used in installation. Confirm that your board is in the default configuration before using the board.

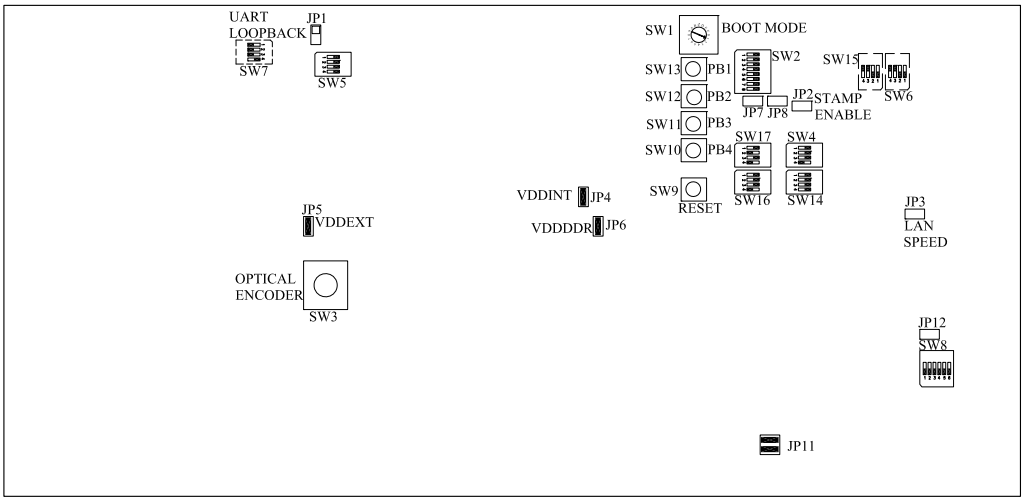


Figure 1-1. EZ-KIT Lite Hardware Setup

CCES Install and Session Startup

For information about CCES and to download the software, go to www.analog.com/CCES. A link for the ADSP-BF548 EZ-KIT Lite Board Support Package (BSP) for CCES can be found at http://www.analog.com/Blackfin/EZKits.

Follow these instructions to ensure correct operation of the product software and hardware.

Step 1: Connect the EZ-KIT Lite board to a personal computer (PC) running CCES using one of two options: an Analog Devices emulator or via the debug agent.

Using an Emulator:

1. Plug one side of the USB cable into the USB connector of the emulator. Plug the other side into a USB port of the PC running CCES.
2. Attach the emulator to the header connector ZP4 (labeled JTAG) on the EZ-KIT Lite board.

Using the on-board Debug Agent:

1. Plug one side of the USB cable into the USB connector of the debug agent ZJ1 (labeled USB).
2. Plug the other side of the cable into a USB port of the PC running CCES.

Step 2: Attach the provided cord and appropriate plug to the 7.5V power adaptor.

1. Plug the jack-end of the power adaptor into the power connector J7 (labeled 7.5V) on the EZ-KIT Lite board.
2. Plug the other side of the power adaptor into a power outlet. The power LED (labeled LED7) is lit green when power is applied to the board.
3. Power the emulator (if used). Plug the jack-end of the assembled power adaptor into the emulator and plug the other side of the power adaptor into a power outlet. The enable/power is lit green when power is applied.

Step 3 (if connected through the debug agent): Verify that the yellow USB monitor LED (labeled ZLED3) is on. This signifies that the board is communicating properly with the host PC and ready to run CCES.

Session Startup

It is assumed that the CrossCore Embedded Studio software is installed and running on your PC.

Note: If you connect the board or emulator first (before installing CCES) to the PC, the Windows driver wizard may not find the board drivers.

1. Navigate to the CCES environment via the **Start** menu.

   Note that CCES is not connected to the target board.

2. Use the system configuration utility to connect to the EZ-KIT Lite board.

   If a debug configuration exists already, select the appropriate configuration and click **Apply and Debug** or **Debug**. Go to step 8.

   To create a debug configuration, do one of the following:

   - Click the down arrow next to the little bug icon, select **Debug Configurations**
   - Choose **Run > Debug Configurations**.

   The **Debug Configuration** dialog box appears.

3. Select **CrossCore Embedded Studio Application** and click  (**New launch configuration**).

   The **Select Processor** page of the **Session Wizard** appears.

4. Ensure **Blackfin** is selected in **Processor family**. In **Processor type**, select **ADSP-BF548**. Click **Next**.

   The **Select Connection Type** page of the **Session Wizard** appears.

5. Select one of the following:

   - For standalone debug agent connections, **EZ-KIT Lite** and click **Next**.
   - For emulator connections, **Emulator** and click **Next**.

   The **Select Platform** page of the **Session Wizard** appears.

6. Do one of the following:
    - For standalone debug agent connections, ensure that the selected platform is **ADSP-BF548 EZ-KIT** Lite via Debug Agent.
    - For emulator connections, choose the type of emulator that is connected to the board.
7. Click **Finish** to close the wizard.

   The new debug configuration is created and added to the program(s) to load list.
8. In the **Program(s) to load** section, choose the program to load when connecting to the board. If not loading any program upon connection to the target, do not make any changes.

   Note that while connected to the target, there is no way to choose a program to download. To load a program once connected, terminate the session.

To delete a configuration, go to the **Debug Configurations** dialog box and select the configuration to delete. Click and choose **Yes** when asked if you wish to delete the selected launch configuration. Then **Close** the dialog box.

To disconnect from the target board, click the terminate button (red box) or choose **Run > Terminate**.

To delete a session, choose **Target > Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

VisualDSP++ Install and Session Startup

For information about VisualDSP++ and to download the software, go to www.analog.com/VisualDSP.

There are two USB interfaces on the ADSP-BF548 EZ-KIT Lite. Be sure to use the debugger's interface (labelled ZJ1, USB Debug Agent) when connecting your computer to the board with provided USB cable. The other USB interface (labelled USB-OTG) is for applications use.

1. Verify that the yellow USB monitor LED (ZLED3, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the **Start > Programs** menu. The main window appears. Note that VisualDSP++ does not connect to any session. Skip the rest of this step to step 3.

   If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and force VisualDSP++ to start a new session by pressing and holding down the **Ctrl** key while starting VisualDSP++. Do not release the **Ctrl** key until the **Session Wizard** appears on the screen. Go to step 4.
3. To connect to a new EZ-KIT Lite session, start **Session Wizard** by selecting one of the following.
   - From the **Session** menu, **New Session**.
   - From the **Session** menu, **Session List**. Then click **New Session** from the **Session List** dialog box.
   - From the **Session** menu, **Connect to Target**.

4. The **Select Processor** page of the wizard appears on the screen. Ensure **Blackfin** is selected in **Processor family**. In **Choose a target processor**, select **ADSP-BF548**. Click **Next**.

5. The **Select Connection Type** page of the wizard appears on the screen. Select **EZ-KIT Lite** and click **Next**.

6. The **Select Platform** page of the wizard appears on the screen. Ensure that the selected platform is **ADSP-BF548 EZ-KIT Lite via Debug Agent**. Specify your own **Session name** for your session or accept the default name.

   The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and to open a new session.

   Click **Next**.

7. The **Finish** page of the wizard appears on the screen. The page displays your selections. Check the selections. If you are not satisfied, click **Back** to make changes; otherwise, click **Finish**. VisualDSP++ creates the new session and connects to the EZ-KIT Lite. Once connected, the main window's title is changed to include the session name set in step 6.

To disconnect from a session, click the disconnect button  or select **Session > Disconnect from Target**.

To delete a session, select **Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

CCES Evaluation License

The ADSP-BF548 EZ-KIT Lite software is part of the Board Support Package (BSP) for the Blackfin ADSP-BF54x family. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for 90 days after activation. Once the evaluation period ends, the evaluation license becomes permanently disabled. If the evaluation license is installed but not activated, it allows 10 days of unrestricted use and then becomes disabled. The license can be re-enabled by activation.

An evaluation license can be upgraded to a full license. Licenses can be purchased from:

- Analog Devices directly. Call (800) 262-5645 or 781-937-2384 or go to:
  http://www.analog.com/buyonline.
- Analog Devices, Inc. local sales office or authorized distributor. To locate one, go to:
  http://www.analog.com/salesdir/continent.asp.

The EZ-KIT Lite hardware must be connected and powered up to use CCES with a valid evaluation or full license.

VisualDSP++ Evaluation License

The ADSP-BF548 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ restricts a connection to the ADSP-BF548 EZ-KIT Lite via the USB debug agent interface only. Connections to simulators and emulation products are no longer allowed.

- The linker restricts a user's program to 60 KB of memory for code space with no restrictions for data space.

To avoid errors when opening VisualDSP++, the EZ-KIT Lite hardware must be connected and powered up. This is true for using VisualDSP++ with a valid evaluation or full license.

Lockbox Key Security Features

Blackfin processors feature Lockbox® secure technology: hardware-enabled code security and content protection for one-time programmable (OTP) memory. Customers purchasing Blackfin processors can program their own customer public key in OTP.

The ADSP-BF548 EZ-KIT Lites are evaluation boards with the Lockbox key pre-programmed and publicly documented—the burden of key generation and OTP programming of public keys is removed from the customer. Customers can still program other areas of OTP memory on the ADSP-BF548 EZ-KIT Lite. Analog Devices publicly document the EZ-KIT Lite's public and private key pair for customer evaluation and support of the Lockbox feature, all while avoiding any keys information exchange. As a result, there is no confidentiality associated with the Lockbox key on EZ-KIT Lites.

To demonstrate Lockbox features using an EZ-KIT Lite, you must use the keys that are provided pre-programmed on your EZ-KIT Lite.

Use the EZ-KIT Lite key pair to generate a demo and then provide the keys to the demo users. Note that the EZ-KIT Lite cannot be used to secure any confidential information. If you wish to create a demo with confidential keys, you must build your own Blackfin board and personalize it with your own keys.

Memory Map

The ADSP-BF548 processor has internal static random access memory (SRAM), used for instruction or data storage; see Table 1-1. The internal memory details can be found in the *ADSP-BF54x Blackfin Processor Hardware Reference*.

The ADSP-BF548 EZ-KIT Lite board includes five types of external memory: double data rate (DDR), serial peripheral interconnect (SPI), burst flash, NAND, and secure digital (SD); see Table 1-2. For more information about a specific memory type, refer to the respective section in this chapter.

Table 1-1. EZ-KIT Lite Internal Memory Map

Start Address	Content
0xEF00 0000	BOOT ROM (4K BYTE)
0xEF00 1000	Reserved
0xFEB0 0000	L2 SRAM (128K BYTE)
0xFEB2 0000 0xFF40 0000 0xFF40 4000 0xFF40 8000 0xFF50 0000 0xFF50 4000 0xFF50 8000 0xFF60 0000 0xFF60 4000 0xFF60 8000 0xFF60 C000 0xFF61 0000 0xFF61 4000 0xFF70 0000 0xFF70 1000	Reserved
0xFF80 0000	L1 DATA BANKA SRAM (16K BYTE)
0xFF80 4000	L1 DATA BANKA SRAM/CACHE (16K BYTE)

Table 1-1. EZ-KIT Lite Internal Memory Map (Cont'd)

Start Address	Content
0xFF80 8000	Reserved
0xFF90 0000	L1 DATA BANKB SRAM (16K BYTE)
0xFF90 4000	L1 DATA BANKB SRAM/CACHE (16K BYTE)
0xFF90 8000	Reserved
0xFFA0 0000	L1 DATA BANKA LOWER SRAM (16K BYTE)
0xFFA0 4000	L1 DATA BANKA UPPER SRAM (16K BYTE)
0xFFA0 8000	Reserved
0xFFA0 C000	Reserved
0xFFA1 0000	L1 INSTRUCTION SRAM/CACHE (16K BYTE)
0xFFA1 4000 0xFFA1 8000 0xFFA1 C000 0xFFA2 0000	L1 INSTRUCTION BANKB ROM (64K BYTE)
0xFFA2 4000	Reserved
0xFFB0 0000	L1 SCRATCHPAD SRAM (4K BYTE)
0xFFB0 1000	Reserved
0xFFC0 0000	SYSTEM MMR REGISTERS
0xFFE0 0000	CORE MMR REGISTERS

Table 1-2. EZ-KIT Lite External Memory Map

Start Address	End Address	Content
0x0000 0000	0x03FF FFFF	SDRAM bank 0 (SDRAM) See "DDR Interface" on page 1-15.
0x2000 0000	0x20FF FFFF	ASYNC memory bank 0 See "Burst Flash Memory Interface" on page 1-17.
0x2400 0000	0x2400 007F	ASYNC memory bank 1 See "Ethernet Interface" on page 1-24.
0x2800 0000	0x2BFF FFFF	ASYNC memory bank 2

Table 1-2. EZ-KIT Lite External Memory Map (Cont'd)

Start Address	End Address	Content
0x2C00 0000	0x2FFF FFFF	ASYNC memory bank 3
0x3000 0000	0xEEFF FFFF	Reserved

DDR Interface

The ADSP-BF548 processor holds a built-in double data rate (DDR) SDRAM controller, which connects to a Micron MT46V32M16 32M x 16 bits (64 MB) DDR memory chip. The controller connects to the DDR memory bank 0 via the $\overline{\text{DDRCS0}}$ signal of the processor. The DDR memory chip is the only device connected to the processor's DDR interface. The DDR interface can operate at a maximum system clock (SCLK) frequency of 133 MHz.

There is a trade-off between selecting the maximum core clock (CCLK) of the processor and the maximum system clock. Consequently, the respective control registers must be initialized appropriately to get either maximum CCLK or maximum SCLK.

When you are in a CCES or VisualDSP++ session and connected to the EZ-KIT Lite board via the USB debug agent, the DDR registers are configured automatically with values listed in Table 1-3 each time the processor is being reset. The values are used whenever DDR bank 0 is accessed through the debugger (for example, when viewing memory windows or loading a program).

To disable the automatic setting of the DDR registers, do one of the following:

- CCES users, choose **Target > Settings > Target Options** and clear the **Use XML reset values** check box.
- VisualDSP++ users, choose **Settings > Target Options** and clear the **Use XML reset values** check box.

For more information on changing the reset values, refer to the online help.

Table 1-4 shows configuration of the PLL registers using a 120 MHz SCLK and a 133 MHz SCLK. The PLL_CTL and PLL_DIV registers need to be initialized in the user code to achieve maximum performance.

Please remember that the DDR control register values in Table 1-3 are for the SCLK set between 83 MHz and 133 MHz.

Table 1-3. DDR Default Settings With an 83 MHz to 133 MHz SCLK

Register	Value	Function
EBIU_DDRCTL0	0x218A8287	Calculated with SCLK = 83 MHz to 133 MHz 16-bit data path External buffering timing disabled tRC = 8 SCLK cycles tRAS = 6 SCLK cycles tRP = 2 SCLK cycles tRFC = 10 SCLK cycles tREFI = 0x0287 clock cycles
EBIU_DDRCTL1	0x20022222	tWTR = 2 SCLK cycles Device size = 512 Mbit Device width = 16 bits Ext. banks = CS0 only Data width = 16 bits tWR = 2 SCLK cycles tMRD = 2 SCLK cycles tRCD = 2 SCLK cycles

Table 1-3. DDR Default Settings With an 83 MHz to 133 MHz SCLK (Cont'd)

Register	Value	Function
EBIU_DDRCTL2	0x00000021	Processor default values
EBIU_AMGCTL	0x0009	Enables the EBIU of the processor to generate a clock out for all memory banks

Table 1-4. PLL Register Settings

Register	SCLK = 133 MHz CCLK = 400 MHz	SCLK = 120 MHz CCLK = 600 MHz
PLL_CTL	0x2000	0x3000
PLL_DIV	0x3	0x5

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the DDR interface. For more information on how to initialize the registers after a reset, search the online help for "reset values".

Burst Flash Memory Interface

The burst flash memory interface of the ADSP-BF548 EZ-KIT Lite holds a 16 MB (16M x 16-bits) Intel PC28F128K3C115 chip. Flash memory connects gluelessly to the processor and is mapped to the processor's external bank 0. This is accomplished by mapping the flash memory's chip enable pin to the $\overline{\text{AMS0}}$ memory select pin of the processor. The address range for flash memory is 0x2000 0000 to 0x20FF FFFF.

Flash memory is pre-loaded with boot code for the blink and power-on-self test (POST) programs. For more information, refer to "Power-On-Self Test" on page 1-33.

By default, the EZ-KIT Lite boots from 16-bit burst flash memory. The processor boots from the burst flash if the boot mode select switch (SW1) is set to a position of 1 (see "Boot Mode Select Switch (SW1)" on page 2-15).

The flash memory code can be modified. For instructions, refer to the online help and example program included in the EZ-KIT Lite installation directory.

NAND Flash Interface

The ADSP-BF548 processor is equipped with an internal NAND flash controller, which allows the 2 Gbit ST Micro NAND02 device to be attached gluelessly to the processor. NAND flash is attached via the processor's specific NAND flash control lines and external eight-bit data bus on the EBIU interface. NAND flash shares the data bus with burst flash memory, Ethernet controller, ATAPI hard drive, and expansion interface. You can write to each of the mentioned peripherals, one peripheral at a time.

Refer to the ST Microelectronics Web site at http://www.st.com for more information.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the NAND flash interface.

SPI Interface

The ADSP-BF548 processor has three serial peripheral interconnect (SPI) ports that share multi-function I/O pins. The processor's SPI port 0 connects directly to serial flash memory, AD7877 touchscreen controller, and expansion interface.

Serial flash memory is a 16 Mb ST Micro M25P16 device, which is selected using the SPIOSEL1 flag pin of the processor. SPI flash memory is pre-loaded with boot code for the blink and POST programs. For more information, refer to "Power-On-Self Test" on page 1-33. By default the EZ-KIT Lite boots from the 16-bit flash burst memory. The SPI flash can be used to boot up the processor by setting the boot mode select switch (SW1) to position 3 (see "Boot Mode Select Switch (SW1)" on page 2-15).

The SPI flash code can be modified. For instructions, refer to the online help and example program included in the EZ-KIT Lite installation directory.

The AD7877 touchscreen controller for the LCD can be selected using the SPIOSEL2 flag pin of the processor. For more information, refer to "Touchscreen Interface" on page 1-22.

SPI ports 0 and 2 of the processor also connect to the expansion interface and can be accessed with an EZ-Extender® board that interfaces with the ADSP-BF548 EZ-KIT Lite. When using SPI port 0, use the processor's SPIOSEL3 flag pin on an EZ-Extender because SPIOSEl1 and SPIOSEL2 are dedicated for the serial flash and touchscreen controller, respectively.

Refer to the ST Microelectronics Web site at http://www.st.com for more information.

SD Interface

The ADSP-BF548 processor has a secure digital (SD) interface. The interface consists of a CLK pin, a command pin, and a four-bit data bus. The SD interface of the processor gluelessly connects to the on-board memory. The SD interface pins are not shared with other peripherals on the board. The memory can be written to in both one-bit and four-bit modes. The EZ-KIT Lite is accompanied with a 256 MB SD memory card plugged into the SD memory card connector (J5). For more information, refer to "SD Memory Card Connector (J5)" on page 2-35.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the SD interface.

EPPI Interface

The ADSP-BF548 processor provides up to three enhanced parallel peripheral interfaces (EPPIs), supporting data widths up to 24 bits. Each EPPI interface is a half-duplex, bi-directional bus consisting of up to 24 bits of data, a dedicated clock, and synchronization signals. The EZ-KIT Lite board utilizes two EPPI ports. One port connects to a TFT LCD module, while the other port connects to the expansion interface and STAMP connector.

The PPI0 interface is configured to output 18-bit or 24-bit data to an LCD module (see "LCD Module Interface" on page 1-21). The PPI0 interface also connects to the expansion interface and can be used with an EZ-Extender board. When using the PPI0 interface with an EZ-Extender board, the PPI0 signals can be disconnected from the LCD module via the SW14 and SW17 switches. Refer to "LCD/PPI Configuration Switch (SW14)" on page 2-21 and "LCD Module Configuration (SW17)" on page 2-23 for more information.

The PPI1 interface connects to the LCD, STAMP connector, and expansion interface. Since the PPI1 signals are connected to multi-function pins, the signals also can be configured for the host port and keypad interfaces. Refer to "Keypad Interface" on page 1-23 for more information.

The PPI1 interface has a dedicated clock, generated either internally or externally and configured independently by software via the PPI1_SEL signal, which connects to PJ13. The clock source is the on-board 27 MHz oscillator or an external source via the expansion interface. The PPI1_SEL signal is configured via the SW14 switch. Refer to "LCD/PPI Configuration Switch (SW14)" on page 2-21 for more information.

LCD Module Interface

The EZ-KIT Lite features a Sharp LQ043T1DG01 TFT LCD module. This is a 4.3” landscape display with a resolution of 480 x 272 and a color depth of 18 or 24 bits.

Table 1-5 lists the register values when the PPI0 interface is configured for the LCD module. The values are obtained from the timing characteristics section of the LQ043T1DG01 data sheet.

Table 1-5. LCD Module Interface Settings

EPPI Register	Name	Data Sheet Symbol	Value
EPPI0_LINE	Samples per line	TH	525
EPPI0_FRAME	Lines per frame	TV	286
EPPI0_FS1W_HBL	Frame sync 1 width	THp	41
EPPI0_FS1P_AVPL	Frame sync 1 period	TH	525
EPPI0_HDELAY	Horizontal delay	THp + THf	43 (41 + 2)
EPPI0_HCOUNT	Horizontal transfer count	THd	480
EPPI0_FS2W_LVB	Frame sync 2 width	TH x TVp	5250 (525 x 10)
EPPI0_FS2P_LAVF	Frame sync 2 period	H x TV	150150 (525 x 286)
EPPI0_VDELAY	Vertical delay	TVp + TVf	12 (10 + 2)
EPPI0_VCOUNT	Vertical transfer count	TVd	272
EPPI0_CLKDIV	Clock divide register	N/A	0x07
EPPI0_CONTROL (18 bit)	Control	N/A	0x12EE2F
EPPI0_CONTROL (24 bit)	Control	N/A	0x136E2F

The LCD module connects to the EPPI0 port. The LCD interface can be configured to run in either 18-bit or 24-bit mode:

- In 24-bit mode, 16M colors are possible, and the PPI data is mapped as eight bits each of red, green, and blue. The D5-D0 signals of EPPI1 are not available because the signals share pins with D18-23 of EPPI0.
- In 18-bit mode, 256K colors are possible, and the PPI data is mapped as six bits each of red, green, and blue. Since the LCD is a 24-bit display, the lower two least significant bits of red, green, and blue are tied low.

Refer to "LCD Module Configuration (SW17)" on page 2-23 for information on how to configure the board for 18-bit or 24-bit mode.

The LCD module can be disconnected from PPI0 by disabling signals on SW14 and SW17. Refer to "LCD/PPI Configuration Switch (SW14)" on page 2-21 and "LCD Module Configuration (SW17)" on page 2-23 for more information.

The DISP signal is generated internally by software via PE3.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the LCD module.

Touchscreen Interface

The AD7877 touchscreen controller connects to the SPI0 interface. The controller provides the X and Y positions, as well as a measurement for the pressure applied to the touchscreen. The touchscreen can be used with either a stylus or a finger.

The AD7877touchscreen controller connects to the SPI0 interface via the SPI0SEL2 control signal. Two interrupt signals connect to the device:

- The data available output (DAV) signal is mapped to PB4 and is used to notify the ADSP-BF548 processor that the new ADC data is available in the results register.
- The pen interrupt (PENIRQ) signal is mapped to PB5 and is used to notify the ADSP-BF548 processor that the screen has been touched.

Refer to "LCD/PPI Configuration Switch (SW14)" on page 2-21 for information on how to configure the interrupt signals.

The STOPACQ pin connects to PPI0FS1. The STOPACQ signal is used to ensure that an acquisition never occurs during the noisy period when the LCD is being updated.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the touchscreen controller.

Keypad Interface

The EZ-KIT Lite features a 4 x 4 keypad assembly connected to the keypad interface of the ADSP-BF548 processor. The keypad connects to the EZ-KIT Lite via a nine-pin connector (P1). The keypad interface of the processor shares the same multi-function pins as the EPPI1 port and the host interface. Consequently, the same keypad pins connect to the host connector, PPI connector, and expansion interface. If you need to use the processor's pins for functions other than keypad, simply disconnect the keypad via the eight-position keypad switch (SW2). For more information, see "Keypad Enable Switch (SW2)" on page 2-16.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the keypad interface.

Rotary Encoder Interface

The ADSP-BF548 processor has a built-in, up-down counter with support for a rotary encoder. The three-wire rotary encoder interface connects to the rotary switch (SW3) and host connector. The rotary encoder can be turned clockwise for the up function, counter clockwise for the down function, or can be used as a push button for clearing the counter.

If you need to use the processor pins for the host interface, disconnect the rotary encoder switch via the four-position rotary enable switch (SW4). For more information, see "Rotary Encoder Enable Switch (SW4)" on page 2-17.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the rotary encoder interface.

Ethernet Interface

The EZ-KIT Lite has a fully functional, high-performance, single-chip Ethernet controller with HP Auto-MDIX and is fully compliant with IEEE 802.2/802.2u standards. The SMSC LAN9218 chip contains an integrated Ethernet MAC and PHY, supports 10BASE-T and 100BASE-TX operations. The part is attached gluelessly to the ADSP-BF548 processor via the asynchronous memory bus and is mapped directly to the processor's $\overline{\text{AMS1}}$ memory bank. The valid address range for the Ethernet chip access is 0x2400 0000 through 0x2400 007F. The IRQ signal of the Ethernet chip is mapped to the PE8 flag pin of the processor and is connected via the SW16 switch position 3. If PE8 needs to be used elsewhere on the board, turn off the SW16 switch to disconnect it from the Ethernet chip. For more information, see "Peripheral Control Enable (SW16)" on page 2-22.

The Ethernet chip is pre-loaded with a MAC address for the EZ-KIT Lite. The MAC address is stored in the Ethernet serial ROM (U12) and can be

found on a sticker on the bottom side of the EZ-KIT Lite. The serial ROM is connected directly to the LAN9218 and is accessed via the Ethernet chip only.

The PHY portion of the Ethernet chip connects to a Pulse HX1188 (U15) magnetics, then to a standard RJ-45 Ethernet connector (J4). For more information, see "Ethernet Connector (J4)" on page 2-34.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate the Ethernet interface.

Audio Interface

The audio interface of the EZ-KIT Lite consists of an Analog Devices AD1980 audio codec and its associated passive components. The AD1980 is a AC'97 2.3 compliant SoundMAX codec that supports 5.1 surround sound. The codec carries integrated DACs and requires minimal external circuitry. The codec connects to the ADSP-BF548 processor via the processor's serial port 0; the port is dedicated for the audio interface and does not connect to anything else on the board.

The codec connects to multiple connectors which allow you to get audio IN and OUT signals. Connector J10 can be used as a line or head phone out. J10 also can be configured via software as the front surround left and right channel or a 5.1 surround system. Connector J9 has two locations for plugging in 3.5 mm cables. The top location is the center channel on the left channel and the LFE out on the right channel. The bottom location of J9 is left and right back surround channels for a 5.1 surround system. Similarly to J9, J8 has two locations for 3.5 mm cables. The top location is for a stereo microphone, and the bottom location is for a stereo line in.

For more information, see "Dual Audio Connectors (J8 and J9)" on page 2-36 and "Audio Connector (J10)" on page 2-36.

The EZ-KIT Lite is shipped with a headphone and multiple 3.5 mm cables, which allow you to run the example programs provided in the EZ-KIT Lite installation directory and learn about the audio interface.

For more information on the AD1980 codec, go to AD1980.

ATAPI Interface

The ADSP-BF548 processor has a built-in advanced technology attachment packet interface (ATA/ATAPI-6) controller that can be attached to any peripherals that support ATAPI standards. The EZ-KIT Lite is shipped with a 2.5" Toshiba 5V 80GB ATAPI hard disk drive. The ATAPI interface shares pins with other peripherals on the EZ-KIT Lite. Consequently, the ATAPI interface of the processor can connect to an ATAPI device (hard drive) via the PPI port pins or the external address and data bus. The EZ-KIT Lite is wired such that it connects the ATAPI hard drive to the processor via the external address and data bus.

Two external 5V tolerant bus switches (U4 and U24) are used between the 3.3V processor signals and the 5V ATPI hard drive. U24 connects to all control signals of the ATAPI controller and is always enabled. U4 connects to the 16-bit data bus of the processor and is enabled with simple signal conditioning:

- When you write data to the hard drive, the FET switch U4 automatically connects the two devices together.
- When you do not use the ATAPI interface, the FET switch U4 is disconnected, and the processor does not see the capacitive load or the net traces associated with the hard disk drive.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate the ATAPI controller and hard disk drive operations. For more information about Toshiba MK4032GAX, refer to the data sheet provided by the product's manufacturer.

For more information on the ATAPI interface, refer to the *ADSP-BF54x Blackfin Processor Hardware Reference*.

USB OTG Interface

The ADSP-BF548 processor has a built-in, high-speed USB on-the-go (OTG) interface and integrated PHY. This interface connects to a 24 MHz clock (U13), has surge protection, and can be configured as a host or device. When in device mode, the USB 5V regulator (VR1) and FET switch (U39) are turned OFF. When in host mode, the USB 5V regulator and FET are turned ON and can supply 5V at 500 mA.

The control mechanism to turn the two devices ON and OFF are via the PE7 flag pin of the processor. By default PE7 is set low or a logic '0' via a pull-down resistor, and both devices are turned OFF. If you are not using the USB OTG interface and would like to use the PE7 flag pin for other purposes, turn OFF position 2 on the SW16 switch. This disconnects the PE7 flag pin from both the VR1 regulator and U39 FET. For more information, see "Peripheral Control Enable (SW16)" on page 2-22.

The USB OTG interface has a mini-AB connector (P4); cables that plug into P4 are shipped with the EZ-KIT Lite.

Use the example programs in the EZ-KIT Lite installation directory to learn about the ADSP-BF548 processor's device and host modes. For more information on the USB interface, refer to the *ADSP-BF548 Blackfin Processor Hardware Reference*.

UART Interface

The ADSP-BF548 processor has four built-in universal asynchronous receiver transmitters (UARTs). UART3-0 share the same processor pins as other peripherals on the EZ-KIT Lite. As a result, not all of the UARTs are available on the board: UART0 is not available on the board.

UART1 has full RS-232 functionality via the Analog Devices 3.3V ADM3202 (U32) line driver and receiver. The UART can be disconnected from the ADM3202 bit by turning OFF all positions on the SW7 switch. See "UART Enable Switch (SW7)" on page 2-19. When using UART1, jumpers JP1 and JP12 should not be installed. JP1 is a UART loopback jumper and should be installed only when running the POST program. JP12 is installed when you are not using the UART and need to use PP1FS3. See "UART1 Loopback Jumper (JP1)" on page 2-26 and "PPI1FS3 Pull-down Jumper (JP12)" on page 2-30 for more information.

UART2 and UART3 are connected to the expansion interface. UART3 of the processor also is available via a STAMP connector (P12). See "UART3 Connector (P12)" on page 2-41.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate UART and RS-232 operations.

For more information on the UART interface, refer to the *ADSP-BF548 Blackfin Processor Hardware Reference*.

CAN Interface

The Controller Area Network (CAN) interface contains two Philips TJA1041 high-speed CAN transceivers. The two transceivers are connected to the CAN0 and CAN1 ports of the processor. Either of the CAN ports can be used to transmit or receive data. The PC0 programmable flag connects to the error and power-on indication output of CAN0 (CAN0_ERR). The PC5 programmable flag connects to the error and power-on indication output of CAN1 (CAN1_ERR). The transmit and receive pins for both transceivers connect to the dedicated CAN0 and CAN1 transmit and receive pins of the processor.

The CAN0 interface can be disconnected from the processor by turning OFF positions 1 though 4 of the SW6 switch. Similarly, the CAN1 interface can be disconnected from the processor by turning OFF positions 1 though 4 of

the SW15 switch. When OFF, the signals can be used elsewhere on the board. See "CAN0 Enable Switch (SW6)" on page 2-18 and "CAN1 Enable Switch (SW15)" on page 2-22 for more information.

The CAN interface contains two 4-position modular connectors (see "CAN Connectors (J11 and J12)" on page 2-36).

Example programs are included in the EZ-KIT Lite installation directory to demonstrate CAN circuit operation.

Host Interface

The host DMA port of the Blackfin processor is available via a IDC 16x2 header (P3) on the EZ-KIT Lite. The port allows a host device external to the Blackfin processor to be a DMA master and transfer data back and forth.

When using the host interface port, the host device is the master, and the Blackfin processor is a DMA slave device. Since the host signals share pins with other peripherals on the EZ-KIT Lite, certain switches and jumpers must be OFF in order to use the host interface. When turning the switches or jumpers OFF, you disable the respective peripherals and are not able to evaluate the peripherals at the same time as the host interface. Table 1-6 describes the jumpers and switches that must be OFF, the respective host interface signal associated with these jumpers or switches, and the peripherals that are affected by turning these jumpers or switches OFF.

Table 1-6. Host Interface

Switch or Jumper:	Host Signals Affected:	EZ-KIT Lite Peripheral Affected:
SW2 (all OFF)	PPI1D[8:15]/HPD[0:7]	Keypad disabled
SW4 (all OFF)	HPACK, HPA, #HPCE	Rotary encoder disabled
SW5 (position 4 OFF)	HPWAIT	Push button 4 disabled
SW17 (position 3 OFF)	PPI1D[0:5]/HPD[8:13]	LCD 24-bit mode disabled; LCD 18-bit mode operational
JP2 (OFF)	#HPCE, #HPRD, #HPWR	STAMP interface disabled; LED1–2 can not be used as global status indicators.

RTC Interface

The ADSP-BF548 processor has a real-time clock (RTC) and a watchdog timer. Typically the RTC interface is used to implement a real-time watch or a life counter of the time elapsed since the last system reset. The EZ-KIT Lite is equipped with a Panasonic lithium coin 3V 24 MM battery with a 1000 mAh. The 3V battery and the 3.3V supply of the board are connected to the RTC power pin of the processor. When the EZ-KIT Lite is powered, it uses the board power to supply voltage to the RTC pin. When the EZ-KIT Lite is not powered, it uses the lithium battery to maintain the power to the RTC pin.

The battery allows you to evaluate RTC functionality for the life of the EZ-KIT Lite. You can calculate your application's specific power requirements and use a much smaller battery in a custom design.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate the RTC features.

The EZ-KIT Lite is shipped with a protective Mylar sheet placed between the coin battery and the positive pin of the battery holder. Please remember to remove the Mylar sheet before trying to use RTC functionality of the processor.

For more information on the RTC and watchdog timer, refer to the *ADSP-BF548 Blackfin Processor Hardware Reference*.

LEDs and Push Buttons

The EZ-KIT Lite provides four push buttons and six LEDs for general-purpose I/O.

The six LEDs, labeled `LED1` through `LED6`, are accessed via the `PG6-11` pins of the processor. For information on how to program the pins, refer to the *ADSP-BF548 Blackfin Processor Hardware Reference*.

The four general-purpose push button are labeled `PB1` through `PB4`. The status of each individual button can be read through programmable flag (PF) inputs, `PF8-11`. A PF reads `1` when a corresponding switch is being pressed. When the switch is released, the PF reads `0`. A connection between the push button and PF input is established through the `SW5` DIP switch. See "Push Button Enable Switch (SW5)" on page 2-18 for details.

An example program is included in the EZ-KIT Lite installation directory to demonstrate functionality of the LEDs and push buttons.

JTAG Interface

The JTAG emulation port allows an emulator to access the processor's internal and external memory through a six-pin interface. The JTAG emulator port of the processor can be accessed via the on-board USB Debug Agent or with an external emulator via the JTAG connector (`ZP4`). When an external emulator connects to the board, the on-board USB Debug

Agent is disabled. See "JTAG Connector (ZP4)" on page 2-42 for more information.

For more information on emulators, contact Analog Devices or go to: http://www.analog.com/processors/tools/blackfin.

Expansion Interface

The expansion interface consists of three 90-pin connectors, J1–3. These connectors contain a majority of the ADSP-BF548 processor's signals. For the pinout of the connectors, go to "ADSP-BF548 EZ-KIT Lite Schematic" on page B-1. The expansion interface allows an EZ-Extender or a custom-design daughter board to be tested across various hardware platforms. The mechanical dimensions of the expansion connectors can be obtained by contacting Technical Support.

Analog Devices offers many EZ-Extender products. For more information about EZ-Extenders, visit the Analog Devices Web site at: http://www.analog.com/processors/tools/blackfin.

Limits to current and interface speed must be taken into consideration when using the expansion interface. Because current for the expansion interface is sourced from the EZ-KIT Lite, the current should be limited to 1A for both the 5V and 3.3V planes. If more current is required, then a separate power connector and a regulator must be designed on a daughter card. Additional circuitry can add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

Power Measurements

Several locations are provided for measuring the current draw from various power planes. Precision 0.05 ohm shunt resistors are available on the VDDINT, VDDEXT, and VDDDDR pins. For current draw measurements, the associated jumper (JP4, JP5, or JP6) should be removed. Once the jumper is removed, the voltage across the resistor can be measured using an oscilloscope. Once voltage is measured, current can be calculated by dividing the voltage by 0.05. For the highest accuracy, a differential probe should be used for measuring the voltage across the resistor.

For more information, see "VDDINT Power Jumper (JP4)", "VDDEXT Power Jumper (JP5)", and "VDDDDR Power Jumper (JP6)".

Board Design Database

A .zip file containing all of the electronic information required for the design, layout, fabrication and assembly of the product is available for download from the Analog Devices board design database at: http://www.analog.com/board-design-database.

Power-On-Self Test

Once assembled, each EZ-KIT Lite is fully tested for an extended period of time with a power-on-self test (POST). The POST tests all EZ-KIT Lite peripherals and validates functionality as well as connectivity to the processor. The POST is loaded into burst flash memory (U5) and can be activated by resetting the board and pressing the associated push button(s). The POST also can be used as a reference for a custom software design or hardware troubleshooting.

When running the POST, you may need to place switches and jumpers in specific test modes. In some instances, such as Ethernet, you may need to

plug in an Ethernet loopback connector (provided with the EZ-KIT Lite) to run the POST. The user LEDs (`LED1-6`) will convey whether the specific tests have passed or failed.

The POST program is included in the EZ-KIT Lite installation directory. For more information, refer to the readme file in the POST directory.


The POST program is only available when using VisualDSP++.

Example Programs

Example programs are provided with the ADSP-BF548 EZ-KIT Lite to demonstrate various capabilities of the product. The programs are included in the product installation kit and can be found in the `Examples` folder of the installation. Refer to a readme file provided with each example for more information.

CCES users are encouraged to use the example browser to find examples included with the EZ-KIT Lite Board Support Package.

2 ADSP-BF548 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF548 EZ-KIT Lite board.

The following topics are covered.

- "System Architecture" on page 2-2
  Describes the ADSP-BF548 EZ-KIT Lite board configuration and explains how the board components interface with the processor.
- "Programmable Flags" on page 2-3
  Shows the locations and describes the programming flags (PFs).
- "Push Button and Switch Settings" on page 2-15
  Shows the location and describes the push buttons and switches.
- "Jumpers" on page 2-25
  Shows the location and describes the configuration jumpers.
- "LEDs" on page 2-31
  Shows the location and describes the LEDs.
- "Connectors" on page 2-33
  Shows the locations and provides part numbers for the on-board connectors. In addition, the manufacturer and part number information is provided for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board (Figure 2-1).

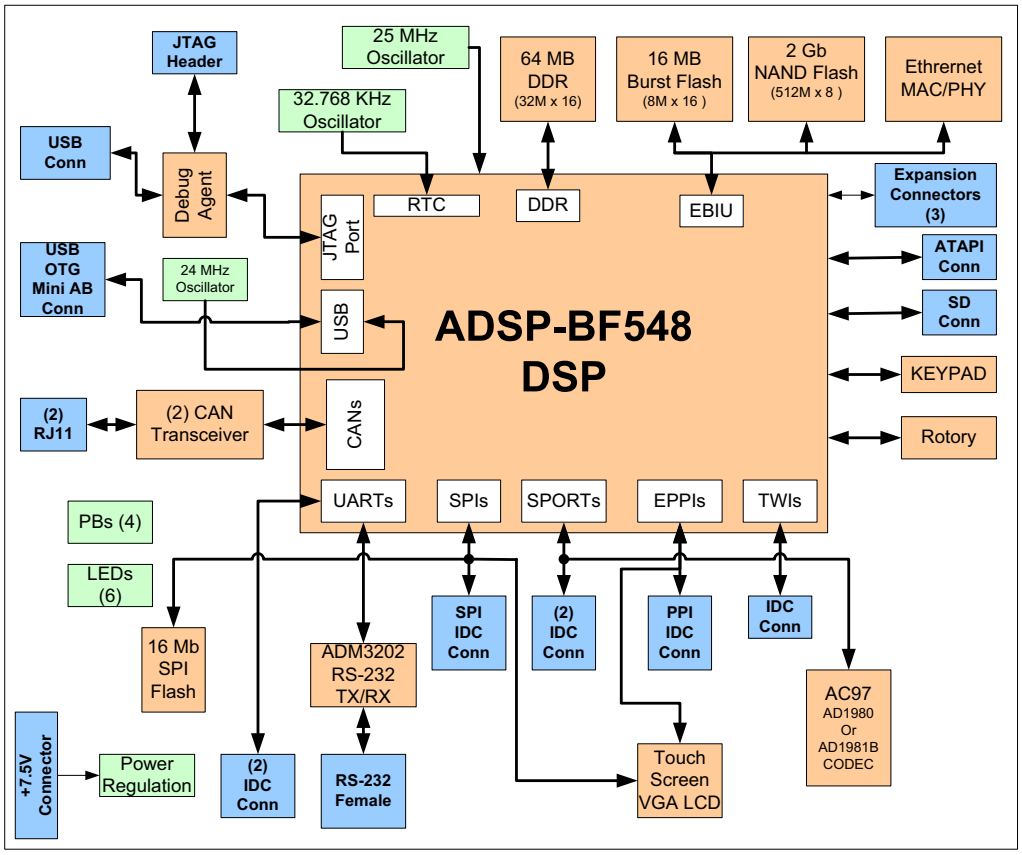


Figure 2-1. System Architecture

This EZ-KIT Lite is designed to test the ADSP-BF548 processor capabilities. The processor has an I/O voltage of 3.3V. The core voltage of the processor is controlled by the internal voltage regulator.

The core voltage and clock rate can be set on the fly by the processor. The input clock is 25 MHz. A 32.768 kHz crystal supplies the real-time clock (RTC) inputs of the processor. The default boot mode for the processor is burst flash boot. See "Boot Mode Select Switch (SW1)" on page 2-15 for information on how to change the default boot mode.

Programmable Flags

The processor has 153 general-purpose input/output (GPIO) signals spread across ten ports (PA, PB, PC, PD, PE, PF, PG, PH, PI, and PJ). The pins are multi-functional and depend on the ADSP-BF548 processor setup. The following tables show how the programmable flag pins are used on the EZ-KIT Lite.

PA programmable flag pins in Table 2-1

PB programmable flag pins in Table 2-2

PC programmable flag pins in Table 2-3

PD programmable flag pins in Table 2-4

PE programmable flag pins in Table 2-5

PF programmable flag pins in Table 2-6

PG programmable flag pins in Table 2-7

PH programmable flag pins in Table 2-8

PI programmable flag pins in Table 2-9

PJ programmable flag pins in Table 2-10

Table 2-1. PA Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PA0	TFS2	Expansion interface, SPORT2 connector
PA1	DT2SEC/TMR4	Expansion interface, SPORT2 connector
PA2	DT2PRI	Expansion interface, SPORT2 connector
PA3	TSCLK2	Expansion interface, SPORT2 connector
PA4	RFS2	Expansion interface, SPORT2 connector
PA5	DR2SEC/TMR5	Expansion interface, SPORT2 connector
PA6	DR2PRI	Expansion interface, SPORT2 connector
PA7	RSCLK2/TACLK0	Expansion interface, SPORT2 connector

Table 2-1. PA Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PA8	TFS3/TACLK1	Expansion interface, SPORT3 connector
PA9	DT3SEC/TMR6	Expansion interface, SPORT3 connector
PA10	DT3PRI/TACLK2	Expansion interface, SPORT3 connector
PA11	TSCLK3/TACLK3	Expansion interface, SPORT3 connector
PA12	RFS3/TACLK4	Expansion interface, SPORT3 connector
PA13	DR3SEC/TMR7/TACLK5	Expansion interface, SPORT3 connector
PA14	DR3PRI/TACLK6	Expansion interface, SPORT3 connector
PA15	RSCLK3/TACLK7 and TACI7	Expansion interface, SPORT3 connector

Table 2-2. PB Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PB0	SCL1	Expansion interface, TWI connector
PB1	SDA1	Expansion interface, TWI connector
PB2	UART3RTS	Default: PPI1CLK Mux select via SW14.3. Expansion interface
PB3	UART3CTS	Default: audio codec reset via SW16.1. Expansion interface
PB4	UART2TX	Default: LCD data available via SW14.1. Expansion interface
PB5	UART2RX/TACI2	Default: LCD IRQ via SW14.2. Expansion interface
PB6	UART3TX	Expansion interface, UART3 connector
PB7	UART3RX/TACI3	Expansion interface, UART3 connector
PB8	SPI2SS/TMR0	Default: PB1 via SW5.1. Expansion interface, timers connector, SPORT2-3 connectors
PB9	SPI2SEL1/TMR1	Default: PB2 via SW5.2. Expansion interface, timers connector, UART3 connector, SPORT2-3 connectors

Table 2-2. PB Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PB10	SPI2SEL2/TMR2	Default: PB3 via SW5.3. Expansion interface, timers connector, UART3 connector, SPORT2-3 connectors
PB11	SPI2SEL3/BOOTWAIT	Default: PB4 via SW5.4. Expansion interface, host interface connector. NOR RESET via SW16.4.
PB12	SPI2SCK	Expansion interface
PB13	SPI2MOSI	Expansion interface
PB14	SPIMISO	Expansion interface

Table 2-3. PC Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PC0	TFS0	Default: CAN0 via SW6.3 SPI connector, TWI connector, SPORT2-3 connectors
PC1	DT0SEC/MMCLK	Not used
PC2	DT0PRI	Audio codec data pin
PC3	TSCLK0	Audio codec clock pin
PC4	RFS0	Audio codec sync pin
PC5	DR0SEC/MBCLK	Default: CAN1 via SW15.3 SPI connector, TWI connector, SPORT2-3 connectors
PC6	DR0PRI	Audio codec data pin
PC7	RSCLK0	Audio codec clock pin
PC8	SD_D0	SD memory data pin
PC9	SD_D1	SD memory data pin
PC10	SD_D2	SD memory data pin
PC11	SD_D3	SD memory data pin

Table 2-3. PC Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PC12	SD_CLK	SD memory clock pin
PC13	SD_CMD	SD memory command pin

Table 2-4. PD Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PD0	PPI1_D0/HOST_D8/ TFS1/PPI0_D18	Default: LCD module via SW17.3. Host interface connector, expansion interface, PPI1 connector
PD1	PPI1_D1/HOST_D9/ DT1SEC/PPI0_D19	Default: LCD module via SW17.3. Host interface connector, expansion interface, PPI1 connector
PD2	PPI1_D2/HOST_D10/ DT1PRI /PPI0_D20	Default: LCD module via SW17.3. Host interface connector, expansion interface, PPI1 connector
PD3	PPI1_D3/HOST_D11/ TSCLK1/PPI0_D21	Default: LCD module via SW17.3. Host interface connector, expansion interface, PPI1 connector
PD4	PPI1_D4/HOST_D12/ RFS1/PPI0_D22	Default: LCD module via SW17.3. Host interface connector, expansion interface, PPI1 connector
PD5	PPI1_D5/HOST_D13/ DR1SEC/PPI0_D23	Default: LCD module via SW17.3. Host interface connector, expansion interface, PPI1 connector
PD6	PPI1_D6/HOST_D14/ DR1PRI	Host interface connector, expansion interface, PPI1 connector
PD7	PPI1_D7/HOST_D15/ RSCLK1	Host interface connector, expansion interface, PPI1 connector
PD8	PPI1_D8/HOST_D0/ PPI2_D0/KEY_ROW0	Default: keypad via SW2.8. Host interface connector, expansion interface, PPI1 connector

Table 2-4. PD Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PD9	PPI1_D9/HOST_D1/ PPI2_D1/KEY_ROW1	Default: keypad via SW2.7. Host interface connector, expansion interface, PPI1 connector
PD10	PPI1_D10/HOST_D2/ PPI2_D2/KEY_ROW2	Default: keypad via SW2.6. Host interface connector, expansion interface, PPI1 connector
PD11	PPI1_D11/HOST_D3/ PPI2_D3/KEY_ROW3	Default: keypad via SW2.5. Host interface connector, expansion interface, PPI1 connector
PD12	PPI1_D12/HOST_D4/ PPI2_D4/KEY_COL0	Default: keypad via SW2.4. Host interface connector, expansion interface, PPI1 connector
PD13	PPI1_D13/HOST_D5/ PPI2_D5/KEY_COL1	Default: keypad via SW2.3. Host interface connector, expansion interface, PPI1 connector
PD14	PPI1_D14/HOST_D6/ PPI2_D6/KEY_COL2	Default: keypad via SW2.2. Host interface connector, expansion interface, PPI1 connector
PD15	PPI1_D15/HOST_D7/ PPI2_D7/KEY_COL3	Default: keypad via SW2.1. Host interface connector, expansion interface, PPI1 connector

Table 2-5. PE Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PE0	SPIOSCK/KEY_COL7	SPI memory, LCD touchscreen controller, expansion interface
PE1	SPIOMISO/KEY_ROW6	SPI memory, LCD touchscreen controller, expansion interface
PE2	SPIOMOSI/KEY_COL6	SPI memory, LCD touchscreen controller, expansion interface
PE3	SPIOSS/KEY_ROW5	Default: LCD DISP via SW14.4. Expansion interface

Table 2-5. PE Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PE4	SPIOSEL1/KEY_COL5	Default: SPI memory. Expansion interface
PE5	SPIOSEL2/KEY_ROW4	Default: LCD touchscreen controller Expansion interface
PE6	SPIOSEL3/KEY_COL4	Expansion interface
PE7	UART0TX/KEY_ROW7	Default: USB OTG VR1 and U39 enable via SW16.2. Expansion interface
PE8	UART0RX/TACI0	Default: Ethernet IRQ via SW16.3. Expansion interface
PE9	UART1RTS	UART1 serial port via SW7.3
PE10	UART1CTS	UART1 serial port via SW7.1
PE11	PPI1_CLK	Expansion interface, PPI1 connector
PE12	PPI1_FS1	Expansion interface, PPI1 connector
PE13	PPI1_FS2	Expansion interface, PPI1 connector
PE14	SCL0	Expansion interface, SPORT2-3 connectors, PPI1 connector
PE15	SDA0	Expansion interface, SPORT2-3 connectors, PPI1 connector

Table 2-6. PF Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PF0	PPI0_D0	Default: LCD module via SW17. Expansion interface
PF1	PPI0_D1	Default: LCD module via SW17. Expansion interface
PF2	PPI0_D2	Default: LCD module via SW17. Expansion interface
PF3	PPI0_D3	Default: LCD module via SW17. Expansion interface

Table 2-6. PF Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PF4	PPIO_D4	Default: LCD module via SW17. Expansion interface
PF5	PPIO_D5	Default: LCD module via SW17. Expansion interface
PF6	PPIO_D6	Default: LCD module via SW17. Expansion interface
PF7	PPIO_D7	Default: LCD module via SW17. Expansion interface
PF8	PPIO_D8	Default: LCD module via SW17. Expansion interface
PF9	PPIO_D9	Default: LCD module via SW17. Expansion interface
PF10	PPIO_D10	Default: LCD module via SW17. Expansion interface
PF11	PPIO_D11	Default: LCD module via SW17. Expansion interface
PF12	PPIO_D12	Default: LCD module via SW17. Expansion interface
PF13	PPIO_D13	Default: LCD module via SW17. Expansion interface
PF14	PPIO_D14	Default: LCD module via SW17. Expansion interface
PF15	PPIO_D15	Default: LCD module via SW17. Expansion interface

Table 2-7. PG Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PG0	PPIO_CLK/TMRCLK	Default: LCD module via SW17. Expansion interface
PG1	PPIO_FS1	Default: LCD module via SW17. Expansion interface

Table 2-7. PG Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PG2	PPI0_FS2	Default: LCD module via SW17. Expansion interface
PG3	PPI0_D16	Default: LCD module via SW17. Expansion interface
PG4	PPI0_D17	Default: LCD module via SW17. Expansion interface
PG5	SPI1SEL1/HOST_CE/ PPI2_FS2/ CZM	Default: rotary encoder via SW4.3. Host interface connector SPI connector via JP2 SPORT2 connector via JP2 SPORT3 connector via JP2 PPI1 connector via JP2
PG6	SPI1SEL2/HOST_RD/ PPI2_FS1	Default: LED1. Expansion interface Host interface connector SPI connector via JP2 SPORT2 connector via JP2 SPORT3 connector via JP2 PPI1 connector via JP2
PG7	SPI1SEL3/HOST_WR/ PPI2_CLK	Default: LED2. Expansion interface Host interface connector SPI connector via JP2 SPORT2 connector via JP2 SPORT3 connector via JP2
PG8	SPI1SCK	Default: LED3. Expansion interface SPI connector via JP2 SPORT2 connector via JP2 SPORT3 connector via JP2 PPI1 connector via JP2

Table 2-7. PG Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PG9	SPI1MISO	Default: LED4. Expansion interface SPI connector via JP2 SPORT2 connector viaJP2 SPORT3 connector via JP2 PPI1 connector via JP2
PG10	SPI1MOSI	Default: LED5. Expansion interface SPI connector via JP2, JP7, and JP8 SPORT2 connector via JP2, JP7, and JP8 SPORT3 connector via JP2, JP7, and JP8 PPI1 connector via JP2, JP7, and JP8
PG11	SPI1SS/MTXON	Default: LED6. Expansion interface SPI connector via JP2 SPORT2 connector via JP2 SPORT3 connector via JP2 PPI1 connector via JP2
PG12	CAN0TX	CAN0
PG13	CAN0RX/TACI4	Default: CAN0 via SW6.4 SPI connector, TWI connector, timers connector, SPORT2-3 connectors, PPI1 connector
PG14	CAN1TX	CAN1
PG15	CAN1RX/TACI5	Default: CAN1 via SW15.4 SPI connector, TWI connector, timers connector, SPORT2-3 connectors, PPI1 connector

Programmable Flags

Table 2-8. PH Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PH0	UART1_TX/PPI1_FS3	Default: UART1 serial port. Expansion interface, PPI1 connector
PH1	UART1_RX/PPI2_FS3/TACI1	Default: UART1 serial port via SW7.2. Expansion interface
PH2	ATAPI_RESET/TMR8/ PPI0_FS3	ATAPI reset; expansion interface
PH3	HOST_ADDR/TMR9/CUD	Default: rotary encoder via SW4.2. Host interface connector
PH4	HOST_ACK/TMR10/CDG	Default: rotary encoder via SW4.1. Host interface connector
PH5	MTX/DMAR0/TACI8 and TACLK8	Not used
PH6	MRX/DMAR1/TACI9 and TACLK9	Not used
PH7	MRXON/BOOTWAIT/TACI10 and TACLK10	Expansion interface, host interface connector
PH8	A4	Address line on burst flash memory, Ethernet controller, expansion interface
PH9	A5	Address line on burst flash memory, Ethernet controller, expansion interface
PH10	A6	Address line on burst flash memory, Ethernet controller, expansion interface
PH11	A7	Address line on burst flash memory, Ethernet controller, expansion interface
PH12	A8	Address line on burst flash memory, expansion interface
PH13	A9	Address line on burst flash memory, expansion interface

Table 2-9. PI Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PI0	A10	Address line on burst flash memory, expansion interface
PI1	A11	Address line on burst flash memory, expansion interface
PI2	A12	Address line on burst flash memory, expansion interface
PI3	A13	Address line on burst flash memory, expansion interface
PI4	A14	Address line on burst flash memory, expansion interface
PI5	A15	Address line on burst flash memory, expansion interface
PI6	A16	Address line on burst flash memory, expansion interface
PI7	A17	Address line on burst flash memory, expansion interface
PI8	A18	Address line on burst flash memory, expansion interface
PI9	A19	Address line on burst flash memory, expansion interface
PI10	A20	Address line on burst flash memory, expansion interface
PI11	A21	Address line on burst flash memory, expansion interface
PI12	A22	Address line on burst flash memory, expansion interface
PI13	A23	Address line on burst flash memory, expansion interface
PI14	A24	Address line on burst flash memory, expansion interface
PI15	A25/NORCLK	Clock for burst flash memory

Programmable Flags

Table 2-10. PJ Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PJ0	ARDY/WAIT	WAIT for burst flash memory, expansion interface
PJ1	ND_CE	Chip enable for NAND
PJ2	ND_RB	Ready/busy for NAND
PJ3	ATAPI_DIORB	ATAPI (hard disk drive) interface
PJ4	ATAPI_DIOWB	ATAPI (hard disk drive) interface
PJ5	ATAPI_CS0B	ATAPI (hard disk drive) interface
PJ6	ATAPI_CS1B	ATAPI (hard disk drive) interface
PJ7	ATAPI_DMACKB	ATAPI (hard disk drive) interface
PJ8	ATAPI_DMARQ	ATAPI (hard disk drive) interface
PJ9	ATAPI_INTRQ	ATAPI (hard disk drive) interface
PJ10	ATAPI_IORDY	ATAPI (hard disk drive) interface
PJ11	BR	Expansion interface
PJ12	BG	Expansion interface
PJ13	BGH	Expansion interface

Push Button and Switch Settings

This section describes operation of the push buttons and switches. The push button and switch locations are shown in Figure 2-2.

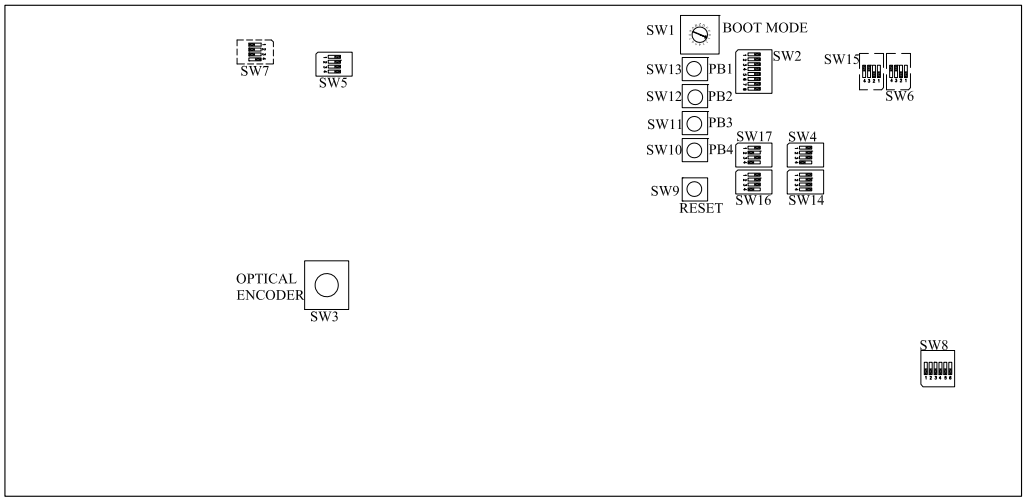


Figure 2-2. Push Button and Switch Locations

Boot Mode Select Switch (SW1)

The rotary switch (SW1) determines the boot mode of the processor. Table 2-11 shows the available boot mode settings. By default the ADSP-BF548 processor boots from the on-board burst flash memory.

Table 2-11. Boot Mode Select Switch (SW1)

SW1 Position	Processor Boot Mode
0	Idle—no boot
1	**Boot from 16-bit burst flash memory (default)**
2	Boot from 16-bit asynchronous FIFO

Table 2-11. Boot Mode Select Switch (SW1) (Cont'd)

SW1 Position	Processor Boot Mode
3	Boot from serial SPI memory
4	Boot from SPI host device
5	Boot from serial TWI memory
6	Boot from TWI host
7	Boot from UART host
8–9	Reserved
A	Boot from double-data rate (DDR) SDRAM
B, C, D	Reserved
E	Boot from 16-bit host DMA
F	Boot from eight-bit host DMA

Keypad Enable Switch (SW2)

The keypad enable switch (SW2) disconnects the keypad signals from the GPIO pins of the processor. When the switch is OFF, its associated GPIO signals can be used on the PPI1 port, host interface, or expansion interface (see Table 2-12).

Table 2-12. Keypad Enable Switch (SW2)

EZ-KIT Lite Signal	SW2 Switch Position (Default)	Processor Signal
PPI1D15/HPD7/KPC3	1 (ON)	PD15
PPI1D14/HPD6/KPC2	2 (ON)	PD14
PPI1D13/HPD5/KPC1	3 (ON)	PD13
PPI1D12/HPD4/KPC0	4 (ON)	PD12
PPI1D11/HPD3/KPR3	5 (ON)	PD11
PPI1D10/HPD2/KPR2	6 (ON)	PD10

Table 2-12. Keypad Enable Switch (SW2) (Cont'd)

EZ-KIT Lite Signal	SW2 Switch Position (Default)	Processor Signal
PPI1D9/HPD1/KPR1	7 (ON)	PD9
PPI1D8/HPD0/KPR0	8 (ON)	PD8

Rotary Encoder with Momentary Switch (SW3)

The rotary encoder can be turned clockwise for an up count or counter-clockwise for a down count. The encoder also features a momentary switch that allows you to zero the counter. The rotary encoder can be disabled from the processor by using the rotary encoder enable switch (SW4). See "Rotary Encoder Enable Switch (SW4)" for more information.

Rotary Encoder Enable Switch (SW4)

The rotary encoder enable switch (SW4) disconnects the rotary encoder signals from the GPIO pins of the processor. When the switch is OFF, its associated GPIO signals can be used on the host interface (see Table 2-13).

Table 2-13. Rotary Encoder Enable Switch (SW4)

EZ-KIT Lite Signal	SW4 Switch Position (Default)	Processor Signal
HPACK/CNTCUD	1 (ON)	PH4
HPA/CNTCDG	2 (ON)	PH3
#HPCE/CNTCZM	3 (ON)	PG5
N/A	4 (OFF)	N/A

Push Button Enable Switch (SW5)

The push button enable switch (SW5) disconnects the associated push button circuit from the GPIO pins of the processor. When SW5 is OFF, the associated GPIO signals can be used on the expansion interface, host interface, or STAMP (0.1" IDC) headers (see Table 2-14).

Table 2-14. Push Button Enable Switch (SW5)

Push Button	EZ-KIT Lite Signal	SW5 Switch Position (Default)	Processor Signal
PB1 (SW13)	PUSHBUTTON1	1 (ON)	PB8
PB2 (SW12)	PUSHBUTTON2	2 (ON)	PB9
PB3 (SW11)	PUSHBUTTON3	3 (ON)	PB10
PB4 (SW10)	PUSHBUTTON4/HPWAIT	4 (ON)	PB11

CAN0 Enable Switch (SW6)

The CAN0 enable switch (SW6) disconnects the CAN0 signals from the GPIO pins of the processor and deactivates the CAN0 transceiver (U21). When SW6 is in the default positions (shown in Table 2-15), the switch connects to CAN0; otherwise, the associated GPIO signal of SW6 can be used as a STAMP GPIO.

Table 2-15. CAN0 Enable Switch (SW6)

CAN0 Signal	EZ-KIT Lite Signal	SW6 Switch Position (Default)	Processor Signal
ENABLE	N/A	1 (OFF)	N/A
STANDBY	N/A	2 (OFF)	N/A
ERROR	CAN0_ERR	3 (ON)	PC0
RECEIVE DATA	CANORX	4 (ON)	PG13

UART Enable Switch (SW7)

The UART enable switch (SW7) disconnects the UART1 signals from the GPIO pins of the processor. When the switch is OFF, the associated GPIO signal of SW7 can be used elsewhere on the board (see Table 2-16).

Table 2-16. UART Enable Switch (SW7)

EZ-KIT Lite Signal	SW7 Switch Position (Default)	Processor Signal
UART1CTS	1 (ON)	PE10
UART1_RX	2 (ON)	PH1
UART1RTS	3 (ON)	PE9
N/A	4 (OFF)	N/A

Audio Loopback Test Switch (SW8)

The audio loopback test switch (SW8) connects the inputs signals of the audio interface to the output signals. This allows the EZ-KIT Lite to be placed in a loopback test mode for signal and circuit continuity and functionality (see "Power-On-Self Test" on page 1-33). All positions of the switch should be ON when running POST. In all other cases, the switch should be kept OFF. Table 2-17 shows the default settings for the SW8 switch.

Table 2-17. Audio Loopback Test Switch (SW8)

EZ-KIT Lite Input Signal	SW8 Switch Position (Default)	EZ-KIT Lite Output Signal
LINEIN_L	1 (OFF)	SURROUT_L
LINEIN_R	2 (OFF)	SURROUT_R
LINEIN_L	3 (OFF)	CENTER_OUT
LINEIN_R	4 (OFF)	LFE_OUT
MIC_L	5 (OFF)	LINEOUT_L
MIC_R	6 (OFF)	LINEOUT_R

Reset Push Button (SW9)

The reset push button (SW9) resets all of the ICs on the board. One exception is the USB interface chip. The chip is not reset when the push button is pressed after the USB cable has been plugged in and communication with the PC has been initialized correctly. After USB communication has been initialized, the only way to reset the USB chip is by powering down the board.

Programmable Flag Push Buttons (SW10–13)

Four momentary push buttons (SW10-13) are provided for general-purpose user input. The buttons connect to the PB11-8 programmable flag pins of the processor. The push buttons are active high and, when pressed, send a high (1) to the processor. The push button enable switch (SW5) disconnects the push buttons from the corresponding PB signal (refer to "Push Button Enable Switch (SW5)" on page 2-18 for more information). The programmable flag signals and associated switches are shown in Table 2-18.

Table 2-18. Programmable Flag Switches

Push Button	EZ-KIT Lite Signal	Processor Signal
PB1 (SW13)	PUSHBUTTON1	PB8
PB2 (SW12)	PUSHBUTTON2	PB9
PB3 (SW11)	PUSHBUTTON3	PB10
PB4 (SW10)	PUSHBUTTON4/HPWAIT	PB11

LCD/PPI Configuration Switch (SW14)

The LCD/PPI configuration switch (SW14) connects the GPIO pins of the processor to the LCD or PPI configuration pins:

- SW14 position 1 connects PB4 to the data available output (DAV) of the touchscreen controller (U9).
- SW14 position 2 connects PB5 to the pen interrupt output (PENIRQ) of the touchscreen controller (U9).
- SW14 position 3 connects PB2 to the PPI1CLK multiplexter (U20). This allows you to connect the PPI1CLK to the clock signal generated on the expansion interface or the on-board 27 MHz oscillator (U19).
- SW14 position 4 connects PE3 to the DISP signal of the LCD via the LCD data connector (P15).

When SW14 is OFF, its associated GPIO signals can be used on the expansion interface (see Table 2-19).

Table 2-19. LCD/PPI Configuration Switch (SW14)

EZ-KIT Lite Signal	SW14 Switch Position (Default)	Processor Signal
LCD_DAV	1 (ON)	UART2TX/PB4
LCD_IRQ	2 (ON)	UART2RX/PB5
PPI1_SEL	3 (ON)	UART3RTS/PB2
LCD_DISP	4 (ON)	PE3

CAN1 Enable Switch (SW15)

The CAN1 enable switch (SW15) disconnects the CAN1 signals from the GPIO pins of the processor and deactivates the CAN1 transceiver (U33). When SW15 is in the default positions (shown in Table 2-20), the switch connects to CAN1. When otherwise, the associated GPIO signal of SW15 can be used as a STAMP GPIO.

Table 2-20. CAN1 Enable Switch (SW15)

CAN1 Signal	EZ-KIT Lite Signal	SW15 Switch Position (Default)	Processor Signal
ENABLE	N/A	1 (OFF)	N/A
STANDBY	N/A	2 (OFF)	N/A
ERROR	CAN1_ERR	3 (ON)	PC5
RECEIVE DATA	CAN1RX	4 (ON)	PG15

Peripheral Control Enable (SW16)

The peripheral control enable (SW16) connects the GPIO pins of the processor to the enable pins of the audio codec, USB regulator, or Ethernet controller:

- SW16 position 1 connects PB3 to the reset pin of the audio codec (U11). This allows the audio codec to be reset via software.
- SW16 position 2 connects PE7 to the 5 volt VBUS USB regulator (VR1) and FET switch (U39). This allows the software to control the enable pins of both the regulator and the FET switch if the VBUS line is powered with 5 volts by some other host device. When in USB OTG host mode, the signal needs to be a logic 1. This will cause the EZ-KIT to supply the 5V to the VBUS line. When in USB OTG device mode, the signal needs to be a logic 0. This will allow the host device to power the VBUS line and allow the Blackfin processor to remain in device mode.

- SW16 position 3 connects PE8 to the interrupt signal of the Ethernet controller (U14).
- SW16 position 4 connects PB11 to the reset of burst flash memory. This allows the software to reset the burst flash. In order to use this signal as a reset for burst flash, SW5.4 needs to be set OFF. When the signal is used as a reset for the burst flash, the HOSTWAIT signal and PB4 are not be available. By default the switch is set to OFF and is not used.

When the switch is OFF, its associated GPIO signals can be used on the expansion interface (see Table 2-21).

Table 2-21. Peripheral Control Enable (SW16)

EZ-KIT Lite Signal	SW16 Switch Position (Default)	Processor Signal
AUDIO_RESET	1 (ON)	UART3CTS/PB3
USB_VRSEL	2 (ON)	PE7
LAN_IRQ	3 (ON)	PE8
NOR_RESET	4 (OFF)	PB11 (PUSHBUTTON4/HPWAIT)

LCD Module Configuration (SW17)

The LCD module configuration switch (SW17) is used to set up the LCD module in 24-bit mode, 18-bit mode, or to disconnect the LCD in order to use the processor EPPI signals on other areas of the board. The default setting is for the LCD module to operate in 24-bit mode; the corresponding switch settings are shown in Table 2-22. To operate the LCD module in 18-bit mode, set SW17 as shown in Table 2-23.

In order to disconnect the LCD module so that PPI1 or PPI0 can be used elsewhere on the board, follow the settings in Table 2-24. When the switch is OFF, its associated PPI1 and PPI0 signals can be used on the expansion interface, host interface, or STAMP PPI1 header.

Table 2-22. LCD Module Configuration in 24-bit Mode (SW17)

SW17 Switch Position (Default)	Processor Signal	EZ-KIT Lite Signal
1 (ON)	PPI0CLK PPI0FS1 PPI0FS2	LCD_PPI0CLK LCD_PPI0FS1 LCD_PPI0FS2
2 (OFF)	PPI0D[0-17]	LCD_R[2-7] LCD_G[2-7] LCD_B[2-7]
3 (ON)	PPI0D[0-17] PPI1D[0-5]/HPD[8-13]	LCD_R[0-7] LCD_G[0-7] LCD_B[0-7]
4 (OFF)	N/A	N/A

Table 2-23. LCD Module Configuration in 18-bit Mode (SW17)

SW17 Switch Position	Processor Signal	EZ-KIT Lite Signal
1 (ON)	PPI0CLK PPI0FS1 PPI0FS2	LCD_PPI0CLK LCD_PPI0FS1 LCD_PPI0FS2
2 (ON)	PPI0D[0-17]	LCD_R[2-7] LCD_G[2-7] LCD_B[2-7]
3 (OFF)	PPI0D[0-17] PPI1D[0-5]/HPD[8-13]	LCD_R[0-7] LCD_G[0-7] LCD_B[0-7]
4 (OFF)	N/A	N/A

Table 2-24. LCD Module Configuration Disconnected (SW17)

SW17 Switch Position	Processor Signal	EZ-KIT Lite Signal
1 (OFF)	PPI0CLK PPI0FS1 PPI0FS2	LCD_PPI0CLK LCD_PPI0FS1 LCD_PPI0FS2
2 (OFF)	PPI0D[0-17]	LCD_R[2-7] LCD_G[2-7] LCD_B[2-7]
3 (OFF)	PPI0D[0-17] PPI1D[0-5]/HPD[8-13]	LCD_R[0-7] LCD_G[0-7] LCD_B[0-7]
4 (OFF)	N/A	N/A

Jumpers

This section describes functionality of the configuration jumpers. Figure 2-3 shows the jumper locations.

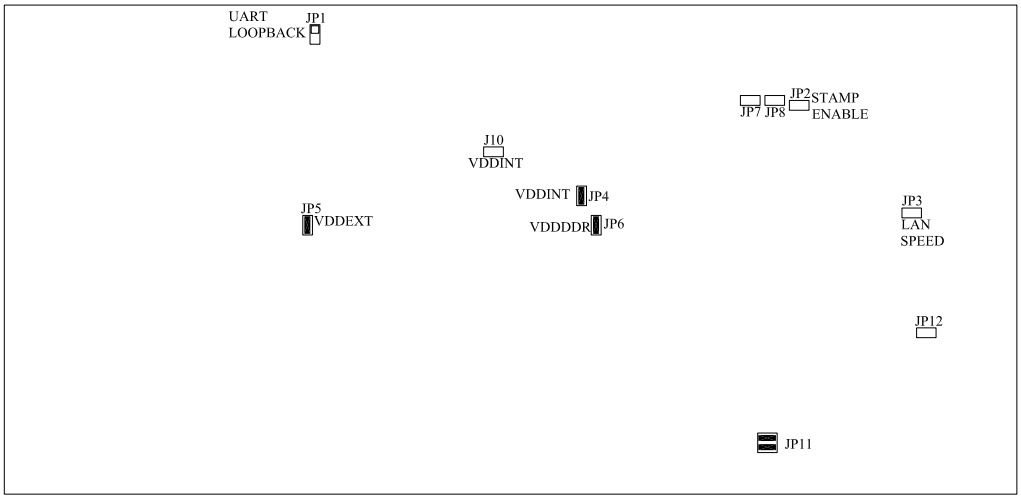


Figure 2-3. Configuration Jumper Locations

UART1 Loopback Jumper (JP1)

The UART1 loopback jumper (JP1) is used to place the UART1 port of the processor in a loopback condition. The jumper connects the UART1_TX line of the processor to the UART1_RX signal of the processor. The jumper is required only when the power-on-self-test (POST) is used to test the serial port interface. The jumper setting is shown in Table 2-25.

Table 2-25. UART1 Loopback Jumper (JP1)

JP1 Setting	Mode
OFF	**Normal operation. UART1_TX to UART1_RX is disconnected (default)**
ON	Loopback operation. Connects UART1_TX to UART1_RX

SPI1 Enable Jumper (JP2)

The SPI1 enable jumper (JP2) activates a buffer and enables the SPI1 port of the processor to be connected to the STAMP headers. The default for these signals is the buffer being disabled, and the SPI1 port not connecting to the STAMP headers. Be aware that using the SPI1 port and its associated signals will disable the user LEDs (LED1-6) because the port and LEDs share the same pins on the processor. The jumper setting is shown in Table 2-26.

Table 2-26. SPI1 Enable Jumper (JP2)

JP2 Setting	Mode
OFF	**SPI1 port deactivated (default)**
ON	SPI1 port activated

Ethernet Speed Select Jumper (JP3)

The Ethernet speed select jumper (JP3) selects the speed of the LAN9218 Ethernet controller. No jumper is required by default. The default setting operates the LAN9218 (U14) in 100 Mbps mode and enables auto negotiation. When JP3 is populated, the controller operates in 10 Mbps mode with auto negotiation disabled. The jumper setting is shown in Table 2-27.

Table 2-27. Ethernet Speed Select Jumper (JP3)

JP3 Setting	Mode
OFF	**LAN9218 in 100 Mbps mode; auto negotiation ON (default)**
ON	LAN9218 in 10 Mbps mode; auto negotiation OFF

VDDINT Power Jumper (JP4)

The VDDINT power jumper (JP4) is used to measure the core voltage and current supplied to the processor core. By default JP4 is ON, and the power flows through the two-pin IDC header. To measure power, remove the jumper and measure the voltage across the 0.05 ohm resistor. Once the voltage is measured, the power can be calculated. For more information, refer to "Power Measurements" on page 1-33. The jumper setting is shown in Table 2-28.

Table 2-28. VDDINT Power Jumper (JP4)

JP4 Setting	Mode
ON	**No power measurement (default)**
OFF	For power measurement

VDDEXT Power Jumper (JP5)

The VDDEXT power jumper (JP5) is used to measure the processor's I/O voltage and current. By default JP5 is ON, and the power flows through the two-pin IDC header. To measure power, remove the jumper and measure the voltage across the 0.05 ohm resistor. Once the voltage is measured, the power can be calculated. For more information, refer to "Power Measurements" on page 1-33. The jumper setting is shown in Table 2-29.

Table 2-29. VDDINT Power Jumper (JP5)

JP5 Setting	Mode
ON	**No power measurement (default)**
OFF	For power measurement

VDDDDR Power Jumper (JP6)

The VDDDDR power jumper (JP6) is used to measure the voltage and current supplied to the DDR interface of the processor. By default JP6 is ON, and the power flows through the two-pin IDC header. To measure power, remove the jumper and measure the voltage across the 0.05 ohm resistor. Once the voltage is measured, the power can be calculated. For more information, refer to "Power Measurements" on page 1-33. The jumper setting is shown in Table 2-30.

Table 2-30. VDDDDR Power Jumper (JP6)

JP6 Setting	Mode
ON	**No power measurement (default)**
OFF	For power measurement

MOSI1 Out Jumper (JP7)

The MOSI out jumper (JP7) connects the PG10/MOSI1 pin of the processor to the STAMP headers. To flow data from the processor to the STAMP headers, connect the jumper. To flow data from the STAMP headers to the processor, do not populate the header but the JP8 jumper. Be aware that using the SPI1 port and its associated signals will disable the user LEDs (LED1-6) because the port and LEDs share the same pins on the processor. The jumper setting is shown in Table 2-31.

Table 2-31. MOSI1 Out Jumper (JP7)

JP7 Setting	Mode
OFF	**No connection between the MOSI1 of the processor to the STAMP headers (default)**
ON	MOSI1 of the processor transmitting data to the STAMP headers

MOSI1 In Jumper (JP8)

The MOSI in jumper (JP8) connect the PG10/MOSI1 pin of the processor to the STAMP headers. To flow data to the processor from the STAMP headers, connect the jumper. To flow data to the STAMP headers from the processor, do not populate the header but the JP7 jumper. Be aware that using the SPI1 port and its associated signals disable the user LEDs (LED1-6) because the port and LEDs share the same pins on the processor. The jumper setting is shown in Table 2-32.

Table 2-32. MOSI1 In Jumper (JP8)

JP8 Setting	Mode
OFF	**No connection between the MOSI1 of the processor to the STAMP headers (default)**
ON	MOSI1 of the processor receiving data from the STAMP headers

USB OTG Power Jumper (JP11)

The USB on-the-go (OTG) power jumper (JP11) connects the supply voltage for the USB OTG interface to the supply voltage of the USB interface of the processor. JP11 should always be populated. The jumper setting is shown in Table 2-33.

Table 2-33. USB OTG Power Jumper (JP11)

USB Power for	JP11 Pins 1 and 3	JP11 Pins 2 and 4
ADSP-BF548 processor	ON	ON

PPI1FS3 Pull-down Jumper (JP12)

The PPI1FS3 pull-down jumper (JP12) connects the PPI1FS3 signal of the processor to GND via a pull-down resistor. The jumper should be used when the processor pin is being used for EPPI, and the PPIIFS3 pin is not used. The pull-down assures that the PPI1FS3 signal is not floating and is used for certain modes of the EPPI interface, in which the signal needs to be low. Be aware that installing this jumper while using the serial port (J6) will cause data communication errors on the UART1. By default JP12 is not populated. The jumper setting is shown in Table 2-34.

Table 2-34. PPI1FS3 Pull-down Jumper (JP12)

JP12 Setting	Mode
OFF	**No pull-down resistor to GND on PPIFS3/UART1_TX; Using the serial port J6 (default)**
ON	Pull-down resistor connected to GND on PPIFS3/UART1_TX; Not using the serial port J6

LEDs

This section describes the on-board LEDs. Figure 2-4 shows the LED locations.

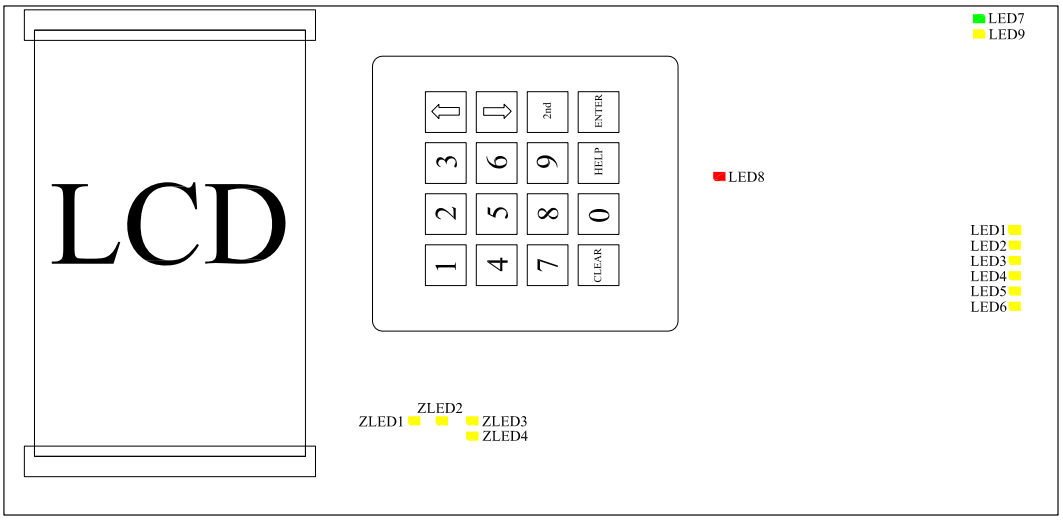


Figure 2-4. LED Locations

User LEDs (LED1–6)

Six LEDs connect to six general-purpose I/O pins of the processor (see Table 2-35). The LEDs are active high and are lit by writing a `1` to the correct `PG` signal.

Table 2-35. User LEDs

LED Reference Designator	Processor Programmable Flag Pin
LED1	PG6
LED2	PG7
LED3	PG8

Table 2-35. User LEDs (Cont'd)

LED Reference Designator	Processor Programmable Flag Pin
LED4	PG9
LED5	PG10
LED6	PG11

Power LED (LED7)

When LED7 is lit (green), it indicates that power is being properly supplied to the board.

Reset LED (LED8)

When LED8 is lit, it indicates that the master reset of all the major ICs is active. The reset LED is controlled by the Analog Devices ADM708 supervisory reset circuit. You can assert the reset push button (SW9) to assert the master reset and to activate LED8. For more information, see "Reset Push Button (SW9)" on page 2-20.

Ethernet Link/Activity LED (LED9)

When LED9 is lit solid, it indicates that the SMSC LAN9218 (U14) chip detects a valid link. When transmit or receive activity is sensed, LED9 flashes as an activity indicator. For more information on the LED, refer to the LAN9218 data sheet provided by the product manufacturer.

Connectors

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in Figure 2-5.

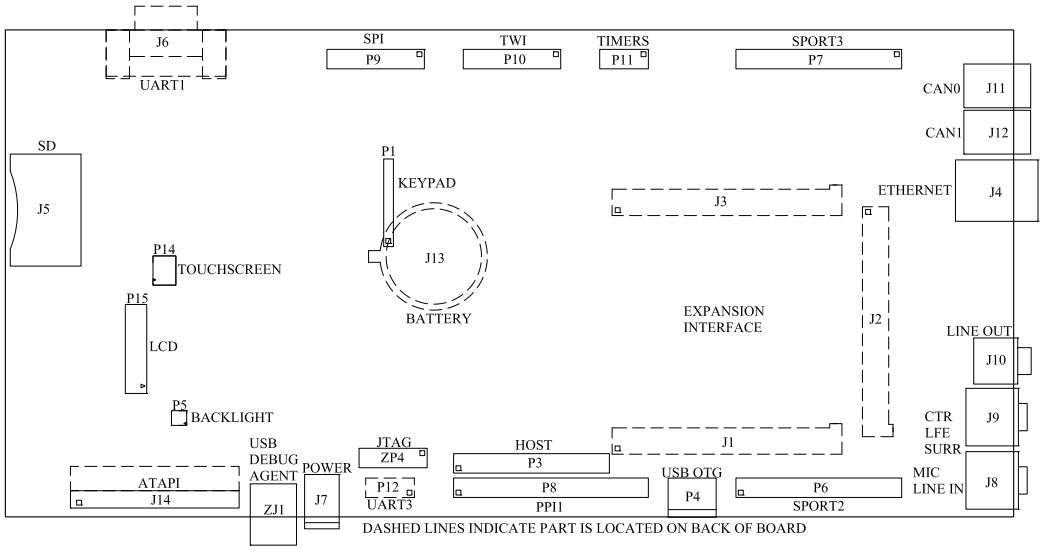


Figure 2-5. Connector Locations

Expansion Interface Connectors (J1–3)

Three board-to-board connector footprints provide signals for most of the processor's peripheral interfaces. The connectors are located at the bottom of the board. For more information, see "Expansion Interface" on page 1-32. For availability and pricing of the `J1-3` connectors, contact Samtec.

Part Description	Manufacturer	Part Number
90-position 0.05" spacing, SMT	SAMTEC	SFC-145-T2-F-D-A
Mating Connector		
90-position 0.05" spacing (through hole)	SAMTEC	TFM-145-x1 series
90-position 0.05" spacing (surface mount)	SAMTEC	TFM-145-x2 series
90-position 0.05" spacing (low cost)	SAMTEC	TFC-145 series

Ethernet Connector (J4)

Part Description	Manufacturer	Part Number
RJ-45 Ethernet jack	STEWART	SS-6488-NF
Mating Cable (shipped with EZ-KIT Lite)		
Cat 5E patch cable	RANDOM	PC10/100T-007
Cat 5E crossover cable	RANDOM	PC10/100TC-007
Mating Connector (shipped with EZ-KIT Lite)		
RJ-45 loopback connector	RANDOM	RAN830

SD Memory Card Connector (J5)

Part Description	Manufacturer	Part Number
SD 9-pin connector	ITT CANON	CCM05-5777LFT T50
Mating Memory Card (shipped with EZ-KIT Lite)		
256 MB	SanDISK	SDSDB-256-A10

RS-232 Connector (J6)

Part Description	Manufacturer	Part Number
DB9, female, right angle mount	TYCO	5747844-4
Mating Cable		
2m female-to-female cable	DIGI-KEY	AE1020-ND

Power Connector (J7)

The power connector provides all of the power necessary to operate the EZ-KIT Lite board.

Part Description	Manufacturer	Part Number
2.5 mm power jack	SWITCHCRAFT	RAPC712X
Mating Power Supply (shipped with EZ-KIT Lite)		
7.5VDC@4A power supply	CUI INC	DTS075400UDC-P6P-DB

Dual Audio Connectors (J8 and J9)

Part Description	Manufacturer	Part Number
3.5 mm dual stereo jack	SWITCHCRAFT	35RAPC7JS
Mating Cable (shipped with EZ-KIT Lite)		
3.5mm male/male 6’ cable	RANDOM	10A3-01106
Mating Headphone (shipped with EZ-KIT Lite)		
3.5 mm stereo headphones	KOSS	151225 UR5

Audio Connector (J10)

Part Description	Manufacturer	Part Number
3.5 mm stereo jack	SWITCHCRAFT	RAPC712X
Mating Cable (shipped with EZ-KIT Lite)		
3.5mm male/male 6’ cable	RANDOM	10A3-01106
Mating Headphone (shipped with EZ-KIT Lite)		
3.5 mm stereo headphones	KOSS	151225 UR5

CAN Connectors (J11 and J12)

Part Description	Manufacturer	Part Number
RJ11 4-pin modular jack	TYCO	5558872-1
Mating Cable		
4-conductor modular jack cable	L-COM	TSP3044
Mating Loopback Cable (shipped with EZ-KIT Lite)		
4-conductor modular jack cable	RANDOM	RAN290

Battery Holder (J13)

Part Description	Manufacturer	Part Number
24 mm battery holder	KEYSTONE	1025-7
Mating Battery (shipped with EZ-KIT Lite)		
3V 1000MAH 24 mm LI-COIN	PANASONIC	CR2477

ATAPI Connector (J14)

Part Description	Manufacturer	Part Number
ATAPI 44-pin 22 x 2 mm	SAMTEC	ASP-130199-02
Mating Hard Drive (shipped with EZ-KIT Lite)		
5V ATAPI hard disk drive	TOSHIBA	MK4032GAX

Keypad Connector (P1)

Part Description	Manufacturer	Part Number
IDC header female	SAMTEC	SSW-109-01-TM-S
Mating Keypad (shipped with EZ-KIT Lite)		
4 x 4 keypad	ACT COMPONENTS	ACT-07-30008-000-R

Host Interface Connector (P3)

The pinout of the P3 connector can be found in "ADSP-BF548 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	SAMTEC	TSW-116-26-T-D
Mating Connector		
IDC socket	SAMTEC	TSW-116-01-T-D

USB OTG Connector (P4)

The pinout of the P4 connector can be found in "ADSP-BF548 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
USB 5-pin mini AB	MOLEX	56579-0576
Mating Cables (shipped with EZ-KIT Lite)		
5-in-1 USB 2.0 cable	JO-DAN INTERNAT	GXQU-06

LCD Backlight Connector (P5)

Part Description	Manufacturer	Part Number
FPC 4-pin 0.5 mm	KYOCERA ELCO	046298004000883+
Mating LCD Display Module (shipped with EZ-KIT Lite)		
4" TFT LCD with touchscreen	SHARP	LQ043T1DG01

SPORT2 Connector (P6)

The pinout of the P6 connector can be found in "ADSP-BF548 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-434HLF
Mating Connector		
IDC socket	DIGI-KEY	S4217-ND

SPORT3 Connector (P7)

The pinout of the P7 connector can be found in "ADSP-BF548 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-434HLF
Mating Connector		
IDC socket	DIGI-KEY	S4217-ND

PPI1 Connector (P8)

The pinout of the P8 connector can be found in "ADSP-BF548 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-440HLF
Mating Connector		
IDC socket	DIGI-KEY	S4220-ND

SPI Connector (P9)

The pinout of the P9 connector can be found in "ADSP-BF548 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-420HLF
Mating Connector		
IDC socket	DIGI-KEY	S4210-ND

Two-Wire Interface Connector (P10)

The pinout of the P10 connector can be found in "ADSP-BF548 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-420HLF
Mating Connector		
IDC socket	DIGI-KEY	S4210-ND

TIMERS Connector (P11)

The pinout of the P11 connector can be found in "ADSP-BF548 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-410HLF
Mating Connector		
IDC socket	DIGI-KEY	S4205-ND

UART3 Connector (P12)

The pinout of the P12 connector can be found in "ADSP-BF548 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-410HLF
Mating Connector		
IDC socket	DIGI-KEY	S4205-ND

LCD Touchscreen Connector (P14)

Part Description	Manufacturer	Part Number
FPC 4-pin 1mm	JST	04FMS-1.0SP-TF(LF)(SN)
Mating LCD Display Module (shipped with EZ-KIT Lite)		
4" TFT LCD with touchscreen	SHARP	LQ043T1DG01

LCD Data Connector (P15)

Part Description	Manufacturer	Part Number
FPC 40-pin 0.5mm	HIROSE	FH12-40S-0.5SH(55)
Mating LCD Display Module (shipped with EZ-KIT Lite)		
4" TFT LCD with touchscreen	SHARP	LQ043T1DG01

USB Debug Agent Connector (ZJ1)

The USB debug agent connector is the connecting point for the JTAG USB debug agent interface. The JTAG header (ZP4) should not be used whenever ZJ1 and its mating cable are used to communicate to the processor via CCES or VisualDSP++.

JTAG Connector (ZP4)

The JTAG header is the connecting point for a JTAG in-circuit emulator pod. When an emulator connects to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

A ADSP-BF548 EZ-KIT LITE BILL OF MATERIALS

The bill of materials corresponds to "ADSP-BF548 EZ-KIT Lite Schematic" on page B-1.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	2	74LVC14A SOIC14	U10,U30	TI	74LVC14AD
2	1	IDT74FCT3244 APY SSOP20	U29	IDT	IDT74FCT3244APYG
3	1	24.576MHZ OSC005	Y1	EPSON	MA-505 24.5760M-C3:ROHS
4	1	25MHZ OSC005	Y3	EPSON	MA-505 25.0000 MHZ
5	1	32.768KHZ OSC008	Y2	EPSON	MC-156-32.7680KA-A0:ROHS
6	1	25MHZ OSC003	U7	EPSON	SG-8002CA MP
7	2	SN74LVC1G08 SOT23-5	U25,U31	TI	SN74LVC1G08DBVR
8	2	TJA1041 SOIC14	U21,U33	PHILIPS	TJA1041T
9	1	FDS9431A SOIC8	U28	FAIRCHILD	FDS9431A
10	1	NAND02 TSOP48	U3	ST MICRO	NAND02GW3B2CN6E
11	1	27MHZ OSC003	U19	EPSON	SG-8002CA-MP

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
12	2	FDS9926A SOIC8	U22-23	MOUSER	512-FDS9926A
13	1	SI4411DY SO-8	U16	VISHAY	Si4411DY-T1-E3
14	1	HX1188 ICS007	U15	DIGI-KEY	553-1340-ND
15	1	LAN9218 TQFP100	U14	SMSC	LAN9218-MT
16	1	24MHZ OSC003	U13	EPSON	SG-8002CA-MP
17	1	MT46V32M16 TSOP66	U1	MICRON	MT46V32M16P-5B:F
18	1	BF548 PC28F128P33 “U5”	U5	INTEL	PC28F128P33T85
19	1	SN74LVC1G02 SOT23-5	U35	DIGI-KEY	296-11597-1-ND
20	2	SN74CB3Q162 11 TSSOP56	U37-38	DIGI-KEY	296-17629-1-ND
21	1	SN74CB3Q324 5 TSSOP20	U36	DIGI-KEY	296-19130-1-ND
22	1	MIC2025-1 SOIC8	U39	DIGI-KEY	576-1057-ND
23	1	93LC46A SOIC8	U12	MICRO-CHIP	93LC46A-E/SN
24	1	BF548 M25P16 “U6”	U6	ST MICRO	M25P16-VMW6G
25	1	74CBTLV3244 TSSOP20	U26	IDT	IDT74CBTLV3244PGG
26	2	SN74CB3T1621 0 TSSOP48	U4,U24	DIGI-KEY	296-19147-1-ND
27	1	ADM708SARZ SOIC8	U27	ANALOG DEVICES	ADM708SARZ

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
28	3	ADP3336ARMZ MSOP8	VR1-2,VR5	ANALOG DEVICES	ADP3336ARMZ-REEL7
29	1	ADG752BRTZ SOT23-6	U20	ANALOG DEVICES	ADG752BRTZ-REEL
30	1	ADM3202ARN Z SOIC16	U32	ANALOG DEVICES	ADM3202ARNZ
31	1	ADSP-BF548 MBGA400	U2	ANALOG DEVICES	ADSP-BF548BBCZ-5X
32	1	ADP1864AUJZ SOT23-6	VR3	ANALOG DEVICES	ADP1864AUJZ-R7
33	1	ADP1823 LFCSP32	VR7	ANALOG DEVICES	ADP1823ACPZ-R7
34	1	AD7877 LFCSP32	U9	ANALOG DEVICES	AD7877ACPZ-500RL7
35	1	AD1980 LQFP48	U11	ANALOG DEVICES	AD1980JSTZ
36	1	ADP1611 MSOP8	VR8	ANALOG DEVICES	ADP1611ARMZ-R7
37	1	ADP1715 MSOP8	VR4	ANALOG DEVICES	ADP1715ARMZ-R7
38	1	PWR 2.5MM_JACK CON005	J7	SWITCH-CRAFT	RAPC712X
39	3	.05 45X2 CON019	J1-3	SAMTEC	SFC-145-T2-F-D-A
40	1	DIP8 SWT016	SW2	C&K	TDA08H0SB1
41	1	DIP6 SWT017	SW8	CTS	218-6LPST
42	8	DIP4 SWT018	SW4-7,SW14-17	ITT	TDA04HOSB1
43	1	DB9 9PIN DB9F	J6	TYCO	5747844-4

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
44	2	RJ11 4PIN CON039	J11-12	TYCO	5558872-1
45	7	IDC 2X1 IDC2X1	JP2-8	FCI	90726-402HLF
46	2	IDC 2X1 IDC2X1	JP1,JP12	FCI	90726-402HLF
47	2	IDC 5X2 IDC5X2	P11-12	FCI	68737-410HLF
48	2	IDC 10X2 IDC10X2	P9-10	BURG-FCI	54102-T08-10LF
49	2	IDC 17X2 IDC17X2	P6-7	BURG-FCI	54102-T08-17LF
50	1	IDC 20X2 IDC20X2	P8	BURG-FCI	54102-T08-20LF
51	1	IDC 2X2 IDC2X2	JP11	FCI	68737-404HLF
52	1	3.5MM STEREO_JACK CON001	J10	DIGI-KEY	CP1-3525NG-ND
53	1	5A RESE-TABLE FUS005	F1	MOUSER	650-RGEF500
54	1	ROTARY SWT023	SW1	DIGI-KEY	563-1047-ND
55	1	ROTARY_ENC ODER SWT022	SW3	CTS	290UAB0R201B2
56	2	3.5MM DUAL_STERE O CON050	J8-9	SWITCH-CRAFT	35RAPC7JS
57	1	SD_CONN 9PIN CON051	J5	DIGI-KEY	401-1954-ND
58	1	IDC 16x2 IDC16x2	P3	SAMTEC	TSW-116-26-T-D

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
59	1	USB_MINI-AB 5PIN CON052	P4	MOLEX	56579-0576
60	1	BATT_HOLDER 24MM CON054	J13	KEYSTONE	1025-7
61	1	RJ45 8PIN CON_RJ45_12P	J4	DIGI-KEY	380-1022-ND
62	1	ATAPI44 44PIN 22x2_2MM	J14	SAMTEC	ASP-130199-02
63	5	MOMENTARY SWT024	SW9-13	PANA-SONIC	EVQ-Q2K03W
64	1	FPC 40PIN CON057	P15	HIROSE	FH12-40S-0.5SH(55)
65	1	FPC 4PIN CON060	P5	KYOCERA ELCO	046298004000883+
66	1	FPC 4PIN CON061	P14	JST	04FMS-1.0SP-TF(LF)(SN)
67	1	IDC 9X1 IDC9X1	P1	SAMTEC	SSW-109-01-TM-S
68	1	0 1/4W 5% 1206	R76	KOA	0.0ECTRk7372BTTED
69	7	YELLOW LED001	LED1-6,LED9	PANA-SONIC	LN1461C
70	3	22PF 50V 5% 0805	C115-116,C225	AVX	08055A220JAT
71	4	0.1UF 50V 10% 0805	C30-32,C266	AVX	08055C104KAT
72	1	1M 1/10W 5% 0805	R78	VISHAY	CRCW08051M00JNEA
73	7	100 1/10W 5% 0805	R34-36,R100-101, R103,R138	VISHAY	CRCW0805100RJNEA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
74	11	600 100MHZ 200MA 0603	FER1-10,FER20	DIGI-KEY	490-1014-2-ND
75	5	600 100MHZ 500MA 1206	FER11-12,FER15-17	STEWARD	HZ1206B601R-10
76	7	1UF 16V 10% 0805	C129,C139,C203-205,C278-279	KEMET	C0805C105K4RAC TU
77	2	30PF 100V 5% 1206	C143-144	AVX	12061A300JAT2A
78	1	10UH 20% IND001	L1	TDK	445-2014-1-ND
79	4	0 1/10W 5% 0805	R147,R216,R227, R259	VISHAY	CRCW08050000Z0EA
80	1	190 100MHZ 5A FER002	FER19	MURATA	DLW5BSN191SQ2
81	2	1A ZHCS1000 SOT23-312	D5,D21	ZETEX	ZHCS1000TA pb-free
82	6	22 125MW 5% RNS001	RN11-16	CTS	744C083220JP
83	4	1UF 10V 10% 0805	C210,C220-222	AVX	0805ZC105KAT2A
84	20	10UF 6.3V 10% 0805	C9,C26,C49,C60, C67,C74,C84,C122-123,C149,C152, C167,C206,C208, C232-233,C235-237, C255	AVX	08056D106KAT2A
85	5	4.7UF 6.3V 10% 0805	C138,C140,C198, C202,C209	AVX	08056D475KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
86	38	0.1UF 10V 10% 0402	C1-2,C25,C27,C96, C109,C114,C119-121,C124-125,C132, C134,C142,C153-166,C175,C177-179, C240,C256,C275-277	AVX	0402ZD104KAT2A
87	104	0.01UF 16V 10% 0402	C3-8,C10-19,C23-24,C33-48,C50-59, C61-66,C68-73,C75-83,C85-92,C112-113,C130-131,C136-137,C141,C148, C150-151,C170-171, C180,C184-186, C188,C192,C195-197,C211,C229-230, C243-244,C249-250, C257-259	AVX	0402YC103KAT2A
88	64	10K 1/16W 5% 0402	R8-13,R16-19,R26, R29,R55-56,R60, R77,R95,R108-111, R120-123,R131-133, R148,R158,R161-163,R166,R168, R171,R173,R178, R182,R187,R198, R200-203,R206, R209,R213-214, R222-225,R229-230, R248-249,R254, R257,R273-275, R282,R284	VISHAY	CRCW040210K0FKED
89	9	4.7K 1/16W 5% 0402	R43,R45-49,R65, R143,R212	VISHAY	CRCW04024K70JNED

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
90	32	0 1/16W 5% 0402	R20,R30,R57-59, R61,R146,R149, R172,R174-177, R205,R207,R210-211,R215,R232-243, R278-279	PANA-SONIC	ERJ-2GE0R00X
91	4	1.2K 1/16W 5% 0402	R139-140,R276-277	PANA-SONIC	ERJ-2GEJ122X
92	7	22 1/16W 5% 0402	R151-154,R169-170, R283	PANA-SONIC	ERJ-2GEJ220X
93	20	33 1/16W 5% 0402	R7,R14,R21,R27-28, R66,R244-247,R250-253,R255,R268-272	VISHAY	CRCW040233R0JNEA
94	2	18PF 50V 5% 0805	C28-29	AVX	08055A180JAT2A
95	6	100UF 10V 10% C	CT1-3,CT5,CT8-9	AVX	TPSC107K010R0075
96	2	64.9K 1/10W 1% 0805	R69,R165	VISHAY	CRCW080564K9FKEA
97	2	210.0K 1/4W 1% 0805	R68,R164	VISHAY	CRCW0805210KFKEA
98	1	0.022UF 50V 5% 0805	C145	AVX	08055C223JAT2A
99	10	49.9 1/10W 1% 0805	R83-92	DIGI-KEY	311-49.9CRCT-ND
100	6	0.1UF 16V 10%0603	C189,C260,C264-265,C272,C274	AVX	0603YC104KAT2A
101	9	1UF 16V 10% 0603	C94,C103-104,C118, C187,C215-216, C241-242	PANA-SONIC	ECJ-1VB1C105K
102	1	4.7UF 25V 20% 0805	C102	AVX	0805ZD475KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
103	1	68PF 50V 5% 0603	C200	AVX	06035A680JAT2A
104	11	470PF 50V 5% 0603	C93,C97-101,C105-106,C110-111,C199	AVX	06033A471JAT2A
105	1	220UF 6.3V 20% D2E	CT4	SANYO	10TPE220ML
106	3	10K 1/10W 5% 0603	R99,R263-264	VISHAY	CRCW060310K0JNEA
107	1	10M 1/10W 5% 0603	R15	VISHAY	CRCW060310M0FNEA
108	3	100K 1/10W 5% 0603	R188-189,R261	VISHAY	CRCW0603100KJNEA
109	9	330 1/10W 5% 0603	R119,R124-130, R141	VISHAY	CRCW0603330RJNEA
110	1	1M 1/10W 5% 0603	R67	VISHAY	CRCW06031M00FNEA
111	2	0 1/10W 5% 0603	R73,R156	PHYCOMP	232270296001L
112	8	10 1/10W 5% 0603	R102,R104,R134-137,R218,R220	VISHAY	CRCW060310R0JNEA
113	2	75.0K 1/16W 1% 0603	R71,R179	VISHAY	CRCW060375K0FKEA
114	2	1K 1/10W 5% 0603	R37,R42	DIGI-KEY	311-1.0KGRTR-ND
115	3	4700PF 16V 10% 0603	C168,C218,C226	DIGI-KEY	311-1083-2-ND
116	4	100PF 50V 5% 0603	C169,C172, C227-228	AVX	06035A101JAT2A
117	1	12.4K 1/10W 1% 0603	R80	DIGI-KEY	311-12.4KHRTR-ND
118	4	62.0 1/10W 1% 0603	R105-106,R219, R221	DIGI-KEY	311-62.0HRTR-ND

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
119	1	680PF 50V 5% 0603	C231	PANA-SONIC	ECJ-1VC1H681J
120	2	75.0 1/10W 1% 0603	R93-94	DALE	CRCW060375R0FKEA
121	2	270PF 50V 5% 0603	C95,C117	DIGI-KEY	311-1185-2-ND
122	2	1UF 6.3V 20% 0402	C107-108	PANA-SONIC	ECJ-0EB0J105M
123	3	100 1/16W 5% 0402	R1,R50-51	DIGI-KEY	311-100JRTR-ND
124	1	390PF 25V 5% 0603	C261	AVX	06033A391FAT2A
125	1	24.9K 1/10W 1% 0603	R155	DIGI-KEY	311-24.9KHTR-ND
126	6	1.05K 1/16W 1% 0603	R74-75,R81,R96-98	PANA-SONIC	ERJ-3EKF1051V
127	4	10UF 10V 10% 0805	C135,C193,C271, C273	PANA-SONIC	ECJ-2FB1A106K
128	1	20.0K 1/16W 1% 0603	R266	PANA-SONIC	ERJ-3EKF2002V
129	4	0.05 1/2W 1% 1206	R157,R192-194	SEI	CSF 1/2 0.05 1%R
130	3	10UF 16V 10% 1210	C201,C234,C238	AVX	1210YD106KAT2A
131	1	GREEN LED001	LED7	PANA-SONIC	LN1361CTR
132	1	RED LED001	LED8	PANA-SONIC	LN1261CTR
133	2	1000PF 50V 5% 1206	C190-191	AVX	12065A102JAT2A
134	1	255.0K 1/10W 1% 0603	R160	VISHAY	CRCW06032553FK

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
135	1	80.6K 1/10W 1% 0603	R159	DIGI-KEY	311-80.6KHRCT-ND
136	1	200MA BAT54A SOT23D	D12	MOUSER	512-BAT54A
137	2	200MA BAT54 SOT23D	D10-11	MOUSER	512-BAT54
138	1	8.2UH 20% IND012	L4	COILCRAFT	MSS6132-822ML
139	1	10UH 20% IND012	L3	COILCRAFT	MSS6132-103ML
140	2	1.1K 1/16W 1% 0402	R191,R208	PANA-SONIC	ERJ-2RKF1101X
141	1	18K 1/16W 5% 0402	R183	DIGI-KEY	311-18KJRCT-ND
142	1	820 1/16W 5% 0402	R184	DIGI-KEY	311-820JRCT-ND
143	1	12.0K 1/16W 1% 0402	R79	DIGI-KEY	311-12.0KLRCT-ND
144	1	430 1/16W 1% 0402	R180	DIGI-KEY	311-430LRCT-ND
145	1	1200PF 50V 10% 0402	C219	DIGI-KEY	490-1304-1-ND
146	1	82PF 50V 5% 0402	C217	DIGI-KEY	490-1290-1-ND
147	2	22000PF 25V 10% 0402	C223,C239	DIGI-KEY	490-3252-1-ND
148	1	1500PF 50V 10% 0402	C224	DIGI-KEY	490-3245-1-ND
149	3	5A MBRS540T3G SMC	D4,D13,D15	ON SEMI	MBRS540T3G

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
150	3	15KV PGB1010603 0603	D1,D8-9	LITTLE-FUSE	PGB1010603MR
151	1	VARISTOR V5.5MLA 30A 0603	R142	LITTLE-FUSE	V5.5MLA0603
152	1	THERM 0.5A 0.4 1206	R72	LITTLE-FUSE	1206L050-C
153	19	33 125MW 5% RNS001	RN1-10,RN17-25	CTS	744C083330JP
154	1	20MA MA3X717E DIO005	D16	PANA-SONIC	MA3X717E
155	2	100MA MA27D27 DIO006	D2,D7	PANA-SONIC	MA27D27
156	1	2A CZRF52C2V2 DIO007	D3	DIGI-KEY	641-1052-1-ND
157	1	2.5UH 30% IND013	L2	COILCRAFT	MSS1038-252NLB
158	4	47.0K 1/16W 1% 0402	R38-41	ROHM	MCR01MZPF4702
159	2	3.01K 1/16W 1% 0402	R52-53	ROHM	MCR01MZPF3011
160	1	5.6K 1/16W 5% 0402	R25	PANA-SONIC	ERJ-2GEJ562X
161	5	1.0K 1/16W 1% 0402	R2-3,R31-33	PANA-SONIC	ERJ-2RKF1001X
162	2	1000PF 2000V 10% 1206	C146-147	AVX	1206GC102KAT1A
163	3	82 1/16W 5% 0402	R4-6	ROHM	MCR01MZPJ820

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
164	1	1UF 50V 10% 0603	C267	DIGI-KEY	587-1257-1-ND
165	1	154.0K 1/16W 1% 0402	R70	DIGI-KEY	541-154KLCT-ND
166	1	10.0 1/10W 1% 0603	R82	DIGI-KEY	311-10.0HRTR-ND
167	3	10.0K 1/16W 1% 0402	R181,R185,R265	DIGI-KEY	541-10.0KLCT-ND
168	1	60.4 1/8W 1% 0805	R262	ROHM	MCR10EZPF60R4
169	1	15uH 20% IND015	L5	COILCRAFT	MSS4020-153ML
170	3	.5A B0540W SOD-123	D17-19	DIODES INC	B0540W-7-F
171	1	.5A BZT52C33S SOD-323	D20	DIODES INC	BZT52C33S-7-F
172	4	2.2UF 25V 10% 0805	C263,C268-270	DIGI-KEY	490-3331-1-ND
173	1	1.0 1/16W 1% 0402	R260	DIGI-KEY	541-1.00LCT-ND
174	1	34.0K 1/10W 1% 0603	R186	DIGI-KEY	541-34.0KHCT-ND

2

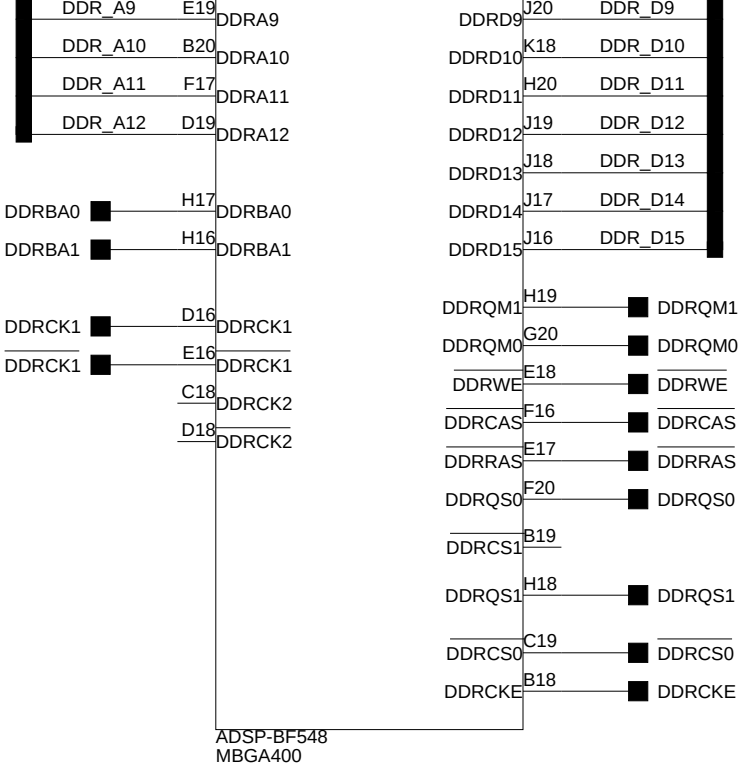
3

4

ADSP-I

A

B



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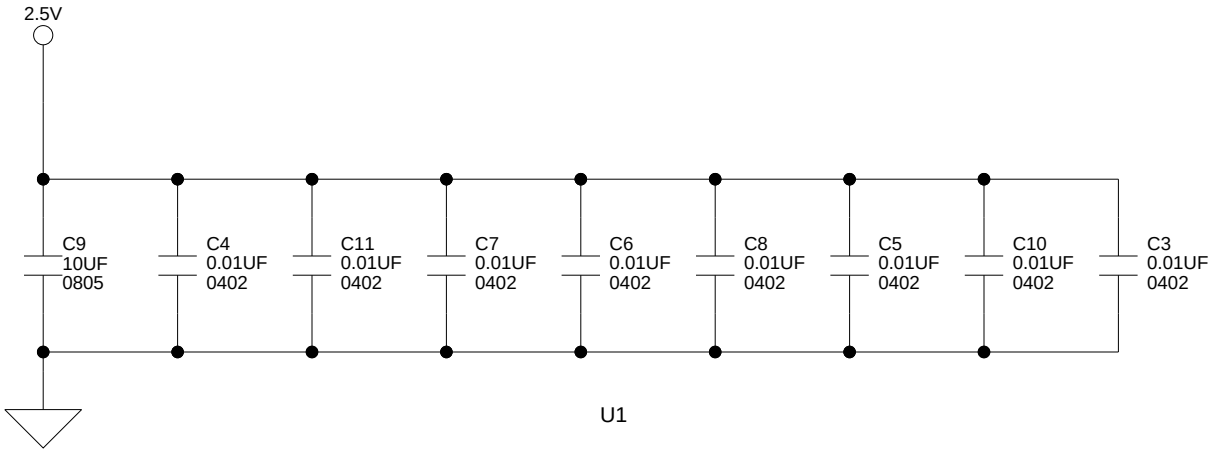


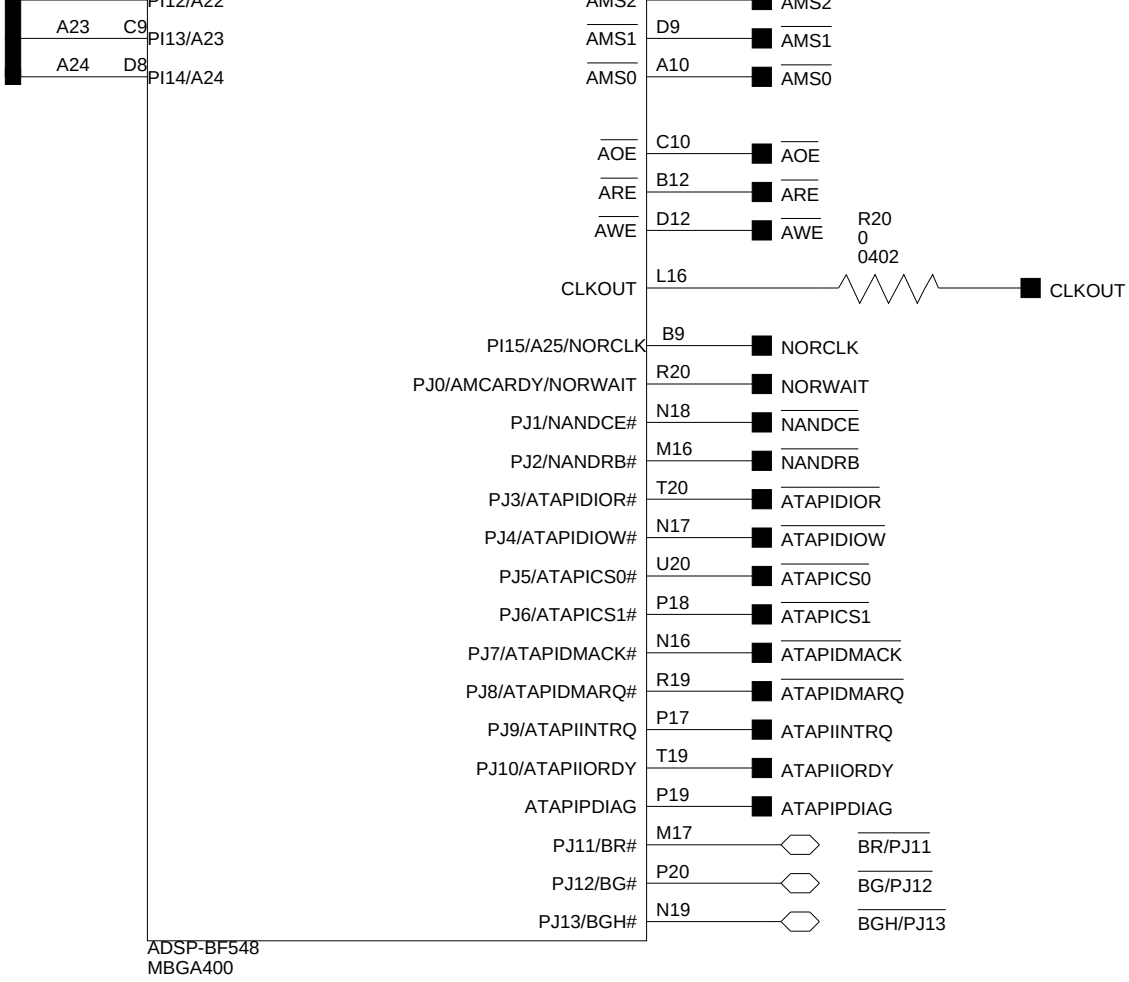
2

3

4

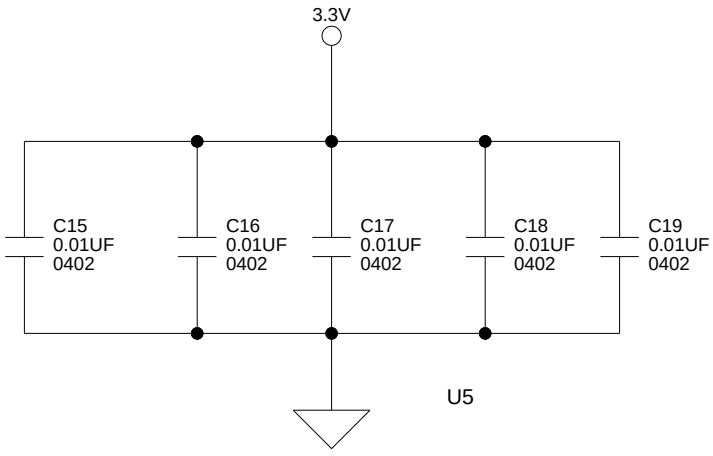
A

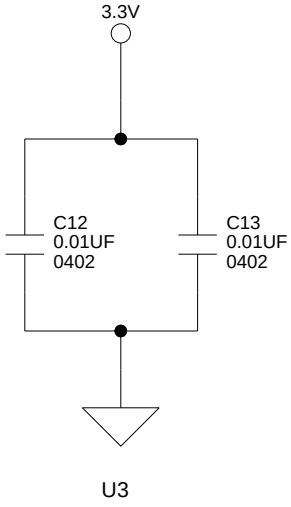
B

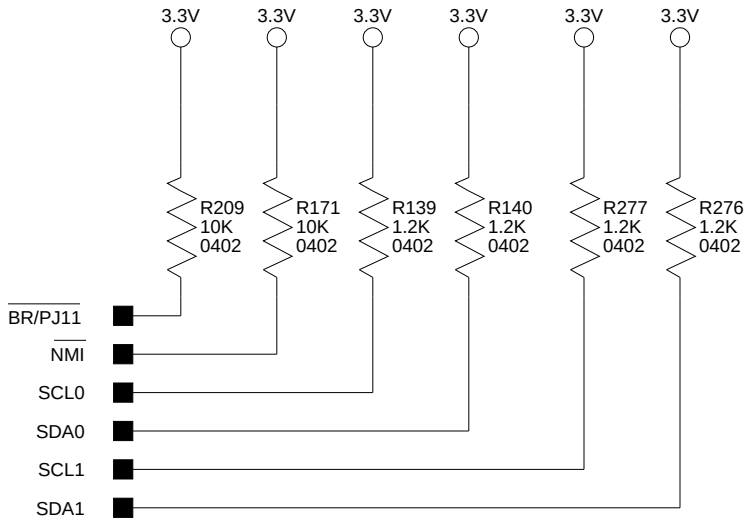


Memory Map

START	END	BANK	DEVICE
0x0000 0000	0x01FF FFFF	DDR Bank 0	64MB DDR
0x2000 0000	0x21FF FFFF	ASYNC Memory Bank 0	32MB BURST FLASH
0x2400 0000	0x2400 007F	ASYNC Memory Bank 1	ETHERNET
0x2800 0000	0x27FF FFFF	ASYNC Memory Bank 2	NOT USED
0x2C00 0000	0x2FFF FFFF	ASYNC Memory Bank 3	NOT USED



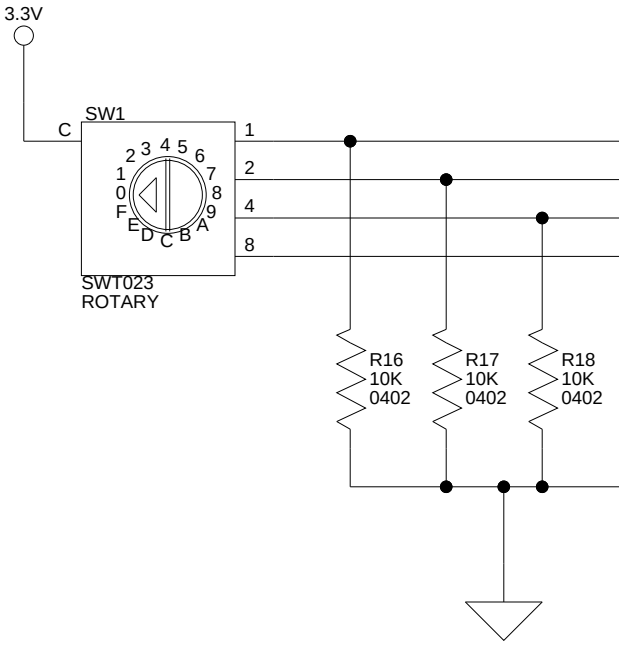


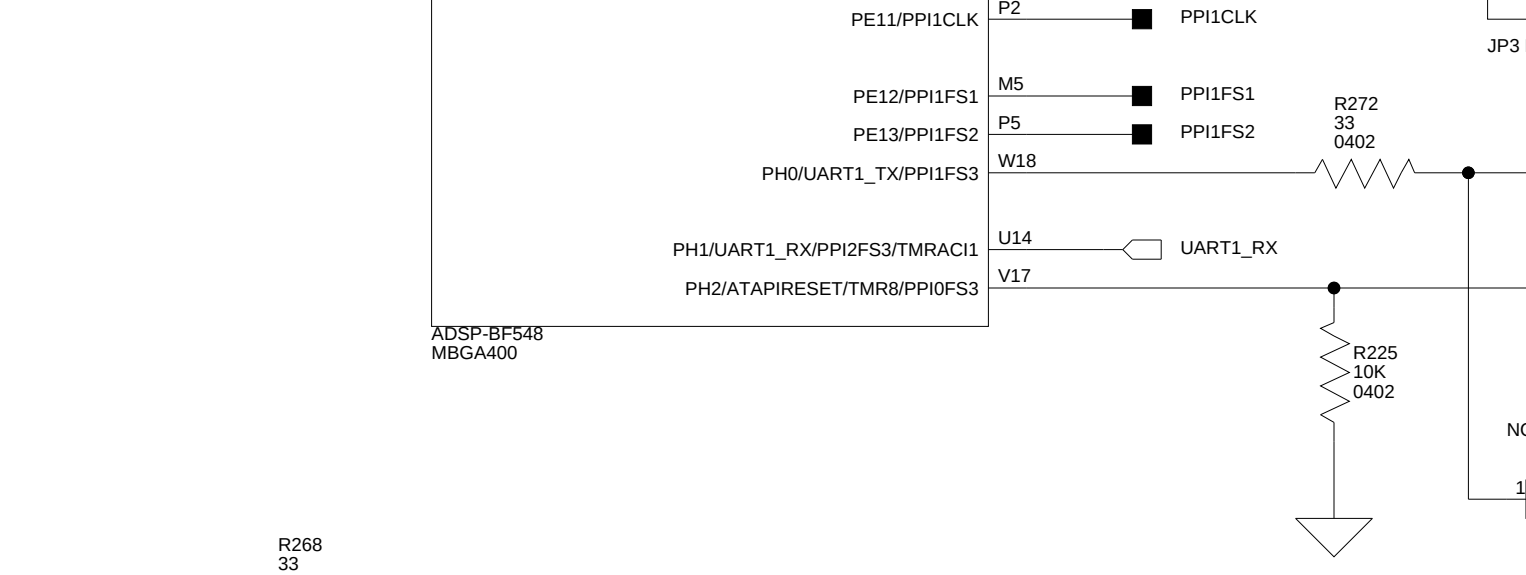


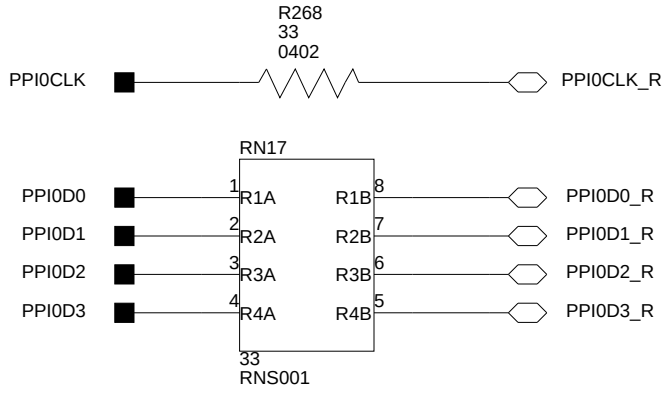
SW1: Boot Mode Select Switch

POSITION	BOOT MODE
0	Idle-no boot
1	Boot from 16-bit flash memory
2	Boot from 16-bit asynchronous FIFO
3	Boot from serial SPI memory
4	Boot from SPI host device
5	Boot from serial TWI memory
6	Boot from TWI host
7	Boot from UART host
8	Reserved
9	Reserved
A	Boot from DDR SDRAM
B	Reserved
C	Reserved
D	Reserved
E	Boot from16-bit Host DMA
F	Boot from 8-bit Host DMA

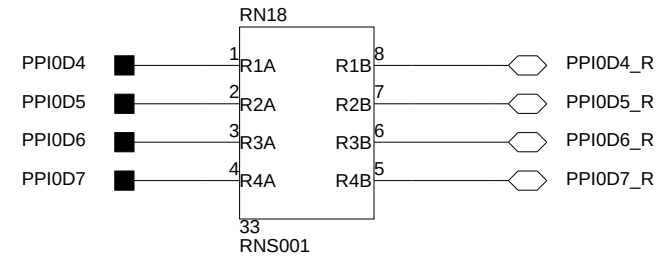
DEFAULT

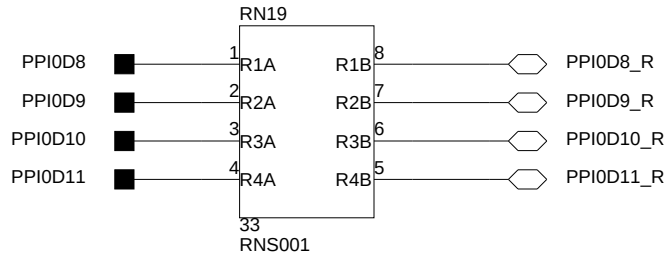


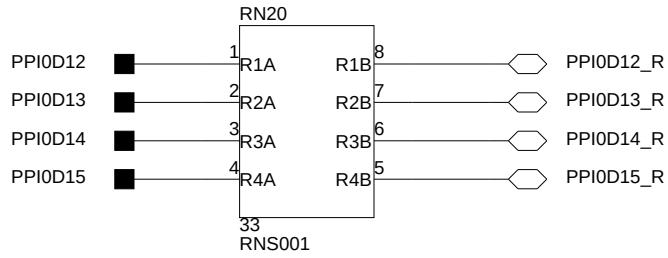

PE11/PPI1CLK
P2
PPI1CLK
PE12/PPI1FS1
M5
PPI1FS1
PE13/PPI1FS2
P5
PPI1FS2
PH0/UART1_TX/PPI1FS3
W18
R272
33
0402
PH1/UART1_RX/PPI2FS3/TMRACI1
U14
UART1_RX
PH2/ATAPIRESET/TMR8/PPI0FS3
V17
ADSP-BF548
MBGA400
R225
10K
0402
JP3

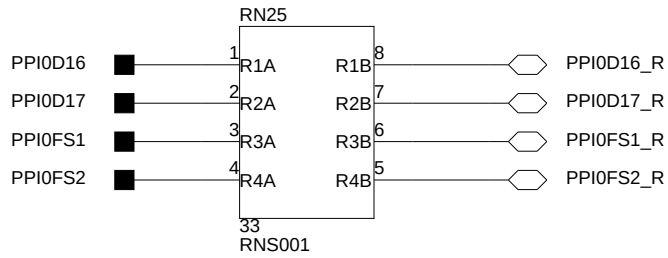

R268
33
0402
PPI0CLK
PPI0CLK_R

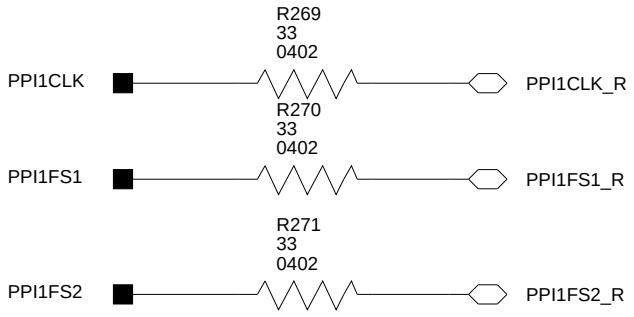
RN17
PPI0D0
PPI0D1
PPI0D2
PPI0D3
R1A
R2A
R3A
R4A
R1B
R2B
R3B
R4B
PPI0D0_R
PPI0D1_R
PPI0D2_R
PPI0D3_R
33
RNS001

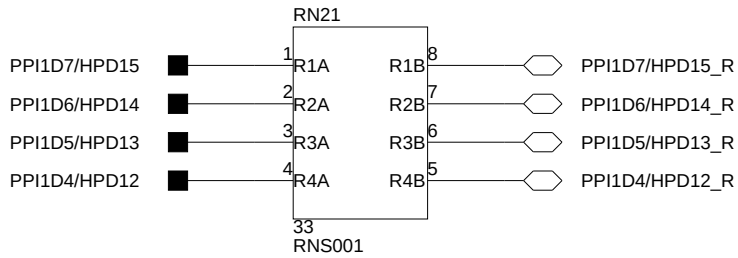

RN18
PPI0D4
PPI0D5
PPI0D6
PPI0D7
PPI0D4_R
PPI0D5_R
PPI0D6_R
PPI0D7_R
33
RNS001

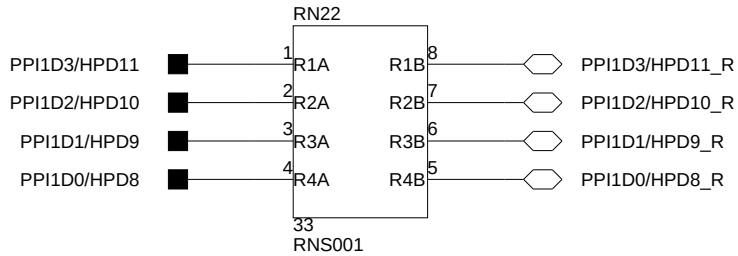

RN19
PPI0D8
PPI0D9
PPI0D10
PPI0D11
PPI0D8_R
PPI0D9_R
PPI0D10_R
PPI0D11_R
33
RNS001

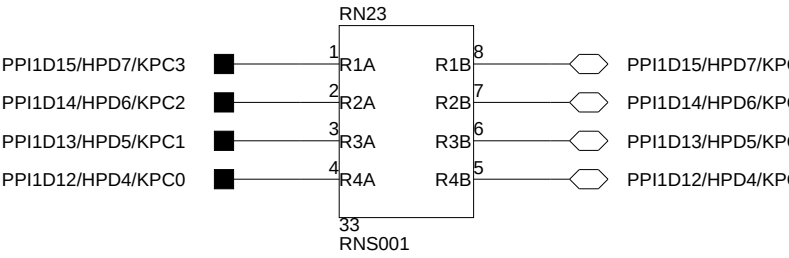

RN20
PPI0D12
PPI0D13
PPI0D14
PPI0D15
PPI0D12_R
PPI0D13_R
PPI0D14_R
PPI0D15_R
33
RNS001

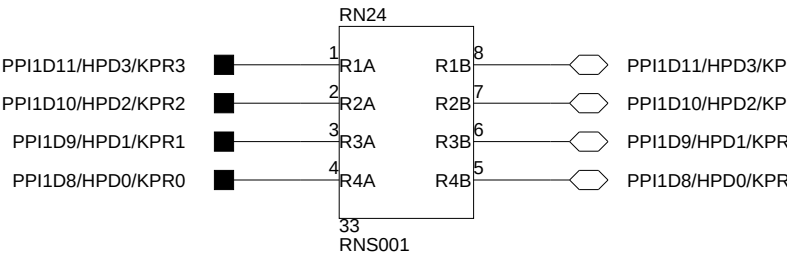

RN25
PPI0D16
PPI0D17
PPI0FS1
PPI0FS2
PPI0D16_R
PPI0D17_R
PPI0FS1_R
PPI0FS2_R
33
RNS001

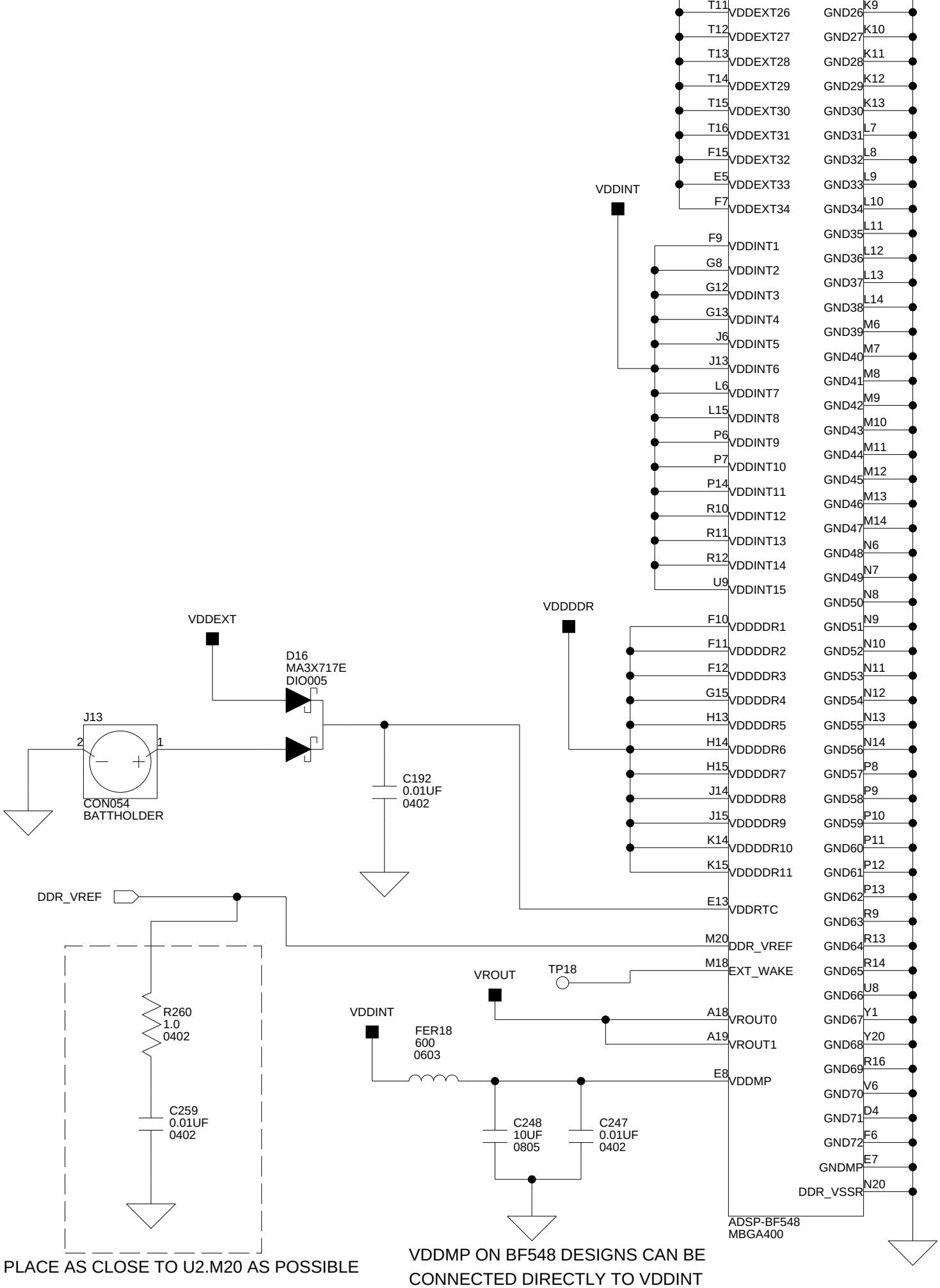

R269
33
0402
PPI1CLK
PPI1CLK_R
R270
33
0402
PPI1FS1
PPI1FS1_R
R271
33
0402
PPI1FS2
PPI1FS2_R

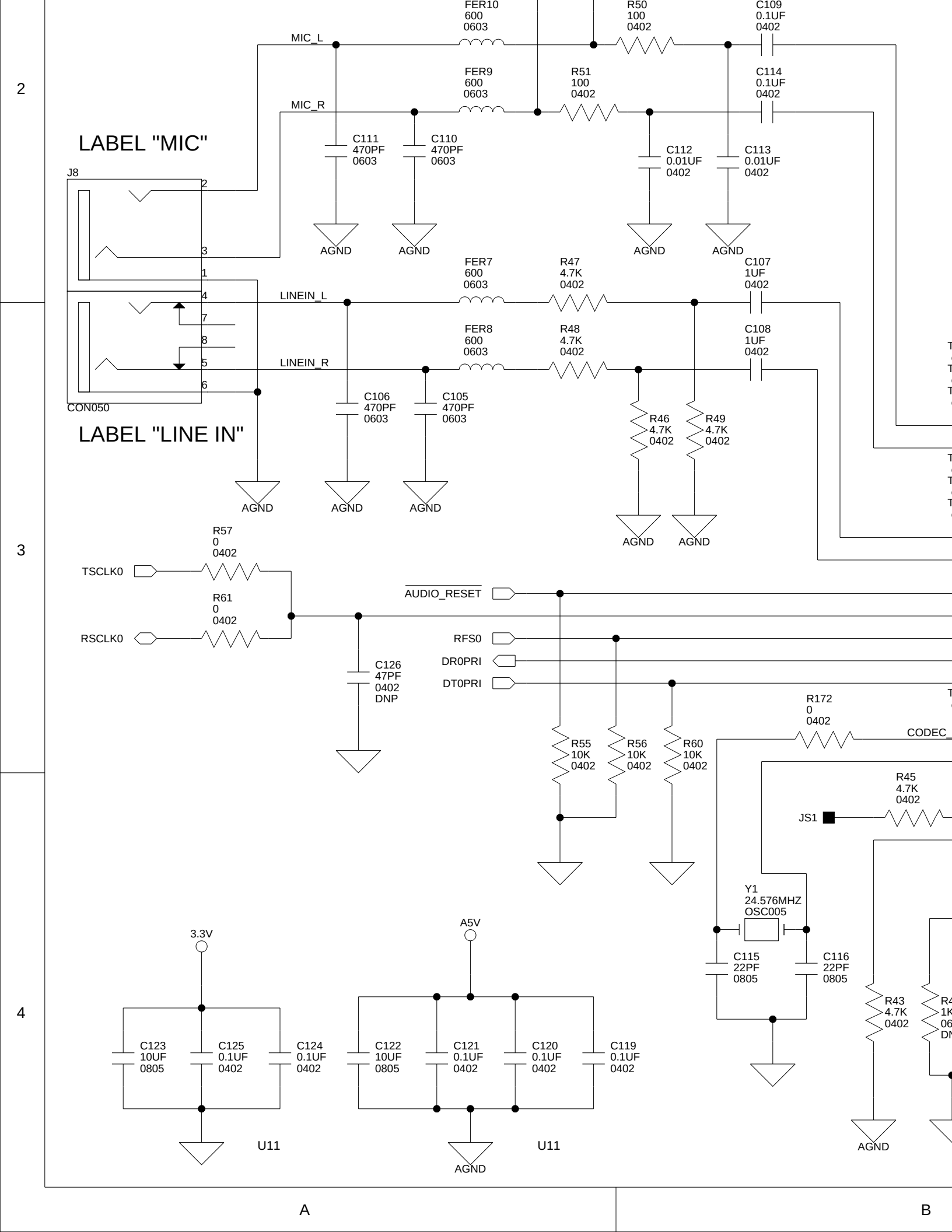

RN21
PPI1D7/HPD15
PPI1D6/HPD14
PPI1D5/HPD13
PPI1D4/HPD12
PPI1D7/HPD15_R
PPI1D6/HPD14_R
PPI1D5/HPD13_R
PPI1D4/HPD12_R
33
RNS001

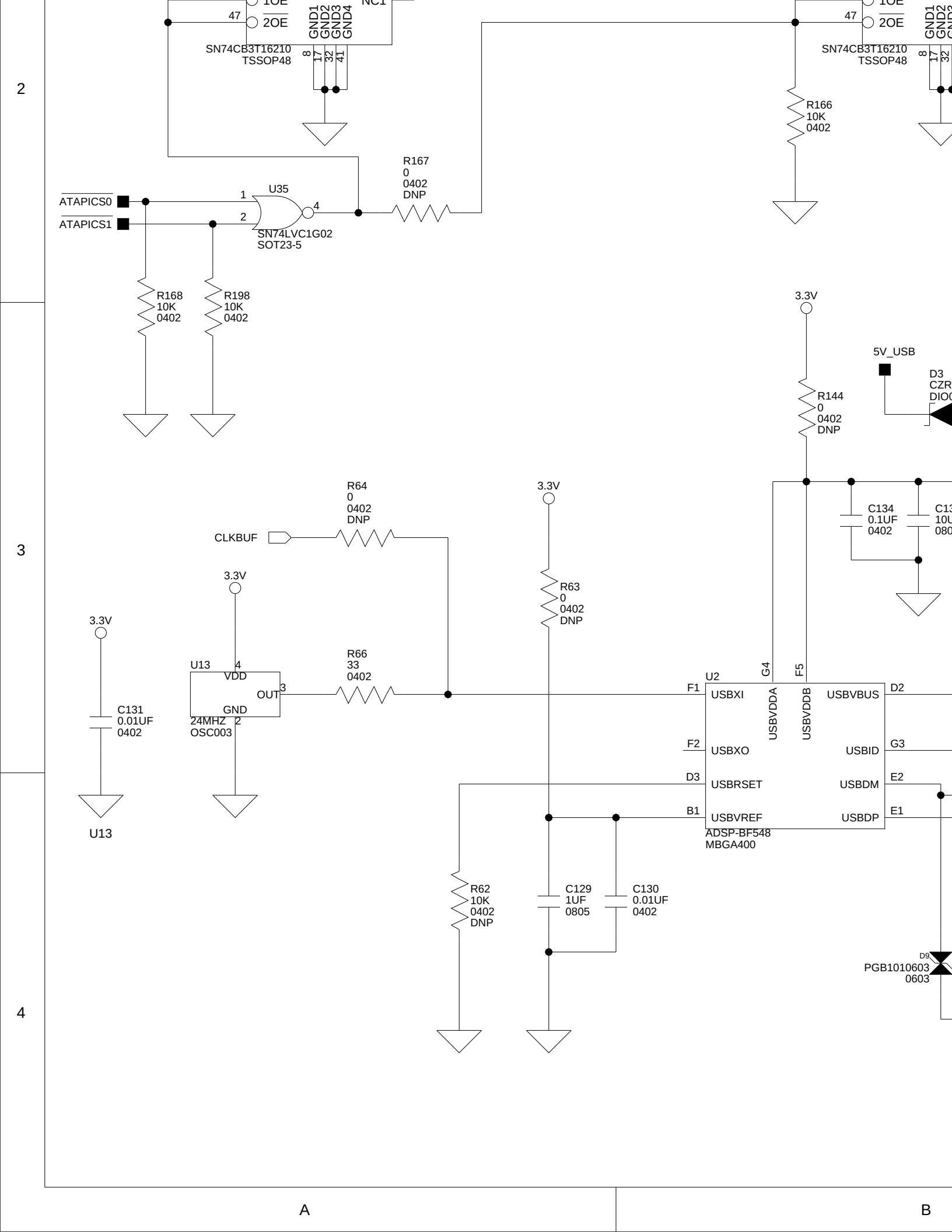

RN22
PPI1D3/HPD11
PPI1D2/HPD10
PPI1D1/HPD9
PPI1D0/HPD8
PPI1D3/HPD11_R
PPI1D2/HPD10_R
PPI1D1/HPD9_R
PPI1D0/HPD8_R
33
RNS001

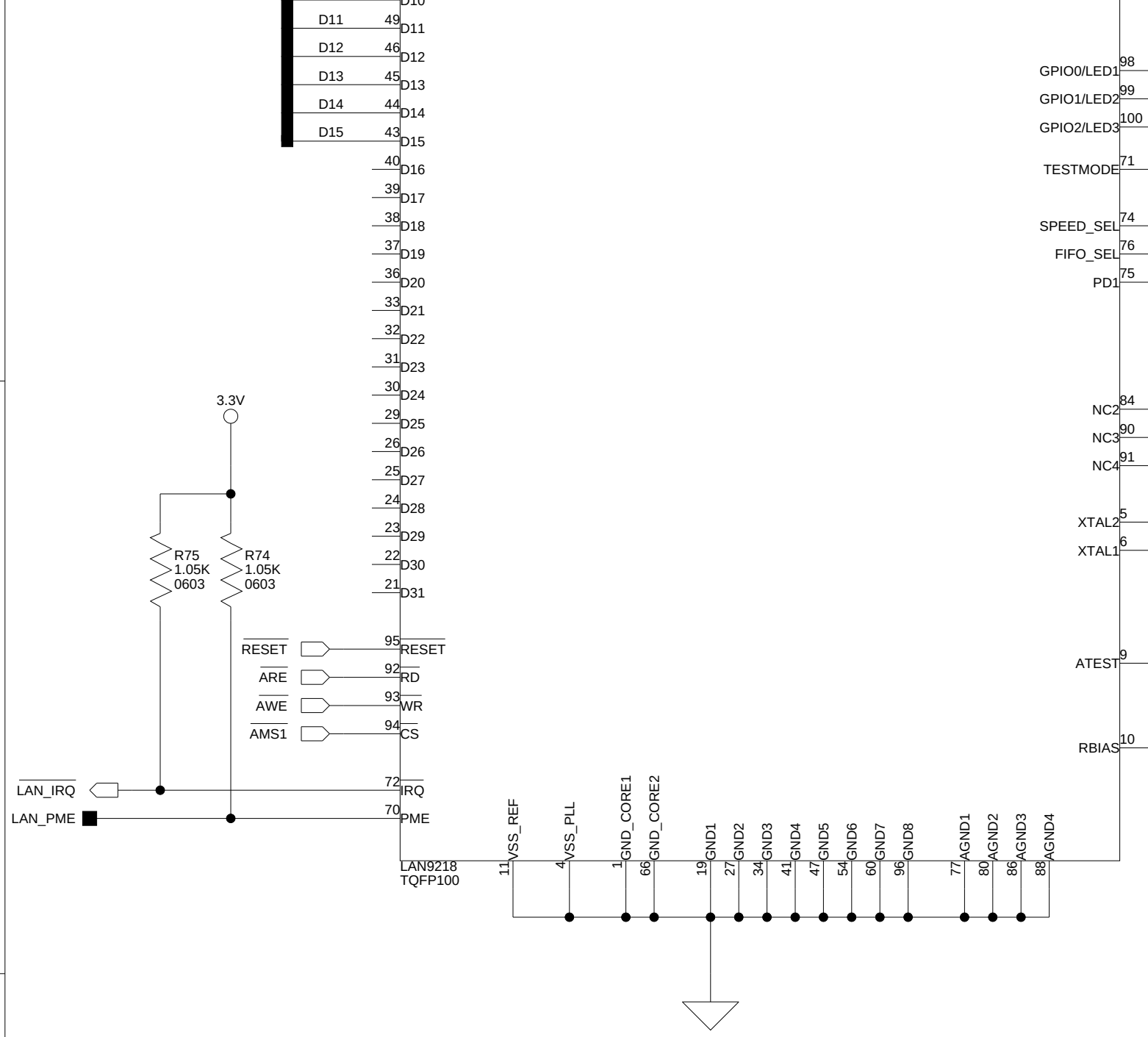

RN23
PPI1D15/HPD7/KPC3
PPI1D14/HPD6/KPC2
PPI1D13/HPD5/KPC1
PPI1D12/HPD4/KPC0
33
RNS001


RN24
PPI1D11/HPD3/KPR3
PPI1D10/HPD2/KPR2
PPI1D9/HPD1/KPR1
PPI1D8/HPD0/KPR0
33
RNS001


T11 VDDEXT26
T12 VDDEXT27
T13 VDDEXT28
T14 VDDEXT29
T15 VDDEXT30
T16 VDDEXT31
F15 VDDEXT32
E5 VDDEXT33
F7 VDDEXT34
VDDINT
F9 VDDINT1
G8 VDDINT2
G12 VDDINT3
G13 VDDINT4
J6 VDDINT5
J13 VDDINT6
L6 VDDINT7
L15 VDDINT8
P6 VDDINT9
P7 VDDINT10
P14 VDDINT11
R10 VDDINT12
R11 VDDINT13
R12 VDDINT14
U9 VDDINT15
VDDDDR
F10 VDDDDR1
F11 VDDDDR2
F12 VDDDDR3
G15 VDDDDR4
H13 VDDDDR5
H14 VDDDDR6
H15 VDDDDR7
J14 VDDDDR8
J15 VDDDDR9
K14 VDDDDR10
K15 VDDDDR11
E13 VDDRTC
M20 DDR_VREF
M18 EXT_WAKE
A18 VROUT0
A19 VROUT1
E8 VDDMP
GND26 K9
GND27 K10
GND28 K11
GND29 K12
GND30 K13
GND31 L7
GND32 L8
GND33 L9
GND34 L10
GND35 L11
GND36 L12
GND37 L13
GND38 L14
GND39 M6
GND40 M7
GND41 M8
GND42 M9
GND43 M10
GND44 M11
GND45 M12
GND46 M13
GND47 M14
GND48 N6
GND49 N7
GND50 N8
GND51 N9
GND52 N10
GND53 N11
GND54 N12
GND55 N13
GND56 N14
GND57 P8
GND58 P9
GND59 P10
GND60 P11
GND61 P12
GND62 P13
GND63 R9
GND64 R13
GND65 R14
GND66 U8
GND67 Y1
GND68 Y20
GND69 R16
GND70 V6
GND71 D4
GND72 F6
GNDMP E7
DDR_VSSR N20
ADSP-BF548
MBGA400
VDDEXT
D16
MA3X717E
DIO005
J13
2
1
CON054
BATTHOLDER
C192
0.01UF
0402
DDR_VREF
R260
1.0
0402
C259
0.01UF
0402
VROUT
TP18
VDDINT
FER18
600
0603
C248
10UF
0805
C247
0.01UF
0402
PLACE AS CLOSE TO U2.M20 AS POSSIBLE
VDDMP ON BF548 DESIGNS CAN BE
CONNECTED DIRECTLY TO VDDINT

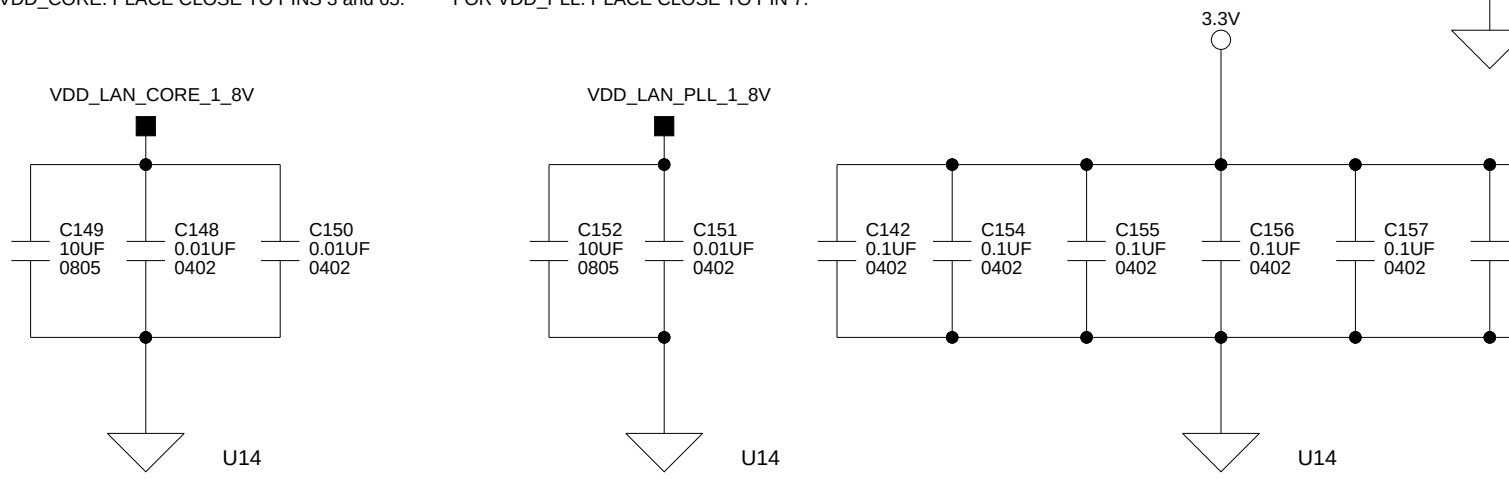

2
3
4
A
B
MIC_L
MIC_R
FER10
600
0603
FER9
600
0603
R50
100
0402
R51
100
0402
C109
0.1UF
0402
C114
0.1UF
0402
LABEL "MIC"
C111
470PF
0603
C110
470PF
0603
C112
0.01UF
0402
C113
0.01UF
0402
AGND
J8
2
3
1
4
7
8
5
6
CON050
LINEIN_L
LINEIN_R
FER7
600
0603
FER8
600
0603
R47
4.7K
0402
R48
4.7K
0402
C107
1UF
0402
C108
1UF
0402
LABEL "LINE IN"
C106
470PF
0603
C105
470PF
0603
R46
4.7K
0402
R49
4.7K
0402
R57
0
0402
TSCLK0
R61
0
0402
RSCLK0
AUDIO_RESET
RFS0
DR0PRI
DT0PRI
C126
47PF
0402
DNP
R55
10K
0402
R56
10K
0402
R60
10K
0402
R172
0
0402
CODEC_
R45
4.7K
0402
JS1
Y1
24.576MHZ
OSC005
C115
22PF
0805
C116
22PF
0805
R43
4.7K
0402
3.3V
A5V
C123
10UF
0805
C125
0.1UF
0402
C124
0.1UF
0402
C122
10UF
0805
C121
0.1UF
0402
C120
0.1UF
0402
C119
0.1UF
0402
U11
U11


1OE
47
2OE
GND1
GND2
GND3
GND4
NC1
SN74CB3T16210
TSSOP48
8
17
32
41
R166
10K
0402
R167
0
0402
DNP
U35
ATAPICS0
ATAPICS1
1
2
4
SN74LVC1G02
SOT23-5
R168
10K
0402
R198
10K
0402
3.3V
5V_USB
D3
CZR
DIO
R144
0
0402
DNP
C134
0.1UF
0402
R64
0
0402
DNP
CLKBUF
R63
0
0402
DNP
R66
33
0402
U13
VDD
OUT
GND
24MHZ
OSC003
C131
0.01UF
0402
U2
G4
F5
F1
USBXI
USBVDDA
USBVDDB
USBVBUS
D2
F2
USBXO
USBID
G3
D3
USBRSET
USBDM
E2
B1
USBVREF
USBDP
E1
ADSP-BF548
MBGA400
R62
10K
0402
DNP
C129
1UF
0805
C130
0.01UF
0402
D9
PGB1010603
0603
2
3
4
A
B



FOR VDD_CORE. PLACE CLOSE TO PINS 3 and 65.

FOR VDD_PLL. PLACE CLOSE TO PIN 7.



A

B

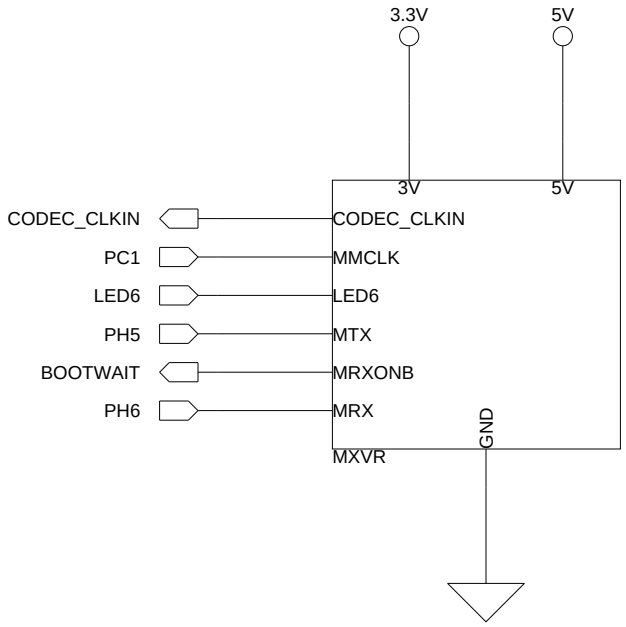
CAN1_ER

CAN1RX

CAN1T

SW15: CAN1 Enable Switch

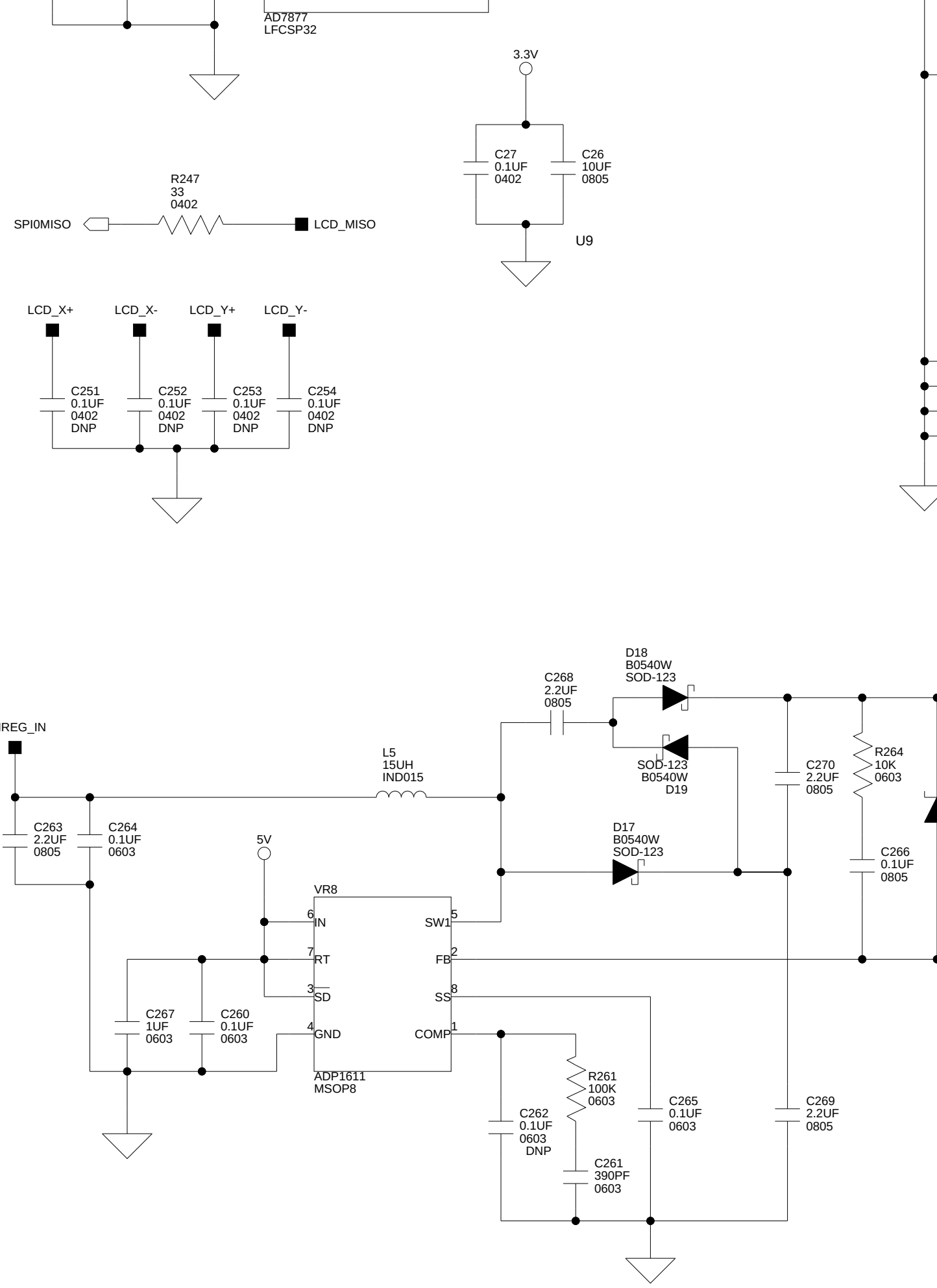
POS.	FROM	TO	DEFAULT	ALTERNATE FUNCTION
SW15.1	ENABLE	GND	OFF	
SW15.2	~STB	GND	OFF	
SW15.3	CAN1_ERR	U2 - PC5	ON	STAMP_GPIO3
SW15.4	CAN1RX	U2 - PG15	ON	STAMP_GPIO2

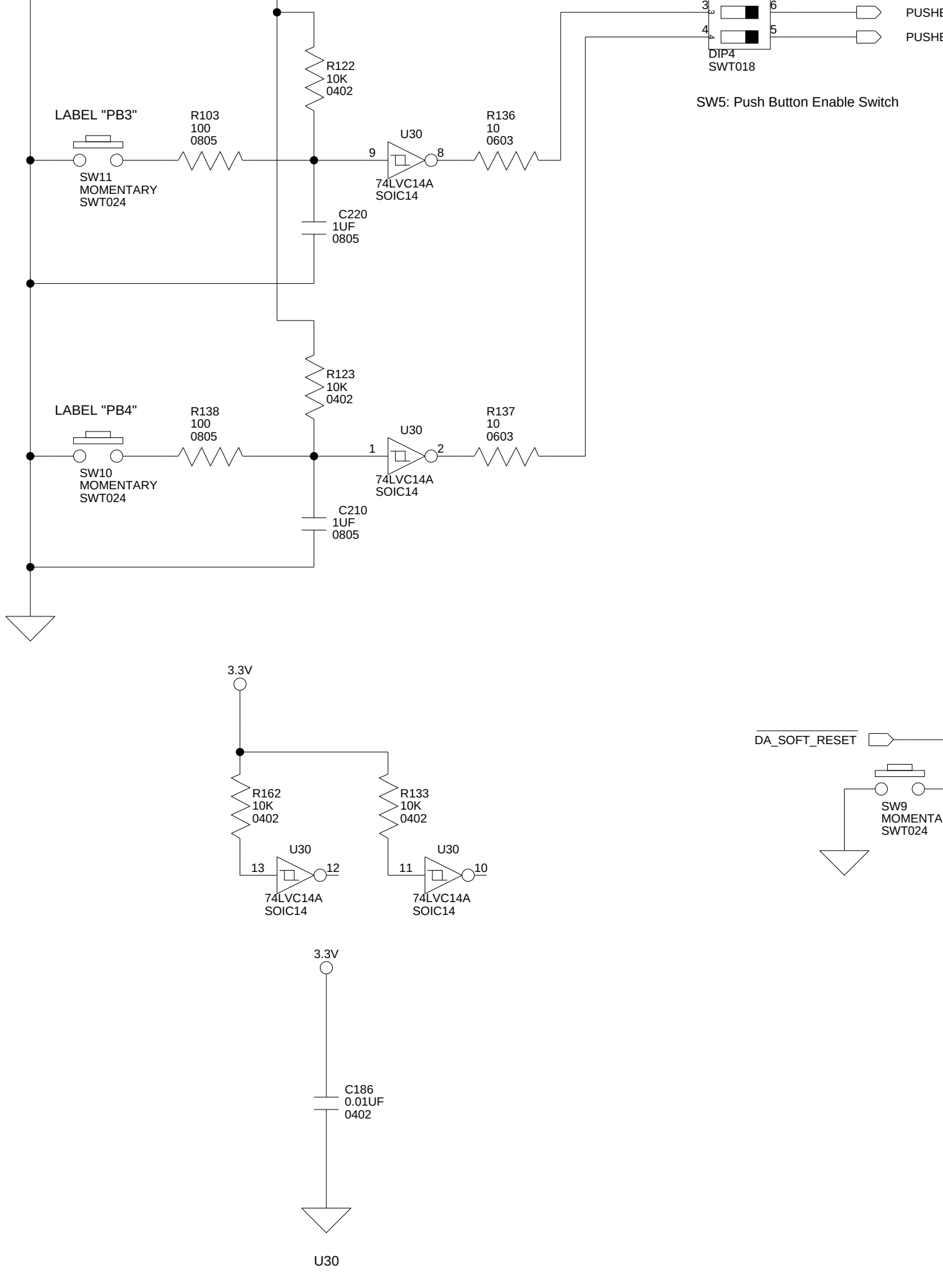


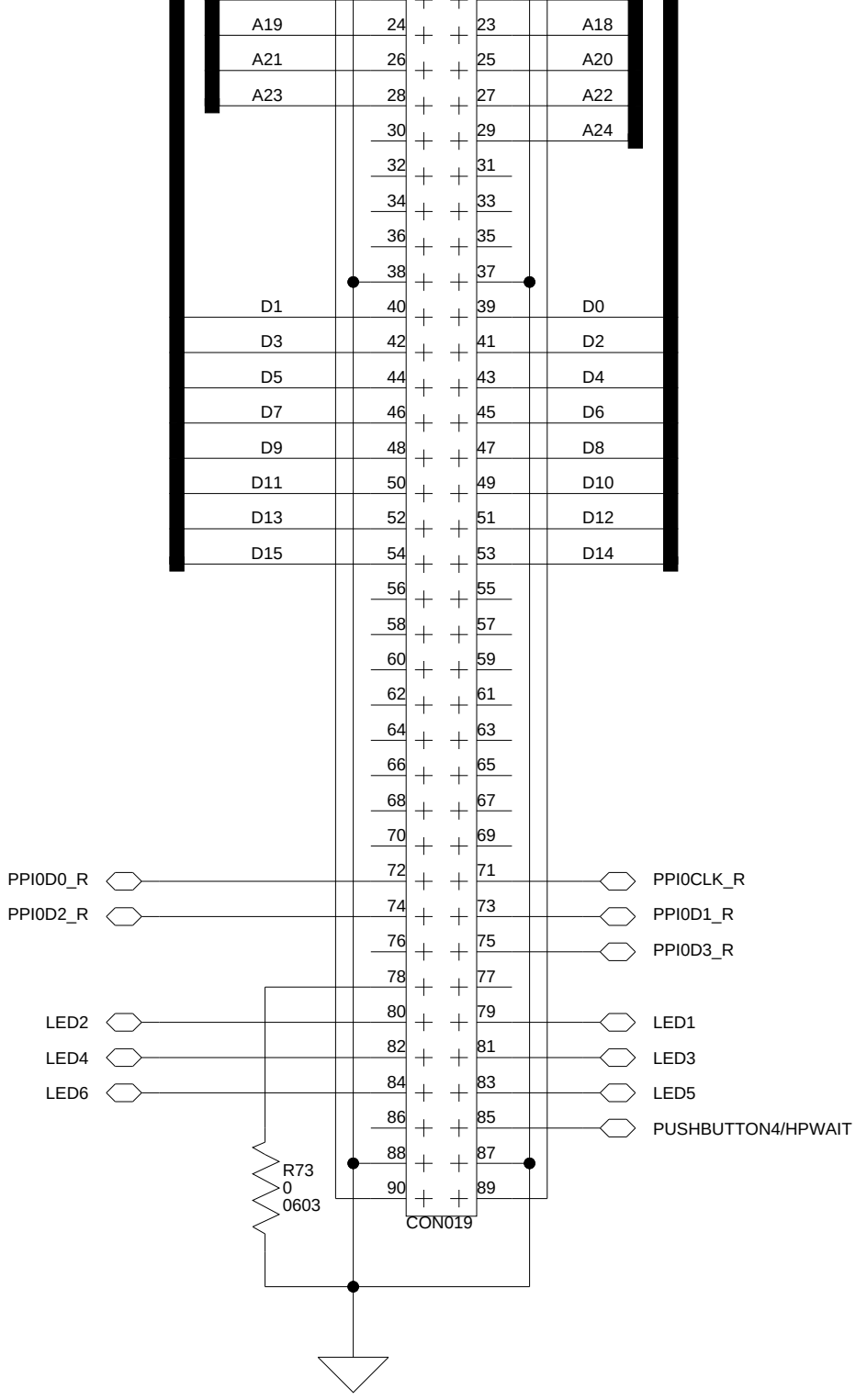
THE MXVR PORT IS ONLY AVAILABLE

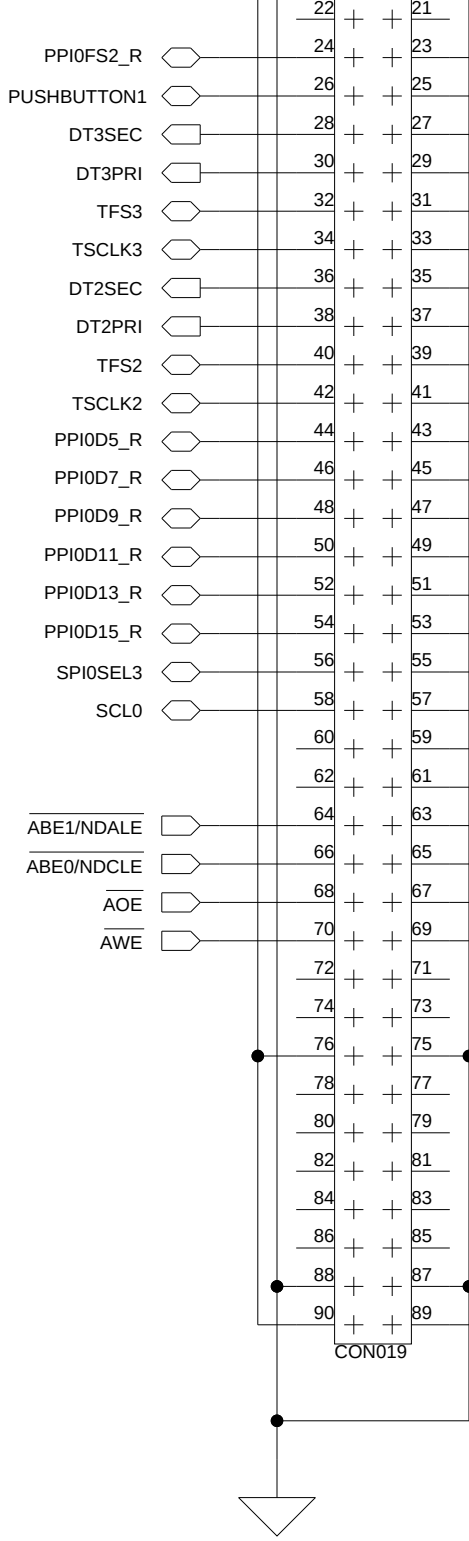
SOME OF THESE PINS STILL NEED TO

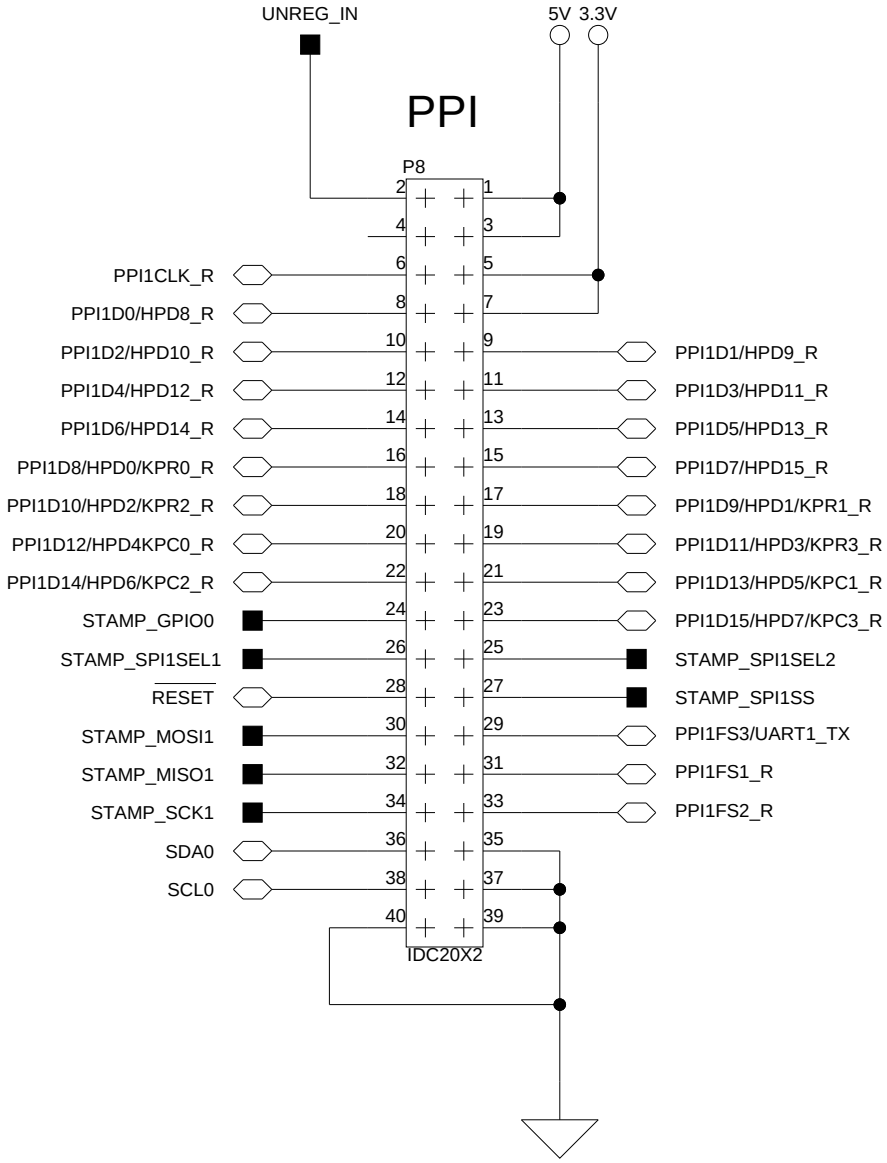
PLEASE REFER TO BF548 DATASHEET

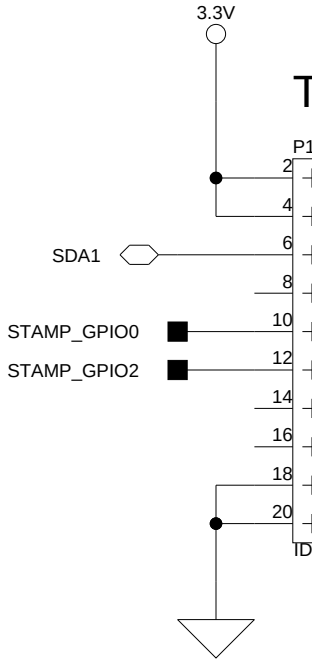

AD7877
LFCSP32
3.3V
C27
0.1UF
0402
C26
10UF
0805
U9
R247
33
0402
SPI0MISO
LCD_MISO
LCD_X+
LCD_X-
LCD_Y+
LCD_Y-
C251
0.1UF
0402
DNP
C252
0.1UF
0402
DNP
C253
0.1UF
0402
DNP
C254
0.1UF
0402
DNP
UNREG_IN
L5
15UH
IND015
C263
2.2UF
0805
C264
0.1UF
0603
5V
VR8
6
IN
7
RT
3
SD
4
GND
SW1
5
FB
2
SS
8
COMP
1
ADP1611
MSOP8
C267
1UF
0603
C260
0.1UF
0603
C268
2.2UF
0805
D18
B0540W
SOD-123
SOD-123
B0540W
D19
D17
B0540W
SOD-123
C270
2.2UF
0805
R264
10K
0603
C266
0.1UF
0805
R261
100K
0603
C262
0.1UF
0603
DNP
C261
390PF
0603
C265
0.1UF
0603
C269
2.2UF
0805

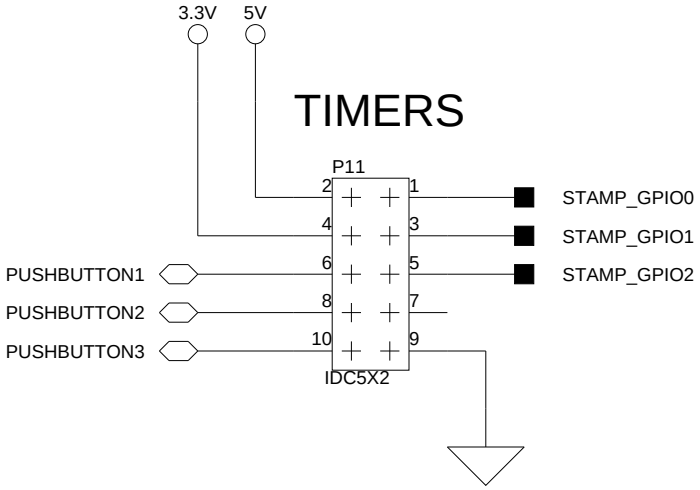

R122
10K
0402
LABEL "PB3"
R103
100
0805
SW11
MOMENTARY
SWT024
U30
9
8
74LVC14A
SOIC14
R136
10
0603
C220
1UF
0805
R123
10K
0402
LABEL "PB4"
R138
100
0805
SW10
MOMENTARY
SWT024
U30
1
2
74LVC14A
SOIC14
R137
10
0603
C210
1UF
0805
3
4
DIP4
SWT018
6
5
PUSHE
PUSHE
SW5: Push Button Enable Switch
3.3V
R162
10K
0402
R133
10K
0402
U30
13
12
74LVC14A
SOIC14
U30
11
10
74LVC14A
SOIC14
DA_SOFT_RESET
SW9
MOMENTA
SWT024
3.3V
C186
0.01UF
0402
U30

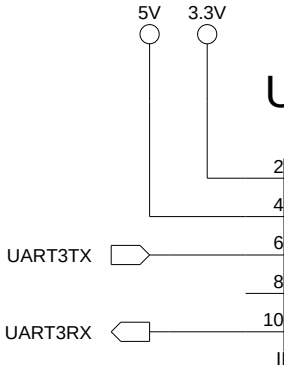

A19
A21
A23
A18
A20
A22
A24
D1
D3
D5
D7
D9
D11
D13
D15
D0
D2
D4
D6
D8
D10
D12
D14
PPI0D0_R
PPI0D2_R
PPI0CLK_R
PPI0D1_R
PPI0D3_R
LED2
LED4
LED6
LED1
LED3
LED5
PUSHBUTTON4/HPWAIT
R73
0
0603
CON019


PPI0FS2_R
PUSHBUTTON1
DT3SEC
DT3PRI
TFS3
TSCLK3
DT2SEC
DT2PRI
TFS2
TSCLK2
PPI0D5_R
PPI0D7_R
PPI0D9_R
PPI0D11_R
PPI0D13_R
PPI0D15_R
SPI0SEL3
SCL0
ABE1/NDALE
ABE0/NDCLE
AOE
AWE
CON019

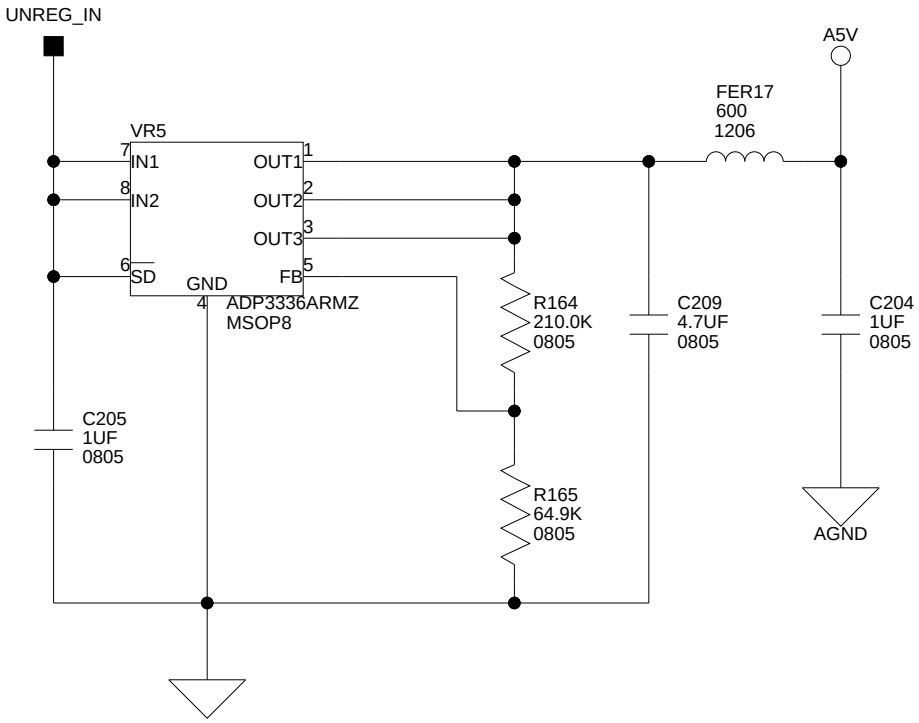


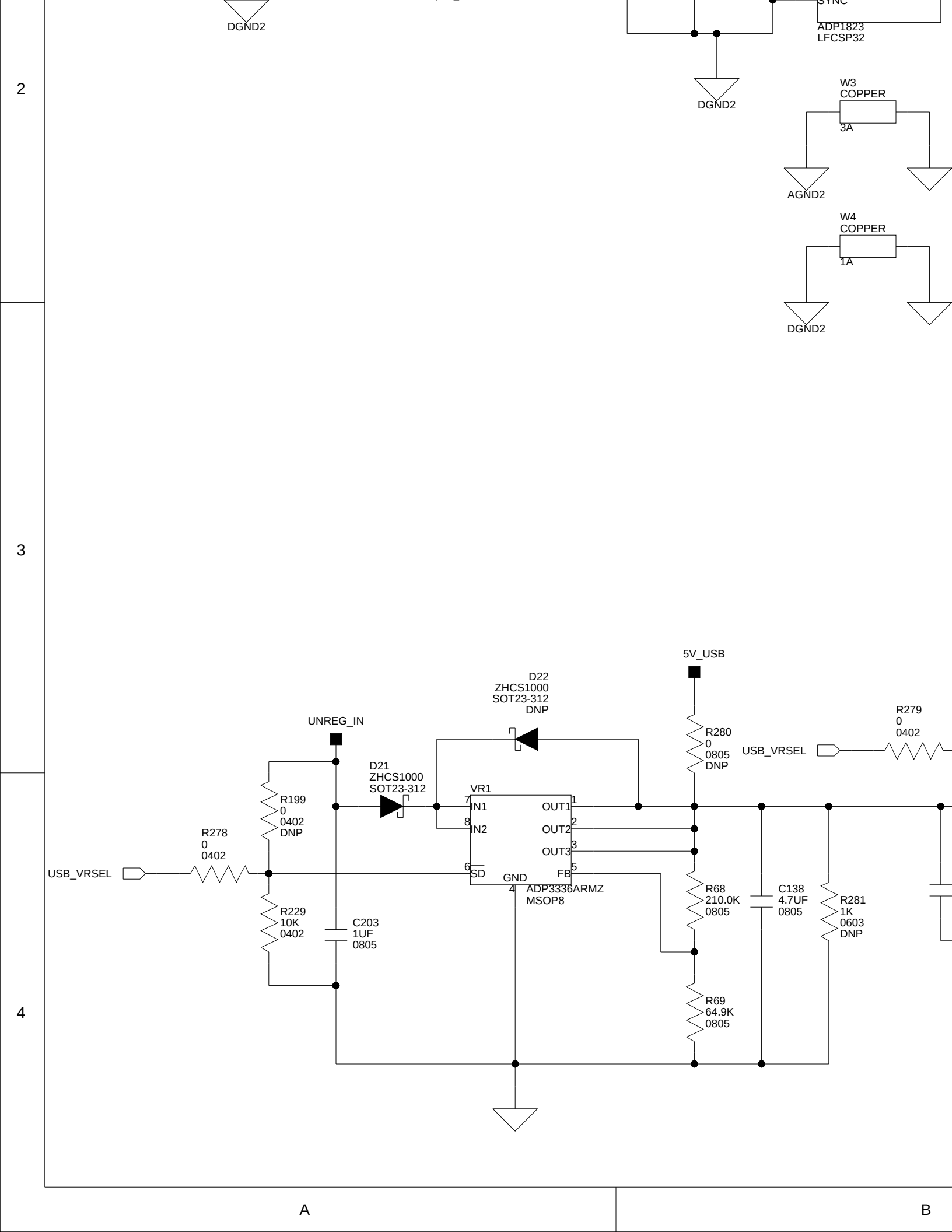


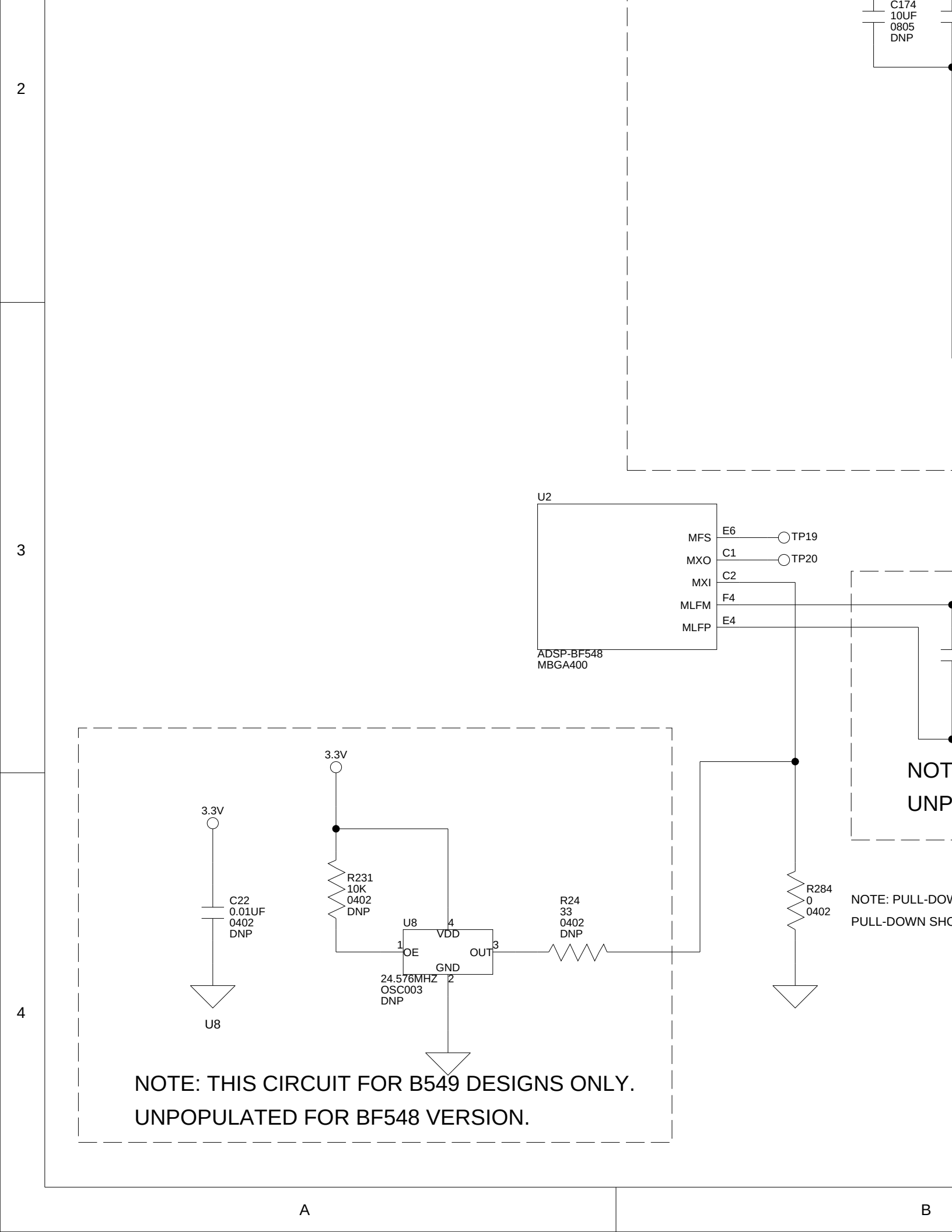




NOTE: PUSHBUTTONS AND TIMERS [2:0] SHARE THE SAME NET NAMES


UNREG_IN
A5V
FER17
600
1206
VR5
7
IN1
8
IN2
6
SD
GND
4
OUT1
1
OUT2
2
OUT3
3
FB
5
ADP3336ARMZ
MSOP8
R164
210.0K
0805
C209
4.7UF
0805
C204
1UF
0805
C205
1UF
0805
R165
64.9K
0805
AGND


DGND2
SYNC
ADP1823
LFCSP32
DGND2
W3
COPPER
3A
AGND2
W4
COPPER
1A
DGND2
5V_USB
D22
ZHCS1000
SOT23-312
DNP
UNREG_IN
D21
ZHCS1000
SOT23-312
R280
0
0805
DNP
R279
0
0402
USB_VRSEL
R199
0
0402
DNP
VR1
7 IN1
8 IN2
6 SD
OUT1 1
OUT2 2
OUT3 3
FB 5
GND 4
ADP3336ARMZ
MSOP8
R278
0
0402
USB_VRSEL
R229
10K
0402
C203
1UF
0805
R68
210.0K
0805
C138
4.7UF
0805
R281
1K
0603
DNP
R69
64.9K
0805


C174
10UF
0805
DNP
U2
MFS
E6
TP19
MXO
C1
TP20
MXI
C2
F4
MLFM
MLFP
E4
ADSP-BF548
MBGA400
NOT
UNP
3.3V
3.3V
C22
0.01UF
0402
DNP
R231
10K
0402
DNP
U8
4
VDD
1
OE
OUT
3
GND
2
24.576MHZ
OSC003
DNP
R24
33
0402
DNP
R284
0
0402
NOTE: PULL-DOW
PULL-DOWN SHO
U8
NOTE: THIS CIRCUIT FOR B549 DESIGNS ONLY.
UNPOPULATED FOR BF548 VERSION.

I INDEX

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P

R

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