ADSP-BF561 EZ-KIT Lite®
Evaluation System Manual

Revision 3.3, July 2012

Part Number
82-000811-01

Analog Devices, Inc.
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ANALOG DEVICES

Copyright Information

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Regulatory Compliance

The ADSP-BF561 EZ-KIT Lite is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADSP-BF561 EZ-KIT Lite has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC amended by 93/68/EEC and therefore carries the "**CE**" mark.

The ADSP-BF561 EZ-KIT Lite has been appended to Analog Devices, Inc. Technical File (TCF) referenced '**DSPTOOLS1**' dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body as listed below.

Technical Certificate No: Z600ANA1.016

Issued by: Technology International (Europe) Limited
60 Shrivenham Hundred Business Park
Shrivenham, Swindon, SN6 8TY, UK

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

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PREFACE

Thank you for purchasing the ADSP-BF561 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for Blackfin® processors.

Blackfin processors embody a type of embedded processor designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications. They deliver breakthrough signal-processing performance and power efficiency within a reduced instruction set computing (RISC) programming model.

Blackfin processors support a media instruction set computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics. Blackfin processors deliver signal-processing performance in a microprocessor-like environment.

Based on the Micro Signal Architecture (MSA), Blackfin processors combine a 32-bit RISC instruction set, dual 16-bit multiply accumulate (MAC) DSP functionality, and eight-bit video processing performance that had previously been the exclusive domain of very-long instruction word (VLIW) media processors.

The evaluation board is designed to be used in conjunction with the CrossCore® Embedded Studio (CCES) and VisualDSP++® development environments to test the capabilities of the ADSP-BF561 Blackfin processors. The VisualDSP++ development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-BF561 assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-BF561 processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-BF561 processor and the evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to http://www.analog.com/dsp/tools.

The ADSP-BF561 EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

Product Overview

The board features:

- Analog Devices ADSP-BF561 Blackfin processor
    - 256-pin mini-BGA package
    - 30 MHz `CLKIN` oscillator
- Synchronous dynamic random access memory (SDRAM)
    - 64 MB (16M x 16 bits x 2 chips)
- Flash memory
    - 8 MB (4M x 16 bits)
- Analog audio interface
    - AD1836 A – Analog Devices 96 kHz audio codec
    - 4 input RCA phono jacks (2 stereo channels)
    - 6 output RCA phono jacks (3 stereo channels)
- Analog video interface
    - ADV7183A video decoder w/ 3 input RCA phono jacks
    - ADV7179 video encoder w/ 3 output RCA phono jacks
- Universal asynchronous receiver/transmitter (UART)
    - ADM3202 RS-232 line driver/receiver
    - DB9 male connector

- LEDs
    - 20 LEDs: 1 power (green), 1 board reset (red), 1 USB (red), 16 general-purpose (amber), and 1 USB monitor (amber)
- Push buttons
    - 5 push buttons with debounce logic: 1 reset, 4 programmable flags
- Expansion interface
    - PPI0, PPI1, SPI, EBIU, Timers11-0, UART, programmable flags, SPORT0, SPORT1
- Other features
    - JTAG ICE 14-pin header

The EZ-KIT Lite board holds 8 MB of flash memory, which can be used to store user-specific boot code, allowing the board to run as a stand-alone unit. The board also holds 512-Mb SDRAM, which can be used at run-time. For more information see "Memory Map" on page 1-11.

SPORT0 interfaces with the AD1836A audio codec, facilitating creation of audio signal processing applications. SPORT0 also attaches to an off-board connector to allow communication with other serial devices. For information about SPORT0, see "SPORT Audio Interface" on page 2-3.

The parallel peripheral interfaces (PPIs) of the processor connect to both a video encoder and video decoder, facilitating creation of video signal processing applications. For information on how the board utilizes the processor's PPIs, see "PPI Interfaces" on page 2-5.

The UART of the processor connects to an RS-232 line driver and a DB9 male connector, allowing you to interface with a PC or other serial device. For information about the UART, see "UART Port" on page 2-8.

Additionally, the EZ-KIT Lite board provides access to most of the processor's peripheral ports. Access is provided in the form of a three-connector expansion interface. For information about the expansion interface, see "Expansion Interface" on page 2-8.

Purpose of This Manual

The *ADSP-BF561 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF561 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set.

Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts that describe your target architecture. For the locations of these documents, see "Related Documents".

Programmers who are unfamiliar with CCES or VisualDSP++ should refer to the online help and user's manuals.

Manual Contents

The manual consists of:

- Chapter 1, "Using the ADSP-BF561 EZ-KIT Lite" on page 1-1
  Describes the EZ-KIT Lite functionality from a programmer's perspective and provides an easy-to-access memory map
- Chapter 2, "ADSP-BF561 EZ-KIT Lite Hardware Reference" on page 2-1
  Provides information on the EZ-KIT Lite hardware components.
- Appendix A, "ADSP-BF561 EZ-KIT Lite Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, "ADSP-BF561 EZ-KIT Lite Schematic" on page B-1
  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design. Appendix B is part of the online help.

What's New in This Manual

This is revision 3.3 of the *ADSP-BF561 EZ-KIT Lite Evaluation System Manual*. The manual has been updated to include CCES information. In addition, modifications and corrections based on errata reports against the previous manual revision have been made.

For the latest version of this manual, please refer to the Analog Devices Web site.

Technical Support

You can reach Analog Devices processors and DSP technical support in the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:
  http://ez.analog.com/community/dsp
- Submit your questions to technical support directly at:
  http://www.analog.com/support
- E-mail your questions about processors, DSPs, and tools development software from **CrossCore Embedded Studio** or **VisualDSP++**:

  Choose **Help > Email Support**. This creates an e-mail to processor.tools.support@analog.com and automatically attaches your **CrossCore Embedded Studio** or **VisualDSP++** version information and `license.dat` file.
- E-mail your questions about processors and processor applications to:
  processor.support@analog.com or
  processor.china@analog.com (Greater China support)
- In the **USA only**, call **1-800-ANALOGD** (1-800-262-5643)
- Contact your Analog Devices sales office or authorized distributor. Locate one at:
  www.analog.com/adi-sales

- Send questions by mail to:
  Processors and DSP Technical Support
  Analog Devices, Inc.
  Three Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

This evaluation system supports Analog Devices ADSP-BF561 Blackfin embedded processors.

Product Information

Product information can be obtained from the Analog Devices Web site and the online help system.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, myAnalog is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information

about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. myAnalog provides access to books, application notes, data sheets, code examples, and more.

Visit myAnalog (found on the Analog Devices home page) to sign up. If you are a registered user, just log on. Your user name is your e-mail address.

EngineerZone

EngineerZone is a technical support forum from Analog Devices. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

Related Documents

For additional information about the product, refer to the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-BF561 Blackfin Embedded Symmetric Multiprocessor Data Sheet	General functional description, pinout, and timing of the processor
ADSP-BF561 Blackfin Processor Hardware Reference	Description of the internal processor architecture and all register functions
Blackfin Processor Programming Reference	Description of all allowed processor assembly instructions

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the development environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.

Example	Description
filename	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

Notation Conventions

1 USING THE ADSP-BF561 EZ-KIT LITE

This chapter provides specific information to assist you with development of programs for the ADSP-BF561 EZ-KIT Lite evaluation system.

The information appears in the following sections.

- "LEDs and Push Buttons" on page 1-14·
  Describes the board's LEDs and push buttons.
- "Audio Interface" on page 1-15
  Describes the board's audio interface.
- "Video Interface" on page 1-16
  Describes the board's video interface.
- "Board Design Database" on page 1-17
  Describes the board design.
- "Example Programs" on page 1-18
  Provides information about the example programs included in the ADSP-BF561 EZ-KIT Lite evaluation system.
- "Flash Programming Utility" on page 1-18
  Highlights the advantages of the Flash Programmer utility.

For information on the graphical user interface, including the boot loading, target options, and other facilities of the EZ-KIT Lite system, refer to the online help.

For more detailed information about the ADSP-BF561 Blackfin processor, see the documents referred to at "Related Documents".

Package Contents

Your ADSP-BF561 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-BF561 EZ-KIT Lite board
- Universal 7V DC power supply
- USB 2.0 cable

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-BF561 EZ-KIT Lite board is designed to run outside your personal computer as a standalone unit. You do not have to open your computer case.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components. Figure 1-1 shows the default jumper settings, DIP switch, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before using the board.

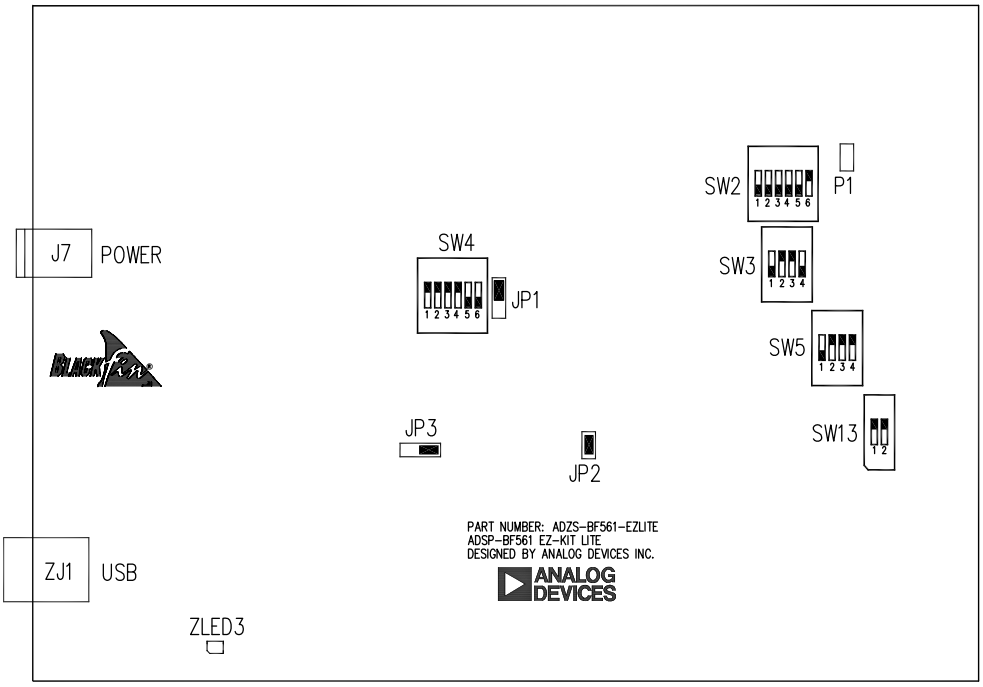


Figure 1-1. EZ-KIT Lite Hardware Setup

CCES Install and Session Startup

For information about CCES and to download the software, go to www.analog.com/CCES. A link for the ADSP-BF561 EZ-KIT Lite Board Support Package (BSP) for CCES can be found at http://www.analog.com/Blackfin/EZKits.

Follow these instructions to ensure correct operation of the product software and hardware.

Step 1: Connect the EZ-KIT Lite board to a personal computer (PC) running CCES using one of two options: an Analog Devices emulator or via the debug agent.

Using an Emulator:

1. Plug one side of the USB cable into the USB connector of the emulator. Plug the other side into a USB port of the PC running CCES.
2. Attach the emulator to the header connector ZP4 (labeled JTAG) on the EZ-KIT Lite board.

Using the on-board Debug Agent:

1. Plug one side of the USB cable into the USB connector of the debug agent ZJ1 (labeled USB).
2. Plug the other side of the cable into a USB port of the PC running CCES.

Step 2: Attach the provided cord and appropriate plug to the power adaptor.

1. Plug the jack-end of the power adaptor into the power connector J7 (labeled Power) on the EZ-KIT Lite board.
2. Plug the other side of the power adaptor into a power outlet. The power LED (labeled LED1) is lit green when power is applied to the board.
3. Power the emulator (if used). Plug the jack-end of the assembled power adaptor into the emulator and plug the other side of the power adaptor into a power outlet. The enable/power is lit green when power is applied.

Step 3 (if connected through the debug agent): Verify that the yellow USB monitor LED (labeled ZLED3) on the debug agent is on. This signifies that the board is communicating properly with the host PC and ready to run CCES.

Session Startup

It is assumed that the CrossCore Embedded Studio software is installed and running on your PC.

Note: If you connect the board or emulator first (before installing CCES) to the PC, the Windows driver wizard may not find the board drivers.

1. Navigate to the CCES environment via the **Start** menu.

   Note that CCES is not connected to the target board.

2. Use the system configuration utility to connect to the EZ-KIT Lite board.

   If a debug configuration exists already, select the appropriate configuration and click **Apply and Debug** or **Debug**. Go to step 8.

   To create a debug configuration, do one of the following:

   - Click the down arrow next to the little bug icon, select **Debug Configurations**
   - Choose **Run > Debug Configurations**.

   The **Debug Configuration** dialog box appears.

3. Select **CrossCore Embedded Studio Application** and click  (**New launch configuration**).

   The **Select Processor** page of the **Session Wizard** appears.

4. Ensure **Blackfin** is selected in **Processor family**. In **Processor type**, select **ADSP-BF561**. Click **Next**.

   The **Select Connection Type** page of the **Session Wizard** appears.

5. Select one of the following:

   - For standalone debug agent connections, **EZ-KIT Lite** and click **Next**.
   - For emulator connections, **Emulator** and click **Next**.

   The **Select Platform** page of the **Session Wizard** appears.

6. Do one of the following:

   - For standalone debug agent connections, ensure that the selected platform is **ADSP-BF561 EZ-KIT** Lite via Debug Agent.
   - For emulator connections, choose the type of emulator that is connected to the board.

7. Click **Finish** to close the wizard.

   The new debug configuration is created and added to the program(s) to load list.

8. In the **Program(s) to load** section, choose the program to load when connecting to the board. If not loading any program upon connection to the target, do not make any changes.

   Note that while connected to the target, there is no way to choose a program to download. To load a program once connected, terminate the session.

To delete a configuration, go to the **Debug Configurations** dialog box and select the configuration to delete. Click and choose **Yes** when asked if you wish to delete the selected launch configuration. Then **Close** the dialog box.

To disconnect from the target board, click the terminate button (red box) or choose **Run > Terminate**.

To delete a session, choose **Target > Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

VisualDSP++ Install and Session Startup

For information about VisualDSP++ and to download the software, go to www.analog.com/VisualDSP.

1. Verify that the yellow USB monitor LED (ZLED3, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the **Start > Programs** menu. The main window appears. Note that VisualDSP++ does not connect to any session. Skip the rest of this step to step 3.

   If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and force VisualDSP++ to start a new session by pressing and holding down the **Ctrl** key while starting VisualDSP++. Do not release the **Ctrl** key until the **Session Wizard** appears on the screen. Go to step 4.

3. To connect to a new EZ-KIT Lite session, start **Session Wizard** by selecting one of the following.
   - From the **Session** menu, **New Session**.
   - From the **Session** menu, **Session List**. Then click **New Session** from the **Session List** dialog box.
   - From the **Session** menu, **Connect to Target**.
4. The **Select Processor** page of the wizard appears on the screen. Ensure **Blackfin** is selected in **Processor family**. In **Choose a target processor**, select **ADSP-BF561**. Click **Next**.
5. The **Select Connection Type** page of the wizard appears on the screen. Select **EZ-KIT Lite** and click **Next**.
6. The **Select Platform** page of the wizard appears on the screen. In the **Select your platform** list, select **ADSP-BF561 EZ-KIT Lite via Debug Agent**. In **Session name**, highlight or specify the session name.

   The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and to open a new session.

   Click **Next**.
7. The **Finish** page of the wizard appears on the screen. The page displays your selections. If you are satisfied, click **Finish**. If not, click **Back** to make changes.

To disconnect from a session, click the disconnect button  or select **Session > Disconnect from Target**.

To delete a session, select **Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

CCES Evaluation License

The ADSP-BF561 EZ-KIT Lite software is part of the Board Support Package (BSP) for the Blackfin ADSP-BF56x family. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for 90 days after activation. Once the evaluation period ends, the evaluation license becomes permanently disabled. If the evaluation license is installed but not activated, it allows 10 days of unrestricted use and then becomes disabled. The license can be re-enabled by activation.

An evaluation license can be upgraded to a full license. Licenses can be purchased from:

- Analog Devices directly. Call (800) 262-5645 or 781-937-2384 or go to:
  http://www.analog.com/buyonline.
- Analog Devices, Inc. local sales office or authorized distributor. To locate one, go to:
  http://www.analog.com/salesdir/continent.asp.

The EZ-KIT Lite hardware must be connected and powered up to use CCES with a valid evaluation or full license.

VisualDSP++ Evaluation License

The ADSP-BF561 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-BF561 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a user's program to 41 KB of memory for code space with no restrictions for data space.

To avoid errors when opening VisualDSP++, the EZ-KIT Lite hardware must be connected and powered up. This is true for using VisualDSP++ with a valid evaluation or full license.

Memory Map

The EZ-KIT Lite board includes two types of external memory, 64-MB SDRAM and 8-MB flash. See the external memory map in Table 1-1. The complete configuration of the ADSP-BF561 processor internal SRAM is detailed in Figure 1-2.

Table 1-1. EZ-KIT Lite External Memory Map

Start Address	End Address	Description
0x00000000	0x3FFFFFF	SDRAM bank 0; see "Memory Map" on page 1-11
0x20000000	0x207FFFFF	ASYNC memory bank 0; see "Memory Map" on page 1-11.
All other locations		Not used

Memory Map

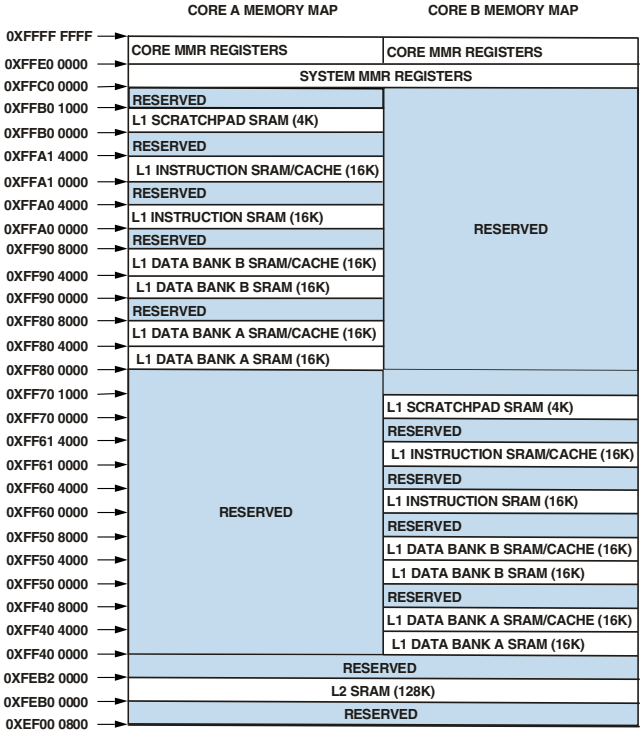


Figure 1-2. ADSP-BF561 Processor Internal Memory Map

The 8 MB of flash memory is organized as 4M x 16 bit and mapped into a ADSP-BF561 processor's ASYNC memory bank 0. The $\overline{\text{AMS0}}$ memory select signal connects to the output enable pin of flash memory.

The 64 MB of SDRAM is organized as 16M x 32 bits wide. The processor's memory select pin $\overline{\text{SMS0}}$ is configured for SDRAM. Three SDRAM control registers must be initialized in order to access the SDRAM memory.

When in a CCES or VisualDSP++ session, you can configure the SDRAM registers automatically:

- CCES users, choose **Target > Settings > Target Options > Use XML reset values**
- VisualDSP++ users, choose **Settings > Target Options > Use XML reset values**

The EBIU_SDGCTL, EBIU_SDBCTL, and EBIU_SDRRC register values have been set in the ADSP-BF561-proc.xml file found in your System\ArchDef folder. These values can be changed to be more optimal depending on the SCLK frequency.

The values in Table 1-2 are set by default whenever bank 0 is accessed through the debugger (for example, when viewing memory windows or loading a program). The numbers are derived for maximum flexibility and work for a system clock frequency between 60 MHz and 133 MHz.

Table 1-2. EZ-KIT Lite Session SDRAM Default Settings

Register	Value	Function
EBIU_SDGCTL	0x0091998D	Calculated with SCLK = 133 MHz
EBIU_SDBCTL	0x00000013	
EBIU_SDRRC	0x000001CF	Calculated with SCLK = 120 MHz

The EBIU_SDGCTL register can be written once after the processor comes out of reset. Therefore, the user code should not re-initialize the register. Clearing the **Use XML reset values** check box allows manual configuration of the EBIU registers. For more information, see online help.

Automatic configuration of SDRAM is not optimized for a specific SCLK frequency. Table 1-3 shows the optimized configuration of the SDRAM registers using a 120 MHz SCLK. The frequency of 120 MHz is the maximum SCLK frequency when using a 600 MHz core frequency, the maximum frequency for the EZ-KIT Lite. Only the EBIU_SDRRC register needs to be modified in the user code to achieve maximum performance.

Table 1-3. SDRAM Optimum Settings[1]

Register	Value
EBIU_SDGCTL	0x0091998D
EBIU_SDBCTL	0x00000013
EBIU_SDRRC	0x000003A0

1 Calculated with SCLK = 120 MHz

For more information, see "External Bus Interface Unit" on page 2-3.

An example program is included in the EZ-KIT installation directory to demonstrate the SDRAM interface setup.

LEDs and Push Buttons

The EZ-KIT Lite provides four push buttons and sixteen LEDs for general-purpose IO.

Sixteen LEDs, labeled LED5 through LED20, are controlled by the processor's programmable flags PF32 through PF47 (equivalent to PPI0_D15-8 and PPI1_D15-8). These LEDs are accessed through the FLAG 2 registers. First, the direction must be configured to output by setting the bits of the FIO2_DIR register to 1. Then the value of the LEDs are modified using one of the FIO2_FLAG_D, FIO2_FLAG_C, FIO2_FLAG_S, or FIO2_FLAG_T registers.

The four general-purpose push buttons are labeled SW6 through SW9. The buttons connect to the programmable flags PF8-5. A status of each

individual button can be read through the FIO0_FLAG_D register. A switch is being pressed-on when the corresponding bit of the register reads 1. When the switch is released, the bit reads 0. A connection between the push button and PF input is established through the SW4 DIP switch.

For information on how to disconnect the switch from the programmable flag and use it for another objective, see "Push Button Enable Switch (SW4)".

An example program is included in the EZ-KIT Lite installation directory to demonstrate functionality of the LEDs and push buttons.

Audio Interface

The AD1836A audio codec provides three channels of stereo audio output and two channels of multichannel 96 kHz input. The SPORT0 interface of the processor links with the stereo audio data input and output pins of the AD1836A codec. The processor is capable of transferring data to the audio codec in time-division multiplexed (TDM) or 2-wire serial interface (TWI) mode.

In TWI mode, the codec can operate at a 96 kHz sample rate but restricts the output to two channels. In TDM mode, the codec can operate at a maximum of 48 kHz sample rate but allows simultaneous use of all input and output channels. When using TWI mode, the TSCLK0 and RSCLK0 pins (as well as the TFS0 and RFS0 pins of the processor) must be tied together externally to the processor. This is accomplished with the SW4 DIP switch. See "Push Button Enable Switch (SW4)" on page 2-12 for more information.

The AD1836A audio codec's internal configuration registers are configured using the processor's PF4 programmable flag pin, used as the select for the audio device. For more information on how to configure the multichannel codec, go to www.analog.com/AD1836A.

The AD1836A codec reset is controlled by the processor's programmable flag PF15. When PF15 is 0, the reset is asserted. When PF15 is 1, the reset is de-asserted. Note that when PF15 is not driven (configured as input), the AD1836A reset is asserted due to the pull-down resistor. See "Programmable Flags" on page 2-4 for more information.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate the AD1836A codec operation.

Video Interface

The board supports video input and output applications. The ADV7179 video encoder provides up to three output channels of analog video, while the ADV7183A video decoder provides up to three input channels of analog video. The video encoder connects to the parallel peripheral interface 1 (PPI1), while the video decoder connects to the parallel peripheral interface 0, (PPI0). Each PPI interface has an individual clock that is configured by the SW5 switch settings. See "PPI Clock Select Switch (SW5)" on page 2-13 for more information.

Both the encoder and the decoder connect to the parallel peripheral interfaces (PPI input clock) of the processor. For additional information on the video interface hardware, refer to "PPI Interfaces" on page 2-5.

For the video interface to be operational, the following basic steps must be performed.

1. Configure the SW2 DIP switch as required by the application. Refer to "Video Configuration Switch (SW2)" on page 2-10 for details.
2. De-assert the video device's reset by setting high a corresponding programmable flag. PF14 controls the ADV7179 encoder's reset, while PF13 controls the ADV7183A decoder's reset.

3. If using the ADV7183A decoder:
    - Enable device by driving programmable flag output PF2 to 0.
    - Select PPI0 clock; for details, refer to "PPI Clock Select Switch (SW5)" on page 2-13.
4. Program internal registers of the video device in use. Both video encoder and decoder use a 2-wire serial interface to access internal registers. The PF0 programmable flag functions as a serial clock (SCL), and PF1 functions as a serial data (SDAT).
5. Program the ADSP-BF561 processor's PPI interfaces (configuration registers, DMA, and so on).

Example programs are included in the EZ-KIT Lite installation directory to demonstrate the capabilities of the video interface.

Board Design Database

A .zip file containing all of the electronic information required for the design, layout, fabrication and assembly of the product is available for download from the Analog Devices board design database at: http://www.analog.com/board-design-database.

Example Programs

Example programs are provided with the ADSP-BF561 EZ-KIT Lite to demonstrate various capabilities of the product. The programs are included in the product installation kit and can be found in the `Examples` folder of the installation. Refer to a readme file provided with each example for more information.

CCES users are encouraged to use the example browser to find examples included with the EZ-KIT Lite Board Support Package.

Flash Programming Utility

The ADSP-BF561 EZ-KIT Lite evaluation system includes a flash programming utility. The utility allows you to program flash memory on the EZ-KIT Lite. The utility installed with VisualDSP++ is called Flash Programmer. The utility installed with CCES is called Device Programmer.

The flash programming driver is core-specific (core A) and must be loaded to core A in order to operate correctly. The flash programming utility relies on the user to set the correct core focus. To set the correct core, select core A in the multiprocessor window before opening the utility interface.

For more information on the flash programming utility, refer to the online help.

2 ADSP-BF561 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF561 EZ-KIT Lite board. The following topics are covered.

- "System Architecture" on page 2-2
  Describes the ADSP-BF561 EZ-KIT Lite configuration and explains how the board components interface with the processor.
- "Jumper and DIP Switch Settings" on page 2-10
  Shows the locations and describes the configuration jumpers and switches.
- "LEDs and Push Buttons" on page 2-15
  Shows the locations and describes the LEDs and push buttons.
- "Connectors" on page 2-18
  Shows the locations and provides part numbers for the on-board connectors. In addition, the manufacturer and part number information is provided for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board.

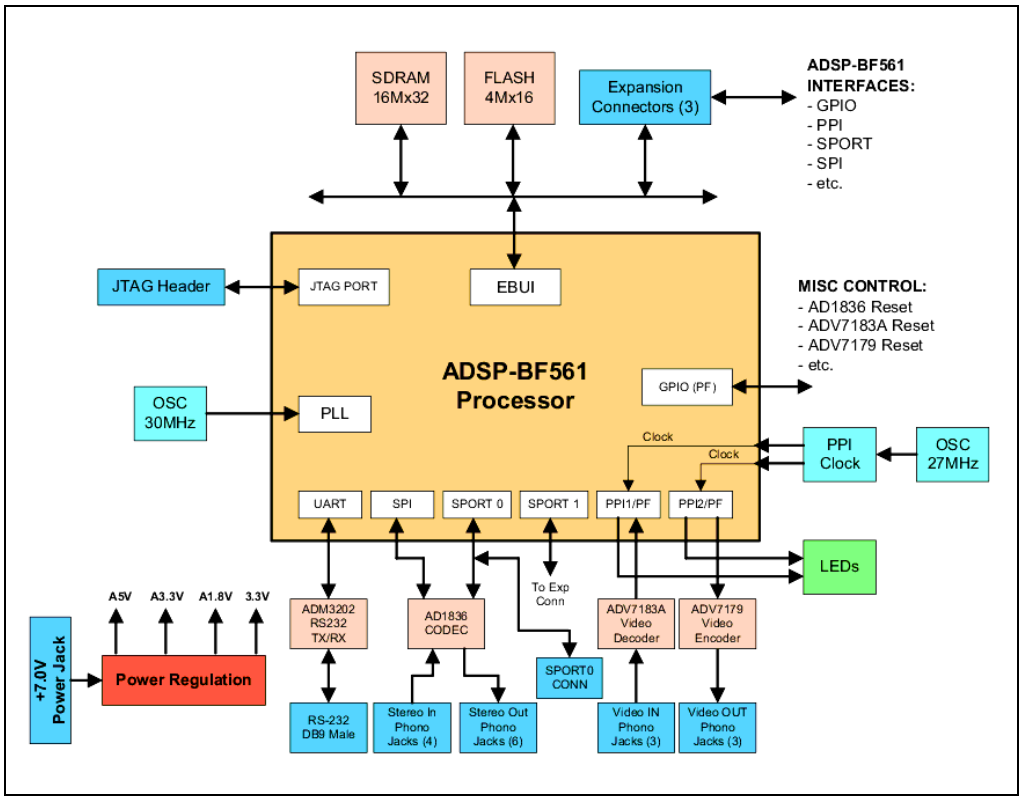


Figure 2-1. System Architecture

This EZ-KIT Lite has been designed to demonstrate the capabilities of the ADSP-BF561 Blackfin processor. The processor has an IO voltage of 3.3V. The core voltage and the core clock rate can be set on the fly by the processor. The input clock is 30 MHz.

External Bus Interface Unit

The external bus interface unit (EBIU) connects external memory to the ADSP-BF561 processor. It includes a 32-bit wide data bus, an address bus (A25-2), and a control bus. All of the 8-bit, 16-bit, and 32-bit accesses are supported. On the EZ-KIT Lite board, the EBI unit connects to SDRAM and flash memory. For more information on using the external memory see "Memory Map" on page 1-11.

All of the address, data, and control signals are available externally via the expansion interface connectors (J1-3). The pinout of these connectors can be found in "ADSP-BF561 EZ-KIT Lite Schematic" on page B-1.

SPORT Audio Interface

The SPORT0 interface connects to the AD1836A audio codec and the expansion interface. The AD1836A codec uses both the primary and secondary data transmit and receive pins to input and output data from the audio input and outputs.

The SPORT1 interface connects to the SPORT connector (P3).

The pinout of the SPORT and expansion interface connectors can be found in "ADSP-BF561 EZ-KIT Lite Schematic" on page B-1.

SPI Interface

The processor's serial peripheral interface (SPI) connects to the AD1836A audio codec and the expansion interface. The SPI connection to the AD1836A codec is used to access the control registers of the device. The PF4 flag of the processor acts as the device select for the SPI port.

The SPI signals are available on the expansion interface and on the SPI connector (P5). The pinout for the interface can be found in "ADSP-BF561 EZ-KIT Lite Schematic" on page B-1.

Programmable Flags

The processor has 48 programmable flag pins (PFs). Many of the flags are multi-functional and depend on the processor's setup. Table 2-1 shows how the programmable flag pins are used on the EZ-KIT Lite.

Table 2-1. Programmable Flag Connections

Processor PF Pin	Processor Function	EZ-KIT Lite Function
PF0	SPI select S, timer 0	Serial clock for programming ADV7179 video encoder and ADV7183A video decoder.
PF1	SPI select 1, timer 1	Serial data for programming ADV7179 video encoder and ADV7183A video decoder.
PF2	SPI select 2, timer 2	ADV7183A video decoder's $\overline{\text{OE}}$.
PF3	SPI select 3, timer 3	ADV7183A FIELD pin. See "Video Configuration Switch (SW2)" on page 2-10.
PF4	SPI select 4, timer 4	AD1836A audio codec's SPI select.
PF5	SPI select 5, timer 5	Push button (SW6). See "LEDs and Push Buttons" on page 1-14 and "Push Button Enable Switch (SW4)" on page 2-12 for information on how to disable the push button.
PF6	SPI select 6, timer 6	Push button (SW7). See "LEDs and Push Buttons" on page 1-14 and "Push Button Enable Switch (SW4)" on page 2-12 for information on how to disable the push button.
PF7	SPI select 7, timer 7	Push button (SW8). See "LEDs and Push Buttons" on page 1-14 and "Push Button Enable Switch (SW4)" on page 2-12 for information on how to disable the push button.
PF8		Push button (SW9). See "LEDs and Push Buttons" on page 1-14 and "Push Button Enable Switch (SW4)" on page 2-12 for information on how to disable the push button.
PF9-12		Not used
PF13		ADV7183A video decoder's reset

Table 2-1. Programmable Flag Connections (Cont'd)

Processor PF Pin	Processor Function	EZ-KIT Lite Function
PF14		ADV7179 video encoder's reset
PF15		AD1836 codec's reset
PF16		SPORT0 transmit frame sync pin
PF17		SPORT0 transmit data secondary pin
PF18		SPORT0 transmit data primary pin
PF19		SPORT0 receive frame sync pin
PF20		SPORT0 receive data secondary pin
PF21		SPORT1 transmit frame pin
PF22		SPORT1 transmit data secondary pin
PF23		SPORT1 transmit data primary pin
PF24		SPORT1 receive frame sync pin
PF25		SPORT1 receive data secondary pin
PF26		UART transmit pin
PF27		UART receive pin
PF28		SPORT0 receive serial clock pin
PF29		SPORT0 transmit serial clock pin
PF30		SPORT1 receive serial clock pin
PF31		SPORT1 transmit serial clock pin
PF39-32	PPI1 data 15-8	LED13-20
PF47-40	PPI0 data 15-8	LED5-12

PPI Interfaces

The ADSP-BF561 processor employs two independent parallel peripheral interfaces (PPIs), PPI0 and PPI1. Each PPI interface is a half-duplex, bi-directional bus consisting of 16 bits of data, a dedicated input clock,

and synchronization signals. The ADSP-BF561 EZ-KIT Lite board utilizes the PPI interfaces for video input and video output.

The PPI0 interface is configured to input video data from the ADV7183A video decoder device: bits 7-0 connect to the video decoder's data outputs. The PPI1 interface is configured to output video data to the ADV7179 video encoder device: bits 7-0 connect to the video encoder's data inputs.

Each PPI interface has a dedicated clock input configured independently by the SW5 switch. The clock source can be one of the following: 27 MHz crystal oscillator, ADV7183A video decoder's clock output, or external clock from the expansion interface. See "PPI Clock Select Switch (SW5)" on page 2-13 for more information about the switch.

The SW2 switch provides a flexible connection between dedicated synchronization IOs (SYNC1 and SYNC2 of each PPI interface) and the encoder's and decoder's horizontal and vertical synchronization pins. See "Video Configuration Switch (SW2)" on page 2-10 for more information about the switch. For a detailed description of the ADSP-BF561 processor's PPI interfaces, refer to the *ADSP-BF561 Blackfin Processor Hardware Reference*.

Table 2-2 describes the PPI pins of the EZ-KIT Lite board.

Table 2-2. PPI Connections

Processor PPI Pin	Other Processor Function	EZ-KIT Lite Function
PPI0 bits 7-0		ADV7183A data outputs P15-8
PPI1 bits 7-0		ADV7179 data inputs P7-0
PPI0 SYNC1	Timer 8	ADV7179 HSYNC. For more information, see "Video Configuration Switch (SW2)" on page 2-10.
PPI0 SYNC2	Timer 9	ADV7179 VSYNC. For more information, see "Video Configuration Switch (SW2)" on page 2-10.
PPI0 clock		A choice of ADV7183A output clock, a local 27 MHz oscillator, or an external clock from ADSP-BF533/BF561 Blackfin EZ-Extender®.

Table 2-2. PPI Connections (Cont'd)

Processor PPI Pin	Other Processor Function	EZ-KIT Lite Function
PPI1 SYNC1	Timer 10	ADV7183A HSYNC. For more information, see "Video Configuration Switch (SW2)" on page 2-10.
PPI1 SYNC2	Timer 11	ADV7183A VSYNC. For more information, see "Video Configuration Switch (SW2)" on page 2-10.
PPI1 clock		A choice of ADV7183A output clock, a local 27 MHz oscillator, or an external clock from ADSP-BF53x/BF561 Blackfin EZ-Extender.

Video Output (PPI1)

The PPI1 interface is configured as output and connects to the on-board video encoder device, ADV7179. The ADV7179 encoder generates three analog video channels on DAC A, DAC B, and DAC C. The PPI1 bits 7-0 connect to P7-0 of the encoder's pixel inputs. The encoder's input clock is fixed and comes from an on-board 27 MHz oscillator.

The encoder's synchronization signals, HSYNC and VSYNC, can be configured as inputs or outputs. Video blanking control signal is at level 1. The HSYNC and VSYNC signals can connect to SYNC1 and SYNC2 of the processor's PPI1 interface via the SW2 switch, as described in "Video Configuration Switch (SW2)" on page 2-10.

Video Input (PPI0)

The PPI0 interface is configured as input and connects to the on-board video decoder device, ADV7183A. The ADV7183A decoder receives three analog video channels on AIN1, AIN4, and AIN5 input. The decoder's pixel data outputs P15-8 drive the PPI0 inputs 8-0. The decoder's 27 MHz pixel clock output can be selected to drive any of the PPI clocks as shown in Table 2-7 on page 2-13.

Synchronization outputs of the decoder, HS/HACTIVE, VS/VACTIVE, and FIELD can connect to the processor's PPI0_SYNC1, PPI0_SYNC2, and PF3 flag via the SW2 DIP switch, as described in "Video Configuration Switch (SW2)" on page 2-10.

UART Port

The processor's universal asynchronous receiver/transmitter (UART) port connects to the ADM3202 RS-232 line driver as well as to the expansion interface. The RS-232 line driver is attached to the DB9 male connector, providing an interface to a personal computer and other serial devices.

Expansion Interface

The expansion interface consists of the three 90-pin connectors, J1-3. Table 2-3 shows the interfaces each connector provides. For the exact pin-out of the connectors, refer to "ADSP-BF561 EZ-KIT Lite Schematic" on page B-1. The mechanical dimensions of the connectors can be obtained from Technical Support.

Table 2-3. Connector Interfaces

Connector	Interfaces
J1	5V, GND, address, data, PPI0 3-0, PF15-6, PF4
J2	3.3V, GND, SPI, NMI, PPI0 SYNC3-1, SPORT0, SPORT1, PF15-0, EBUI control signals
J3	5V, 3.3V, GND, UART, PPI1 15-0, reset, video control signals

Limits to the current and to the interface speed must be taken into consideration when using the expansion interface. The maximum current limit is dependent on the capabilities of the used regulator. Additional circuitry also can add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access internal and external memories of the processor through a 6-pin interface. The JTAG emulation port of the processor also connects to the USB debugging interface. When an emulator connects to the board at ZP4, the USB debugging interface is disabled. See "JTAG (ZP4)" on page 2-22 for more information about the JTAG connector.

To learn more about available emulators, go to http://www.analog.com/processors/tools/blackfin.

Jumper and DIP Switch Settings

This section describes functionality of the jumpers and DIP switches. The jumper and DIP switch locations are shown in Figure 2-2.

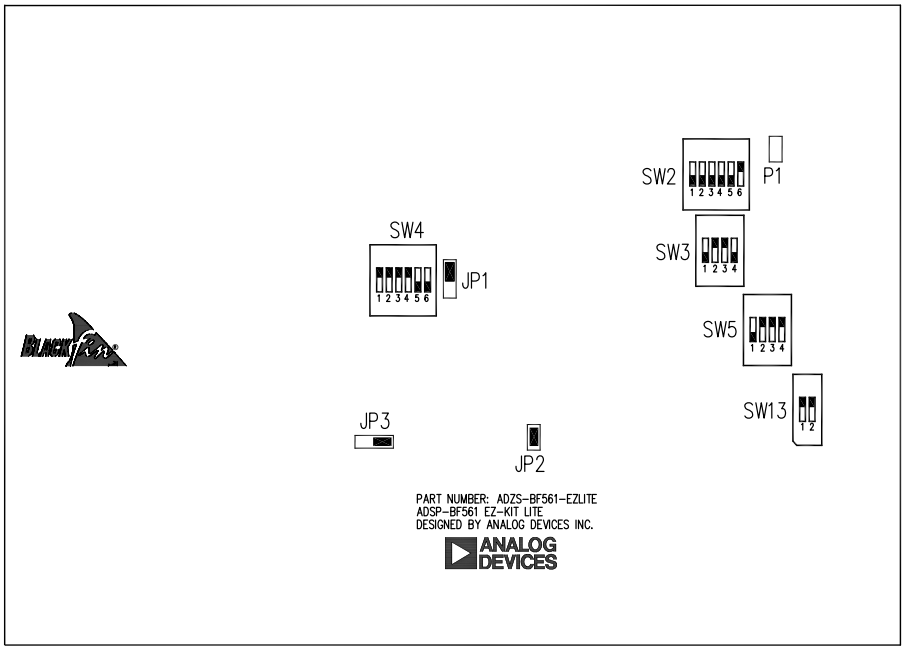


Figure 2-2. DIP Switch Locations

Video Configuration Switch (SW2)

The video configuration switch (SW2) determines how some video signals from the ADV7183A video decoder and ADV7179 video encoder are routed to the processor's PPIs. The switch also determines if the PF2 pin controls the $\overline{\text{OE}}$ signal of the ADV7183A video decoder outputs. See Table 2-4.

Table 2-4. Video Configuration Switch (SW2)

Switch Position (Default)	Processor Signal	Video Signal
1 (OFF)	PPI1 SYNC1	ADV7179
2 (OFF)	PPI0 SYNC1	ADV7183A
3 (OFF)	PPI1 SYNC2	ADV7183A
4 (OFF)	PPI1 SYNC2	ADV7179
5 (OFF)	PF3 (FIELD)	ADV7183A
6 (ON)	PF2	ADV7183A

Positions 1 thorough 5 of SW2 determine how and if the SYNC1, SYNC2, and FIELD control signals of the PPI0 and PPI1 interfaces are routed to the processor's PPIs. In standard configuration of the encoder and decoder, this is not necessary because the processor is capable of reading the control information embedded in the data stream.

Position 6 of SW2 determines whether PF2 connects to the $\overline{\text{OE}}$ signal of the ADV7183A device. When the switch is OFF, PF2 can be used for other operations, and the decoder output enable is held high with a pull-up resistor.

Boot Mode Switch (SW3)

Positions 1 and 2 of the SW3 switch set the boot mode of the processor, as described in Table 2-5. Position 3 sets the processor's PLL on boot—when the position is ON, the PLL is in bypass.

Table 2-5. Boot Mode Select Switch (SW3)

Position 1 BMODE0	Position 2 BMODE1	Boot Mode
ON	ON	Execute from 16-bit external memory (Bypass Boot ROM)
OFF	ON	Boot from 8-bit/16-bit flash (default)
ON	OFF	Boot from SPI host slave mode
OFF	OFF	Boot from SPI serial EEPROM (16-, 24-bit address range)

Push Button Enable Switch (SW4)

Positions 1 through 4 of the push button enable switch (SW4) allow to disconnect the drivers associated with the push buttons from the PF pins of the processor. Positions 5 and 6 connect the transmit and receive frame syncs and clocks of SPORT0. This is important when the AD1836A audio codec and the processor are communicating in 2-wire interface (TWI) mode. Table 2-6 shows which PF is driven when the switch is ON.

Table 2-6. Push Button Enable Switch (SW4)

Switch Position	Default Setting	Pin #	Signal (Side 1)	Pin #	Signal (Side 2)
1	ON	1	SW6	12	PF5
2	ON	2	SW7	11	PF6
3	ON	3	SW8	10	PF7
4	ON	4	SW9	9	PF8
5	OFF	5	TFS0	8	RFS0
6	OFF	6	RSCLK0	7	TSCLK0

PPI Clock Select Switch (SW5)

The SW5 switch controls a clock selection of the PPI interfaces as described in Table 2-7 and Table 2-8.

Table 2-7. PPICLK1 Clock Source Setup

SW5 Position 1 PPI0_CKSEL0	SW5 Position 2 PPI0_CKSEL1	PPIxCLK1 Source
ON	ON	27 MHz oscillator (default)
OFF	ON	ADV7183 clock out
X	OFF	Expansion interface

Table 2-8. PPICLK2 Clock Source Setup

SW5 Position 3 PPI1_CKSEL0	SW5 Position 4 PPI1_CKSEL1	PPICLK2 Source
ON	ON	27 MHz oscillator (default)
OFF	ON	ADV7183 clock out
X	OFF	Expansion interface

Test DIP Switches (SW10 and SW11)

Two DIP switches (SW10 and SW11) are located on the bottom of the board. The switches are used only for testing and should remain in the OFF position.

Audio Enable Switch (SW12)

The audio enable switch (SW12) disconnects the audio signals from the processor. The default is all positions ON.

SPIS1/SPISS Select (SW13)

The SPIS1/SPISS select switch (SW13) disconnects the SPIS1 and SPISS signals from the board, making them available on the SPI connector (P5). The default is the ON position.

Video Encoder Clock Select Jumper (JP1)

The video encoder clock select jumper (JP1) determines the source of the ADV7179 video encoder's clock. The jumper setting is shown in Table 2-9.

Table 2-9. Video Encoder Clock Select Jumper (JP1)

JP1 Position	Mode
1 and 2	**Input clock for encoder is generated from 27 MHz oscillator (default)**
2 and 3	Input clock for encoder is generated from output clock of decoder. This is used when synchronizing the encoder and decoder clock is required.

VDDINT Select Jumpers (JP2 and JP3)

The processor internal voltage (VDDINT) select jumpers (JP2-3) determine the source of the processor's internal voltage. For the core clock set at 533 MHz and higher, select the on-board external regulator for VDDINT. The jumper settings are shown in Table 2-10.

Table 2-10. Processor Internal Voltage Select Jumpers (JP2 and JP3)

JP2	JP3	VDDINT Source
Not populated	1 and 2 ON	Provided by the on-board external regulator
Populated	2 and 3 ON	Provided by the processor through the VROUT pins (internal regulator)

UART Loop Jumper (P1)

The UART loop jumper (P1) is for looping the transmit and receive signals. The default is the OFF position.

LEDs and Push Buttons

This section describes functionality of the LEDs and push buttons. Figure 2-3 shows the locations of the LEDs and push buttons.

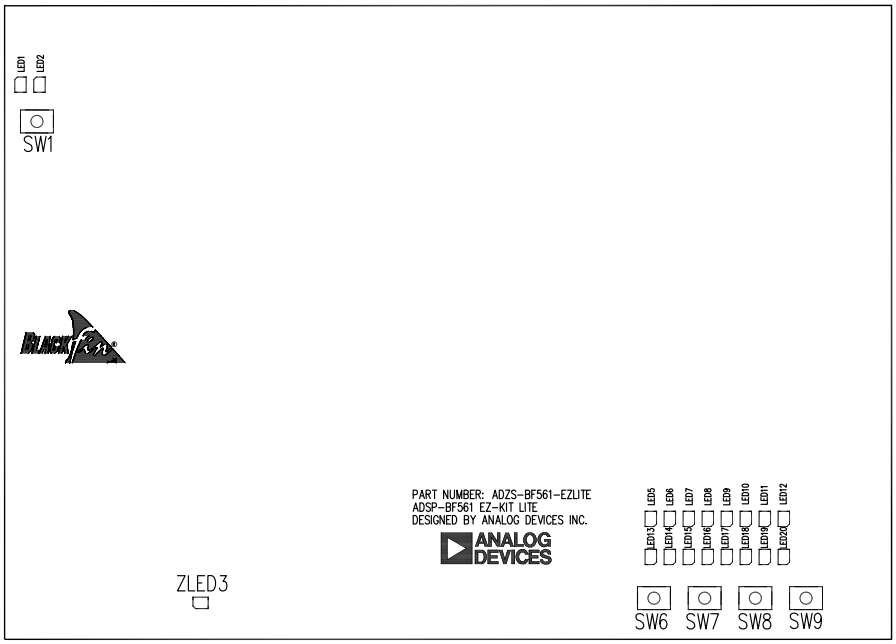


Figure 2-3. LED and Push Button Locations

Reset Push Button (SW1)

The RESET push button resets all of the ICs on the board. One exception is the USB interface chip (U34). The chip is not being reset when the push button is pressed after the USB cable has been plugged in and communication with the PC has been initialized correctly. Once communication is initialized, the only way to reset the USB is by powering down the board.

Programmable Flag Push Buttons (SW6–9)

Four push buttons, SW6-9, are provided for general-purpose user input. The buttons connect to the programmable flag pins of the processor (PF5-8). The push buttons are active high and, when pressed, send a high (1) to the processor. Refer to "LEDs and Push Buttons" on page 1-14 for more information on how to use PFs when programming the processor. The push button enable switch (SW4) is capable of disconnecting the push buttons from its associated PF (refer to "Push Button Enable Switch (SW4)" on page 2-12). The programmable flag pins and corresponding switches are shown in Table 2-11.

Table 2-11. Programmable Flag Switches

Processor Programmable Flag Pin	Push Button Reference Designator
PF5	SW6
PF6	SW7
PF7	SW8
PF8	SW9

Power LED (LED1)

When LED1 is lit (green), it indicates that power is being supplied to the board properly.

Reset LED (LED2)

When LED2 is lit, it indicates that the master reset of all major ICs is active.

USB Monitor LED (ZLED3)

The USB monitor LED (ZLED3) indicates that USB communication has been initialized successfully and you can connect to the processor using an EZ-KIT Lite session. This takes approximately 15 seconds. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver.

When the development software is actively communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.

User LEDs (LED5–12, LED13–20)

Sixteen LEDs connect to the processor's programmable flags. Eight LEDs labeled LED5 through LED12 are controlled by programmable flags PF40 through PF47 (equivalent to PPI0_D15-8). Eight LEDs labeled LED13 through LED20 are controlled by programmable flags PF32 through PF39 (equivalent to PPI1_D15-8). To learn how to use the LEDs, refer to "LEDs and Push Buttons" on page 1-14.

Table 2-12. User LEDs

LED Reference Designator	Flag Port Name	LED Reference Designator	Flag Port Name
LED5	PB40	LED13	PB32
LED6	PB41	LED14	PB33
LED7	PB42	LED15	PB34
LED8	PB43	LED16	PB35
LED9	PB44	LED17	PB36

Table 2-12. User LEDs (Cont'd)

LED Reference Designator	Flag Port Name	LED Reference Designator	Flag Port Name
LED10	PB45	LED18	PB37
LED11	PB46	LED19	PB38
LED12	PB47	LED20	PB39

Connectors

This section describes the connector functionality and provides information about mating connectors. The connector locations are shown in Figure 2-4.

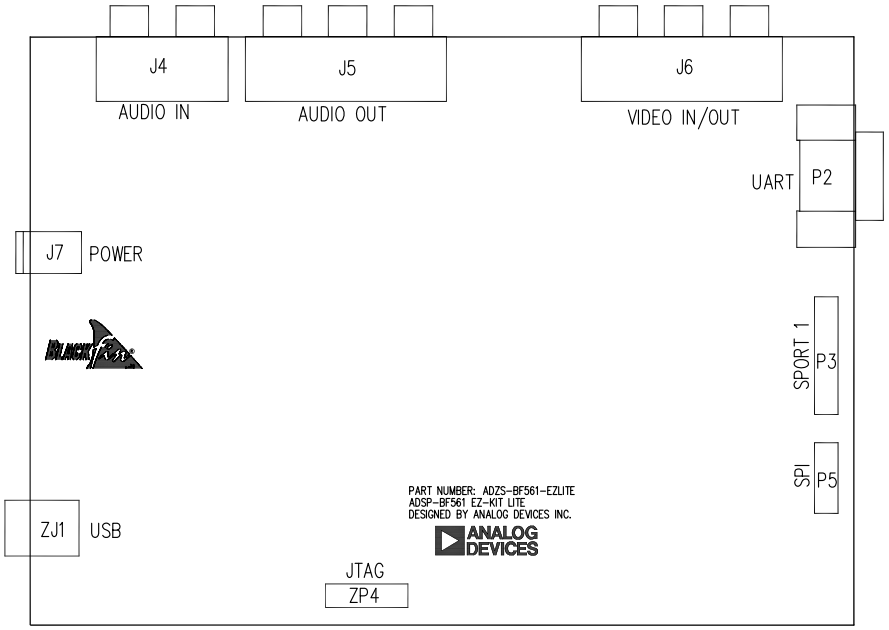


Figure 2-4. Connector Locations

Expansion Interface (J1–3)

Three board-to-board connector footprints provide signals for most of the processor's peripheral interfaces. The connectors are located at the bottom of the board. For more information about the interface, see "Expansion Interface" on page 2-8. For the availability and pricing of the J1, J2, and J3 connectors, contact Samtec.

Part Description	Manufacturer	Part Number
90-position 0.05" spacing, SMT (J1, J2, J3)	SAMTEC	SFC-145-T2-F-D-A
Mating Connector		
90-position 0.05" spacing (through hole)	SAMTEC	TFM-145-x1 series
90-position 0.05" spacing (surface mount)	SAMTEC	TFM-145-x2 series
90-position 0.05" spacing (low cost)	SAMTEC	TFC-145 series

Audio (J4 and J5)

Part Description	Manufacturer	Part Number
2x2 RCA jacks (J4)	SWITCHCRAFT	PJRAS2X2S01X
3x2 RCA jacks (J5)	SWITCHCRAFT	PJRAS3X2S01X
Mating Connector		
Two channel RCA interconnect cable	MONSTER CABLE	BI100-1M

Video (J6)

Part Description	Manufacturer	Part Number
3x2 RCA jacks (J6)	SWITCHCRAFT	PJRAS3X2S01X

Power (J7)

The power connector provides all of the power necessary to operate the EZ-KIT Lite board.

Part Description	Manufacturer	Part Number
2.5 mm power jack (J7)	SWITCHCRAFT	RAPC712X
Mating Power Supply (shipped with EZ-KIT Lite)		
7V power supply	CUI INC.	DMS070214-P6P-SZ

The power connector supplies DC power to the EZ-KIT Lite board.

RS-232 (P2)

Part Description	Manufacturer	Part Number
DB9, male, right angle (P2)	TYCO	5747250-4
Mating Assembly		
2m female-to-female cable	DIGI-KEY	AE1016-ND

SPORT1 (P3)

The SPORT1 connector is linked to a 20-pin connector. The connector's pinout can be found in "ADSP-BF561 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-420HLF
Mating Connectors		
IDC socket	DIGI-KEY	S4210-ND

SPI (P5)

The SPI connector is linked to a 12-pin connector. The connector's pinout can be found in "ADSP-BF561 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	SULLINS	GEC06DAAN
Mating Assembly		
IDC socket	DIGI-KEY	S4207-ND

USB Debug Agent Connector (ZJ1)

The USB debug agent connector is the connecting point for the JTAG USB debug agent interface. The JTAG header (ZP4) should not be used whenever ZJ1 and its mating cable are used to communicate to the processor via CCES or VisualDSP++.

JTAG (ZP4)

The JTAG header is the connecting point for a JTAG in-circuit emulator pod. When an emulator connects to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

A ADSP-BF561 EZ-KIT LITE BILL OF MATERIALS

The bill of materials corresponds to "ADSP-BF561 EZ-KIT Lite Schematic" on page B-1.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	1	74LVC14A SOIC14	U47	TI	74LVC14AD
2	2	IDT74FCT3244 APY SSOP20	U13,U30	IDT	IDT74FCT3244APYG
3	1	12.288MHZ OSC003	U16	EPSON	SG-8002CA MP
4	1	NDS8434A SO-8	U29	FAIRCHILD	NDS8434A
5	2	MT48LC16M16 A2TG-75 TSOP54	U32-33	MICRON	MT48LC16M16A2P-75
6	1	27MHZ OSC003	U17	EPSON	SG-8002CA MP
7	2	IDT2305-1DC SOIC8	U19-20	INTE-GRATED SYS	ICS9112AM-16LFT
8	1	SN74LVC1G32 SOT23-5	U10	TI	SN74LVC1G32DBVR
9	1	30MHZ OSC003	U14	EPSON	SG-8002CA MP
10	1	BF561 M29W640D "U27"	U27	ST MICRO	M29W640DT 90N6E
11	2	FDC658P SOT23-6	U28,U49	FAIRCHILD	FDC658P

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
12	1	ADM708SARZ SOIC8	U46	ANALOG DEVICES	ADM708SARZ
13	1	ADP3338AKCZ-33 SOT-223	VR3	ANALOG DEVICES	ADP3338AKCZ-3.3-RL
14	1	ADP3339AKCZ-5 SOT-223	VR1	ANALOG DEVICES	ADP3339AKCZ-5-R7
15	1	ADP3336ARMZ MSOP8	VR2	ANALOG DEVICES	ADP3336ARMZ-REEL7
16	1	10MA AD1580BRTZ SOT23D	D1	ANALOG DEVICES	AD1580BRTZ-REEL7
17	4	ADG752BRTZ SOT23-6	U22-23,U25-26	ANALOG DEVICES	ADG752BRTZ-REEL
18	3	AD8061ARTZ SOT23-5	U1-3	ANALOG DEVICES	AD8061ARTZ-R2
19	1	ADM3202ARNZ SOIC16	U21	ANALOG DEVICES	ADM3202ARNZ
20	8	AD8606ARZ SOIC8	U5-7,U9,U11-12, U18,U24	ANALOG DEVICES	AD8606ARZ
21	1	AD1836AASZ MQFP52	U15	ANALOG DEVICES	AD1836AASZ
22	1	ADSP-BF561SK BCZ MBGA256	U48	ANALOG DEVICES	ADSP-BF561SKBCZ-6V
23	1	ADV7179KCPZ LFCSP40	U8	ANALOG DEVICES	ADV7179KCPZ
24	1	ADV7183BKSTZ LQFP80	U4	ANALOG DEVICES	ADV7183BKSTZ
25	2	ADP1864AUJZ SOT23-6	VR5-6	ANALOG DEVICES	ADP1864AUJZ-R7
26	5	RUBBER FOOT	M1-5	MOUSER	517-SJ-5018BK

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
27	1	PWR 2.5MM_JACK CON005	J7	SWITCH-CRAFT	RAPC712X
28	1	RCA 2X2 CON013	J4	SWITCH-CRAFT	PJRAS2X2S01X
29	5	MOMENTARY SWT013	SW1,SW6-9	PANASONIC	EVQ-PAD04M
30	3	.05 45X2 CON019	J1-3	SAMTEC	SFC-145-T2-F-D-A
31	3	DIP6 SWT017	SW2,SW4,SW10	CTS	218-6LPST
32	2	RCA 3X2 CON024	J5-6	SWITCH-CRAFT	PJRAS3X2S01X
33	4	DIP4 SWT018	SW3,SW5,SW11-12	ITT	TDA04HOSB1
34	1	DIP2 SWT020	SW13	C&K	CKN9064-ND
35	1	IDC 2X1 IDC2X1	P1	FCI	90726-402HLF
36	1	IDC 2X1 IDC2X1	JP2	FCI	90726-402HLF
37	2	IDC 3X1 IDC3X1	JP1,JP3	FCI	90726-403HLF
38	1	IDC 10X2 IDC10X2	P3	BURG-FCI	54102-T08-10LF
39	4	IDC 2PIN_JUMPER_SHORT	SJ1-4	DIGI-KEY	S9001-ND
40	1	DB9 9PIN DB9M	P2	TYCO	5747250-4
41	1	IDC 6X2 IDC6X2	P5	FCI	68737-412HLF
42	1	5A RESETABLE FUS005	F1	MOUSER	650-RGEF500

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
43	14	0 1/4W 5% 1206	R43-44,R55,R71, R73,R83,R133, R159,R163,R223-225,R247,R257	KOA	0.0ECTRk7372 BTTED
44	16	YELLOW LED001	LED5-20	PANASONIC	LN1461C
45	12	330PF 50V 5% 0805	C82,C84,C86, C92-100	AVX	08055A331JAT
46	48	0.01UF 100V 10% 0805	C3,C5,C28,C41, C49,C69-70,C74-75, C101,C112-114, C127,C134,C136-138,C140-141,C146, C149-150,C154, C156-157,C165-166, C168,C173-174, C176,C181-182, C185-188,C190, C192-194,C200-203, C249,C256	AVX	08051C103KAT2A
47	8	0.22UF 25V 10% 0805	C104,C106-108, C125,C129,C143, C162	AVX	08053C224KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
48	69	0.1UF 50V 10% 0805	C1-2,C4,C12,C19-20,C22,C27,C29-30,C35,C37,C48,C51-52,C54-60,C65-66,C71,C73,C83,C85,C87-91,C102,C109-111,C115,C122-124,C126,C131-132,C135,C139,C145,C147-148,C151-152,C155,C158-159,C164,C167,C171-172,C175,C177-179,C183-184,C189,C191,C196,C198-199	AVX	08055C104KAT
49	10	1000PF 50V 5% 0805	C23,C25,C33,C36,C38-40,C67-68,C133	AVX	08055A102JAT2A
50	3	10UF 16V 10% C	CT17,CT23-24	SPRAGUE	293D106X9016C2TE3
51	43	10K 1/10W 5% 0805	R2,R7,R11-12,R14,R24,R42,R45-47,R52,R57,R85,R87-88,R98,R131,R143,R158,R160-162,R167-170,R174-177,R181-183,R189-190,R196,R229,R239,R246,R248-251	VISHAY	CRCW080510K0 JNEA
52	9	33 1/10W 5% 0805	R39,R41,R59-61,R165-166,R171-172	VISHAY	CRCW080533R0 JNEA
53	2	4.7K 1/10W 5% 0805	R86,R90	VISHAY	CRCW08054K70 JNEA
54	1	1.5K 1/10W 5% 0805	R1	VISHAY	CRCW08051K50 FKEA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
55	1	1.2K 1/8W 5% 1206	R23	VISHAY	CRCW12061K20 JNEA
56	6	49.9K 1/8W 1% 1206	R108-113	VISHAY	CRCW120649K9 FKEA
57	12	100PF 100V 5% 1206	C6-11,C26,C34, C61-63,C72	AVX	12061A101JAT2A
58	6	10UF 16V 10% B	CT1-4,CT15-16	AVX	TAJB106K016R
59	4	100 1/10W 5% 0805	R242-245	VISHAY	CRCW0805100 RJNEA
60	6	220PF 50V 10% 1206	C13-18	AVX	12061A221JAT2A
61	4	600 100MHZ 200MA 0603	FER18-21	DIGI-KEY	490-1014-2-ND
62	1	2A S2A DO-214AA	D7	VISHAY	S2A-E3
63	12	600 100MHZ 500MA 1206	FER2-4,FER6,FER8-12,FER14-16	STEWARD	HZ1206B601R-10
64	4	237.0 1/8W 1% 1206	R25-26,R53-54	VISHAY	CRCW1206237 RFKEA
65	4	750.0K 1/8W 1% 1206	R132,R156,R164, R173	VISHAY	CRCW1206750 KFKEA
66	16	5.76K 1/8W 1% 1206	R8,R15-16,R40,R49-50,R58,R62-64,R69-70,R121-124	VISHAY	CRCW12065K76 FKEA
67	6	11.0K 1/8W 1% 1206	R144-149	VISHAY	CRCW120611K0 FKEA
68	8	120PF 50V 5% 1206	C103,C105,C128, C130,C142,C144, C161,C163	AVX	12065A121JAT2A
69	12	75 1/8W 5% 1206	R4-6,R100-102, R104-105,R107, R114,R134-135	VISHAY	CRCW120675R0 JNEA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
70	1	68UF 6.3V 20% D	CT22	AVX	TAJD686K016R
71	6	680PF 50V 1% 0805	C116-121	AVX	08055A681FAT2A
72	5	10UF 25V +80-20% 1210	C31,C47,C50,C195, C197	DIGI-KEY	587-1393-2-ND
73	6	2.74K 1/8W 1% 1206	R150-155	VISHAY	CRCW12062K74 FKEA
74	12	5.49K 1/8W 1% 1206	R17-22,R27,R30-31, R34-35,R38	VISHAY	CRCW12065K49 FKEA
75	6	3.32K 1/8W 1% 1206	R137-142	VISHAY	CRCW12063K32 FKEA
76	6	1.65K 1/8W 1% 1206	R28-29,R32-33,R36-37	VISHAY	CRCW12061K65 FKEA
77	10	10UF 16V 20% CAP002	CT5-14	PANASONIC	EEE1CA100SR
78	1	10UH 20% IND001	L11	TDK	445-2014-1-ND
79	6	0 1/10W 5% 0805	R66,R99,R103, R106,R178,R192	VISHAY	CRCW08050000 Z0EA
80	1	190 100MHZ 5A FER002	FER22	MURATA	DLW5BSN191SQ2
81	4	22 1/10W 5% 0805	R67-68,R187-188	VISHAY	541-22ATR-ND
82	6	0.68UH 10% 0805	L1-4,L6,L8	MURATA	LQM21NNR68K10D
83	1	.082UF 50V 5% 0805	C64	AVX	08055C823JAT2A
84	1	1A ZHCS1000 SOT23-312	D5	ZETEX	ZHCS1000TA pb-free
85	3	2.2UH 10% 0805	L5,L7,L9	DIGI-KEY	490-1119-2-ND

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
86	3	1UF 10V 10% 0805	C21,C24,C32	AVX	0805ZC105KAT2A
87	1	76.8K 1/10W 1% 1206	R48	VISHAY	CRCW120676K8 FKEA
88	1	147.0K 1/10W 1% 1206	R56	VISHAY	CRCW1206147 KFKEA
89	10	10 62.5MW 5% RNS006	RN1,RN4-12	PANASONIC	EXB-38V100JV
90	2	68PF 50V 5% 0603	C160,C257	AVX	06035A680JAT2A
91	2	470PF 50V 5% 0603	C153,C258	AVX	06033A471JAT2A
92	2	0 1/10W 5% 0603	R74,R254	PHYCOMP	232270296001L
93	2	24.9K 1/10W 1% 0603	R72,R256	DIGI-KEY	311-24.9KHTR-ND
94	2	10UF 16V 10% 1210	C169,C260	AVX	1210YD106KAT2A
95	1	680 1/8W 5% 1206	R119	VISHAY	CRCW1206680RFNEA
96	1	150.0 1/8W 1% 1206	R3	VISHAY	CRCW1206150RFKEA
97	1	GREEN LED001	LED1	PANASONIC	LN1361CTR
98	1	RED LED001	LED2	PANASONIC	LN1261CTR
99	2	1000PF 50V 5% 1206	C43,C46	AVX	12065A102JAT2A
100	6	2200PF 50V 5% 1206	C76-81	AVX	12065A222JAT050
101	6	1K 1/8W 5% 1206	R10,R115-118,R136	VISHAY	CRCW12061K00 FKEA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
102	2	100K 1/8W 5% 1206	R9,R13	VISHAY	CRCW1206100K FKEA
103	17	270 1/8W 5% 1206	R120,R213-220, R230-237	VISHAY	CRCW1206270 RJNEA
104	6	604.0 1/8W 1% 1206	R125-130	VISHAY	CRCW1206604R FKEA
105	4	1UF 20V 20% A	CT25-28	AVX	TAJA105K020R
106	1	255.0K 1/10W 1% 0603	R89	VISHAY	CRCW06032553FK
107	2	80.6K 1/10W 1% 0603	R80,R255	DIGI-KEY	311-80.6KHRCT-ND
108	2	6.8UH 25% IND009	L10,L12	DIGI-KEY	308-1328-1-ND
109	2	4A SSB43L DO-214AA	D4,D8	VISHAY	SSB43L
110	2	5A MBRS540T3G SMC	D2-3	ON SEMI	MBRS540T3G
111	1	0.027 1/2W 1% 1206	R79	SUSUMU	RL1632T-R027-F-N
112	1	54.9K 1/10W 1% 0603	R252	VISHAY	CRCW060354K9 FKEA
113	1	0.047 1/2W 1% 1206	R253	SUSUMU	RL1632S-R047-F
114	2	100UF 6.3V 20%C	CT19,CT29	SANYO	6TPB100MC

2

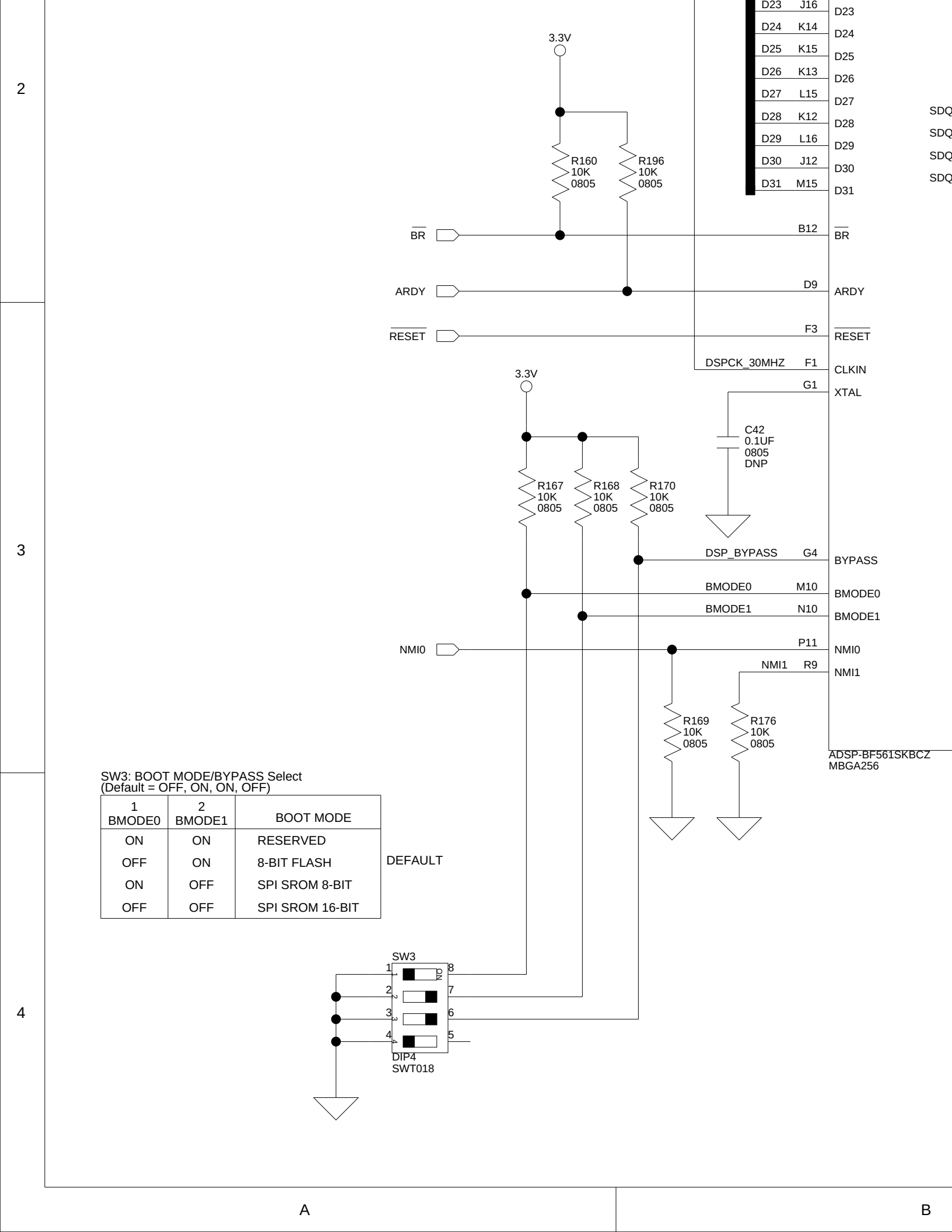
3

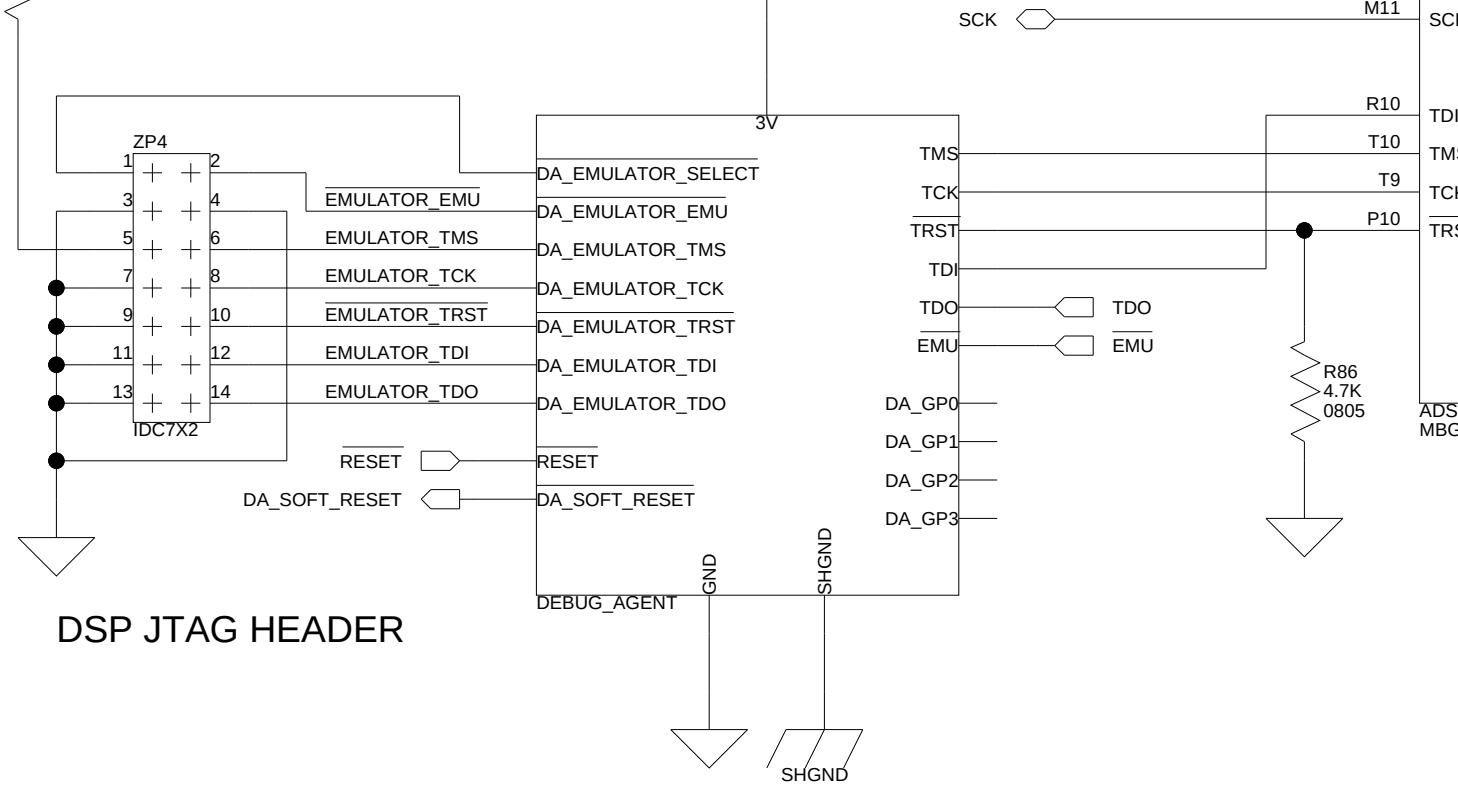
4

ADSP

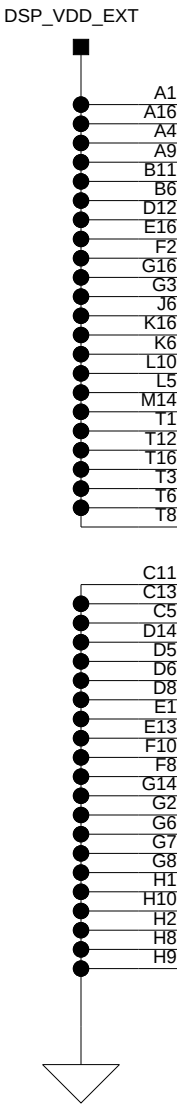
A

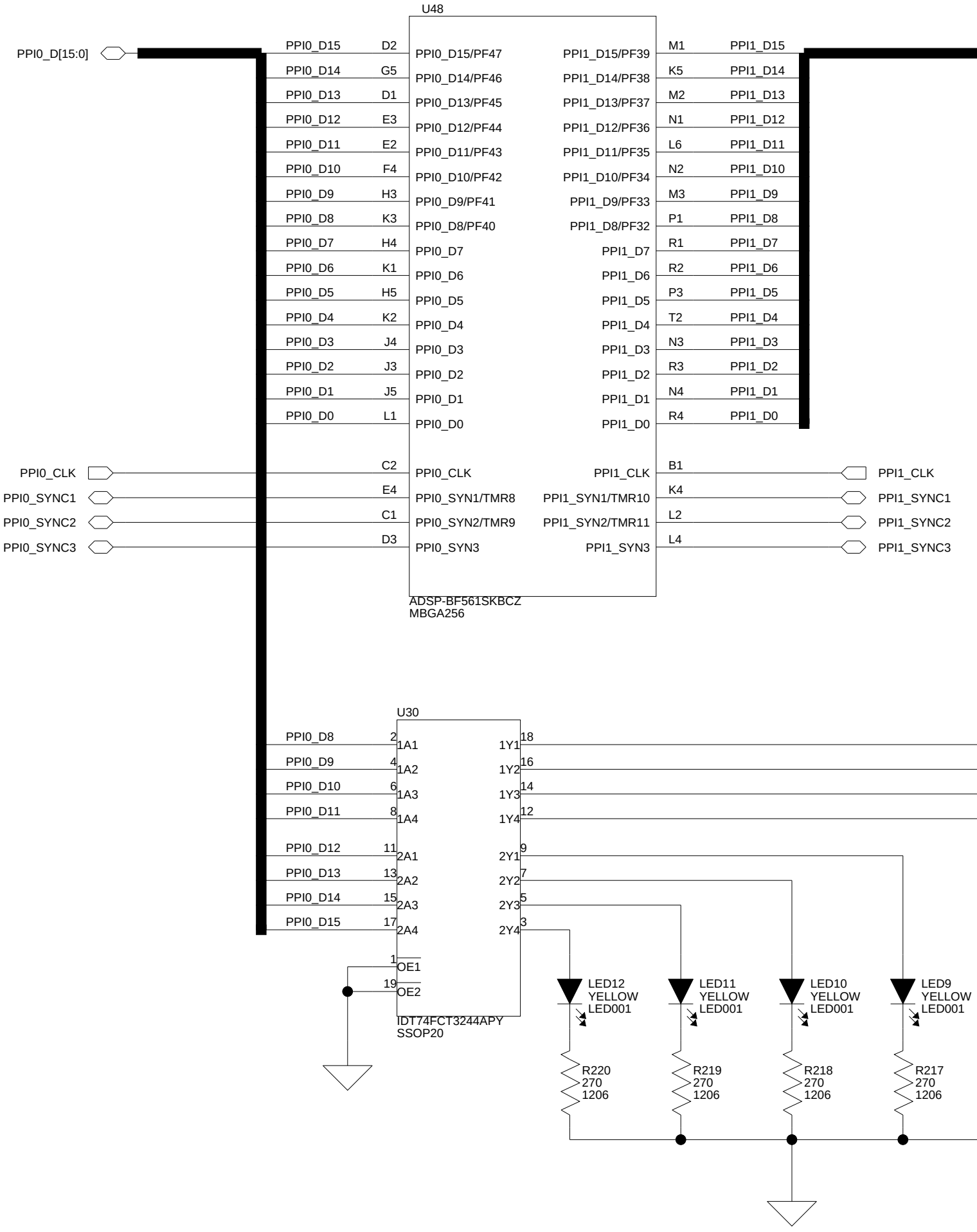
B

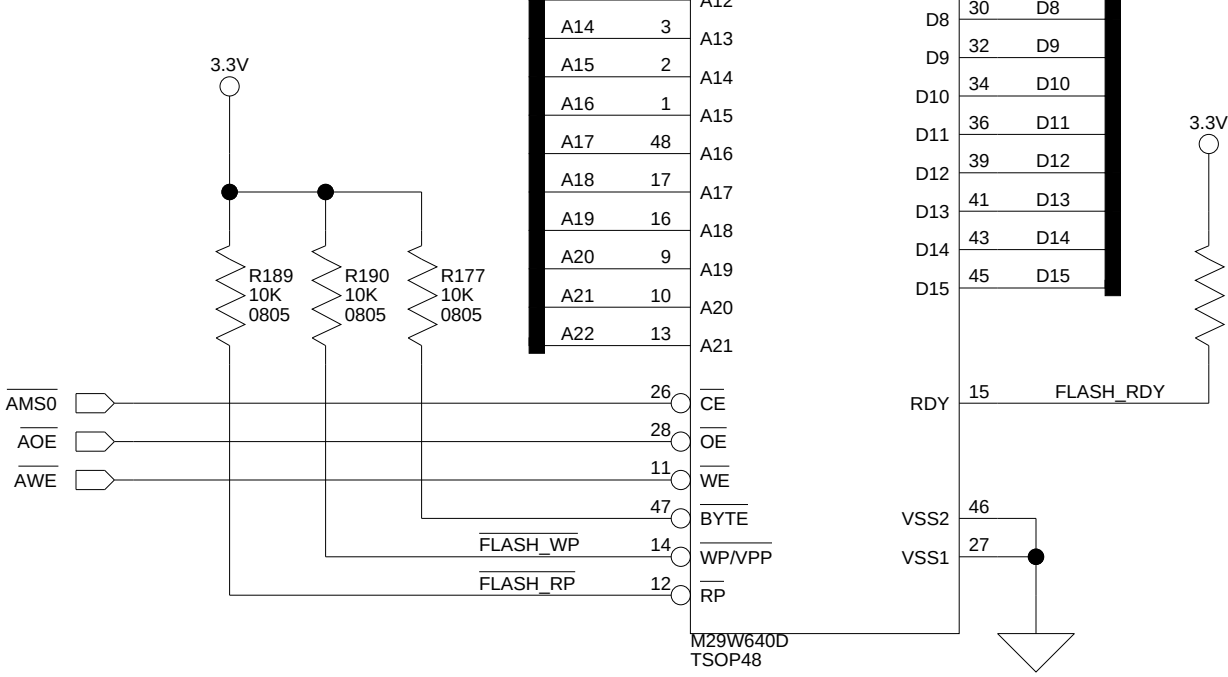

3.3V
R160
10K
0805
R196
10K
0805
BR
ARDY
RESET
D23 J16 D23
D24 K14 D24
D25 K15 D25
D26 K13 D26
D27 L15 D27
D28 K12 D28
D29 L16 D29
D30 J12 D30
D31 M15 D31
SDQ
SDQ
SDQ
SDQ
B12 BR
D9 ARDY
F3 RESET
DSPCK_30MHZ F1 CLKIN
G1 XTAL
3.3V
C42
0.1UF
0805
DNP
R167
10K
0805
R168
10K
0805
R170
10K
0805
DSP_BYPASS G4 BYPASS
BMODE0 M10 BMODE0
BMODE1 N10 BMODE1
NMI0
P11 NMI0
NMI1 R9 NMI1
R169
10K
0805
R176
10K
0805
ADSP-BF561SKBCZ
MBGA256
SW3: BOOT MODE/BYPASS Select
(Default = OFF, ON, ON, OFF)
1 BMODE0
2 BMODE1
BOOT MODE
ON ON RESERVED
OFF ON 8-BIT FLASH
DEFAULT
ON OFF SPI SROM 8-BIT
OFF OFF SPI SROM 16-BIT
SW3
ON
1 8
2 7
3 6
4 5
DIP4
SWT018
2
3
4
A
B



DSP JTAG HEADER

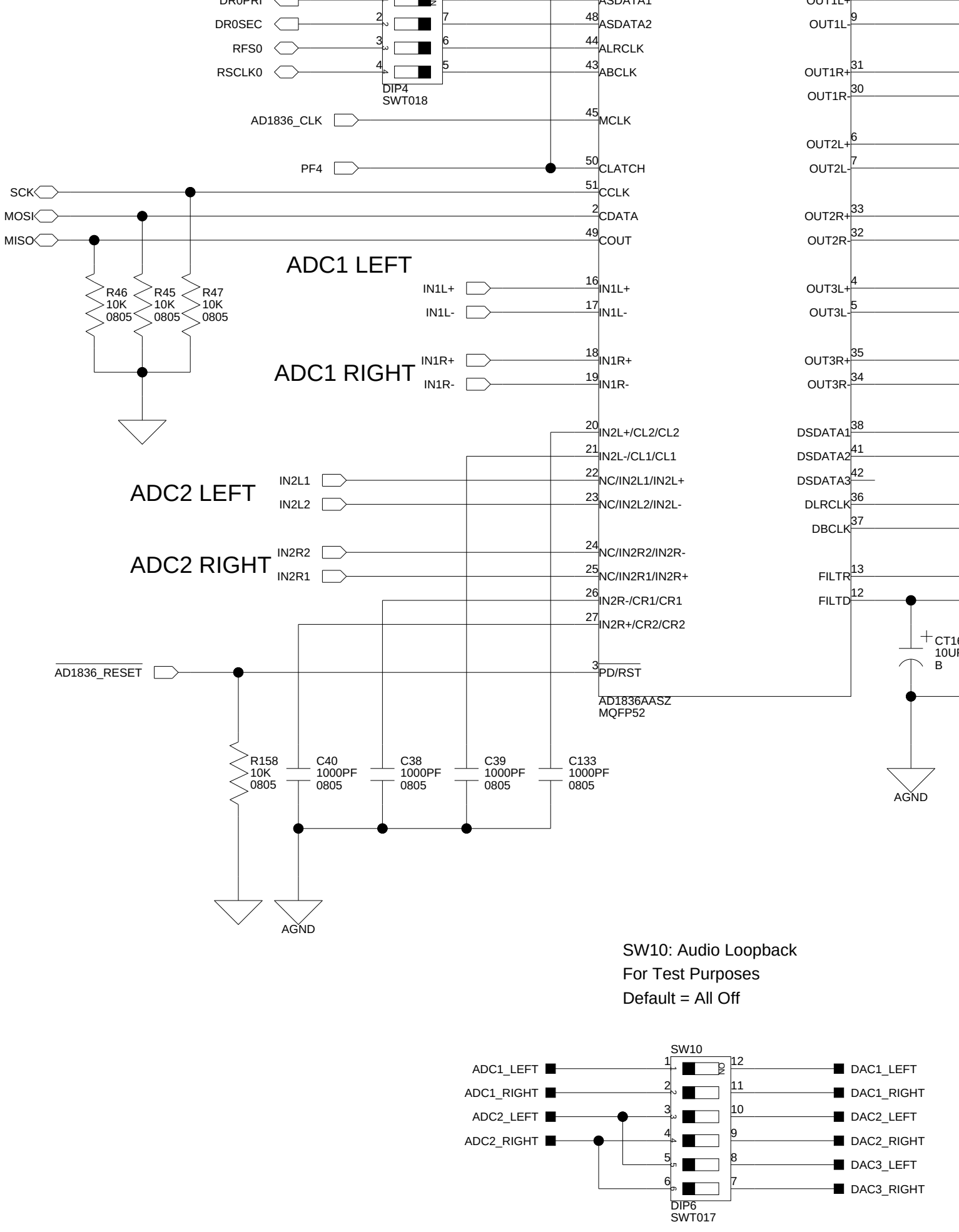


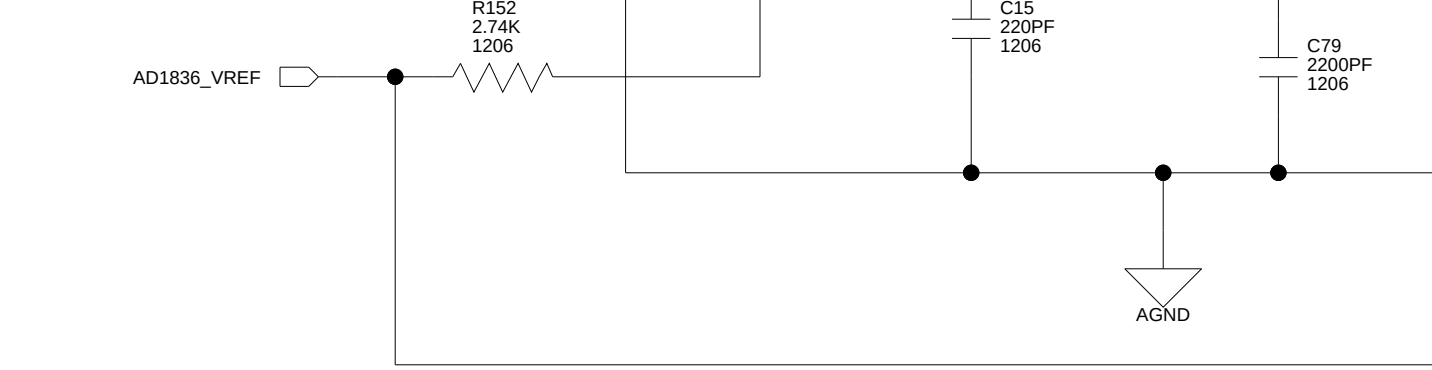

U48
PPI0_D[15:0]
PPI0_D15 D2
PPI0_D14 G5
PPI0_D13 D1
PPI0_D12 E3
PPI0_D11 E2
PPI0_D10 F4
PPI0_D9 H3
PPI0_D8 K3
PPI0_D7 H4
PPI0_D6 K1
PPI0_D5 H5
PPI0_D4 K2
PPI0_D3 J4
PPI0_D2 J3
PPI0_D1 J5
PPI0_D0 L1
PPI0_D15/PF47
PPI0_D14/PF46
PPI0_D13/PF45
PPI0_D12/PF44
PPI0_D11/PF43
PPI0_D10/PF42
PPI0_D9/PF41
PPI0_D8/PF40
PPI0_D7
PPI0_D6
PPI0_D5
PPI0_D4
PPI0_D3
PPI0_D2
PPI0_D1
PPI0_D0
PPI1_D15/PF39
PPI1_D14/PF38
PPI1_D13/PF37
PPI1_D12/PF36
PPI1_D11/PF35
PPI1_D10/PF34
PPI1_D9/PF33
PPI1_D8/PF32
PPI1_D7
PPI1_D6
PPI1_D5
PPI1_D4
PPI1_D3
PPI1_D2
PPI1_D1
PPI1_D0
M1 PPI1_D15
K5 PPI1_D14
M2 PPI1_D13
N1 PPI1_D12
L6 PPI1_D11
N2 PPI1_D10
M3 PPI1_D9
P1 PPI1_D8
R1 PPI1_D7
R2 PPI1_D6
P3 PPI1_D5
T2 PPI1_D4
N3 PPI1_D3
R3 PPI1_D2
N4 PPI1_D1
R4 PPI1_D0
PPI0_CLK
PPI0_SYNC1
PPI0_SYNC2
PPI0_SYNC3
C2 PPI0_CLK
E4 PPI0_SYN1/TMR8
C1 PPI0_SYN2/TMR9
D3 PPI0_SYN3
PPI1_CLK
PPI1_SYN1/TMR10
PPI1_SYN2/TMR11
PPI1_SYN3
B1 PPI1_CLK
K4 PPI1_SYNC1
L2 PPI1_SYNC2
L4 PPI1_SYNC3
ADSP-BF561SKBCZ
MBGA256
U30
PPI0_D8 2 1A1
PPI0_D9 4 1A2
PPI0_D10 6 1A3
PPI0_D11 8 1A4
PPI0_D12 11 2A1
PPI0_D13 13 2A2
PPI0_D14 15 2A3
PPI0_D15 17 2A4
1 OE1
19 OE2
1Y1 18
1Y2 16
1Y3 14
1Y4 12
2Y1 9
2Y2 7
2Y3 5
2Y4 3
IDT74FCT3244APY
SSOP20
LED12 YELLOW LED001
LED11 YELLOW LED001
LED10 YELLOW LED001
LED9 YELLOW LED001
R220 270 1206
R219 270 1206
R218 270 1206
R217 270 1206

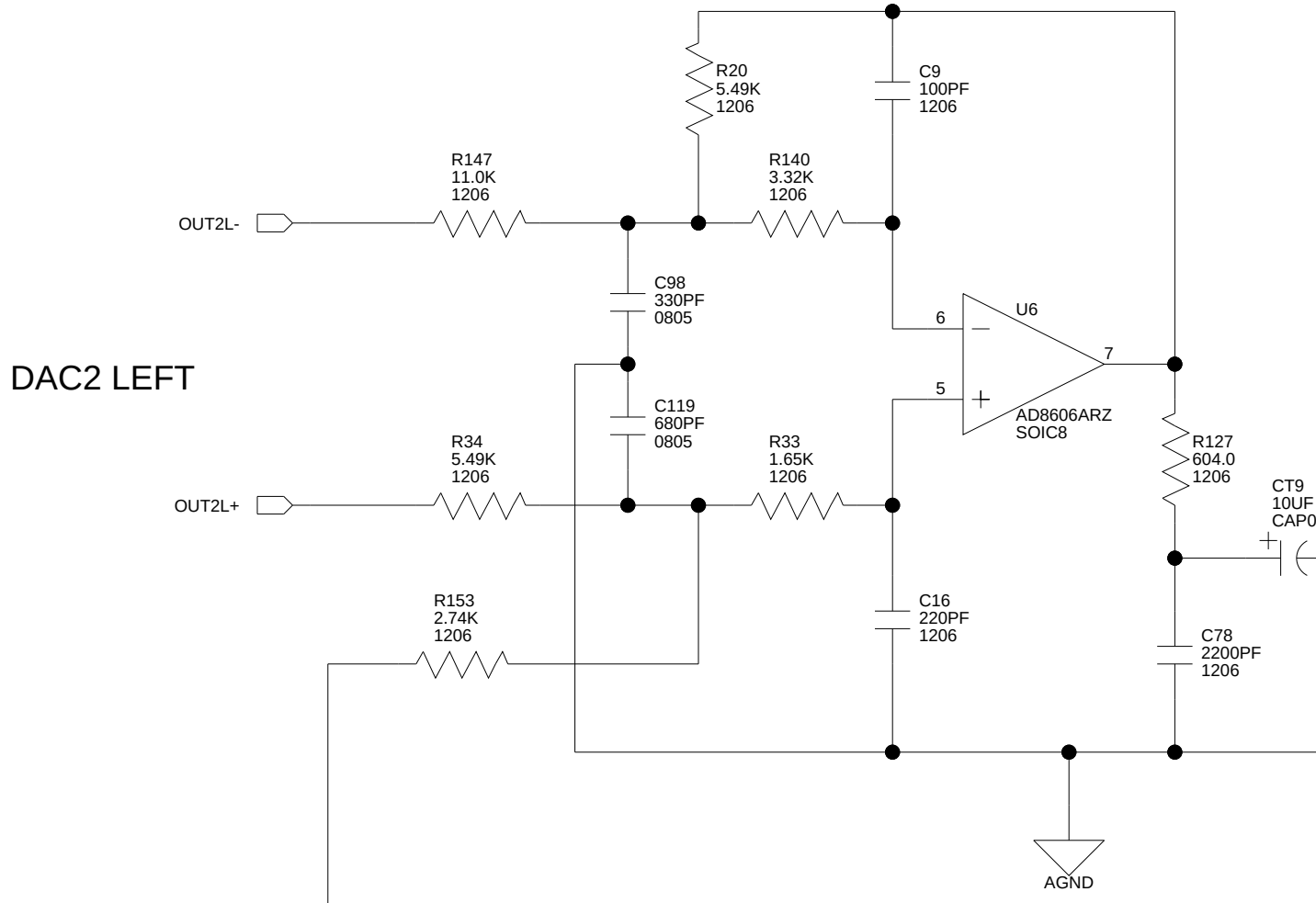


Memory Map

START	END	BANK	DEVICE
0x0000 0000	0x03FF FFFF	SDRAM Bank 0	64MB SDRAM
0x2000 0000	0x207F FFFF	ASYNC Memory Bank 0	8MB FLASH


DR0PRI
DR0SEC
RFS0
RSCLK0
DIP4
SWT018
AD1836_CLK
PF4
SCK
MOSI
MISO
R46
10K
0805
R45
10K
0805
R47
10K
0805
ADC1 LEFT
ADC1 RIGHT
ADC2 LEFT
ADC2 RIGHT
IN1L+
IN1L-
IN1R+
IN1R-
IN2L1
IN2L2
IN2R2
IN2R1
AD1836_RESET
R158
10K
0805
C40
1000PF
0805
C38
1000PF
0805
C39
1000PF
0805
C133
1000PF
0805
AGND
ASDATA1
ASDATA2
ALRCLK
ABCLK
MCLK
CLATCH
CCLK
CDATA
COUT
IN1L+
IN1L-
IN1R+
IN1R-
IN2L+/CL2/CL2
IN2L-/CL1/CL1
NC/IN2L1/IN2L+
NC/IN2L2/IN2L-
NC/IN2R2/IN2R-
NC/IN2R1/IN2R+
IN2R-/CR1/CR1
IN2R+/CR2/CR2
PD/RST
AD1836AASZ
MQFP52
OUT1L+
OUT1L-
OUT1R+
OUT1R-
OUT2L+
OUT2L-
OUT2R+
OUT2R-
OUT3L+
OUT3L-
OUT3R+
OUT3R-
DSDATA1
DSDATA2
DSDATA3
DLRCLK
DBCLK
FILTR
FILTD
AGND
SW10: Audio Loopback
For Test Purposes
Default = All Off
SW10
ADC1_LEFT
ADC1_RIGHT
ADC2_LEFT
ADC2_RIGHT
DAC1_LEFT
DAC1_RIGHT
DAC2_LEFT
DAC2_RIGHT
DAC3_LEFT
DAC3_RIGHT
DIP6
SWT017





DAC2 LEFT

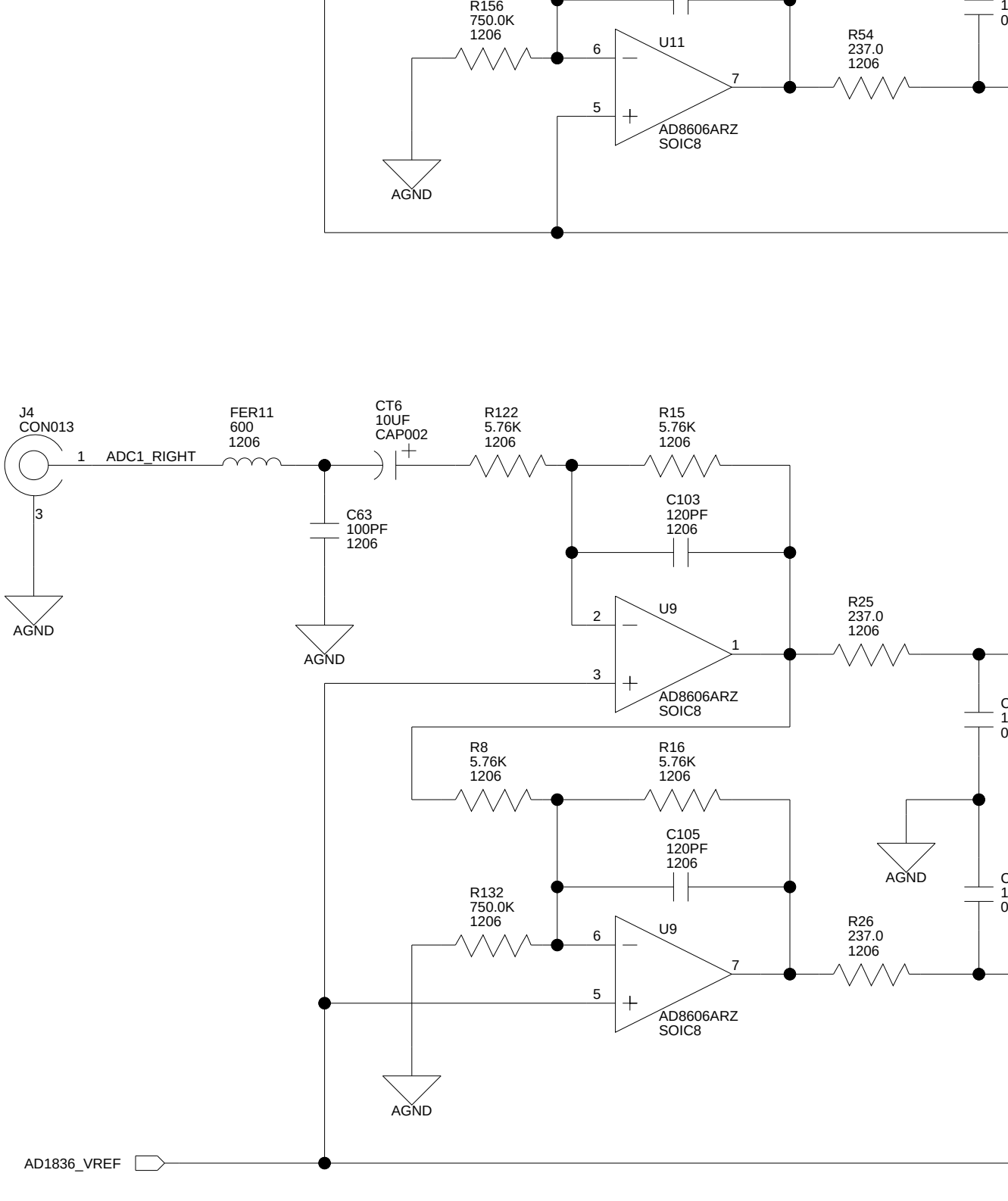
2

3

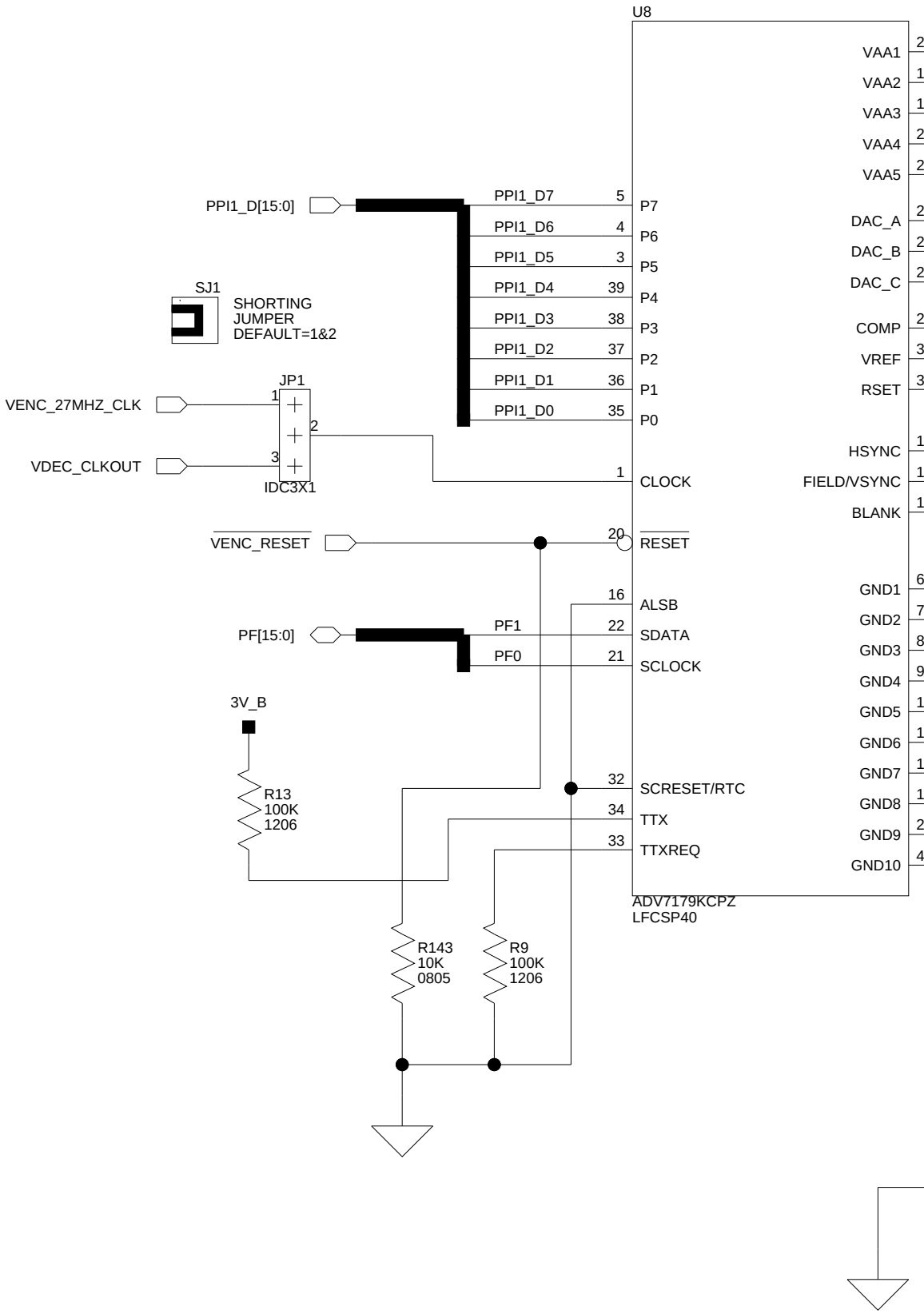
4

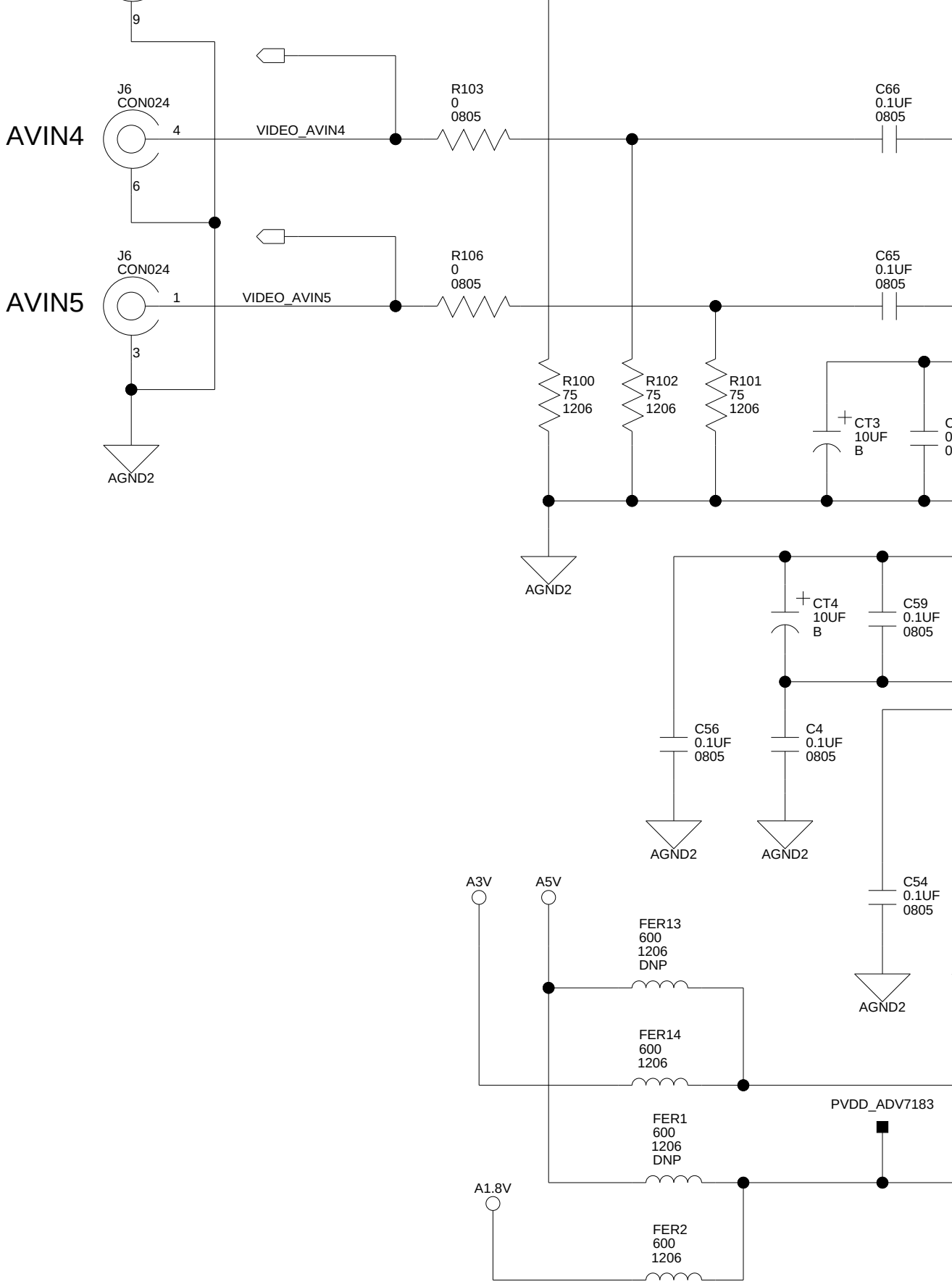
A

B


R156
750.0K
1206
6
U11
7
5
AD8606ARZ
SOIC8
R54
237.0
1206
AGND
J4
CON013
1
ADC1_RIGHT
FER11
600
1206
CT6
10UF
CAP002
R122
5.76K
1206
R15
5.76K
1206
3
C63
100PF
1206
C103
120PF
1206
AGND
AGND
2
U9
1
3
AD8606ARZ
SOIC8
R25
237.0
1206
R8
5.76K
1206
R16
5.76K
1206
C105
120PF
1206
AGND
R132
750.0K
1206
6
U9
7
5
AD8606ARZ
SOIC8
R26
237.0
1206
AGND
AD1836_VREF

VIDEO ENCODER




AVIN4
J6
CON024
4
6
VIDEO_AVIN4
R103
0
0805
C66
0.1UF
0805
AVIN5
J6
CON024
1
3
VIDEO_AVIN5
R106
0
0805
C65
0.1UF
0805
R100
75
1206
R102
75
1206
R101
75
1206
CT3
10UF
B
AGND2
CT4
10UF
B
C59
0.1UF
0805
C56
0.1UF
0805
C4
0.1UF
0805
C54
0.1UF
0805
A3V
A5V
FER13
600
1206
DNP
FER14
600
1206
PVDD_ADV7183
FER1
600
1206
DNP
A1.8V
FER2
600
1206

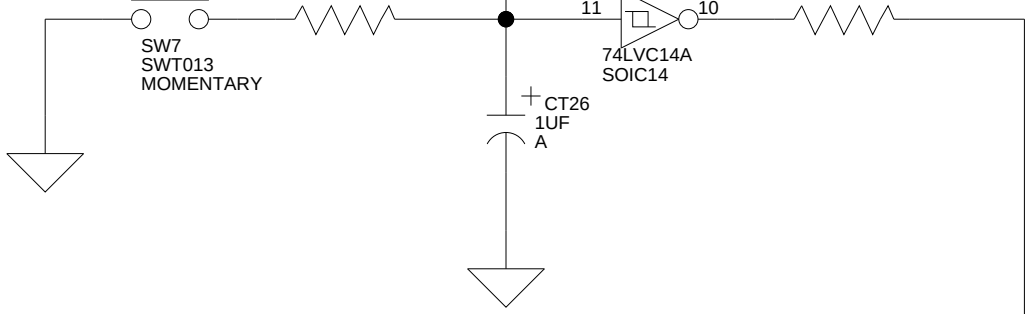
2

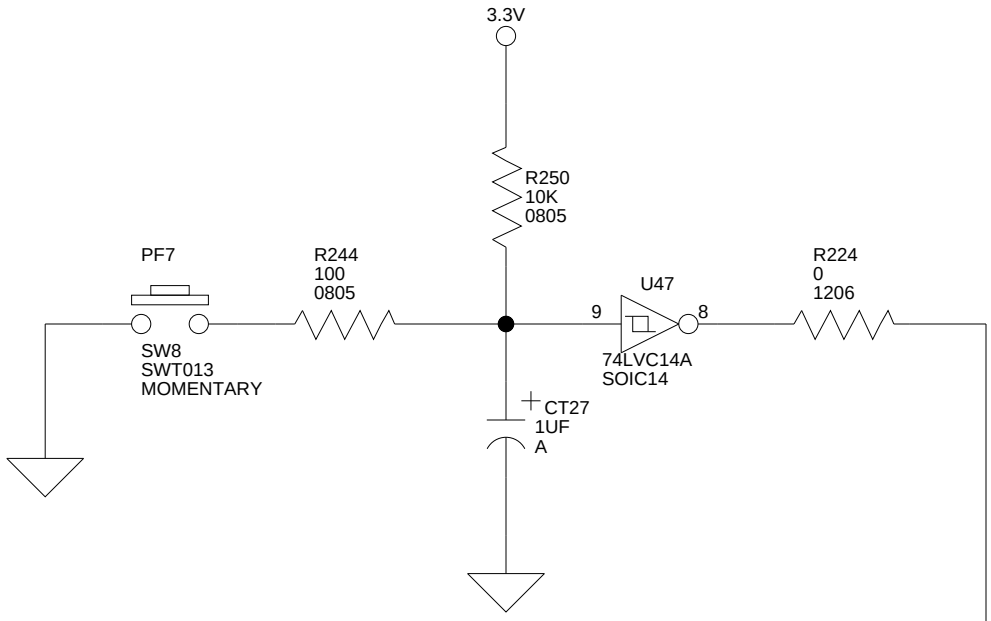
3

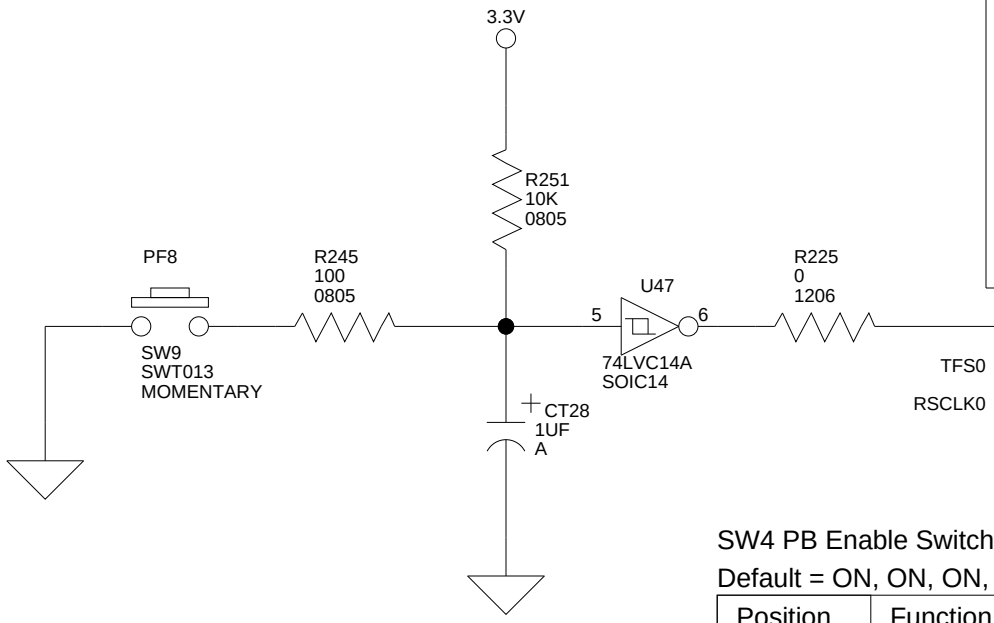
4

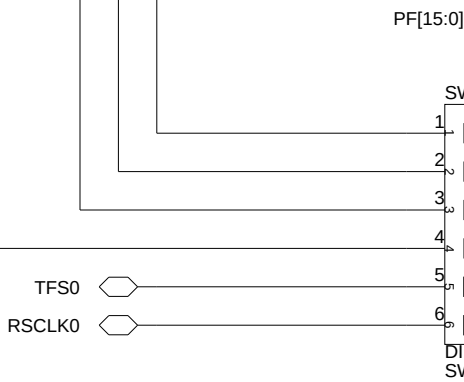
A

B





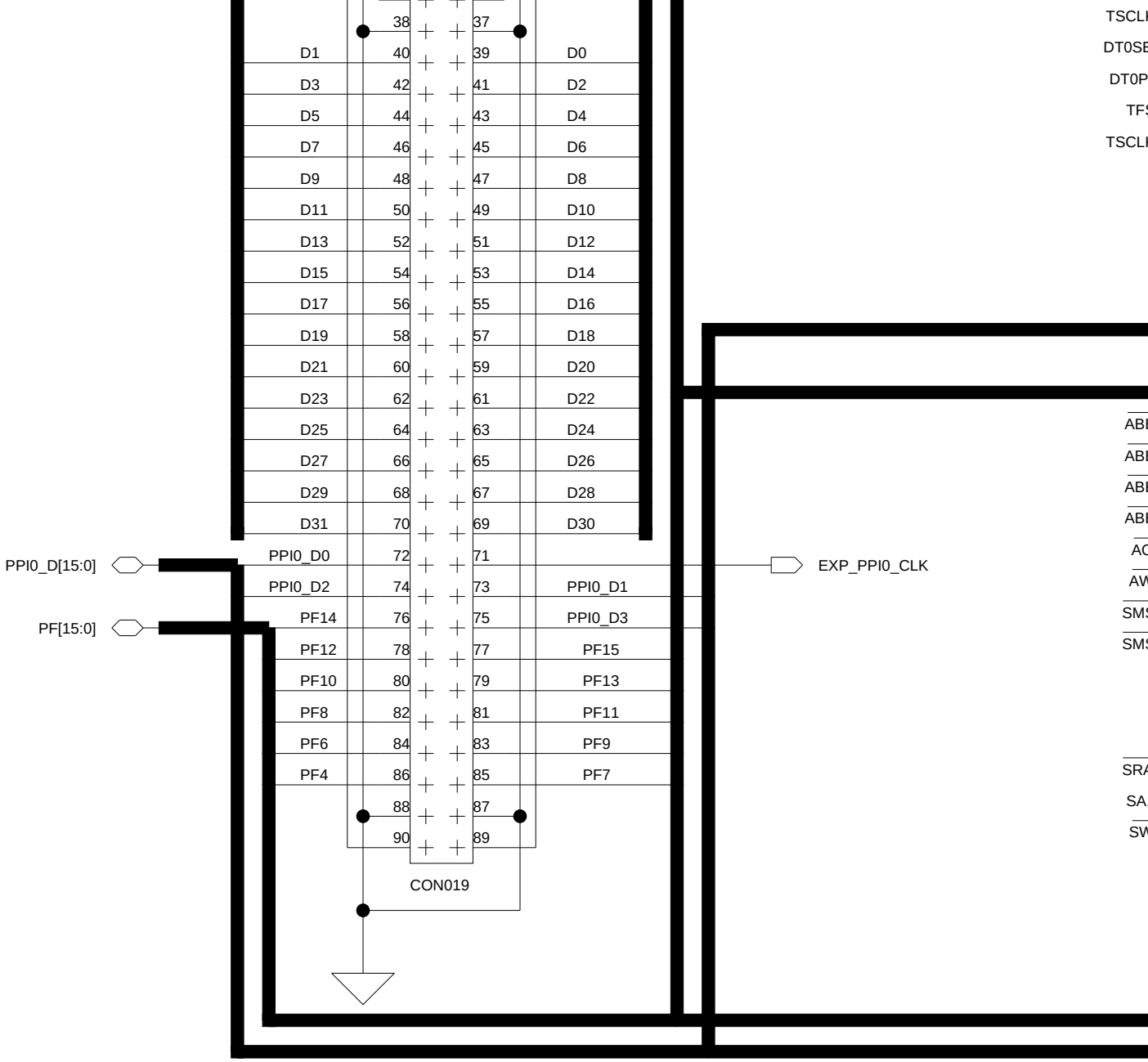




SW4 PB Enable Switch

Default = ON, ON, ON, ON, OFF, OFF

Position	Function
1-4	Connects the push buttons to the Progra Useful if using the PFs for another purpo
5,6	OFF, OFF = AD1836A -> TDM Mode ON, ON = AD1836A -> I2S Mode


38
37
D1
40
39
D0
D3
42
41
D2
D5
44
43
D4
D7
46
45
D6
D9
48
47
D8
D11
50
49
D10
D13
52
51
D12
D15
54
53
D14
D17
56
55
D16
D19
58
57
D18
D21
60
59
D20
D23
62
61
D22
D25
64
63
D24
D27
66
65
D26
D29
68
67
D28
D31
70
69
D30
PPI0_D[15:0]
PPI0_D0
72
71
PPI0_D2
74
73
PPI0_D1
PF[15:0]
PF14
76
75
PPI0_D3
PF12
78
77
PF15
PF10
80
79
PF13
PF8
82
81
PF11
PF6
84
83
PF9
PF4
86
85
PF7
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87
90
89
CON019
EXP_PPI0_CLK
TSCLI
DT0SE
DT0P
TFS
TSCLI
ABI
ABI
ABI
ABI
AC
AW
SMS
SMS
SRA
SA
SW

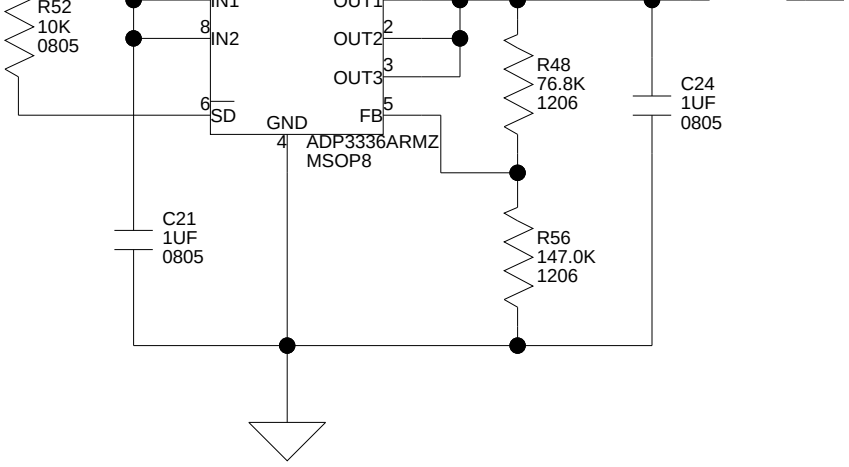
2

3

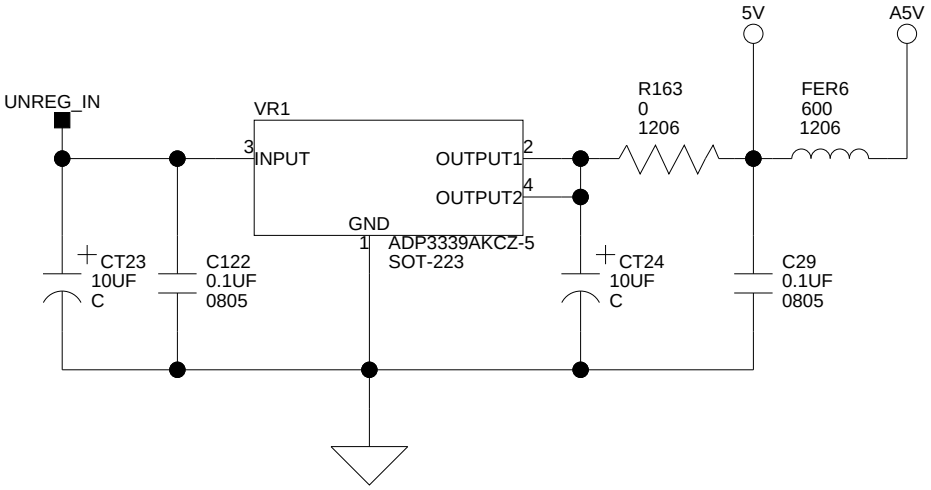
4

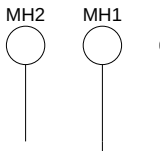
A

B

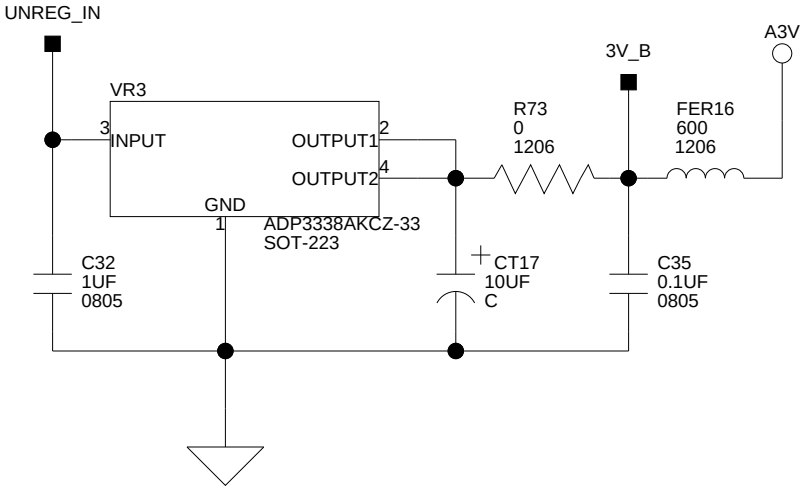


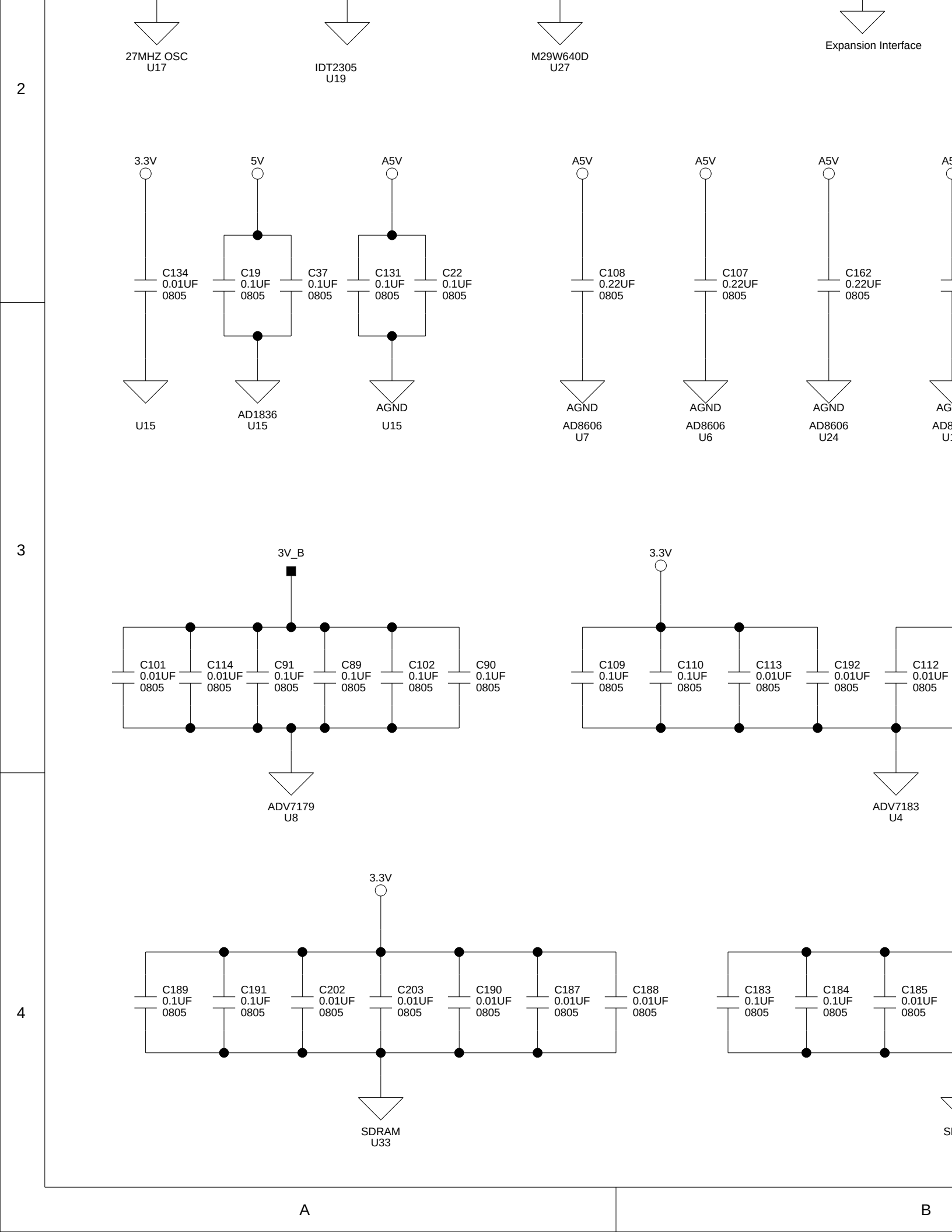
Current 1.5A





Current 1A




27MHZ OSC
U17
IDT2305
U19
M29W640D
U27
Expansion Interface
3.3V
C134
0.01UF
0805
U15
5V
C19
0.1UF
0805
C37
0.1UF
0805
AD1836
U15
A5V
C131
0.1UF
0805
C22
0.1UF
0805
AGND
U15
A5V
C108
0.22UF
0805
AGND
AD8606
U7
A5V
C107
0.22UF
0805
AGND
AD8606
U6
A5V
C162
0.22UF
0805
AGND
AD8606
U24
3V_B
C101
0.01UF
0805
C114
0.01UF
0805
C91
0.1UF
0805
C89
0.1UF
0805
C102
0.1UF
0805
C90
0.1UF
0805
ADV7179
U8
3.3V
C109
0.1UF
0805
C110
0.1UF
0805
C113
0.01UF
0805
C192
0.01UF
0805
C112
0.01UF
0805
ADV7183
U4
3.3V
C189
0.1UF
0805
C191
0.1UF
0805
C202
0.01UF
0805
C203
0.01UF
0805
C190
0.01UF
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C188
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