Blackfin® FPGA EZ-Extender® Manual

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ANALOG DEVICES

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Regulatory Compliance

The Blackfin FPGA EZ-Extender is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The Blackfin FPGA EZ-Extender has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the "**CE**" mark.

The Blackfin FPGA EZ-Extender has been appended to Analog Devices Development Tools Technical Construction File referenced "**DSPTOOLS1**" dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body and is on file.

CE

The Blackfin FPGA EZ-Extender contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused extender boards in the protective shipping package.

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PREFACE

Thank you for purchasing the Blackfin® Field-Programmable Gate Array (FPGA) EZ-Extender®, Analog Devices, Inc. (ADI) extension board to the EZ-KIT Lite® evaluation system for ADSP-BF533, ADSP-BF537, and ADSP-BF561 Blackfin processors.

The Blackfin processors are embedded processors that support a Media Instruction Set Computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing characteristics towards delivering signal processing performance in a microprocessor-like environment.

The EZ-KIT Lite and FPGA EZ-Extender are designed to be used in conjunction with the CrossCore® Embedded Studio (CCES) and VisualDSP++® software development environments. The development environment facilitates advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and FPGA EZ-Extender assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

To learn more about Analog Devices development software, go to http://www.analog.com/processors/tools.

Product Overview

The Blackfin FPGA EZ-Extender is a separately sold extension board that plugs onto the expansion interface of the ADSP-BF533, ADSP-BF537, or ADSP-BF561 EZ-KIT Lite evaluation system. The extension board aids the design and prototyping phases of ADSP-BF533, ADSP-BF537, or ADSP-BF561 processor targeted applications.

Please visit www.analog.com/EX1-FPGA for additional information, including CCES support.

The board extends the capabilities of the evaluation system by providing a Xilinx FPGA with external memory, IDC connectors for off-board connections, and a small bread board area.

The Blackfin FPGA EZ-Extender features:

- Xilinx Spartan III Field-Programmable Gate Array
    - XC3S1000
    - FG456 package
- Asynchronous static random access memory (SRAM)
    - Directly connected to FPGA
    - 2 MB (512K x 16 bits x 2 chips)
    - TSOP44 package

- 25 MHz oscillator
    - Directly connected to global clock of FPGA
- Socket for auxiliary oscillator
    - Directly connected to global clock of FPGA
- IDC thru-hole connectors
    - Allows quick access to Blackfin and FPGA pins for probing
    - Allows access to Blackfin and FPGA pins for off-board connections
- High-speed connector
    - Allows access to Blackfin and FPGA pins for high-speed application
- Expansion interface connectors
    - Allows access to ADI's family of Blackfin EZ-Extenders
- Two push buttons
    - Directly connected to FPGA
    - One with external debounce circuitry and one without
- Eight flag LEDs
    - Directly connected to FPGA

Before using any of the interfaces, follow the setup procedure in "FPGA EZ-Extender Setup" on page 1-1.

Example programs are available to demonstrate the capabilities of the Blackfin FPGA EZ-Extender board.

Purpose of This Manual

The *Blackfin FPGA EZ-Extender Manual* describes the operation and configuration of the components on the extension board. A schematic and a bill of materials are provided as a reference for future Blackfin processor board designs.

Intended Audience

This manual is a user's guide and reference to the Blackfin FPGA EZ-Extender. Programmers who are familiar with the Analog Devices Blackfin processor architecture, operation, and development tools are the primary audience for this manual. The user should also be familiar with basic FPGA development and Xilinx's Spartan III family of FPGAs.

Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts that describe your target architecture. For the locations of these documents, see "Related Documents".

Programmers who are unfamiliar with CCES or VisualDSP++ should refer to the online help and user's manuals.

Manual Contents

The manual consists of:

- Chapter 1, "FPGA EZ-Extender Interfaces" on page 1-1
  Provides basic board information.
- Chapter 2, "FPGA EZ-Extender Hardware Reference" on page 2-1
  Provides information on the hardware aspects of the board.

- Appendix A, "FPGA EZ-Extender Bill of Materials" on page A-1 Provides a list of components used to manufacture the EZ-Extender board.
- Appendix B, "FPGA EZ-Extender Schematic" on page B-1 Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design. Appendix B is part of the online help.

What's New in This Manual

This is revision 2.1 of the *Blackfin FPGA EZ-Extender Manual*. The manual has been updated to include CCES information. In addition, modifications and corrections based on errata reports against the previous manual revision have been made.

For the latest version of this manual, please refer to the Analog Devices Web site.

Technical Support

You can reach Analog Devices processors and DSP technical support in the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:
  http://ez.analog.com/community/dsp
- Submit your questions to technical support directly at:
  http://www.analog.com/support

- E-mail your questions about processors, DSPs, and tools development software from **CrossCore Embedded Studio** or **VisualDSP++**:

  Choose **Help > Email Support**. This creates an e-mail to `processor.tools.support@analog.com` and automatically attaches your **CrossCore Embedded Studio** or **VisualDSP++** version information and `license.dat` file.

- E-mail your questions about processors and processor applications to:
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  Three Technology Way
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  Norwood, MA 02062-9106
  USA

Supported Products

The Blackfin FPGA EZ-Extender is designed as an extension board to the ADSP-BF533, ADSP-BF537, and ADSP-BF561 EZ-KIT Lite evaluation systems.

Product Information

Product information can be obtained from the Analog Devices Web site and the online help.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, MyAnalog is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. MyAnalog provides access to books, application notes, data sheets, code examples, and more.

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EngineerZone is a technical support forum from Analog Devices. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

Related Documents

For additional information about the product, refer to the following publications.

Table 1. Related Processor Publications

Title	Description
• *ADSP-BF531/ADSP-BF532/ADSP-BF533 Blackfin Embedded Processor Data Sheet* • *ADSP-BF534/ADSP-BF536/ADSP-BF537 Blackfin Embedded Processor Data Sheet* • *ADSP-BF561 Blackfin Embedded Symmetric Multiprocessor Data Sheet*	General functional description, pinout, and timing
• *ADSP-BF533 Blackfin Processor Hardware Reference* • *ADSP-BF537 Blackfin Processor Hardware Reference* • *ADSP-BF561 Blackfin Processor Hardware Reference*	Description of the internal processor architecture and all register functions
Blackfin Processor Programming Reference	Description of all allowed processor assembly instructions

For more information on the Xilinx Spartan III FPGA, refer to the data sheet located at www.xilinx.com.

1 FPGA EZ-EXTENDER INTERFACES

This chapter provides the setup procedures for both the Blackfin Field-Programmable Gate Array (FPGA) EZ-Extender and EZ-KIT Lite (ADSP-BF533, ADSP-BF537 or ADSP-BF561). It also provides an overview of the extender board.

The information is presented in the following order.

FPGA EZ-Extender Setup

It is very important to set up all of the components of the system containing the FPGA EZ-Extender before applying power to that system. The following procedure is recommended.

Power your system when these steps are completed:

1. Read the applicable design interface section in this chapter—the text provides an overview of the capabilities of the EZ-Extender.
2. Read "System Architecture" on page 2-2 to understand the physical connections of the extender board. For detailed information, refer to "FPGA EZ-Extender Schematic" on page B-1.

3. Remove any rubber feet attached to the EZ-KIT Lite if the feet cover the printed circuit board (PCB) mounting holes. In place of the rubber feet, install the four nylon feet and screws provided with the FPGA EZ-Extender. Install the nylon feet in the mounting holes of the EZ-KIT Lite's PCB. Flip the EZ-KIT Lite upside down so that the three expansion headers (`J1-3`) are facing up.
4. Set the switches and jumpers on the FPGA EZ-Extender board. Use the block diagram in Figure 2-1 on page 2-2 in conjunction with "Jumpers" on page 2-11.
5. Set the switches and jumpers on the EZ-KIT Lite board. If not already, familiarize yourself with the documentation and schematics of the EZ-KIT Lite (see "Related Documents"). Compare the expansion interface signals of the FPGA EZ-Extender board with the signals of the EZ-KIT Lite board to ensure there is no contention. For example, it may be necessary to disable other devices connected to the expansion interface of the processor and disable the push buttons on the EZ-KIT Lite.
6. Install the FPGA EZ-Extender on the EZ-KIT Lite via the three-connector expansion interface. Figure 1-1 shows how an FPGA EZ-Extender plugs onto an EZ-KIT Lite.
7. Configure any other interfacing boards, for example, another EZ-Extender.

FPGA Software and Firmware

For information on the FPGA software, refer to the readme text file located in the `Examples` folder of the installation directory.

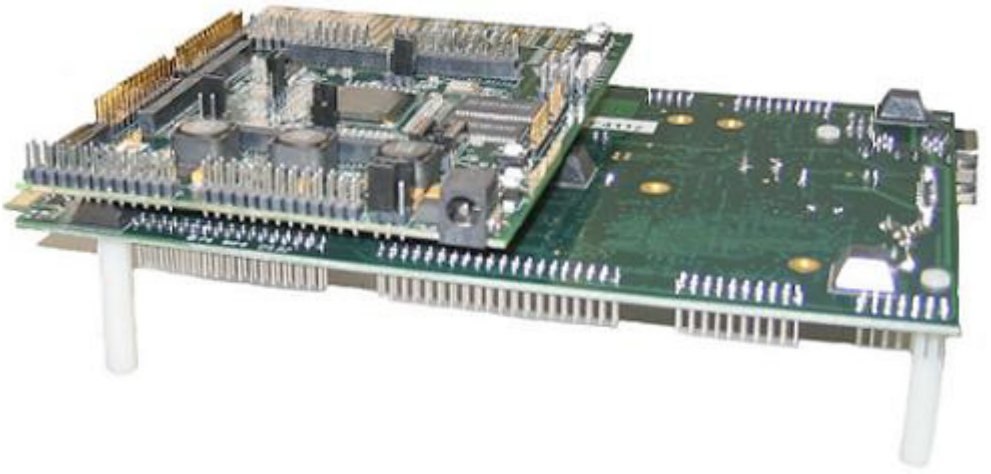


Figure 1-1. FPGA EZ-Extender Setup

FPGA EZ-Extender Overview

The Blackfin FPGA EZ-Extender connects a Xilinx® Spartan III Field-Programmable Gate Array (FPGA for short) to the ADSP-BF533, ADSP-BF537, or the ADSP-BF561 EZ-KIT Lite. The FPGA connects to the Blackfin processor via the expansion interface.

The extender board, by default, is powered by an external 7V power supply provided with the product. You can also power the FPGA EZ-Extender by the expansion interface of the EZ-KIT Lite or an external power supply. An external supply must be used whenever application code exceeds the recommended core and IO power supported by the FPGA EZ-Extender. For more information on the jumper and connector settings required to power the extender, review "Power" on page 2-8 as well as "FPGA EZ-Extender Schematic" on page B-1.

The FPGA EZ-Extender contains 2 MB of asynchronous SRAM memory, powered by a 3.3V supply. The SRAM memory connects to banks 6 and 7 of the FPGA and can perform simple data storage instructions in application-specific code.

The FPGA EZ-Extender includes a 25 MHz oscillator (U6) connected to the FPGA via the dedicated global clock 1 (GCLK1) pin, facilitating development of applications that require a clock. A second clock socket (U7) is left unpopulated to allow a user to place an oscillator with a specific frequency for the FPGA. The second clock socket connects to the global clock 6 (GCLK6) pin of the FPGA.

The extender has eight LEDs (LED1-8) and two push buttons (SW3-4) for applications that require status reporting and user control. The push buttons are active low and when pressed, provide a logic 0 to the respective FPGA nets. For inputs that require a permanent input low, use the jumper inputs on JP4. When a jumper is populated on one of the four nets of JP4, the respective pin is hard wired to a logic 0. For more information about the LEDs, push button switches, and jumper inputs, refer to "FPGA EZ-Extender Hardware Reference" on page 2-1.

There are various ways to program the FPGA. By default, the FPGA is programmed in its slave serial mode by the flash programming utility in CCES or VisualDSP++. The program configures the FPGA using the Blackfin processor's flag pins and/or serial port pins. For more information on how to use the flash programming utility within the development environment, refer to the readme file located in the Examples folder of the installation directory.

A second method of programming the FPGA is by using a Xilinx JTAG cable and software. The Xilinx JTAG cable connects to the FPGA JTAG header (P15). For more information about programming the FPGA via a Xilinx JTAG cable, refer to the manufacturer's website at www.xilinx.com.

The third and final way to program the FPGA is via the Xilinx serial ROM on the FPGA EZ-Extender. The serial ROM used for FPGA is

shipped with the extender and is pre-programmed. If the serial ROM needs to be re-programmed with new code, use an Xilinx JTAG cable and software and connect the Xilinx JTAG cable to the flash JTAG header (P6).

More information about programming the serial ROM can be found at www.xilinx.com. More details about the different ways to program the FPGA can be found in "FPGA EZ-Extender Hardware Reference" on page 2-1.

2 FPGA EZ-EXTENDER HARDWARE REFERENCE

This chapter describes the hardware design of the Field-Programmable Gate Array (FPGA) EZ-Extender.

The following topics are covered.

- "System Architecture" on page 2-2
  Describes the configuration of the extender board and explains how the board components interface with the processor and EZ-KIT Lite.
- "Programming the FPGA" on page 2-3
  Describes the different methods of programming the FPGA.
- "Programming the Serial ROM" on page 2-7
  Describes the method of programming the serial ROM.
- "Power" on page 2-8
  Describes the methods to power the extender board.
- "Jumpers" on page 2-11
  Describes the function of the configuration jumpers.
- "Push Buttons and LEDs" on page 2-15
  Describes the function of the push buttons and LEDs.
- "Connectors" on page 2-17
  Describes the function of the extender connectors.

System Architecture

A block diagram of the Blackfin FPGA EZ-Extender is shown in Figure 2-1.

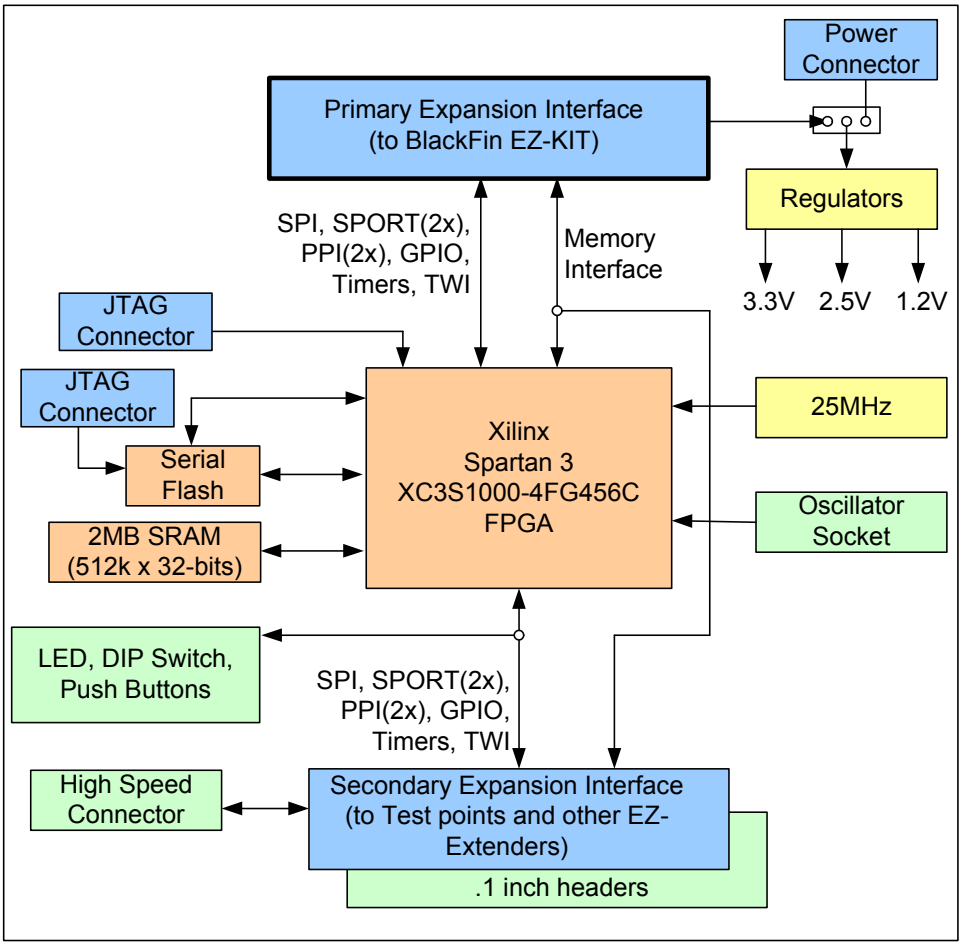


Figure 2-1. Block Diagram

Programming the FPGA

Before using the Blackfin FPGA EZ-Extender, follow the steps in "FPGA EZ-Extender Setup" on page 1-1.

Figure 2-2 is a block diagram of the FPGA programming connections.

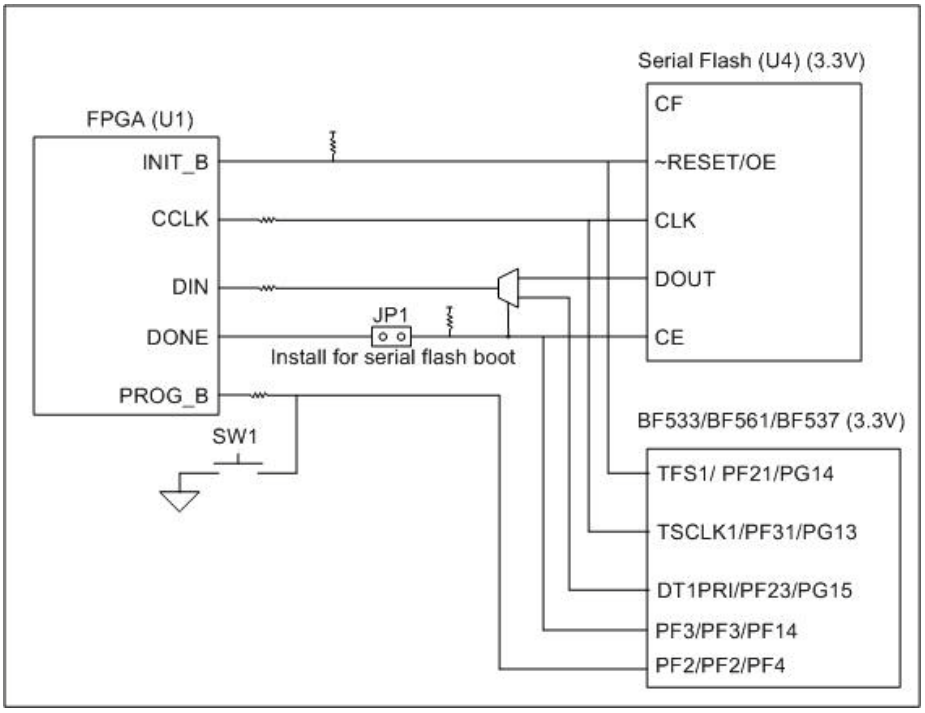


Figure 2-2. FPGA Programming Block Diagram

There are three ways to program the FPGA:

- Using the FPGA JTAG header, as described in "FPGA Programming via JTAG" on page 2-4
- Using the Xilinx serial ROM, as described in "FPGA Programming via Serial ROM" on page 2-5
- Using the Blackfin processor, as described in "FPGA Programming via Blackfin Application" on page 2-6

The done LED (LED10) lights up once the FPGA is programmed, signifying that the task is complete. To erase the contents of the FPGA at any time, de-press the program switch SW1.

FPGA Programming via JTAG

To program the FPGA via the JTAG header, create the appropriate program file using the Xilinx ISE software provided at www.xilinx.com. Once the program file is created, use a Xilinx JTAG cable and connect it to P15 of the FPGA EZ-Extender (the P15 connections are shown in Table 2-1).

Table 2-1. P15 Connections for PFGA Programming via JTAG

P15 Pin Number	Signal Name
1	3.3V
2	GND
3	TCK
4	TDO
5	TDI
6	TMS

In addition to removing JP1 (serial ROM boot jumper) as shown in Table 2-2, set the boot jumper, JP4, to JTAG mode. The JP4 settings for JTAG boot are shown in Table 2-3. See "Boot Jumper (JP4)" on page 2-13 for more information.

Table 2-2. JP1 Settings for FPGA Programming via JTAG

JP1 Pin Name	Pins Connected	Jumper Setting
Flash done	JP1.1 and JP1.2	Unpopulated

Table 2-3. JP4 Settings for FPGA Programming via JTAG

JP4 Pin Name	Pins Connected	Jumper Setting
M0	JP4.1 and JP4.2	Unpopulated
M1	JP4.3 and JP4.4	Populated
M2	JP4.5 and JP4.6	Unpopulated

FPGA Programming via Serial ROM

To program the FPGA with the contents of the serial ROM, populate the JP1 jumper. When populated, JP1 connects the chip enable pin of the serial ROM to the done bit of the FPGA. Once the FPGA is programmed, the done bit automatically goes high, and the enable pin of the serial ROM chip becomes a logic 1. The JP1 settings for serial ROM boot are shown in Table 2-4. See "Programming the Serial ROM" on page 2-7 for more information.

The done LED (LED10) remains lit to signify that the FPGA is programmed. See "Done LED (LED10)" on page 2-17 for more information.

Table 2-4. JP1 Settings for FPGA Programming via Serial ROM

JP1 Pin Name	Pins Connected	Jumper Setting
Flash done	JP1.1 and JP1.2	Populated

In addition to JP1, set the boot mode jumper, JP4, to master serial mode. The JP4 settings for serial ROM boot are shown in Table 2-5. See "Boot Jumper (JP4)" on page 2-13 for more information.

Table 2-5. JP4 Settings for FPGA Programming in Master Serial Mode

JP4 Pin Name	Pins Connected	Jumper Setting
M0	JP4.1 and JP4.2	Populated
M1	JP4.3 and JP4.4	Populated
M2	JP4.5 and JP4.6	Populated

FPGA Programming via Blackfin Application

By default, the FPGA EZ-Extender is configured by the flash programming utility within CCES or VisualDSP++. The software is located in the Examples folder of the installation directory. The FPGA Extender readme text file located in the same folder provides all the necessary instructions required for running the application.

When generating a program file using the Xilinx software tools, remember to generate a slave serial program file in the Intel MCS-86 Hexadecimal Object (.mcs) file format.

To boot the FPGA from the Blackfin processor, unpopulate jumper JP1 and set jumper JP4 to slave serial mode, as shown in Table 2-6 and Table 2-7. See "Serial ROM Boot Jumper (JP1)" on page 2-12 and "Boot Jumper (JP4)" on page 2-13 for more information.

Table 2-6. JP1 Settings for FPGA Programming via Blackfin Processor

JP1 Pin Name	Pins Connected	Jumper Setting
Flash done	JP1.1 and JP1.2	Unpopulated

Table 2-7. JP4 Settings for FPGA Programming via Blackfin Processor

JP4 Pin Name	Pins Connected	Jumper Setting
M0	JP4.1 and JP4.2	Unpopulated
M1	JP4.3 and JP4.4	Unpopulated
M2	JP4.5 and JP4.6	Unpopulated

Programming the Serial ROM

The FPGA EZ-Extender allows the user to program the serial ROM. The serial ROM can be programmed by using a Xilinx JTAG cable, ISE software, and the flash JTAG header on the FPGA EZ-Extender.

Serial ROM via JTAG Header

To program the serial ROM via the JTAG header, create the appropriate program file using the Xilinx software provided at www.xilinx.com. Once the program file is created, use a Xilinx JTAG cable and connect it to P6. The P6 connections are shown in Table 2-8.

Table 2-8. P6 Connections for Serial ROM

P6 Pin Number	Signal Name	P6 Pin Number	Signal Name
1	3.3V	4	TDO
2	GND	5	TDI
3	TCK	6	TMS

Power

The FPGA EZ-Extender can be powered from the enclosed power supply, EZ-KIT Lite, or external power supply. The power source for the extender is selected based on the power requirements of the application.

An external 7V power supply is shipped with the extender board. The power supply uses three switching regulators: VR1 is used to power the 2.5V power plane, VR2 is used to power the 1.2V power plane, and VR3 is used to power the 3.3V plane. All of the regulators can supply a maximum current of 2 Amps. To understand the power requirements of your application, run the Xilinx power estimator software. The software can be located at www.xilinx.com.

Table 2-9 states the current limitations of each method. Each method requires a correctly configured header, described in the following sections.

Table 2-9. Power Limitations

Power Source	1.2V Supply	2.5V Supply	3.3V Supply
ADSP-BF533, ADSP-BF537, or ADSP-BF561 EZ-KIT Lite	500 mA	500 mA	500 mA
FPGA EZ-Extender power supply[1]	**2A**	**2A**	**2A**
External power supply	2A	2A	2A

1 Default setting

Power In Header (P12)

The P12 header supplies the power to the on board 1.2V and the 2.5V regulators. The P42 and P43 headers supply the power to the external 1.2V and 2.5V planes, as described in "2.5V Header (P42)" and "1.2V Header (P43)" on page 2-10.

Power Source	P12 Setting
FPGA EZ-Extender power supply[1]	**Jumper on P12.1 and P12.2**
ADSP-BF533, ADSP-BF537, or ADSP-BF561 EZ-KIT Lite 5V power supply	Jumper on P12.2 and P12.3

1 Default setting

3.3V Header (P13)

Power Source	P13 Setting
ADSP-BF533, ADSP-BF537, or ADSP-BF561 EZ-KIT Lite 3.3V power supply	Jumper on P13.1 and P13.2
FPGA EZ-Extender power supply[1]	**Jumper on P13.2 and P13.3**
External power supply	No jumper; connect supply to P13.2 and GND

1 Default setting

When using an external power supply, *do not* plug in the power supply shipped with the FPGA EZ-Extender. This can seriously damage the board. As an extra measure of precaution, remove all jumpers from P12.

2.5V Header (P42)

Power Source	P42 Setting
FPGA EZ-Extender Power Supply[1]	**No Jumper**
External power supply	Connect P42.1 to external 2.5V Connect P42.2 to external GND

1 Default setting

When using an external power supply, *do not* plug in the power supply shipped with the FPGA EZ-Extender. This can seriously damage the board. As an extra measure of precaution, remove all jumpers from P12.

1.2V Header (P43)

Power Source	P43 Setting
FPGA EZ-Extender power supply[1]	**No Jumper**
External power supply	Connect P42.1 to external 2.5V Connect P42.2 to external GND

1 Default setting

When using an external power supply, *do not* plug in the power supply shipped with the FPGA EZ-Extender. This can seriously damage the board. As an extra measure of precaution, remove all jumpers from P12.

Jumpers

Before using the Blackfin FPGA EZ-Extender, follow the steps in "FPGA EZ-Extender Setup" on page 1-1.

Figure 2-3 shows the locations of all jumper headers. A two-pin jumper can be placed on the respective jumper header for different functionality. The following sections describe all possible jumper settings and associated functionality.

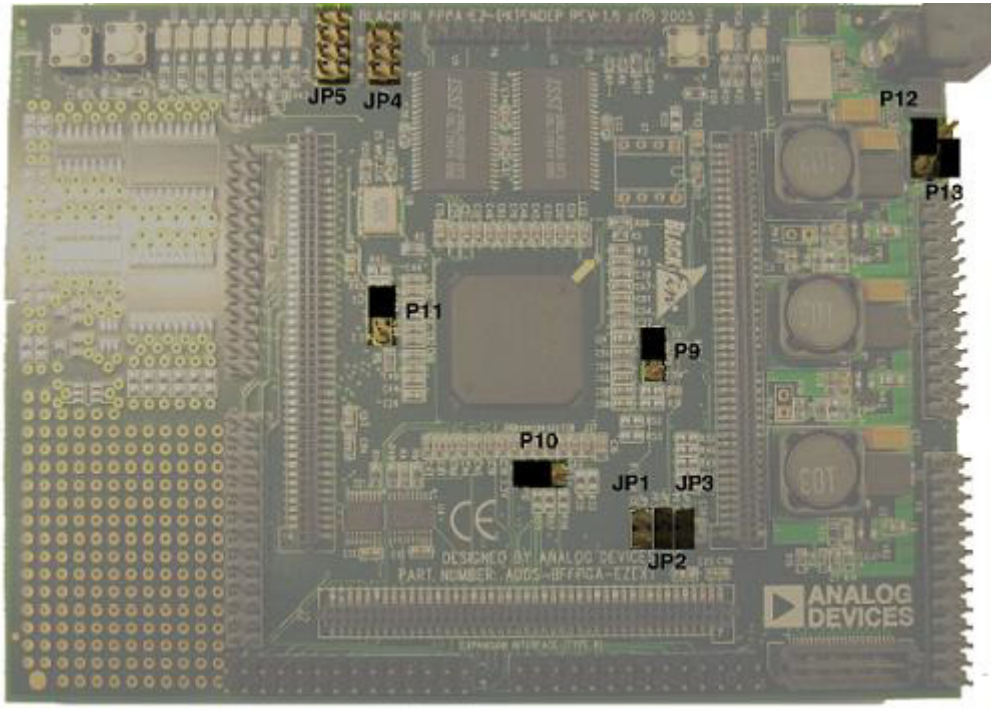


Figure 2-3. Jumper Locations

Serial ROM Boot Jumper (JP1)

By default, the serial ROM boot jumper, JP1, is unpopulated. When unpopulated, the FPGA EZ-Extender programs via the Blackfin processor or the Xilinx JTAG header.

When JP1 is left populated, the jumper connects the serial ROM chip enable pin to the done bit of the FPGA. At power-up, the done bit is driven low by the FPGA, causing the FPGA to enable the serial ROM as a programming source. After the FPGA is programmed, the done bit is driven high by the FPGA, causing the FPGA to drive high the chip enable pin of the serial ROM.

Both JP1 and JP4 must be set up for correct FPGA programming. "Boot Jumper (JP4)" on page 2-13 summarizes the JP4 settings. Table 2-10 summarizes the JP1 settings. See Table 2-4 on page 2-5 and Table 2-6 on page 2-6 for more information on JP1.

Table 2-10. JP1 Settings

Boot Source	JP1 Setting
ADSP-BF533, ADSP-BF537, or ADSP-BF561 processor via CCES or VisualDSP++[1]	**Unpopulated**
JTAG header	Unpopulated
Serial ROM	Populated

1 Default setting

Config Done Jumper (JP2)

The configuration done jumper, JP2, connects the done bit of the FPGA to the Blackfin processor's PF3 flag pin of the ADSP-BF533 and ADSP-BF561 EZ-KIT Lites or PF14 flag pin of the ADSP-BF537 EZ-KIT Lite. By default, the jumper is populated and acts as a monitor for the done bit by the Blackfin processor (the bit indicates that the FPGA programming is complete).

Table 2-11 summarizes the jumper settings.

Table 2-11. JP2 Settings

Functionality	JP2 Setting
Done bit connected to Blackfin processor's PF3 flag pin[1]	**Populated**
Done bit disconnected from Blackfin processor's PF3 flag pin	Unpopulated

1 Default setting

Config Program Jumper (JP3)

The configuration program jumper, JP3, connects the program bit of the FPGA to the Blackfin processor's flag pin. By default, JP3 is populated. The jumper assures that the program bit is asserted by the Blackfin processor to initiate the FPGA programming through development software.

Table 2-12 summarizes the jumper settings.

Table 2-12. JP3 Settings

Functionality	JP3 Setting
Program bit connected to the Blackfin processor's flag pin[1]	**Populated**
Program bit disconnected from the Blackfin processor's flag pin	Unpopulated

1 Default setting

Boot Jumper (JP4)

The boot jumper, JP4, configures the FPGA mode pins (M[2:0]). Based on the jumper settings, the FPGA is set to be programmed by the JTAG header, serial ROM, or Blackfin processor.

Table 2-13 summarizes the jumper settings. See Table 2-3 on page 2-5 for the JTAG header boot settings, Table 2-5 on page 2-6 for the serial ROM boot settings, and Table 2-7 on page 2-7 for the Blackfin processor boot settings.

Table 2-13. JP4 Settings

Boot Source	JP4.1 and JP4.2 M0	JP4.3 and JP4.4 M1	JP4.5 and JP4.6 M2
ADSP-BF533, ADSP-BF537, or ADSP-BF561 processor[1]	**Unpopulated**	**Unpopulated**	**Unpopulated**
JTAG header	Unpopulated	Populated	Unpopulated
Serial ROM	Populated	Populated	Populated

1 Default setting

FPGA Input Jumpers (JP5)

The FPGA input jumpers, `JP5.2-5.8`, drive select FPGA nets to a logic `0` and can be used for any user logic that requires a steady state input. You can set internal pull-ups on these nets in the FPGA and, when a `low` is required, populate the respective jumper.

Table 2-14 summarizes the jumper settings.

Table 2-14. JP5 Settings

Reference Designator	FPGA Pin Number
JP5.2	Y3
JP5.4	Y2
JP5.6	U10
JP5.8	AB11

Push Buttons and LEDs

Before using the Blackfin FPGA EZ-Extender, follow the steps in "FPGA EZ-Extender Setup" on page 1-1.

Figure 2-4 shows the locations of all push buttons and LEDs. The following sections describe the associated functionality of all the push buttons and LEDs.

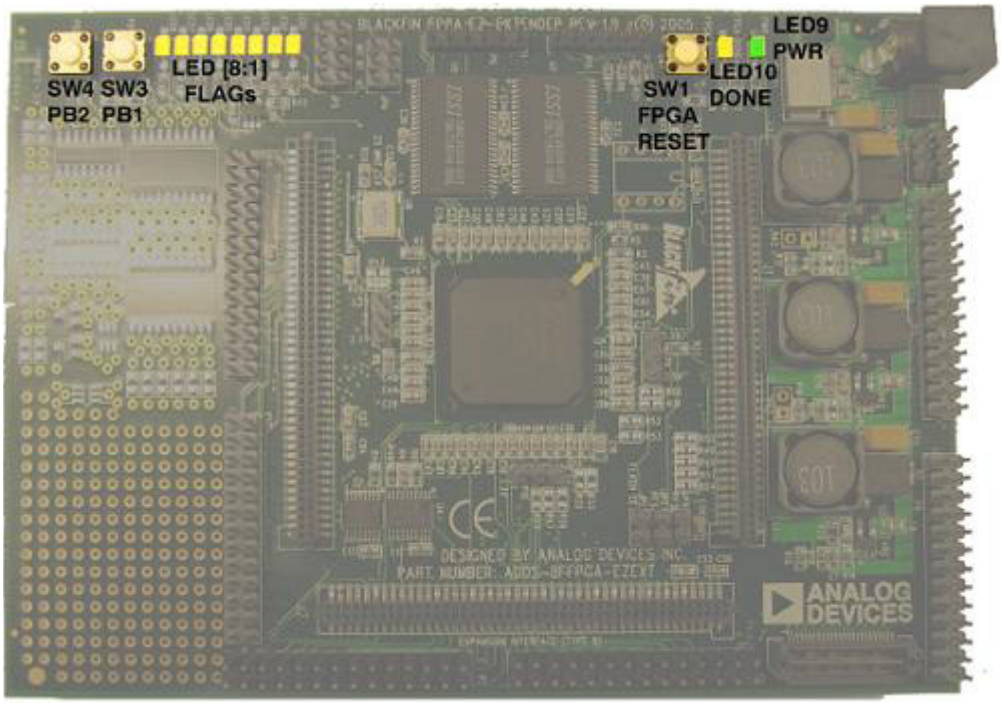


Figure 2-4. Push Button and LED Locations

Program Push Button (SW1)

The program push button, SW1, erases the contents of the FPGA. The push button can be used as a hard reset—the FPGA must be completely re-programmed once SW1 is de-pressed. See "Programming the FPGA" on page 2-3 for more information.

PB1 Push Button (SW3)

The PB1 push button, SW3, is a general-purpose input push button. The switch with a connected debounce circuit eliminates the need to re-create it in the FPGA. The push button connects to pin C11 of the FPGA.

PB2 Push Button (SW4)

The PB2 push button, SW4, is a general-purpose input push button. The switch does not have a connected debounce circuit; you may need to create it in the FPGA if required by a specific application. The push button connects to pin H5 of the FPGA.

Status LEDs (LED1–8)

Eight status LEDs, LED1-8, connect to the FPGA and act as status flags in any application that requires it. Table 2-15 shows the LED/FPGA connections.

Table 2-15. Status LED (LED1–8) Settings

Reference Designator	FPGA Pin Number
LED1	U11
LED2	W11
LED3	AB10
LED4	Y10

Table 2-15. Status LED (LED1–8) Settings (Cont'd)

Reference Designator	FPGA Pin Number
LED5	AB9
LED6	W9
LED7	AB8
LED8	V10

Power LED (LED9)

The power LED, LED9, connects to the 2.5V power supply and, when lit, signifies that the FPGA EZ-Extender is powered properly.

Done LED (LED10)

The done LED, LED10, connects to the done pin of the FPGA. At power-up, the FPGA is blank and needs to be programmed. When lit, the LED indicates that the FPGA is programmed successfully.

Connectors

Before using the Blackfin FPGA EZ-Extender, follow the steps in "FPGA EZ-Extender Setup" on page 1-1.

This section describes the connector functionality and provides information about the mating connectors. The connector locations are shown in Figure 2-5.

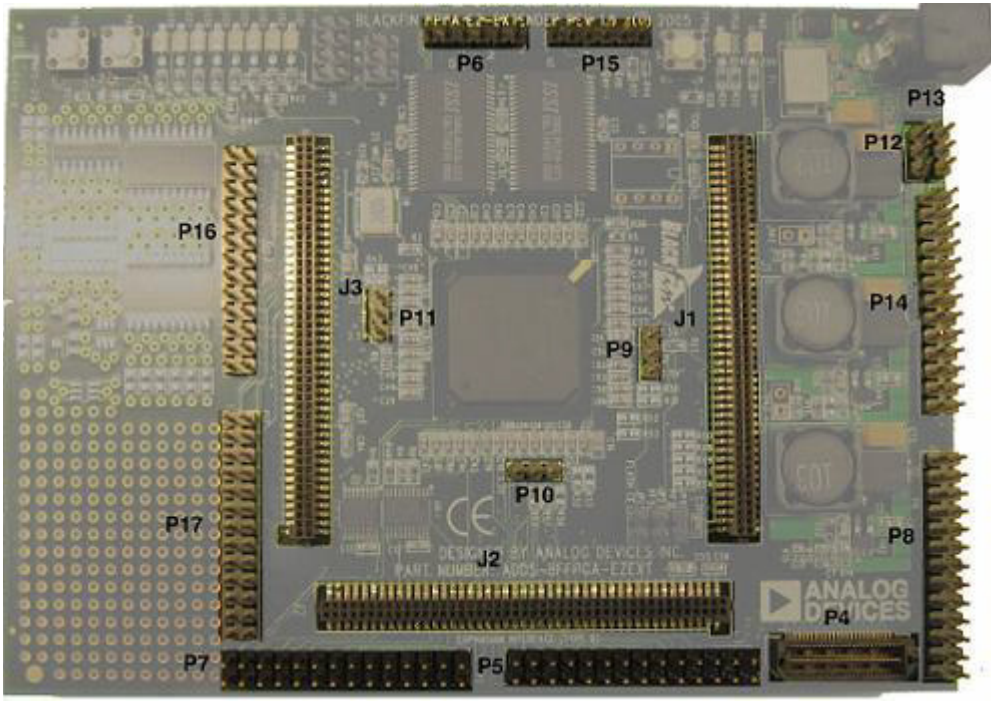


Figure 2-5. Connector Locations

Expansion Interface (P1–3 and J1–3)

Connectors `P1-3` of the expansion interface are used to plug in the EZ-Extender to the ADSP-BF533, ADSP-BF537, or ADSP-BF561 EZ-KIT Lite.

Connectors J1-3 of the expansion interface are used to plug in another extender board, such as the Blackfin USB-LAN EZ-Extender. Your own custom board can be plugged into J1-3 as well.

Plugging in another EZ-Extender or a customer board to the expansion interface can de-grade the overall system performance. The extra overall load can cause the user to add wait states or slow down the system bus to get all of the boards to work properly.

For the J1-3 and P1-3 connector availability and pricing, contact Samtec.

Part Description	Manufacturer	Part Number
90-position 0.05" spacing, SMT (J1, J2, J3)	Samtec	SFC-145-T2-F-D-A
90-position 0.05" spacing (P1, P2, P3)	Samtec	TFC-145-32-F-D

IDC Connectors (P8, P14, P16, and P17)

The P8, P14, P16, and P17 connectors are standard 0.1" IDC headers. The connectors are in a 13 x 2 configuration and designed for signal probing, bread boarding, and other signal accesses.

Part Description	Manufacturer	Part Number
IDC13x2 0.1" header	Berg	54102-T08-13
Mating Connector		
IDC 13x2 0.1" plug	Samtec	SSW-113-01-T-D

IDC Connectors (P5 and P7)

The P5 and P7 connectors are standard 0.1” IDC headers. The connectors are in a 14 x 2 configuration and designed for signal probing, bread boarding, and other signal accesses.

Part Description	Manufacturer	Part Number
IDC14x2 0.1” header	FCI	68737-428HLF
IDC14x2 0.1” header	Sullins	GEC14DAAN
Mating Connector		
IDC 14x2 0.1” plug	Samtec	SSW-114-01-T-D

High-Speed Connector (P4)

The high-speed connector, P4, facilitates development of applications where use of the standard IDC connectors is complicated due to signal integrity issues.

For the P4 connector and cable assembly availability and pricing, contact Samtec.

Part Description	Manufacturer	Part Number
QTS 25x2 high-speed connector	Samtec	QTS-025-01-F-D-A
Mating Connector		
QSS 25x2 high-speed connector	Samtec	QSS-025-01-F-D-A

A FPGA EZ-EXTENDER BILL OF MATERIALS

The bill of materials corresponds to "FPGA EZ-Extender Schematic" on page B-1.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	1	SN74LVC1G125 SOT23-5	U8	TI	74LVC1G125DBVRE4
2	1	25MHZ OSC003	U6	DIGI-KEY	SG-8002CA-PCC-ND (25.00M)
3	1	74LVC157TSSOP16	U2	DIGI-KEY	296-1225-1-ND
4	1	XC3S1000 FG456	U1	XILINX	XC3S1000-4FGG456C
5	3	LM3475MF SOT23-5	VR1-3	NATIONAL SEMI	LM3475MF
6	2	IS61LV51216 TSOP44	U3,U5	ISSI	IS61LV51216-10TLI
7	3	SI2343DS SOT23D	Q1-3	VISHAY	SI2343DS-T1-E3
8	1	BFFPGA XCF04S "U4"	U4	XILINX	XCF04SVOG20C
9	1	PWR 2.5MM_JACK CON005	J4	SWITCHCRAFT	RAPC712X
10	1	DIP 8 DIP8SOC	U7	MILL-MAX	614-43-308-31-007000
11	3	MOMENTARY SWT013	SW1,SW3-4	PANASONIC	EVQ-PAD04M
12	3	0.05 45x2 CON018	P1-3	SAMTEC	TFC-145-32-F-D
13	3	.05 45X2 CON019	J1-3	SAMTEC	SFC-145-T2-F-D-A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
14	2	IDC14X2IDC14X2	P5,P7	FCI	68737-428HLF
15	2	IDC6X1 IDC6X1	P6,P15	FCI	90726-406HLF
16	1	QTS25X2CON041	P4	SAMTEC	QTS-025-01-F-D-A
17	2	IDC2X1 IDC2X1	P42-43	FCI	90726-402HLF
18	3	IDC2X1 IDC2X1	JP1-3	FCI	90726-402HLF
19	1	2.5A RESETABLE FUS001	F1	RAYCHEM	SMD250F-2
20	9	YELLOW LED001	LED1-8, LED10	PANASONIC	LN1461C
21	1	10UF 16V 10% C	C4	AVX	TAJC106K016R
22	3	3A HSM350J DO214AB	D1-3	VISHAY GEN-SEMI	SS36-E3
23	1	600 100MHZ 200MA 0603	FER2	DIGI-KEY	490-1014-2-ND
24	1	2AS2A DO-214AA	D5	VISHAY	S2A-E3
25	1	3900PF 50V 5% 0805	C6	PANASONIC	ECJ2VB1H392K
26	1	190 100MHZ 5A FER002	FER1	MURATA	DLW5BSN191SQ2
27	7	10UF 6.3V 10% 0805	C14-16,C35, C55,C83,C86	AVX	080560106KAT2A
28	4	1000PF 10V 20% 0805	C1-2,C10,C74	DIGI-KEY	311-1136-1-ND
29	3	100UF 10V 10% C	CT1-3	KOA	TMC1ACTTE107K
30	5	0.1UF 16V 10% 0603	C3,C38,C56, C84-85	AVX	0603YC104KAT2A

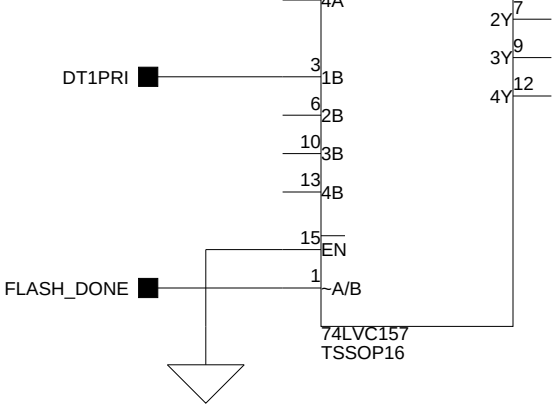
Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
31	56	0.01UF 16V 10% 0603	C11-13, C17-34, C36-37, C39-54, C57-70,C80-82	AVX	0603YC103KAT2A
32	1	1UF 16V 10% 0603	C5	PANASONIC	ECJ-1VB1C105K
33	3	10UH 20% IND005	L1-3	COILCRAFT	MSS1278-103MLB
34	13	10K 1/10W 5% 0603	R1,R6,R21-22, R25,R28-29, R46-51	VISHAY	CRCW060310K0JNEA
35	10	330 1/10W 5% 0603	R10,R24, R34-41	VISHAY	CRCW0603330RJNEA
36	11	0 1/10W 5% 0603	R3,R9,R12, R15-16,R27, R52-54,R58-59	PHYCOMP	232270296001L
37	1	10 1/10W 5% 0603	R42	VISHAY	CRCW060310R0JNEA
38	1	200.0K 1/16W 1% 0603	R20	VISHAY	CRCW0603200KFNEA
39	2	10.0K 1/10W 1% 0603	R14,R19	DIGI-KEY	311-10.0KHRTR-ND
40	3	33.0 1/10W 1% 0603	R2,R4,R26	DIGI-KEY	311-33.0HRTR-ND
41	5	100 1/16W 5% 0402	R5,R7-8,R23, R44	DIGI-KEY	311-100JRTR-ND
42	3	390PF 25V 5% 0603	C7,C72-73	AVX	06033A391FAT2A
43	1	4.99K 1/16W 1% 0603	R13	VISHAY	CRCW06034K99FKEA
44	1	31.6K 1/16W 1% 0603	R17	PANASONIC	ERJ-3EKF3162V
45	1	1.05K 1/16W 1% 0603	R11	PANASONIC	ERJ-3EKF1051V

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
46	1	2.15K 1/16W 1% 0603	R18	VISHAY	CRCW06032K15FKEA
47	3	10UF10V10%0805	C8-9,C71	PANASONIC	ECJ-2FB1A106K

3

4

A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7
3Y
9
4Y
12
DT1PRI
3
1B
6
2B
10
3B
13
4B
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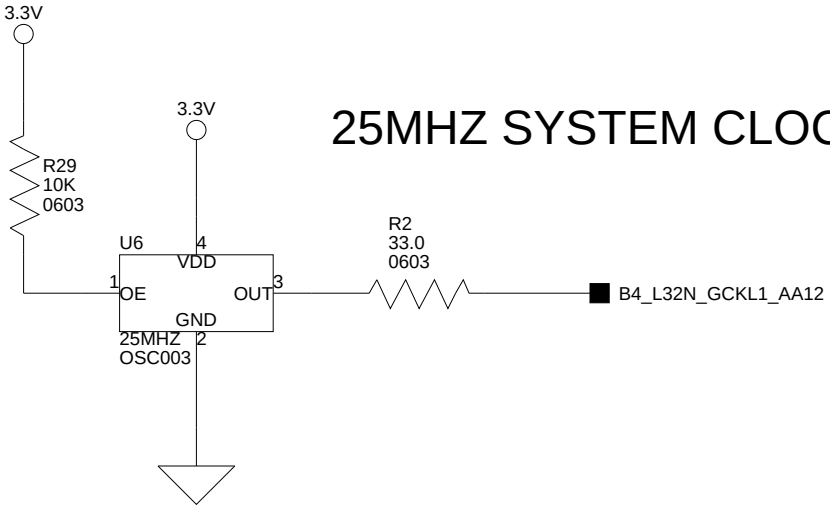
EN
FLASH_DONE
1
A/B
74LVC157
TSSOP16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25MHZ SYSTEM CLOCK
R29
10K
0603
U6
4
VDD
R2
33.0
0603
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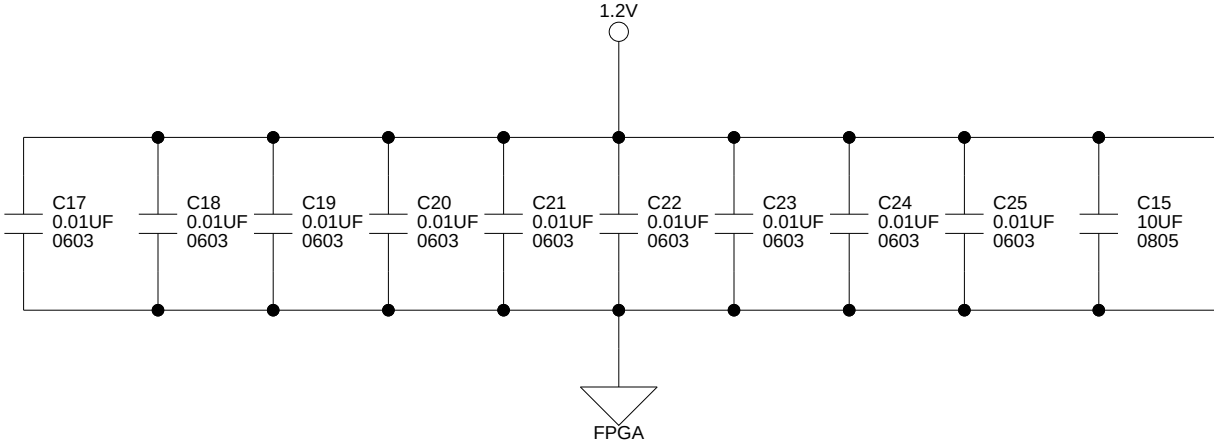
OE
OUT
3
B4_L32N_GCKL1_AA12
GND
25MHZ
OSC003
2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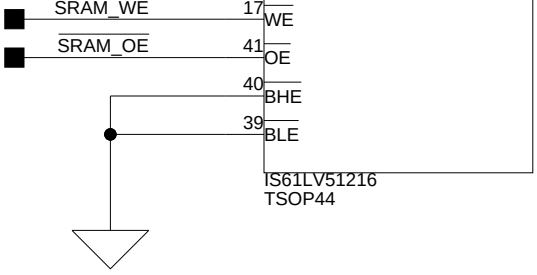
0.01UF
0603
C18
0.01UF
0603
C19
0.01UF
0603
C20
0.01UF
0603
C21
0.01UF
0603
C22
0.01UF
0603
C23
0.01UF
0603
C24
0.01UF
0603
C25
0.01UF
0603
C15
10UF
0805
FPGA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SRAM_OE
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WE
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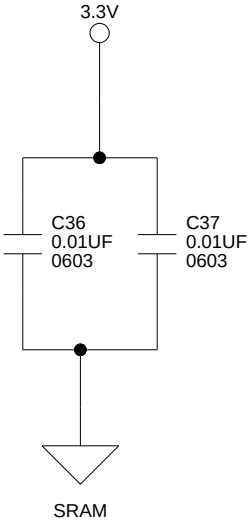
OE
40
BHE
39
BLE
IS61LV51216
TSOP44

3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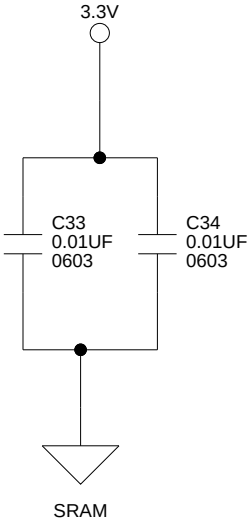
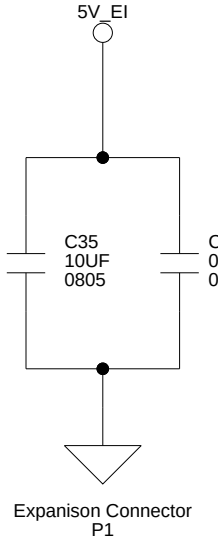
0.01UF
0603
C37
0.01UF
0603
SRAM


3.3V
C33
0.01UF
0603
C34
0.01UF
0603
SRAM

4

A

EXPANSION_PPI_CLK
PP1
PP3
UDEF2
UDEF4
UDEF6
UDEF8
UDEF10



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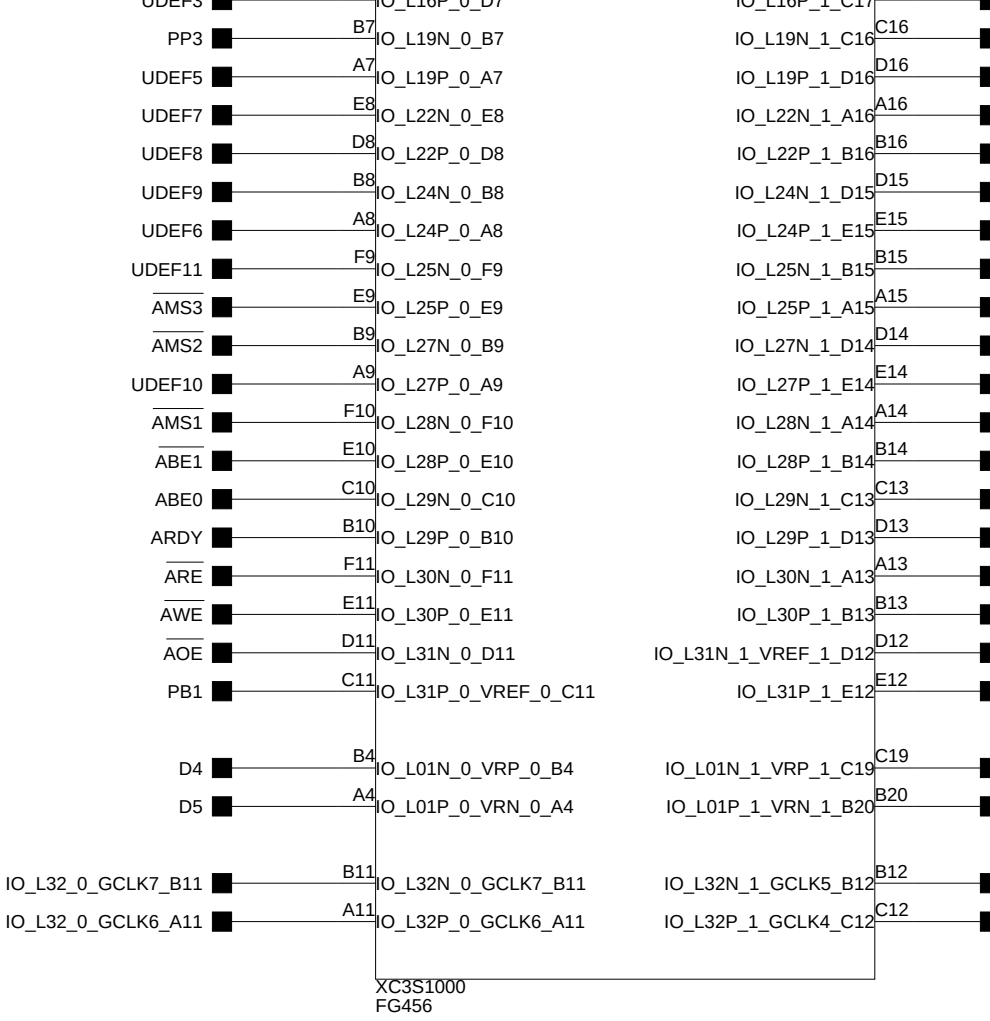
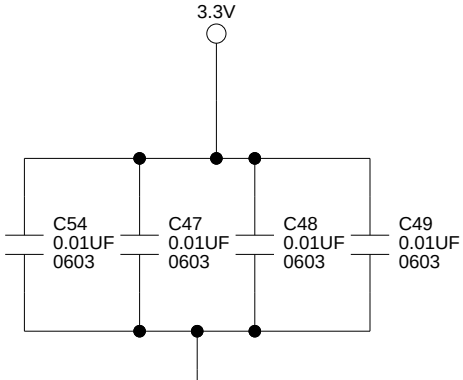
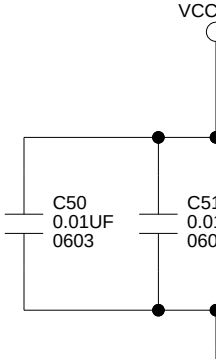

UDEF3
PP3
UDEF5
UDEF7
UDEF8
UDEF9
UDEF6
UDEF11
AMS3
AMS2
UDEF10
AMS1
ABE1
ABE0
ARDY
ARE
AWE
AOE
PB1
D4
D5
IO_L32_0_GCLK7_B11
IO_L32_0_GCLK6_A11
B7
A7
E8
D8
B8
A8
F9
E9
B9
A9
F10
E10
C10
B10
F11
E11
D11
C11
B4
A4
B11
A11
IO_L16P_0_D7
IO_L19N_0_B7
IO_L19P_0_A7
IO_L22N_0_E8
IO_L22P_0_D8
IO_L24N_0_B8
IO_L24P_0_A8
IO_L25N_0_F9
IO_L25P_0_E9
IO_L27N_0_B9
IO_L27P_0_A9
IO_L28N_0_F10
IO_L28P_0_E10
IO_L29N_0_C10
IO_L29P_0_B10
IO_L30N_0_F11
IO_L30P_0_E11
IO_L31N_0_D11
IO_L31P_0_VREF_0_C11
IO_L01N_0_VRP_0_B4
IO_L01P_0_VRN_0_A4
IO_L32N_0_GCLK7_B11
IO_L32P_0_GCLK6_A11
XC3S1000
FG456
IO_L16P_1_C17
IO_L19N_1_C16
IO_L19P_1_D16
IO_L22N_1_A16
IO_L22P_1_B16
IO_L24N_1_D15
IO_L24P_1_E15
IO_L25N_1_B15
IO_L25P_1_A15
IO_L27N_1_D14
IO_L27P_1_E14
IO_L28N_1_A14
IO_L28P_1_B14
IO_L29N_1_C13
IO_L29P_1_D13
IO_L30N_1_A13
IO_L30P_1_B13
IO_L31N_1_VREF_1_D12
IO_L31P_1_E12
IO_L01N_1_VRP_1_C19
IO_L01P_1_VRN_1_B20
IO_L32N_1_GCLK5_B12
IO_L32P_1_GCLK4_C12
C16
D16
A16
B16
D15
E15
B15
A15
D14
E14
A14
B14
C13
D13
A13
B13
D12
E12
C19
B20
B12
C12


3.3V
C54
0.01UF
0603
C47
0.01UF
0603
C48
0.01UF
0603
C49
0.01UF
0603
FPGA

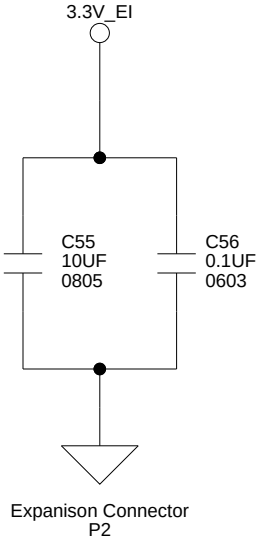

VCC
C50
0.01UF
0603
FPGA

3

4

A

RFS0
RSCLK0
PF15
PF13
PF11
PF9
PF7
PF5
PF3
PF1
AMS3
AMS2
AMS1
AMS0
ARDY
ARE
P2_71
P2_73
P2_77
P2_79
P2_81
P2_83
P2_85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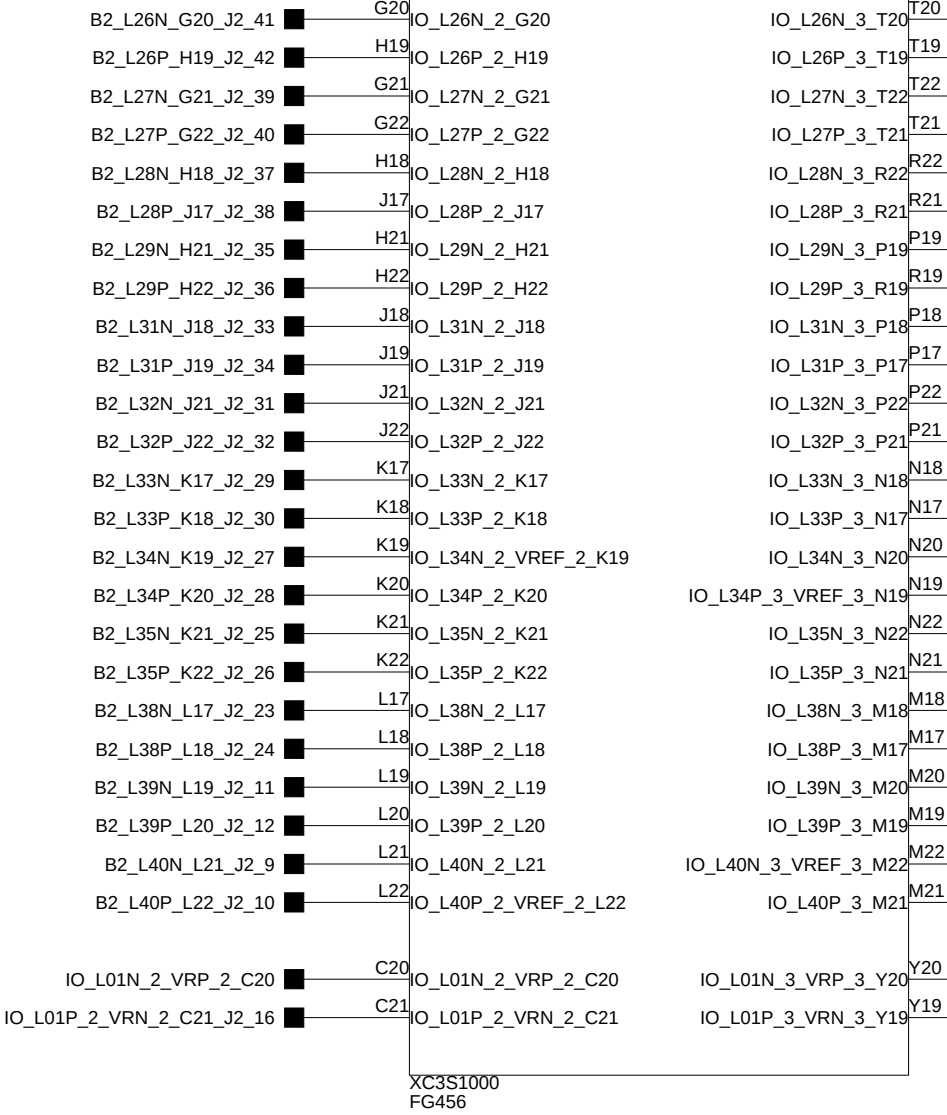
C55
10UF
0805
C56
0.1UF
0603
Expanison Connector
P2

3

4

A


B2_L26N_G20_J2_41
G20
IO_L26N_2_G20
IO_L26N_3_T20
T20
B2_L26P_H19_J2_42
H19
IO_L26P_2_H19
IO_L26P_3_T19
T19
B2_L27N_G21_J2_39
G21
IO_L27N_2_G21
IO_L27N_3_T22
T22
B2_L27P_G22_J2_40
G22
IO_L27P_2_G22
IO_L27P_3_T21
T21
B2_L28N_H18_J2_37
H18
IO_L28N_2_H18
IO_L28N_3_R22
R22
B2_L28P_J17_J2_38
J17
IO_L28P_2_J17
IO_L28P_3_R21
R21
B2_L29N_H21_J2_35
H21
IO_L29N_2_H21
IO_L29N_3_P19
P19
B2_L29P_H22_J2_36
H22
IO_L29P_2_H22
IO_L29P_3_R19
R19
B2_L31N_J18_J2_33
J18
IO_L31N_2_J18
IO_L31N_3_P18
P18
B2_L31P_J19_J2_34
J19
IO_L31P_2_J19
IO_L31P_3_P17
P17
B2_L32N_J21_J2_31
J21
IO_L32N_2_J21
IO_L32N_3_P22
P22
B2_L32P_J22_J2_32
J22
IO_L32P_2_J22
IO_L32P_3_P21
P21
B2_L33N_K17_J2_29
K17
IO_L33N_2_K17
IO_L33N_3_N18
N18
B2_L33P_K18_J2_30
K18
IO_L33P_2_K18
IO_L33P_3_N17
N17
B2_L34N_K19_J2_27
K19
IO_L34N_2_VREF_2_K19
IO_L34N_3_N20
N20
B2_L34P_K20_J2_28
K20
IO_L34P_2_K20
IO_L34P_3_VREF_3_N19
N19
B2_L35N_K21_J2_25
K21
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IO_L35N_3_N22
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IO_L38N_3_M18
M18
B2_L38P_L18_J2_24
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IO_L38P_3_M17
M17
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M20
B2_L39P_L20_J2_12
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M19
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L21
IO_L40N_2_L21
IO_L40N_3_VREF_3_M22
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M21
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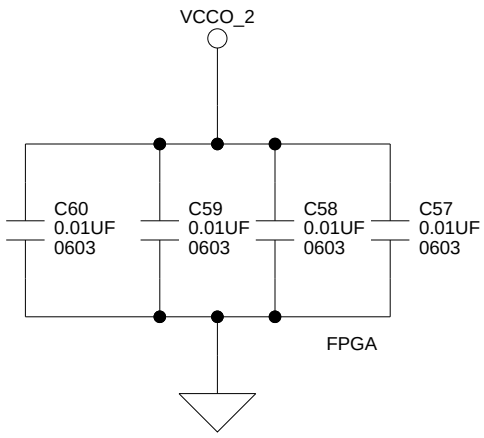
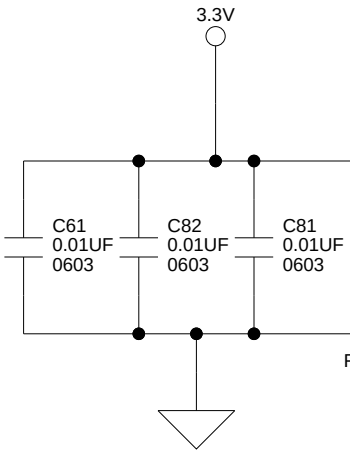
C20
IO_L01N_2_VRP_2_C20
IO_L01N_3_VRP_3_Y20
Y20
IO_L01P_2_VRN_2_C21_J2_16
C21
IO_L01P_2_VRN_2_C21
IO_L01P_3_VRN_3_Y19
Y19
XC3S1000
FG456


VCCO_2
C60
0.01UF
0603
C59
0.01UF
0603
C58
0.01UF
0603
C57
0.01UF
0603
FPGA


3.3V
C61
0.01UF
0603
C82
0.01UF
0603
C81
0.01UF
0603

3

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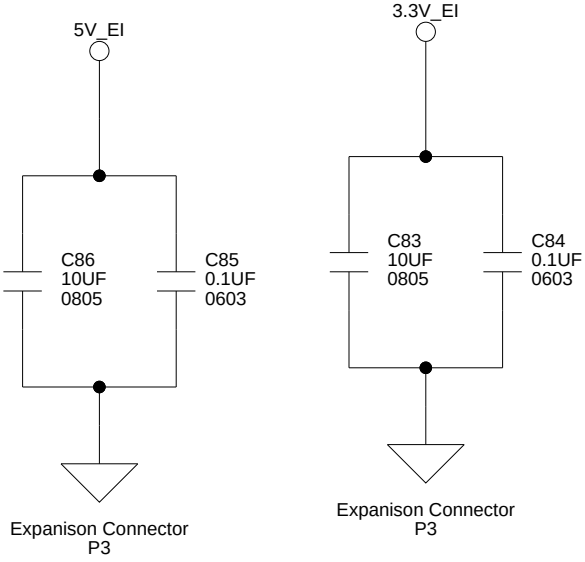
5V_EI
C86
10UF
0805
C85
0.1UF
0603
Expanison Connector
P3
3.3V_EI
C83
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0805
C84
0.1UF
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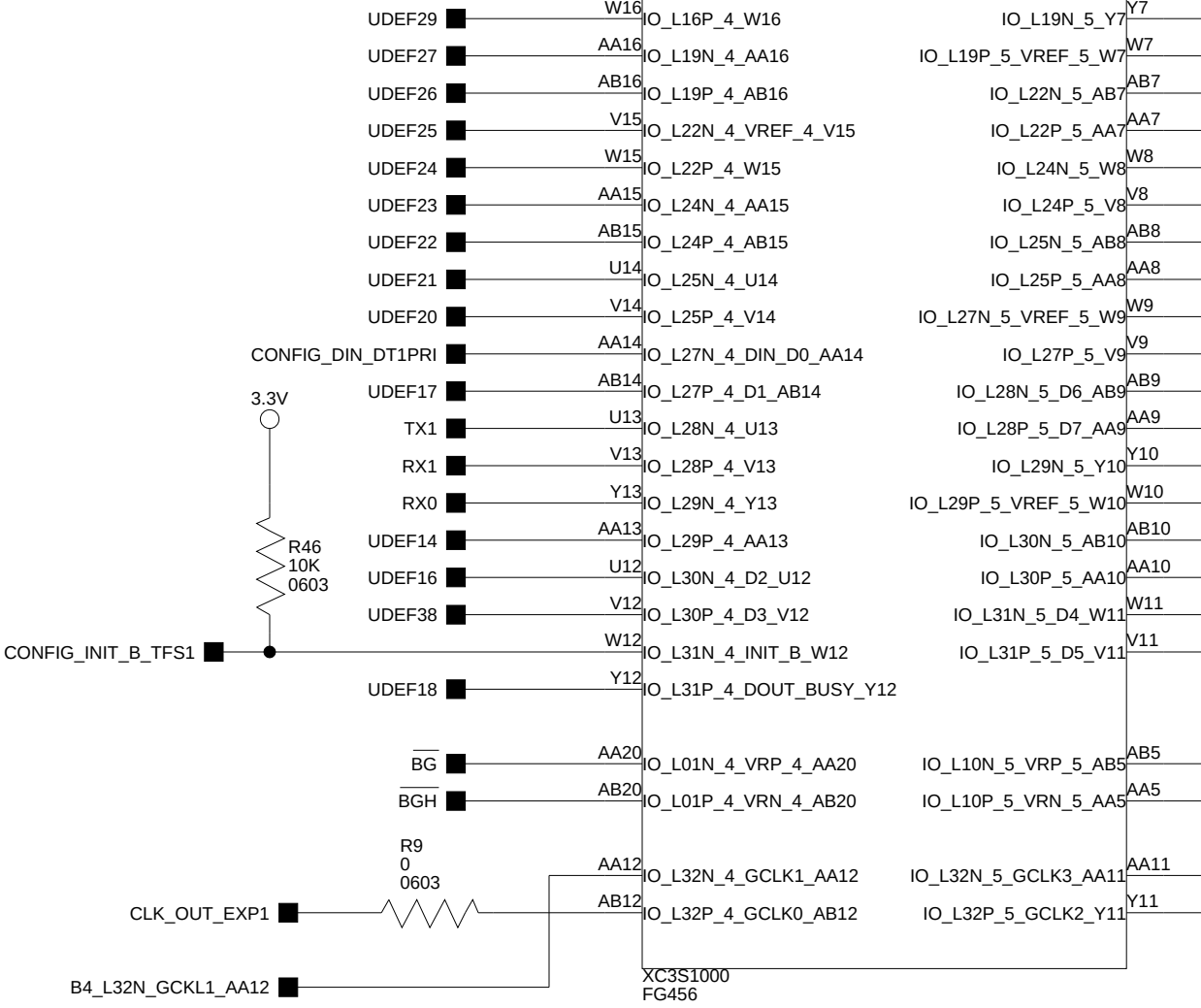
Expanison Connector
P3


UDEF29
W16
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IO_L25N_4_U14
IO_L25P_5_AA8
AA8
UDEF20
V14
IO_L25P_4_V14
IO_L27N_5_VREF_5_W9
W9
CONFIG_DIN_DT1PRI
AA14
IO_L27N_4_DIN_D0_AA14
IO_L27P_5_V9
V9
3.3V
UDEF17
AB14
IO_L27P_4_D1_AB14
IO_L28N_5_D6_AB9
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U13
IO_L28N_4_U13
IO_L28P_5_D7_AA9
AA9
RX1
V13
IO_L28P_4_V13
IO_L29N_5_Y10
Y10
RX0
Y13
IO_L29N_4_Y13
IO_L29P_5_VREF_5_W10
W10
R46
10K
0603
UDEF14
AA13
IO_L29P_4_AA13
IO_L30N_5_AB10
AB10
UDEF16
U12
IO_L30N_4_D2_U12
IO_L30P_5_AA10
AA10
UDEF38
V12
IO_L30P_4_D3_V12
IO_L31N_5_D4_W11
W11
CONFIG_INIT_B_TFS1
W12
IO_L31N_4_INIT_B_W12
IO_L31P_5_D5_V11
V11
UDEF18
Y12
IO_L31P_4_DOUT_BUSY_Y12
BG
AA20
IO_L01N_4_VRP_4_AA20
IO_L10N_5_VRP_5_AB5
AB5
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AB20
IO_L01P_4_VRN_4_AB20
IO_L10P_5_VRN_5_AA5
AA5
R9
0
0603
AA12
IO_L32N_4_GCLK1_AA12
IO_L32N_5_GCLK3_AA11
AA11
CLK_OUT_EXP1
AB12
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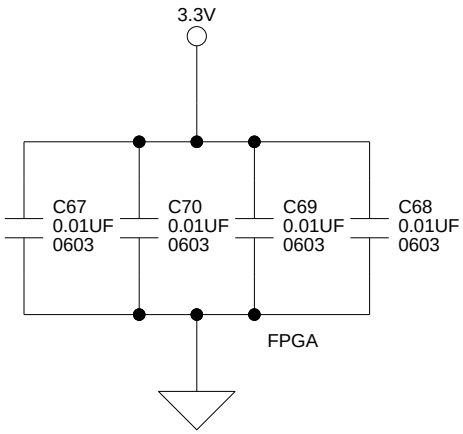
3.3V
C67
0.01UF
0603
C70
0.01UF
0603
C69
0.01UF
0603
C68
0.01UF
0603
FPGA

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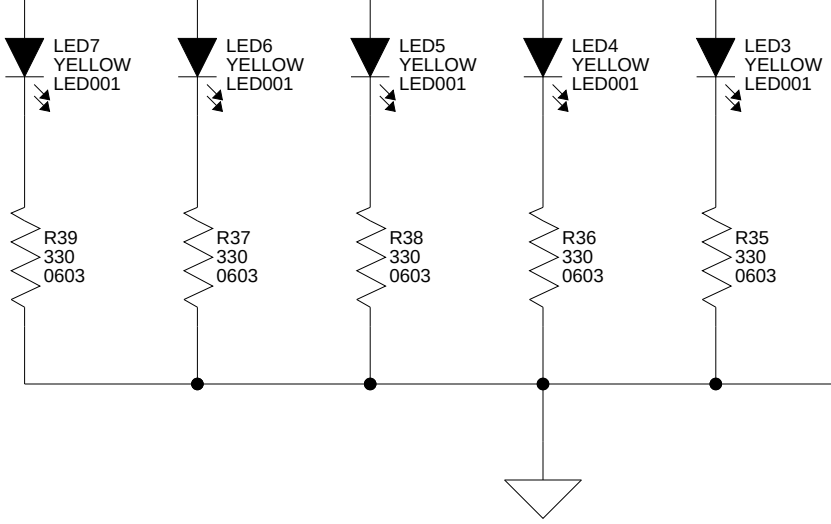
LED7
YELLOW
LED001
LED6
YELLOW
LED001
LED5
YELLOW
LED001
LED4
YELLOW
LED001
LED3
YELLOW
LED001
R39
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R37
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R35
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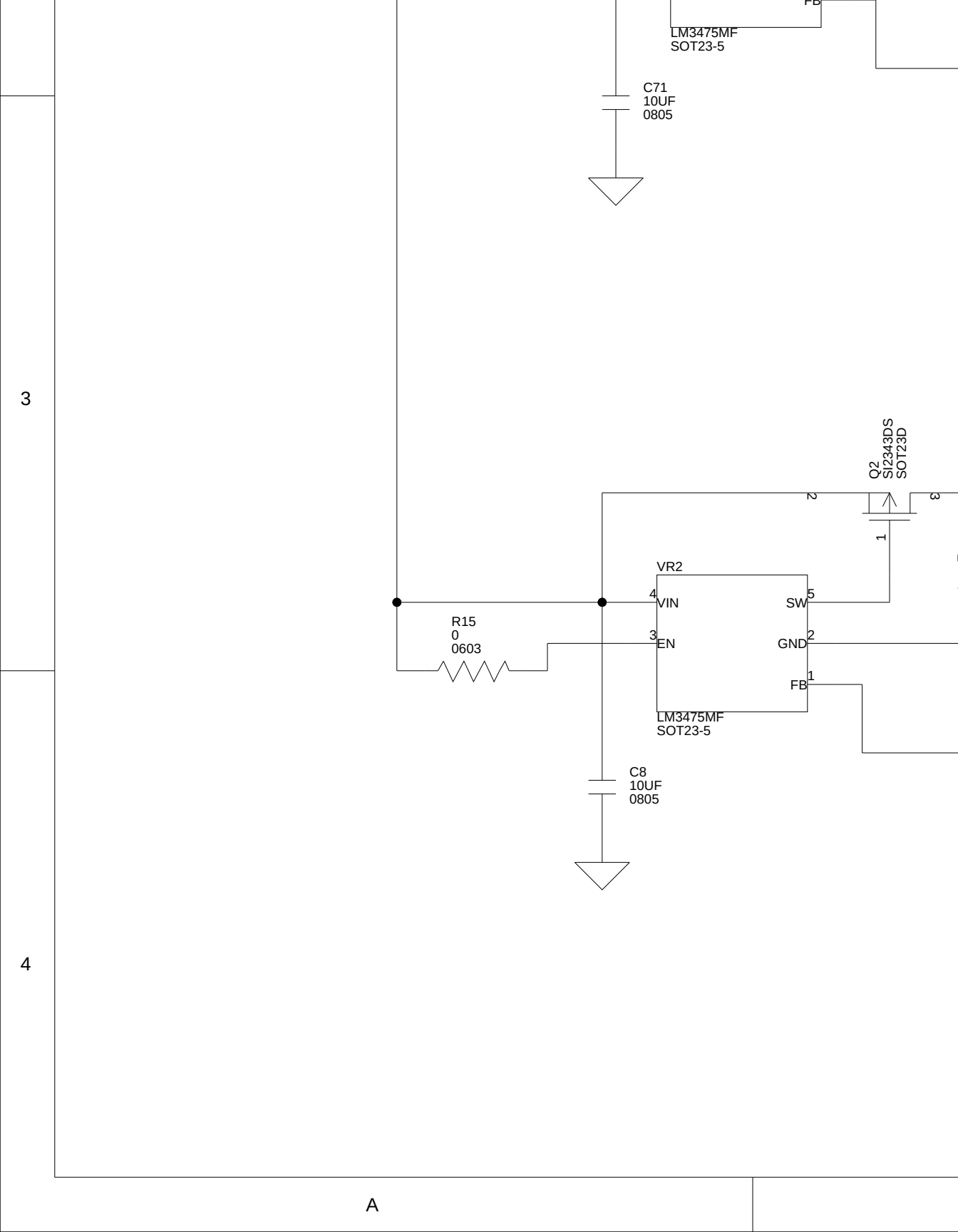
FB
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C71
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3
Q2
SI2343DS
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VR2
4
VIN
SW
5
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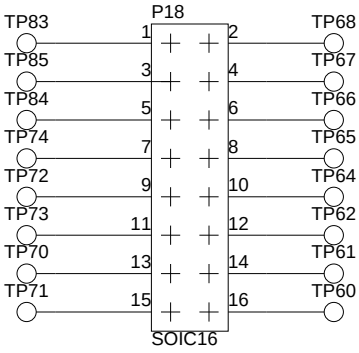
4
A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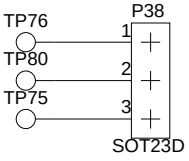
SOIC16


P38
TP76
TP80
TP75
1
2
3
SOT23D

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