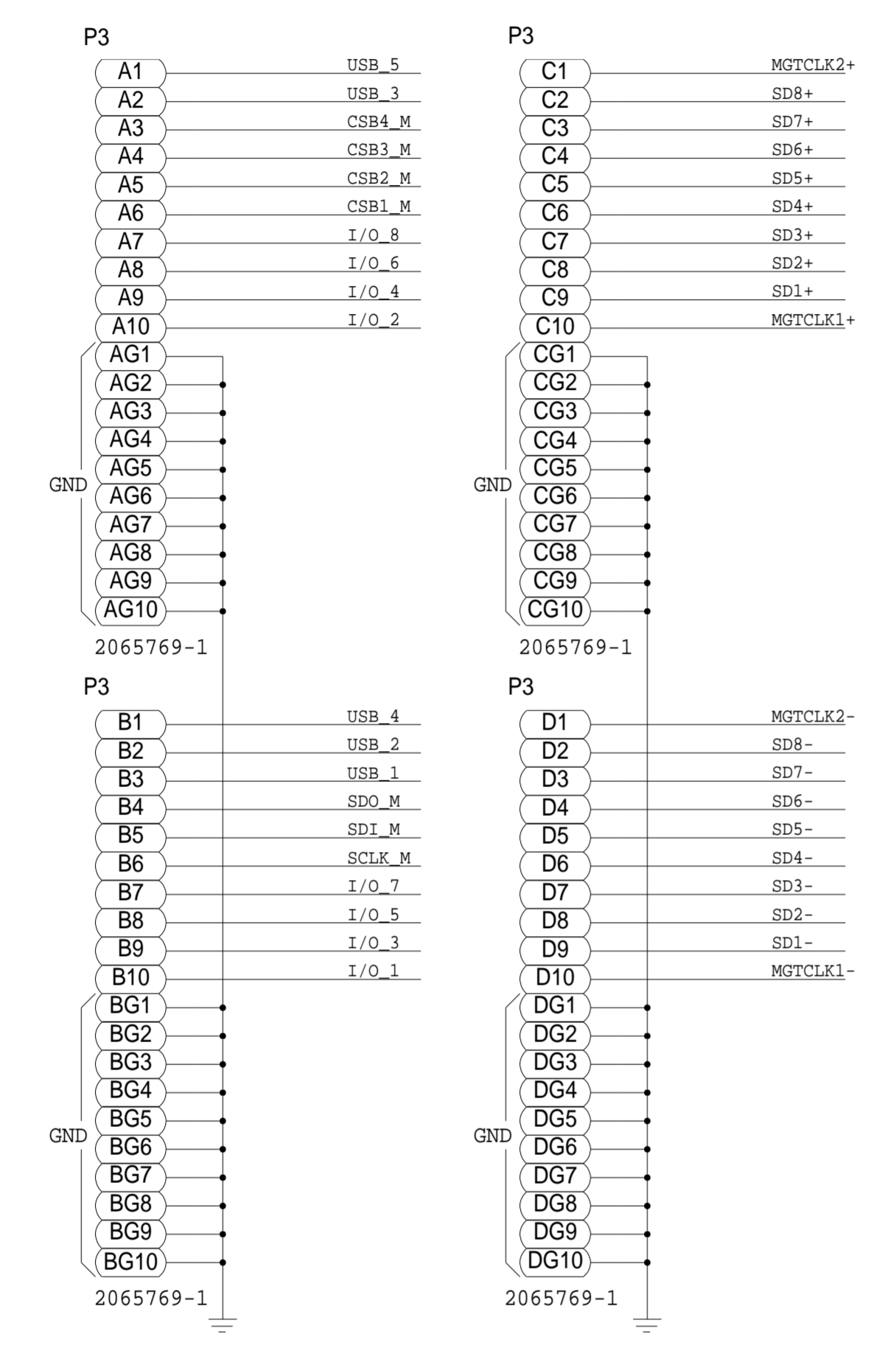


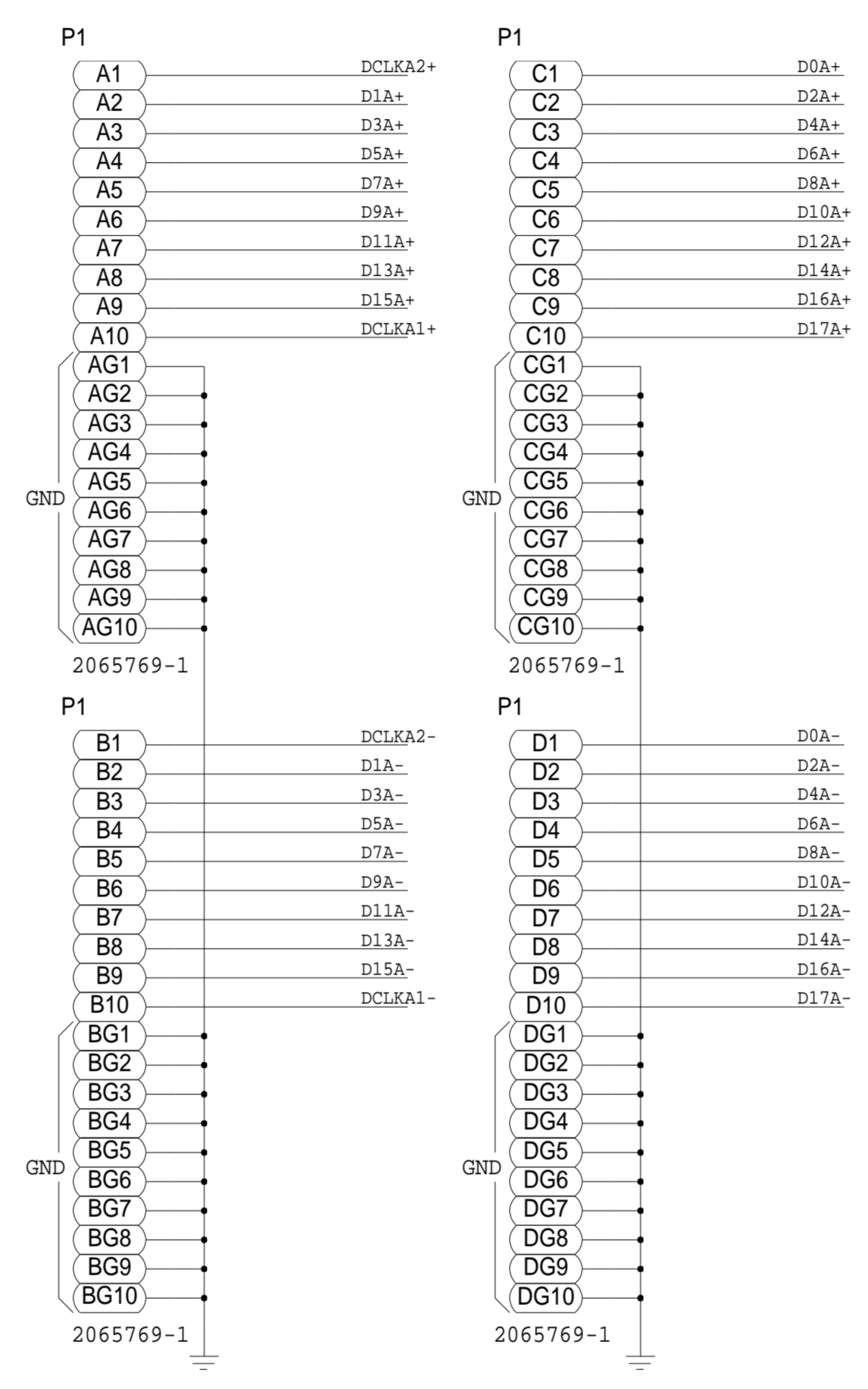
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

EVAL BOARD CONNECTIONS

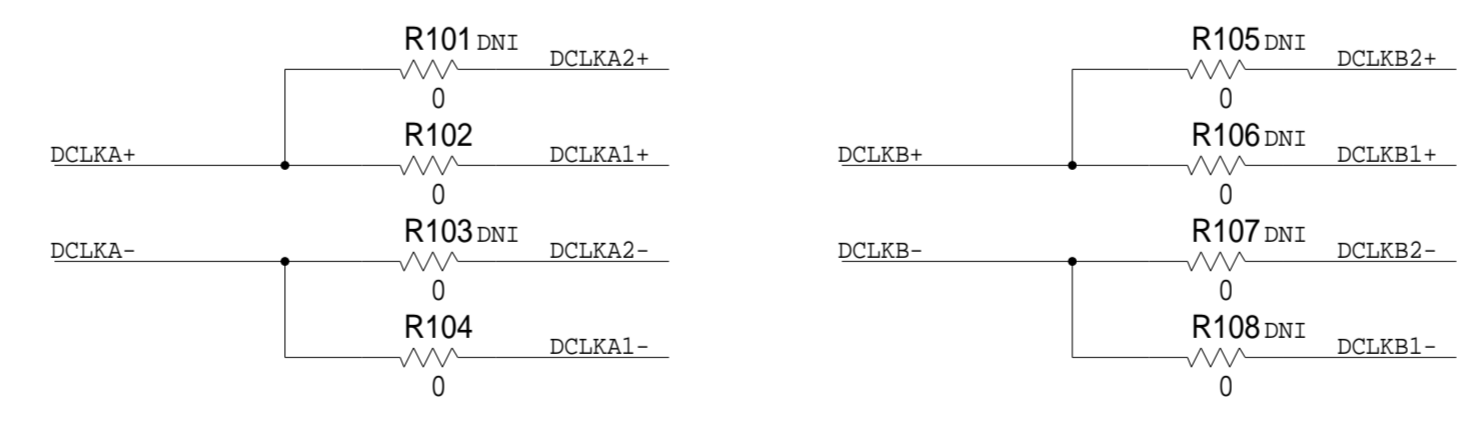
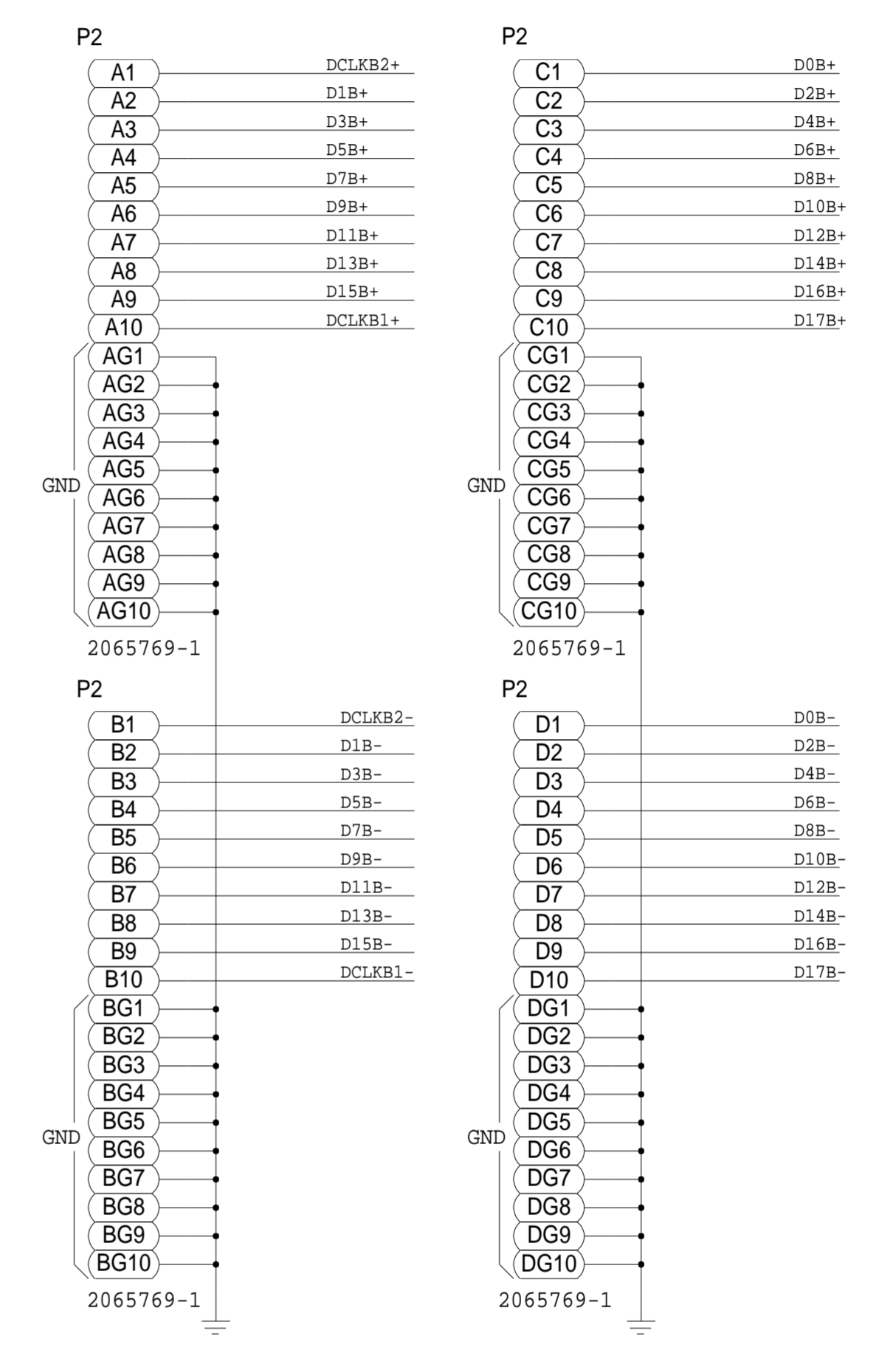
(J1) HS-SERIAL/SPI/AUX



(J3) DATA BUS 2



(J2) DATA BUS 1



SELECT GLOBAL CLOCK OR CLOCK CAPABLE IO

	SCHEMATIC		
	<DRAWING TITLE HEADER> CVTADCFMCINTPZ ENGINEERING BOARD		
	DESIGN VIEW <DESIGN VIEW>	DRAWING NO. CVTADCFMCINTPZ01	REV B
PTD ENGINEER R. Reeder	SIZE D	SCALE NONE	SHEET 1 OF 2

D
C
B
A

D
C
B
A

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

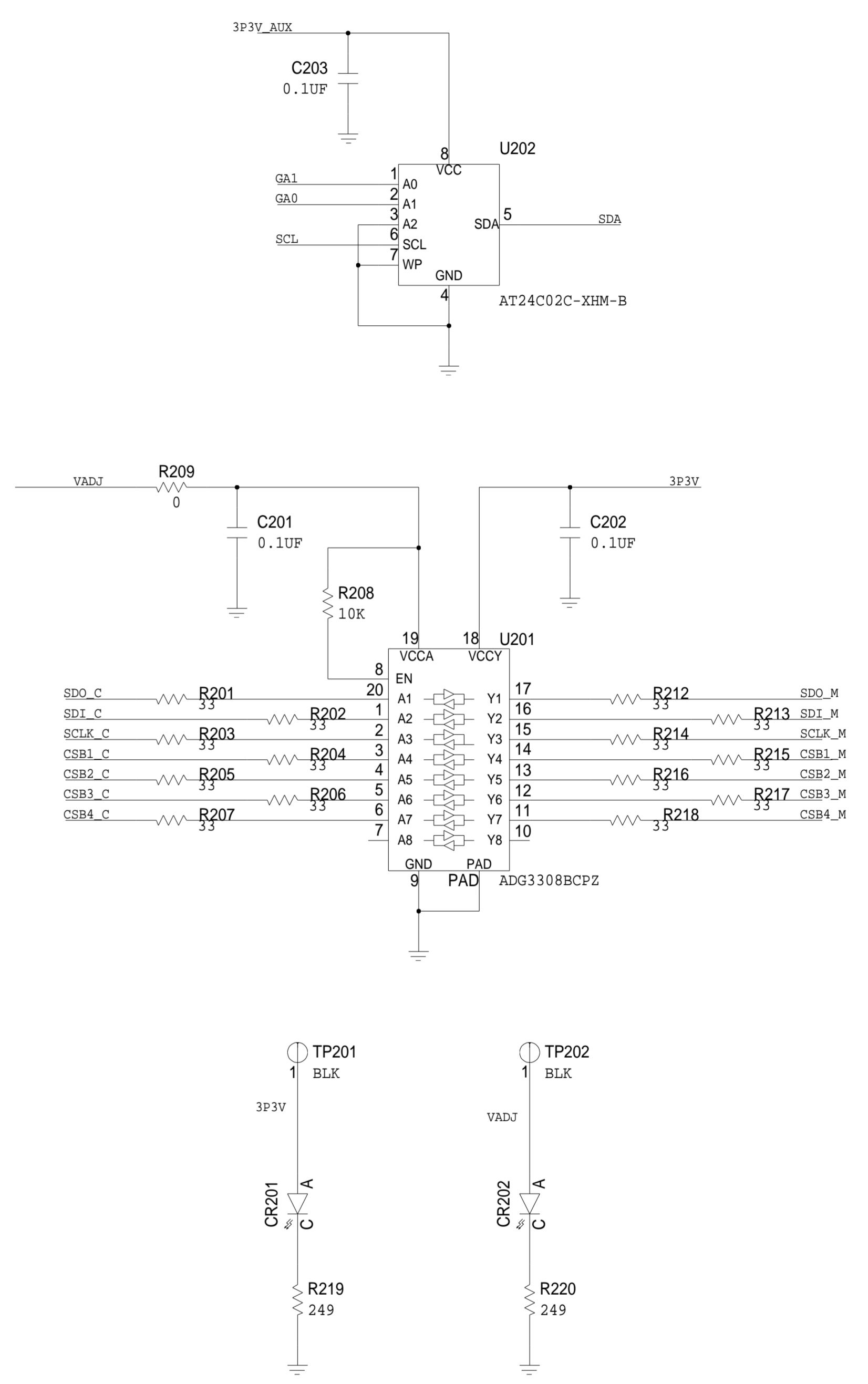
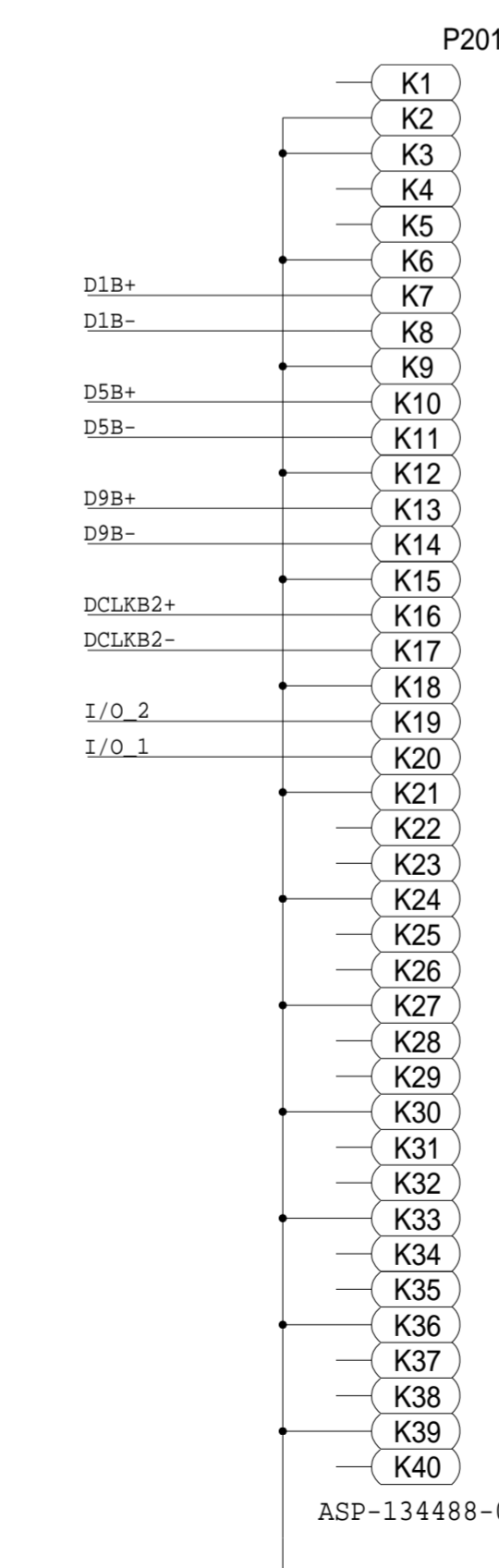
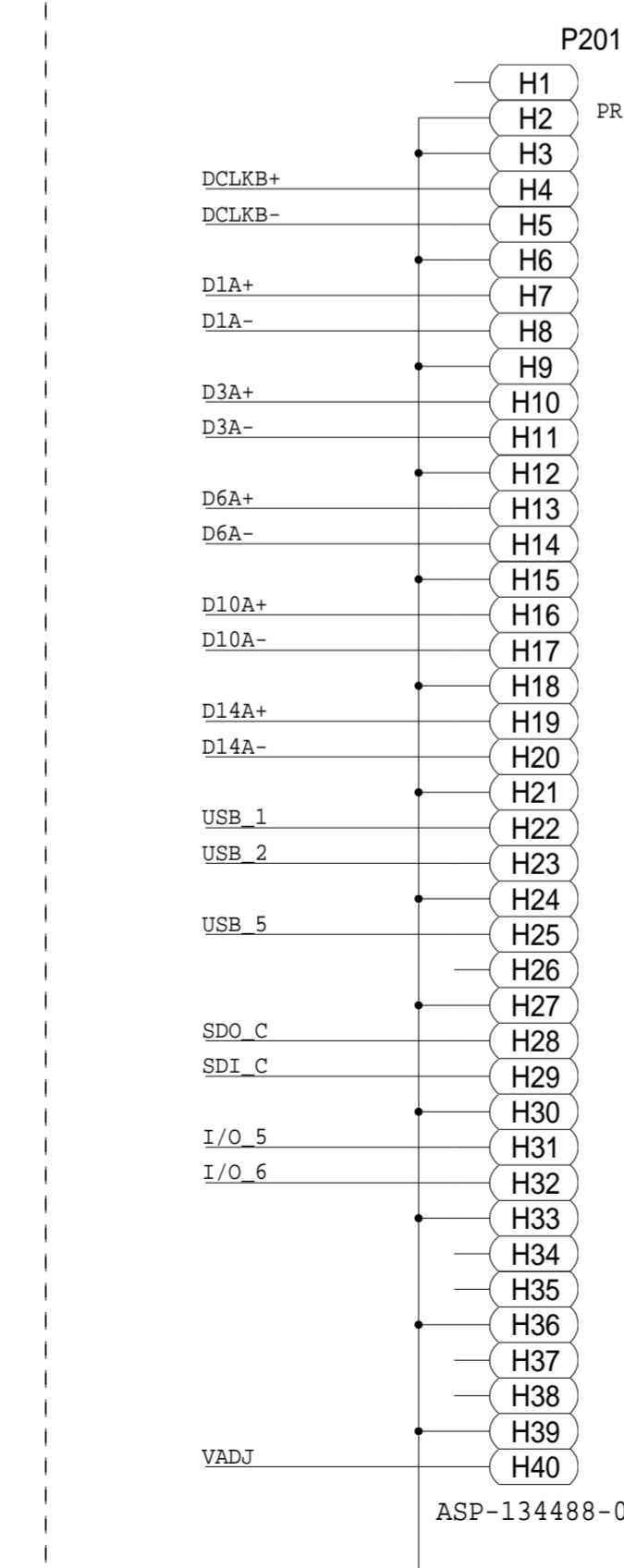
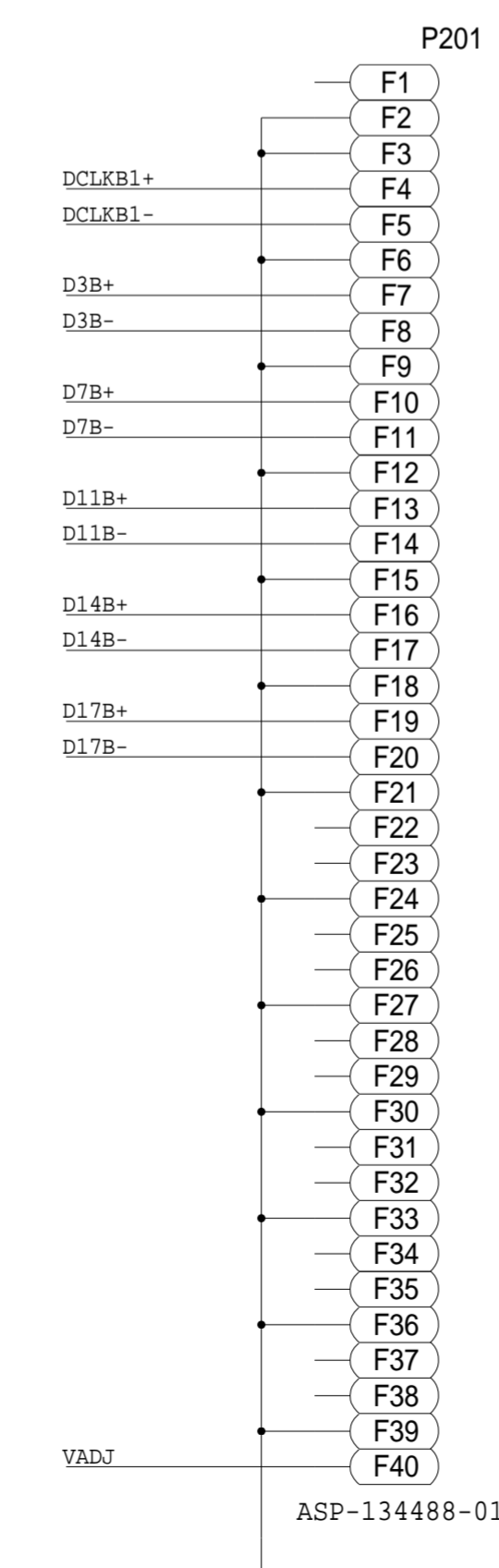
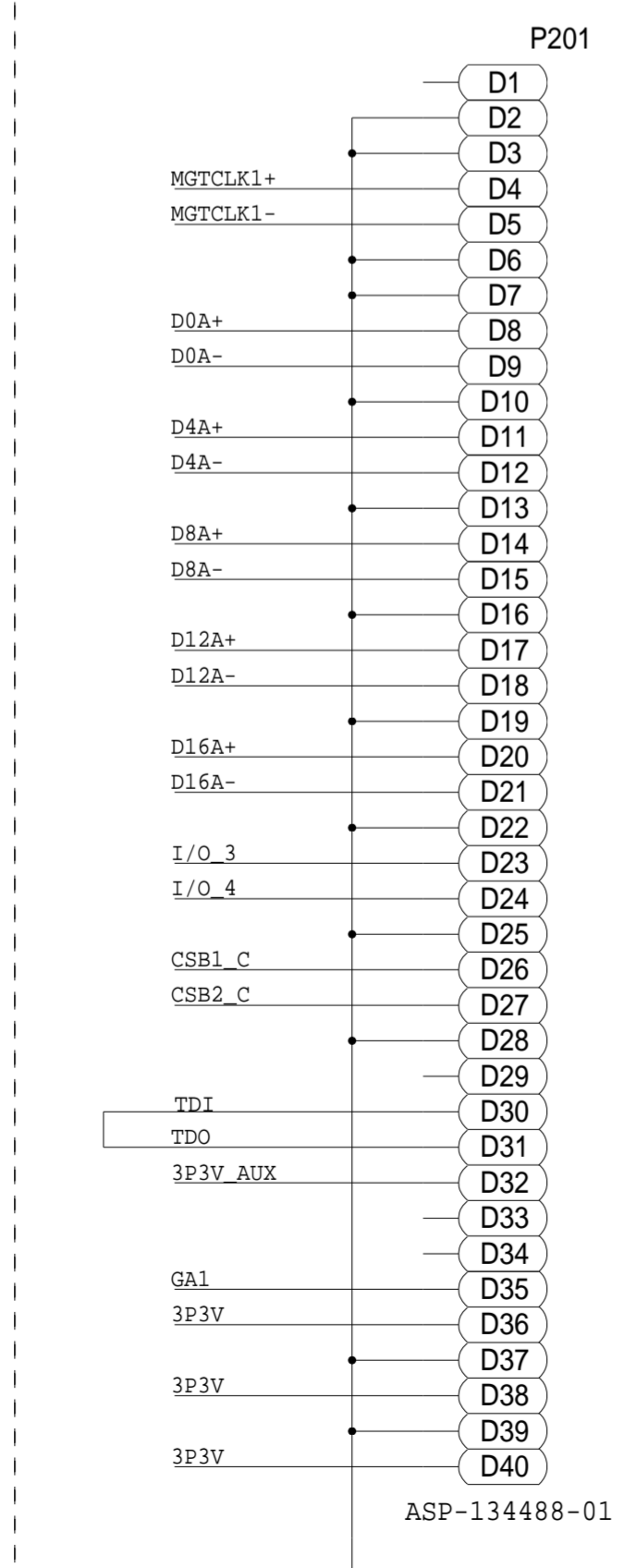
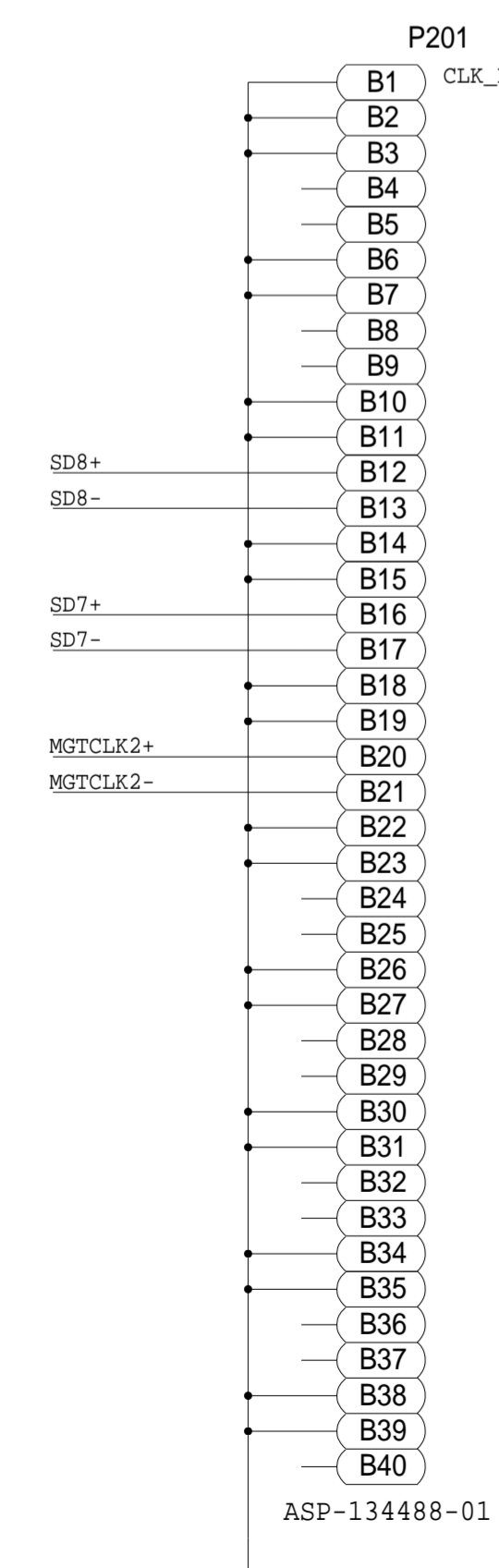
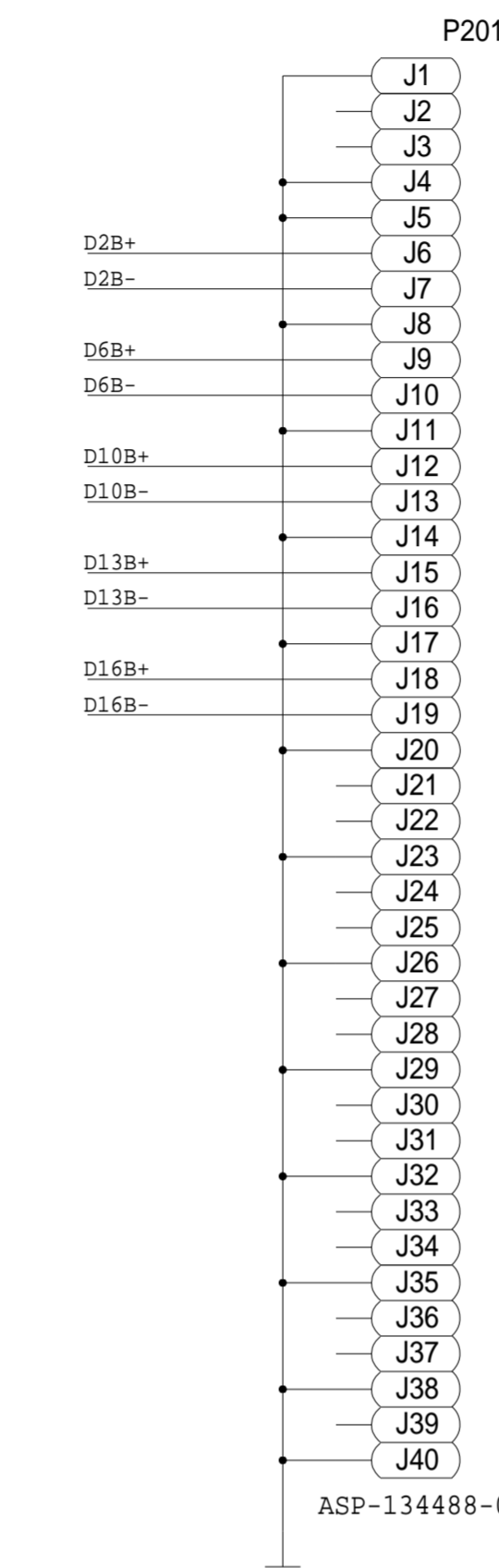
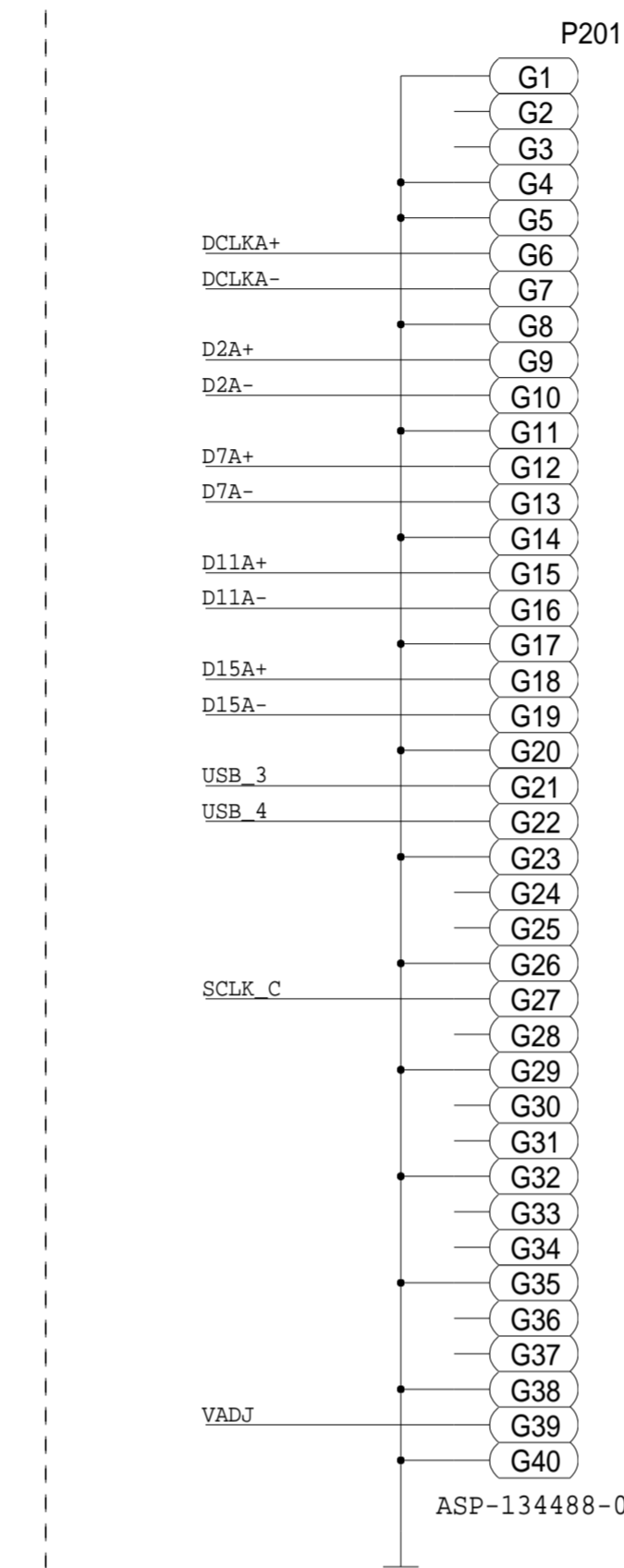
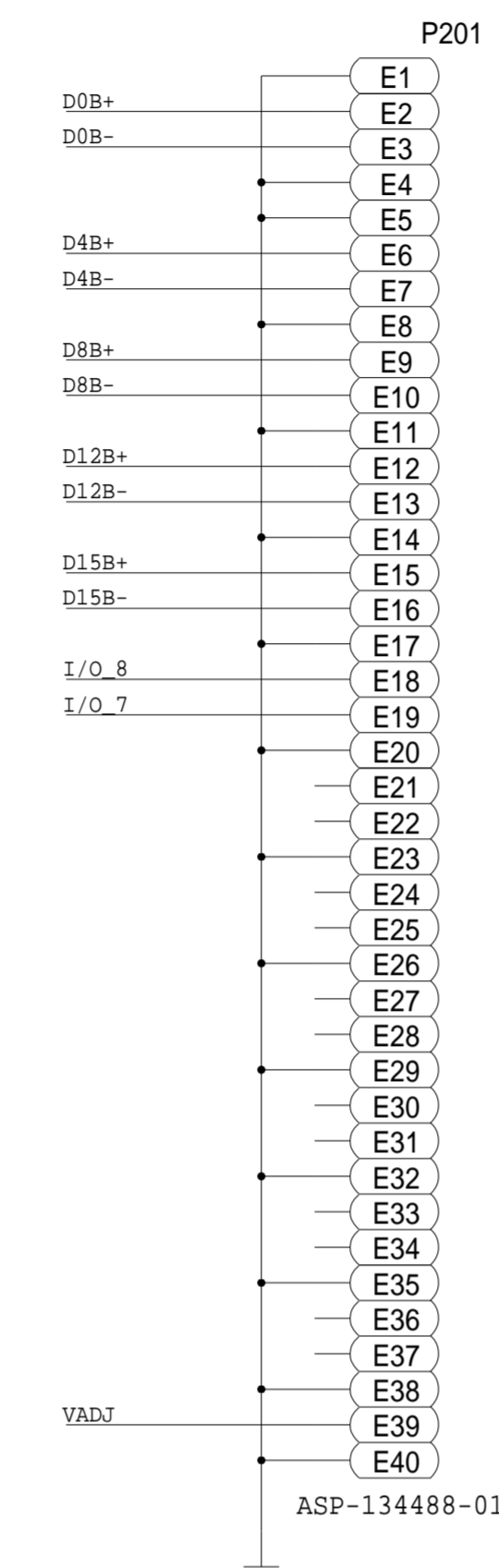
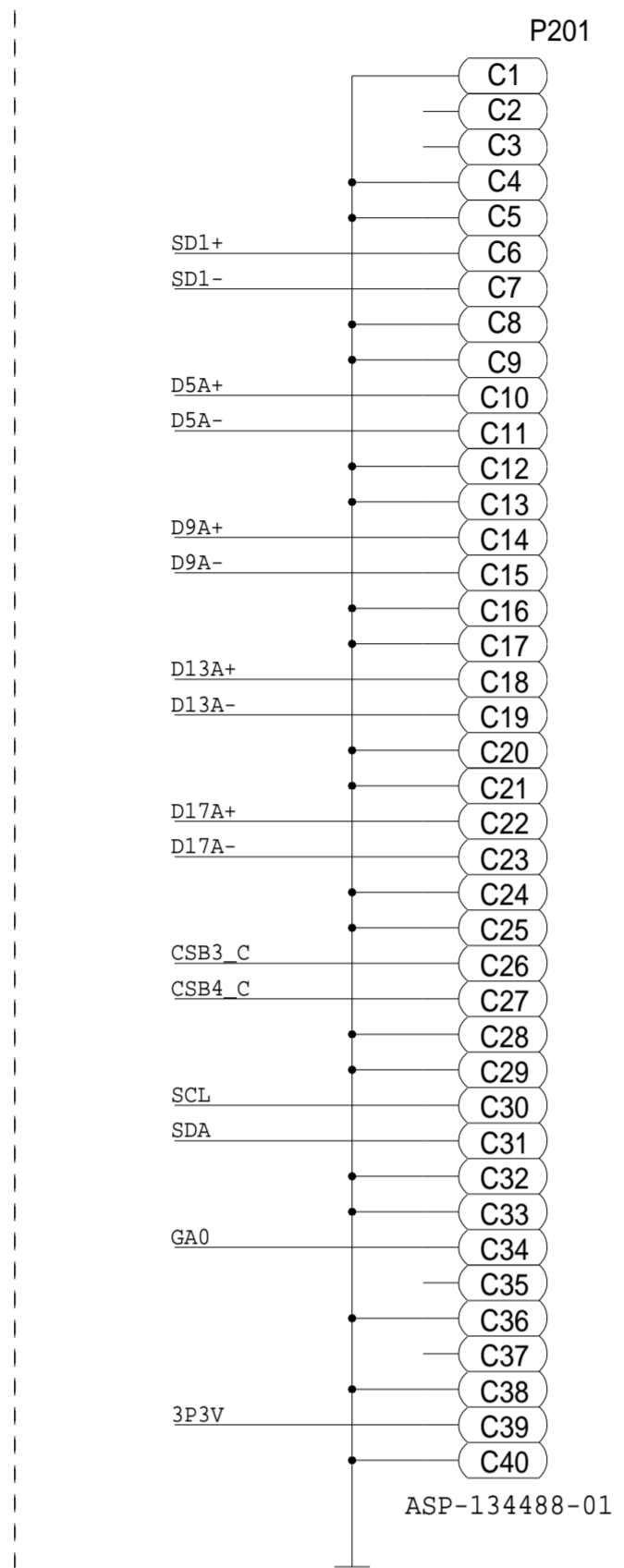
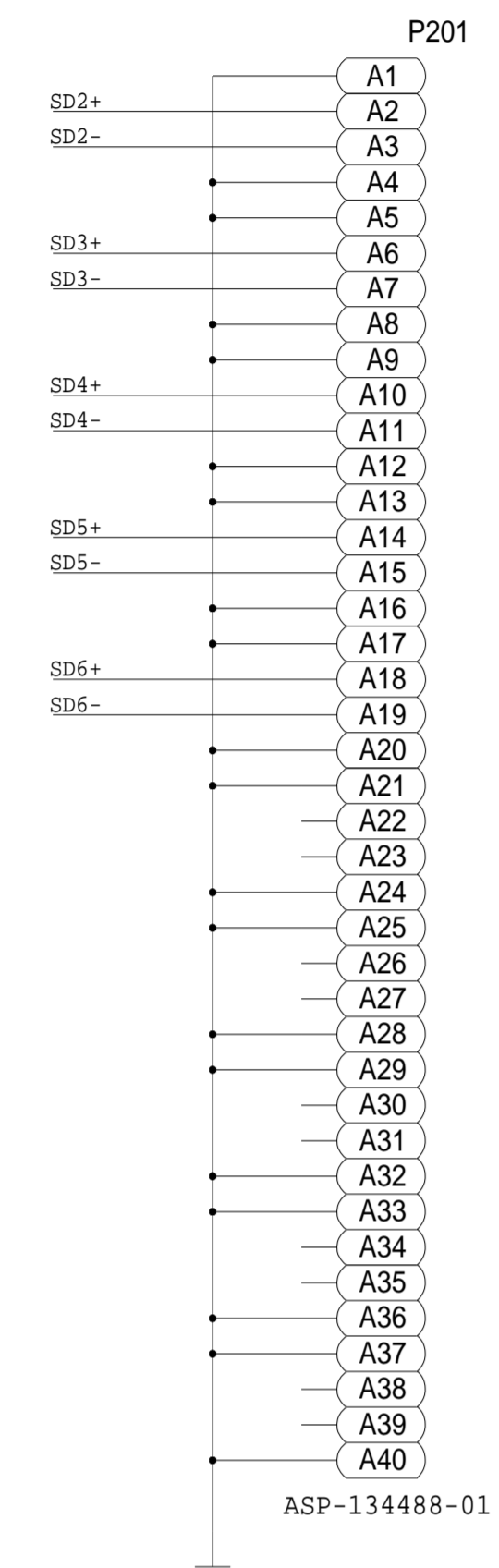
FMC CONNECTIONS

NOTE:

3P3V = 3.3V
VADJ = 3.3V - 0V

D
C
B
A

D
C
B
A



SCHEMATIC			
<DRAWING TITLE HEADER> CVTADCFMCIPTPZ ENGINEERING BOARD			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. CVTADCFMCIPTPZ01	REV B	
PTD ENGINEER R. Reeder	SCALE NONE	SHEET 2 OF 2	

8 7 6 5 4 3 2 1

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