DEMO MANUAL DC048

LTC1066-1 FILTER BOARD

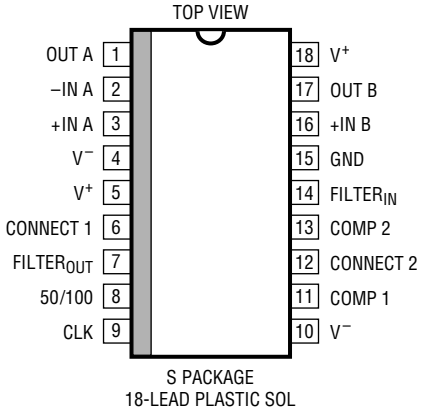
Switched-Capacitor Filter Evaluation Board for LTC1066-1

DESCRIPTION

This demonstration board allows the user to evaluate the LTC®1066-1 switched-capacitor filter over the full operational range. This board demonstrates proper layout, bypassing, buffering and clock line routing to achieve best performance from the LTC filter products. **Gerber files for this circuit board are available. Call the LTC factory.**

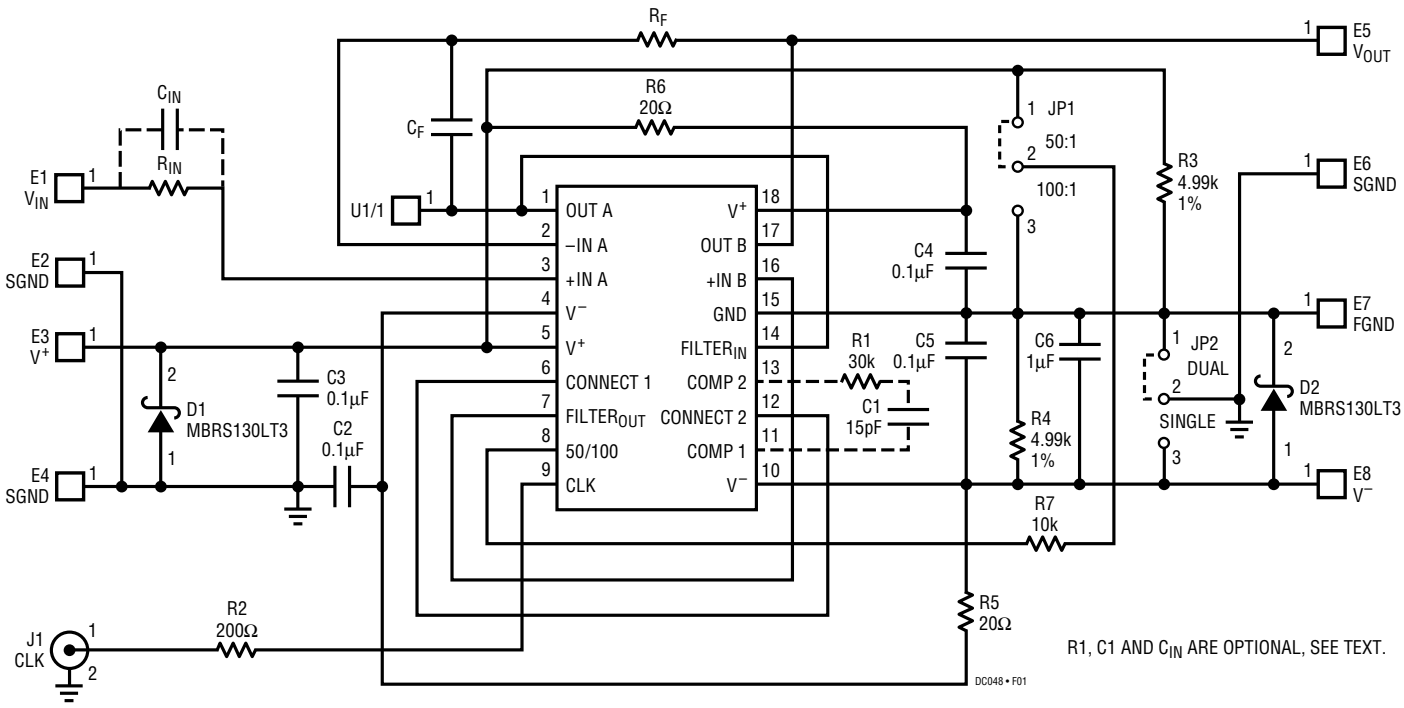
BOARD PHOTO

PACKAGE DIAGRAM



S PACKAGE
18-LEAD PLASTIC SOL

SCHEMATIC DIAGRAM



PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	PHONE NUMBER
C_F, C6 (Note 1)	2	GRM42-6Y5V105Z025AL	Cap, 1.0µF, 25V, 10%	Murata-Erie	(814) 237-1431
C2, C3, C4, C5	4	VJ1206Y104KXAMT	Cap, 0.1µF, 50V, 10%	Vitramon	(203) 268-6261
D1, D2	2	MBRS130LT3	Schottky Diode	Motorola	(602) 244-3576
E1 to E8	8	1502-2	Terminal	Keystone	(718) 956-0666
J1	1	227699-3	PCB Mount BNC	AMP	(717) 564-0100
JP1, JP2	2	TSW-103-07-G-S	Header	Samtec	(812) 944-6744
R_F	1	5043EM20K00J	Res, 20k, 1/4W, 5%	Philips	(817) 325-7871
R_{IN}	1	CD 1/4Z	Res, 0, 1/4W	SEI	(919) 850-9500
R2	1	CR32-201J	Res, 200Ω, 1/8W, 5%	AVX	(803) 448-9411
R3, R4	2	5043EM4K990F	Res, 4.99k, 1/4W, 1%	Philips	(817) 325-7871
R5, R6	2	CR32-200J	Res, 20Ω, 1/8W, 5%	AVX	(803) 448-9411
R7	1	CR32-103J	Res, 10k, 1/8W, 5%	AVX	(803) 448-9411
U1	1	LTC1066-1CS	IC	LTC	(408) 432-1900
	2	SNT-100-BK-T	Shunt	Samtec	(812) 944-6744

Note 1: For filter cutoff frequencies as low as 10Hz, use a C_F = 33µF non-polarized surface mount electrolytic capacitor, Sanyo 16CV33NP (619) 661-6835 or equivalent.

DC048 OPERATION

DEMO BOARD OPERATION AND CONNECTION HINTS

When using the LTC1066-1 switched-capacitor filter evaluation board, the following steps should be followed to ensure correct operation. This demo board was designed for either single or dual supply operation.

Step 1: Connecting Power Supply Lines

For dual supply operation connect V^+ supply to E3 and V^- supply to E8. The power supply ground is connected to E4 and JP2 shorts E7 to SGND.

For single supply operation connect V^+ supply to E3 and the power supply ground to E4. JP2 shorts E8 to SGND. The potential at FGND (E7) is $V^+/2$.

Note the 20Ω resistors (R5, R6) that isolate the filter supply lines from the buffer supply lines. This may effect the output swing slightly (the maximum output voltage swing will be reduced by $20\Omega \times I_{OUT}$).

Step 2: Clock Input

Any TTL or CMOS clock source with a square wave output and 50% duty cycle (±10%) is adequate to connect to J1 (clock input). For single supply operation > 6V, the clock high level should be > 65% of V^+. See Table 1 for more detail on high and low threshold values.

The 200Ω resistor (R2) between J1 and pin 9 slows down the rise and fall times of the clock to further reduce charge coupling.

Table 1. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5V	2.18V	0.5V
Dual Supply = ±5V	1.45V	0.5V
Dual Supply = ±2.5V	0.73V	–2.0V
Single Supply = 12V	7.80V	6.5V
Single Supply = 5V	1.45V	0.5V

Step 3: Ratio 50:1/100:1

The DC level at pin 8 determines the ratio of the clock-to-filter cutoff frequency. When pin 8 is connected to V^+ the clock-to-cutoff frequency ratio (f_{CLK}/f_{CUTOFF}) is 50:1 and the filter response is elliptic. The design of the internal switched-capacitor filter was optimized for a 50:1 operation.

When pin 8 is connected to ground (or 1/2 supply for single supply operation), the f_{CLK}/f_{CUTOFF} ratio is equal to 100:1 and the filter response is pseudo-linear phase. When JP1 is not used and pin 2 of JP1 is connected to V^- (or SGND for single supply), the filter response is transitional Butterworth elliptic and the f_{CLK}/f_{CUTOFF} ratio is equal to 100:1 (please refer to the Typical Performance Characteristics in the LTC1066-1 data sheet).

When JP1 shorts R7 to V^+ the ratio is 50:1. If JP1 shorts R7 to SGND then the ratio is 100:1.

Since the ratio is mechanically switched by JP1, a 10k protection resistor is placed between pin 8 and the DC source.

Step 4: Input Connection

The input of LTC1066-1 is E1 (V_{IN}) which is referenced to E2 (SGND).

For single supply operation the input must be in the linear range of the filter. For example, in a single 5V operation the linear range is 1.4V to 3.6V referenced to E2 (SGND).

Step 5: Output Connection

The output of the LTC1066-1 is available at E5 (V_{OUT}) which is referenced to E6 (SGND).

Step 6: Compensation

If compensation is needed R1 and C1 should be installed. Compensation is recommended for the following cases shown in Table 2.

Table 2. Instances Where an R_C Compensation (15pF in Series with 30kΩ Pins 11, 13) is Recommended, f_{CLK}/f_{CUTOFF} = 50:1

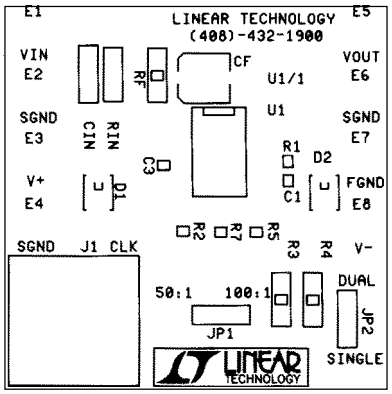
V_S = Single 5V (AGND = 2V)	T_A = 25°C T_A = 70°C	$f_{CUTOFF} \geq$ 28kHz $f_{CUTOFF} \geq$ 24kHz
V_S = ±5V	T_A = 25°C T_A = 70°C	$f_{CUTOFF} \geq$ 60kHz $f_{CUTOFF} \geq$ 50kHz
V_S = ±7.5V	T_A = 25°C T_A = 70°C	$f_{CUTOFF} \geq$ 70kHz $f_{CUTOFF} \geq$ 60kHz

Step 7: R_{IN}, C_{IN}

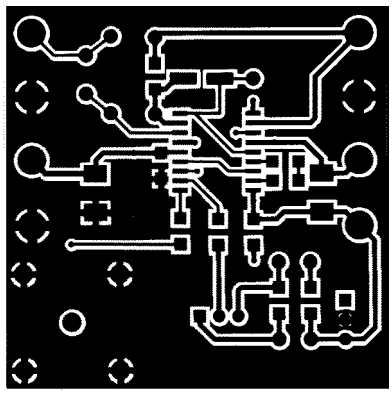
If R_F is greater than 20k, R_{IN} must be changed from a short to a value equal to R_F. C_{IN} must be 0.1µF.

Please refer to the AC performance section under the Applications Information section in the LTC1066-1 data sheet.

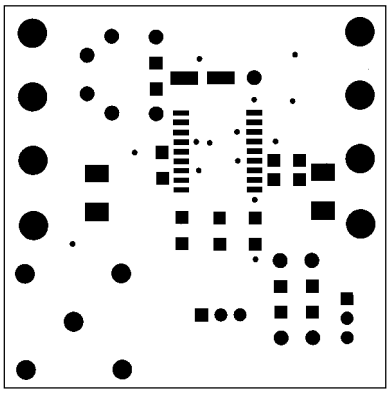
PCB LAYOUT AND FILM



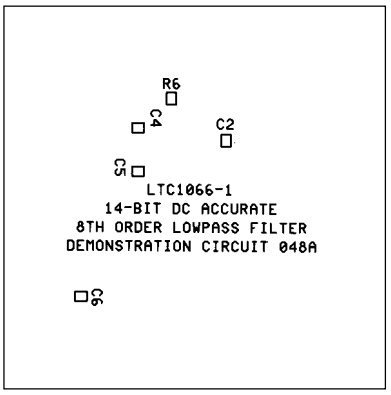
Component Side Silkscreen



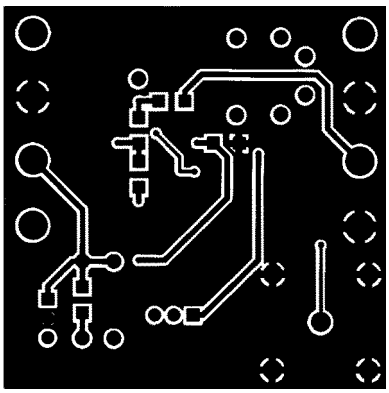
Component Side



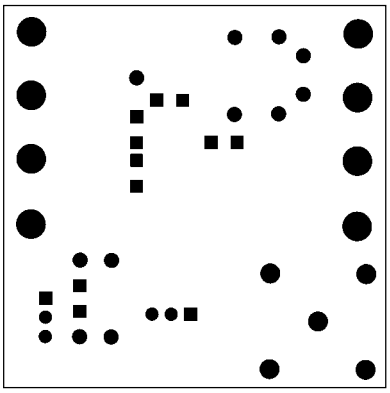
Component Side Solder Mask



Solder Side Silkscreen



Solder Side



Solder Side Solder Mask

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