LINEAR TECHNOLOGY

LTC4310-1/LTC4310-2
Hot Swappable I^{2}C Isolators

DESCRIPTION

Demonstration circuit 1079A features the LTC4310 I^{2}C isolator. The LTC®4310 provides bidirectional I^{2}C communication between two I^{2}C buses whose grounds are isolated from one another. Each LTC4310 encodes I^{2}C bus logic states into signals that are transmitted across an isolation barrier to another LTC4310. The receiving LTC4310 decodes the transmission and drives its I^{2}C bus to the appropriate logic state. The isolation barrier can be bridged by an inexpensive Ethernet (or other) transformer to achieve communications across voltage differences reaching thousands of volts, or it can be bridged by capacitors for lower voltage isolation. DC1079A shows both transformer and capacitor techniques. Separate supplies are connected on opposite sides of the isolation barrier.

Rise time accelerators provide strong pull-up currents on SCL and SDA rising edges to meet rise time specifications for heavily loaded systems. Data and clock Hot Swap™ circuitry prevent data corruption when a card is inserted into or removed from a live bus. When a bus is stuck low for 37ms, the LTC4310 turns off its pull-down devices and generates up to sixteen clocks and a STOP bit in an attempt to free the bus. Driving EN low sets the LTC4310 in a very low current shutdown mode to conserve power. This is set with a jumper for each LTC4310 on the DC1079A.

The READY pin provides a digital output flag that pulls low to indicate that the LTC4310 is driving its SDA and SCL pins with the logic state information it is receiving on its RXP and RXN pins from the other LTC4310. An LED at each READY pin indicates that READY is low.

DC1079A-A is populated with the LTC4310-1 and is intended for use in I^{2}C systems up to 100kHz. DC1079A-B is populated with the LTC4310-2 which is intended for I^{2}C bus speeds from 100kHz to 400kHz.

Design files for this circuit board are available at http://www.linear.com/demo
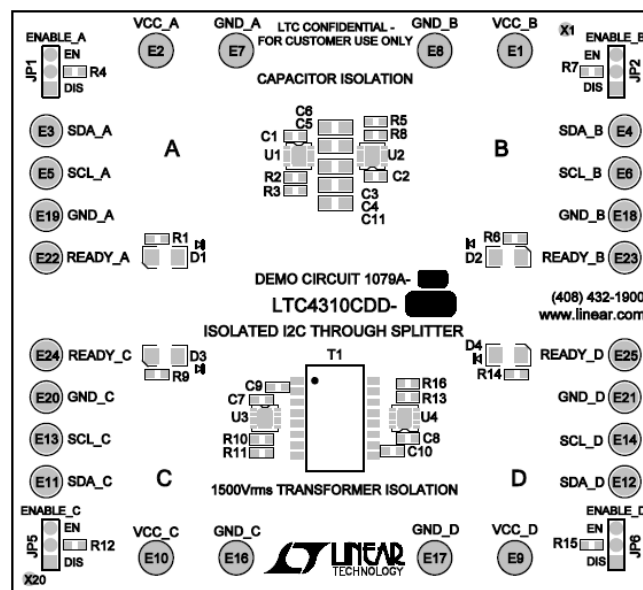
BOARD PHOTO

Figure 1. DC1079A

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PERFORMANCE SUMMARY

Table 1. DC1079A Typical Setup and Performance Summary (T_A = 25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply and Bus Voltage	VCC_A to GND_A, VCC_B to GND_B, VCC_C to GND_C, VCC_D to GND_D	3		5.5	V
Isolation	GND_A to GND_B, 100V Capacitor Coupling GND_C to GND_D, EPF8119S Transformer Coupling		100 1500		V V_{RMS}
Maximum I2C Clock	DC1079A-A, LTC4310-1 DC1079A-B, LTC4310-2		100 400		kHz kHz
Bus Pull-Up Resistors	DC1079A-A, LTC4310-1 DC1079A-B, LTC4310-2		10 3.3		kΩ kΩ

QUICK START PROCEDURE

Demonstration circuit 1079A is easy to set up to evaluate the performance of the LTC4310. Refer to Figure 2 and Figure 3 for proper measurement equipment setup and follow the procedures below.

100V Isolation with Capacitor Coupling (Figure 2):

1. Connect first supply (3V to 5.5V) across VCC_A and GND_A.

2. Connect first I2C bus to SDA_A and SCL_A.

3. Set ENABLE_A Jumper to EN.

4. Connect second supply (3V to 5.5V) across VCC_B and GND_B.

5. Connect second I2C bus to SDA_B and SCL_B.

6. Set ENABLE_B Jumper to EN.

1500V_{RMS} Isolation with Transformer Coupling (Figure 3):

1. Connect first supply (3V to 5.5V) across VCC_C and GND_C.

2. Connect first I2C bus to SDA_C and SCL_C.

3. Set ENABLE_C Jumper to EN.

4. Connect second supply (3V to 5.5V) across VCC_D and GND_D.

5. Connect second I2C bus to SDA_D and SCL_D.

6. Set ENABLE_D Jumper to EN.
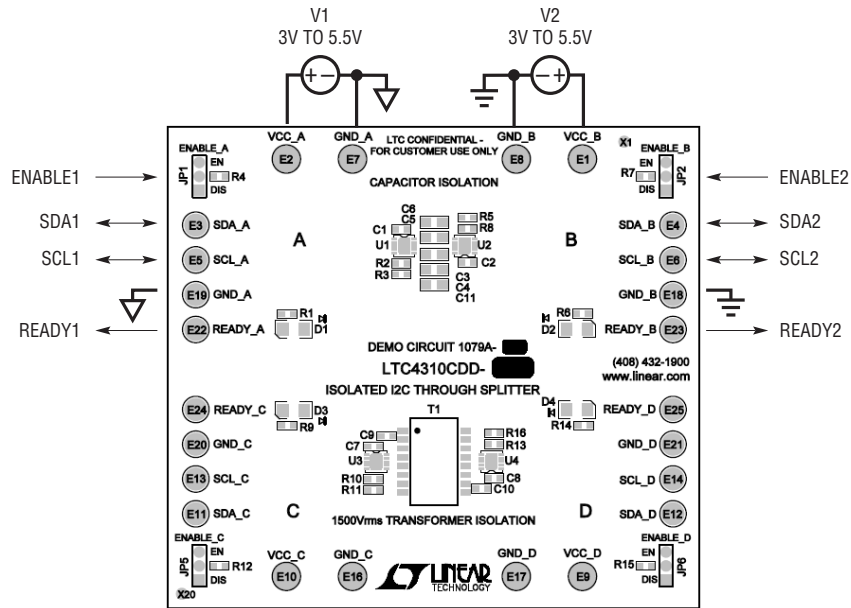
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QUICK START PROCEDURE

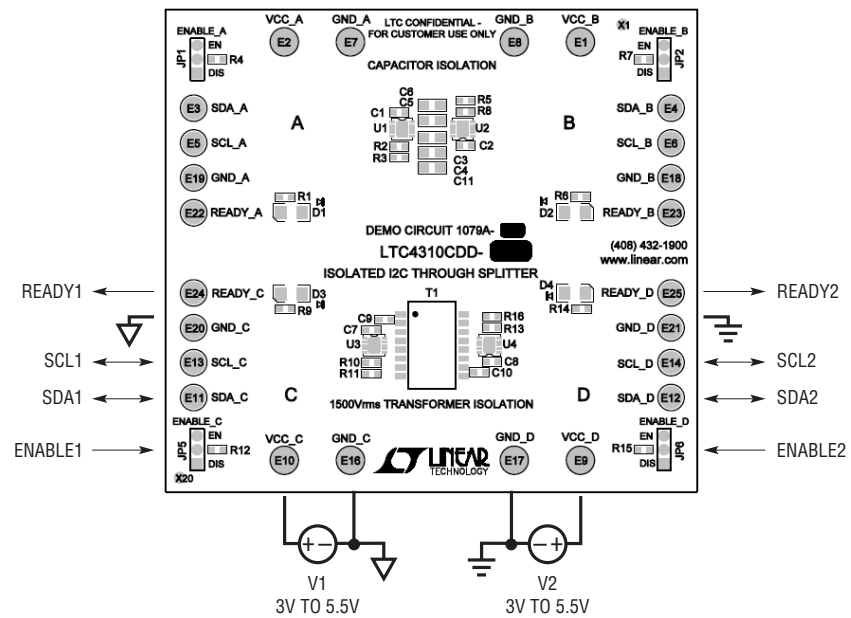Figure 2. DC1079A Setup for Low Voltage Isolation and Capacitor Coupling

Figure 3. DC1079A Setup for High Voltage Isolation and Transformer Coupling

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OPERATION

DC1079A demonstrates I^{2}C communication sent across an isolation barrier with the LTC4310. For low voltage 100V isolation, a power supply between 3V to 5.5V is connected across VCC_A and GND_A. This supply provides the pull-up supply for the I^{2}C bus connected to this side of the ground isolation. A second supply, isolated from the first supply, is connected across VCC_B and GND_B. The second I^{2}C bus is connected to this side and pulled-up to VCC_B.

The state of the I^{2}C bus on GND_A is transmitted by an LTC4310 to the corresponding LTC4310 on GND_B across small 100pF, 100V capacitors. And vice versa, the LTC4310 on GND_B reports its I^{2}C bus state to the LTC4310 on GND_B. When both supplies are up, both LTC4310 devices are enabled (set by jumpers), communication between the two LTC4310 devices is established, and the bus lines are not stuck low, a READY signal is given by each LTC4310. A green LED on each side of the isolation is driven by the respective READY pin and indicates that I^{2}C is linked between the two buses.

In an application with higher voltage isolation of 1500V$_{RMS}$, an inexpensive Ethernet transformer is used in place of the coupling capacitors. This is demonstrated in the bottom half of the DC1079A. The setup and operation is the same above with the capacitor coupling, but the supplies and I^{2}C buses are connected to GND_C and GND_D ground sides.

DC1079A-A and DC1079A-B DIFFERENCES

On the DC1079A-A, the LTC4310-1 is used at U1, U2, U3, and U4 and intended for bus speeds up to 100kHz. The DC1079A-B uses the LTC4310-2 in all four places instead and is intended for bus speeds from 100kHz to 400kHz. When the SDA (or SCL) bus is rising between 0V and 0.35

• V$_{CC}$, the LTC4310 controls the bus rise rate to (0.35 • V$_{CC}$)/900ns for the LTC4310-1 and to (0.35 • V$_{CC}$)/300ns for the LTC4310-2.

Bus pull-up resistors R2 and R3 that go to VCC_A, R5 and R8 that go to VCC_B, R10 and R11 that go to VCC_C, and R13 and R16 that go to VCC_D are also different between the DC1079A-A and the DC1079A-B. The 10k pull-ups along with the LTC4310-1 on the DC1079A-A allows for approximately 50pF of bus capacitance with a supply of 5V, or 3pF with a 3.3V supply. On the DC1079A-B, the 3.3k pull-ups along with the LTC4310-2 allows for close to 100pF of bus capacitance with a supply of 5V or 3.3V. Refer to the SDA, SCL Bus Pull-Up Resistor Value Selection section in the LTC4310 datasheet.

RADIATED EMISSIONS

DC1079A capacitor coupling and transformer coupling circuits have been tested and scanned for radiated emissions. The levels fall below the limits defined in the basic international EMI standard CIPR22 Class B. Figure 4 shows the results for the capacitor coupling and Figure 5 is the results for transformer coupling. Layout, parts placement, component selection, and wire connections will all have an effect with radiated emissions. Attention must be paid towards these items when testing for radiated emissions.

BOARD LAYOUT

DC1079A layout provides galvanic isolation on all four layers between the grounds as well as the vias, copper and pads referenced to the respective ground. Refer to the layout files.
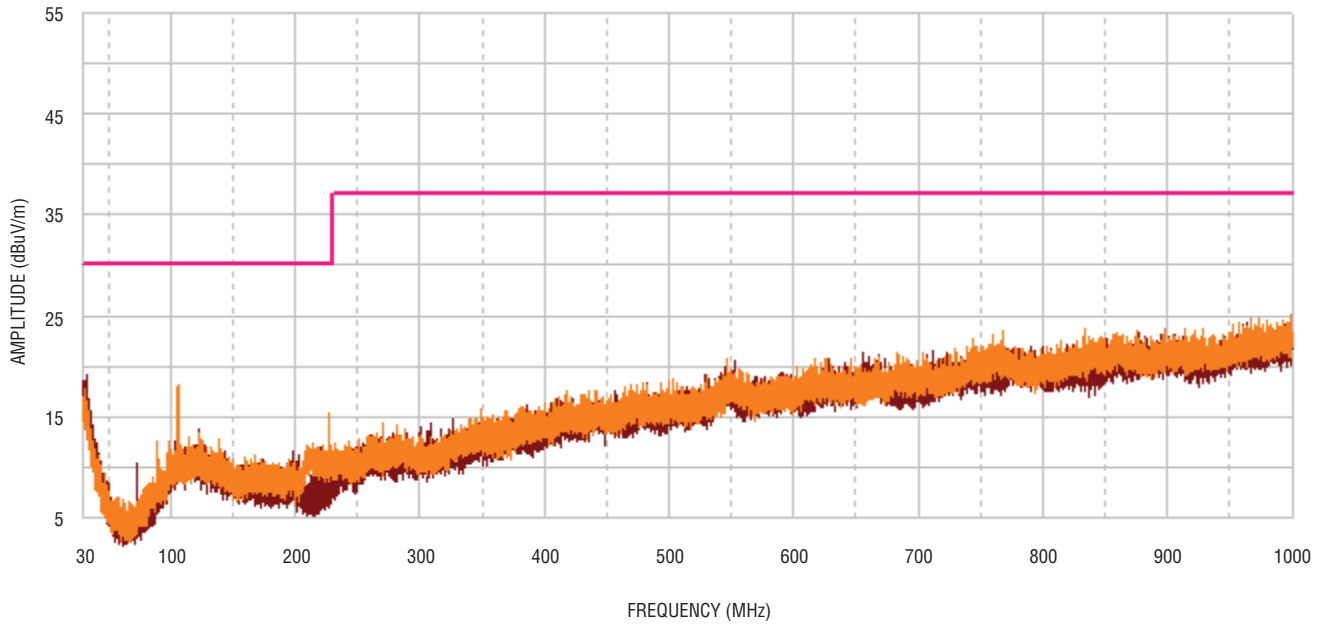
OPERATION

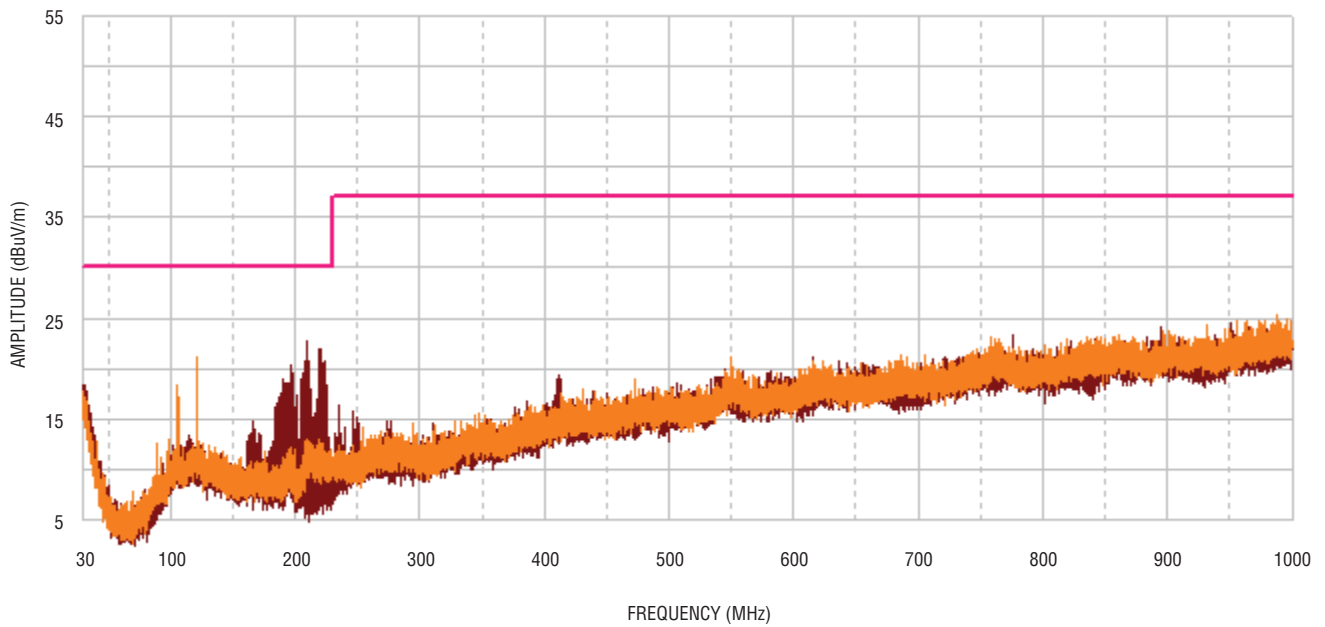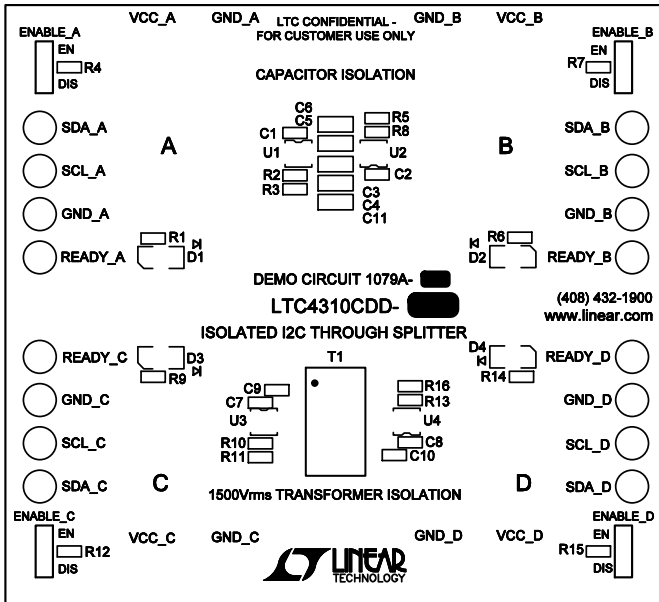**Figure 4. DC1079A, Capacitor Coupling, Radiated Emissions Scan**

Figure 5. DC1079A, Transformer Coupling, Radiated Emissions Scan

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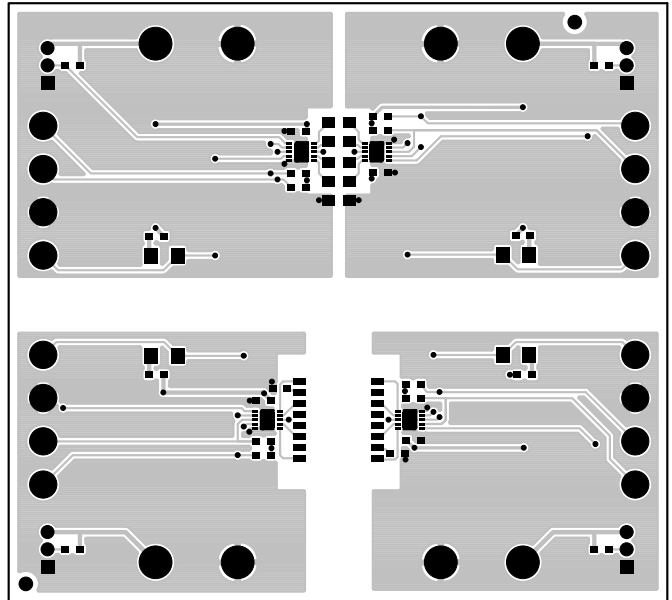
PCB LAYOUT

Top Silkscreen

Layer 1. Component Side
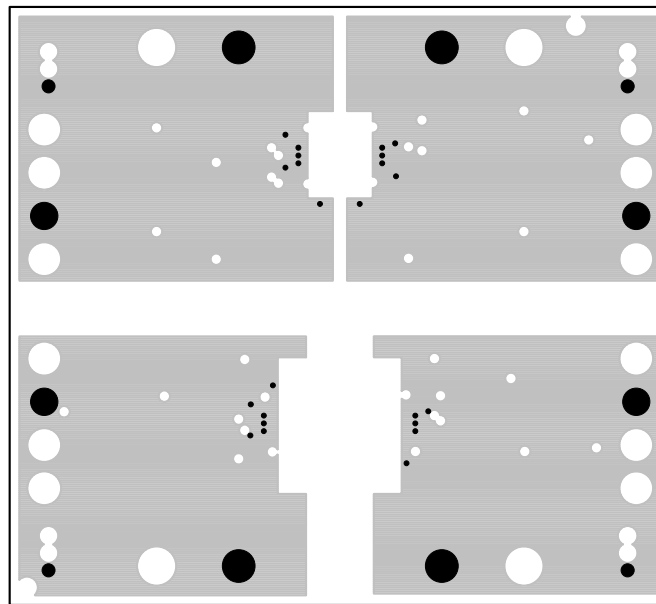
Layer 2. GND Layer

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PCB LAYOUT
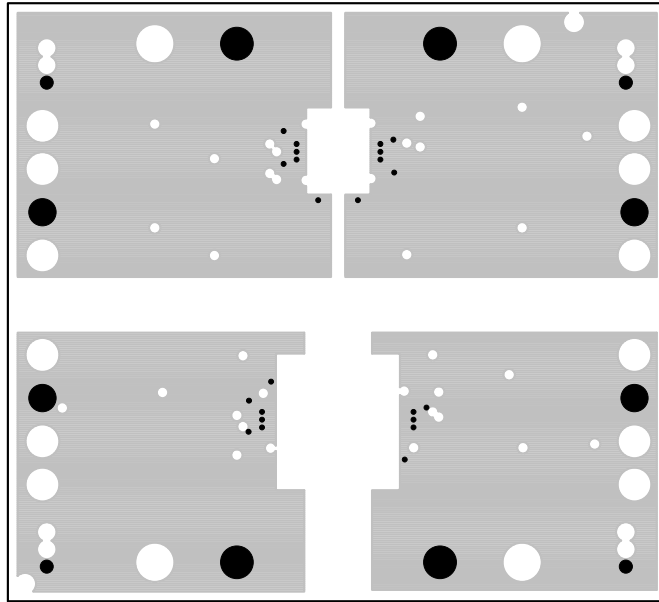
Layer 3. GND Layer
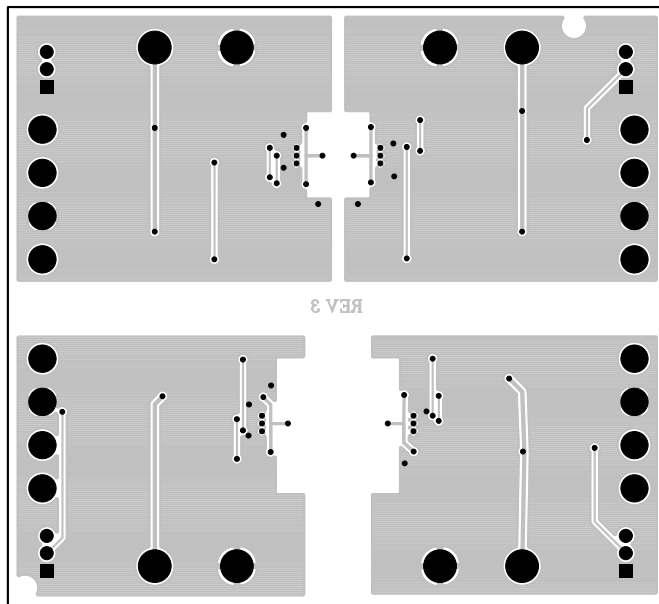
Layer 4. Bottom Layer

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC1079A Rev 3				
1	6	C1, C2, C7, C8, C9, C10	CAP, 0603 0.1µF 10V 10% X7R	AVX 0603ZC104KAT
2	5	C3, C4, C5, C6, C11	CAP, 0805 100pF 5% 100V COG	AVX 08051A101JAT
3	4	D1, D2, D3, D4	LED, GREEN	PANASONIC LN1351C-(TR)
4	8	E1, E2, E7-E10, E16, E17	TURRET	MILL-MAX-2501-2-00-80-00-00-07-0
5	16	E3-E6, E11-E14, E18-E25	TURRET	MILL MAX 2308-2-00-80-00-00-07-0
6	4	JP1, JP2, JP5, JP6	HEADER, 3-PIN, 2mm	SAMTEC TMM-103-02-L-S
7	4	R1, R6, R9, R14	RES, 0603 1kΩ 5% 1/10W	AAC CR16-102JM
8	1	T1	XFMR, GALVANIC GROUND ISOLATION, 1500V	PAC ELEC. EPF8119S
9	4	XJP1, XJP2X, JP5, XJP6	SHUNT, 2mm	SAMTEC 2SN-BK-G
DC1079A-A Rev 3				
1	1		PCB ASSEMBLY	LINEAR TECH DC1079A REV 3
2	12	R2-R5, R7, R8, R10-R13, R16	RES, 0603 10kΩ 5% 1/10W	AAC CR16-103JM
3	4	U1, U2, U3, U4	IC, I^{2}C THROUGH SPLITTER	LINEAR TECH. LTC4310CDD-1
DC1079A-B Rev 3				
1	1		PCB ASSEMBLY	LINEAR TECH DC1079A REV 3
2	8	R2, R3, R5, R8, R10, R11, R13, R16	RES, 0603 3.3kΩ 5% 1/10W	VISHAY CRCW06033K30JNEA
3	4	R4, R7, R12, R15	RES, 0603 10kΩ 5% 1/10W	AAC CR16-103JM
4	4	U1, U2, U3, U4	IC, I^{2}C THROUGH SPLITTER	LINEAR TECH. LTC4310CDD-2

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SCHEMATIC DIAGRAM

ISOLATED I2C THROUGH SPLITTER

DEMO CIRCUIT 1079A
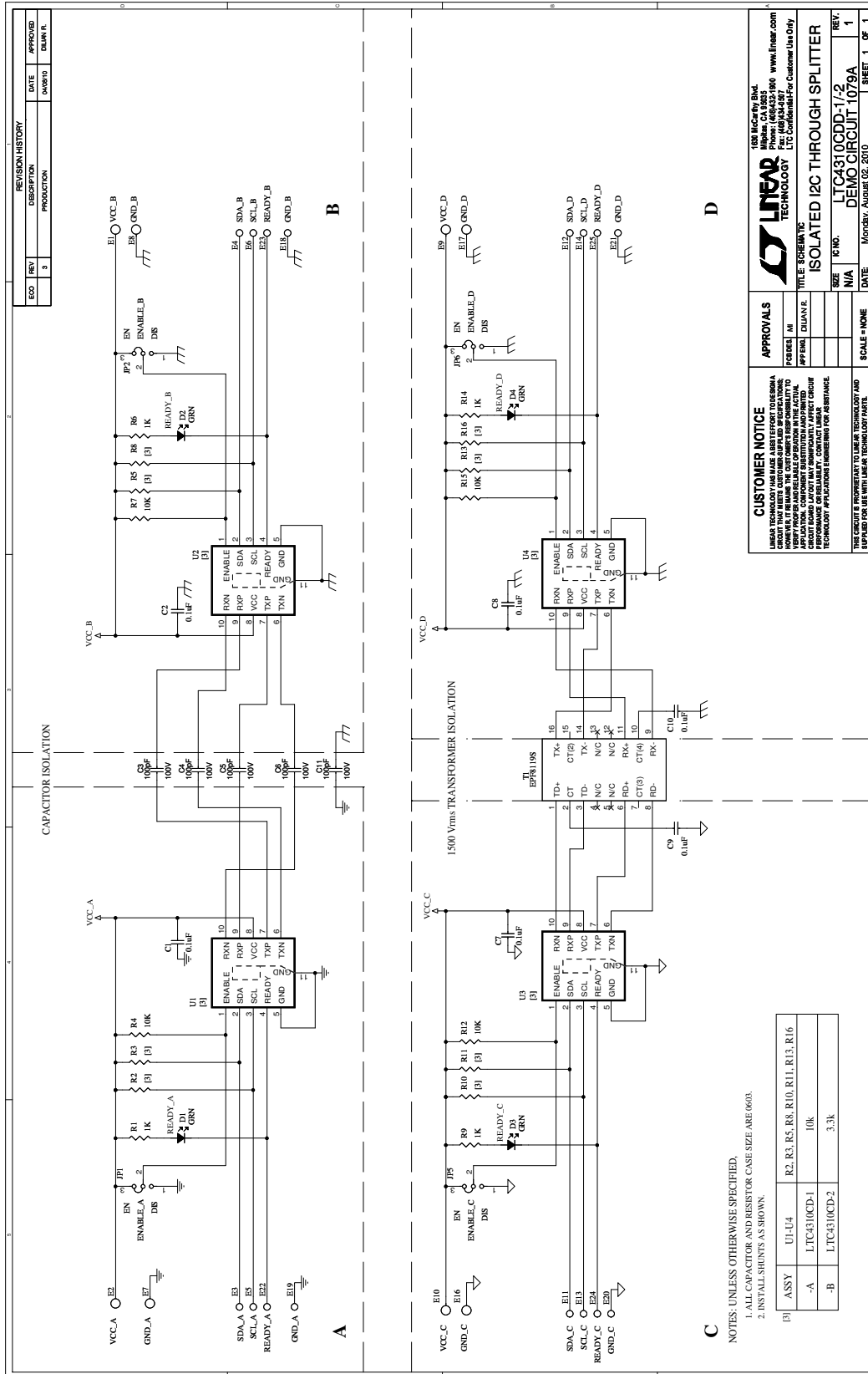
DEMONSTRATION BOARD IMPORTANT NOTICE

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