

LTM4603 Synchronizable 20V, 6A Step-Down μ Module Regulator

DESCRIPTION

Demonstration circuit DC1083A-A features the LTM[®]4603, the high efficiency, high density step-down μ Module[®] regulator. The input voltage range is from 4.5V to 20V. The output voltage is jumper programmable from 0.6V to 5V. The rated load current is 6A, while derating is necessary for certain V_{IN} , V_{OUT} , and thermal conditions. Applying an external clock signal to the PLLIN pin forces the μ Module regulator to operate at the same frequency. The output

ramp-up and ramp-down may be programmed through the TRACK/SS pin. Margining function is provided for the user who wants to stress their system by varying supply voltages during testing. The LTM4603 data sheet must be read in conjunction with this demo manual prior to working on or modifying demo circuit DC1083A-A.

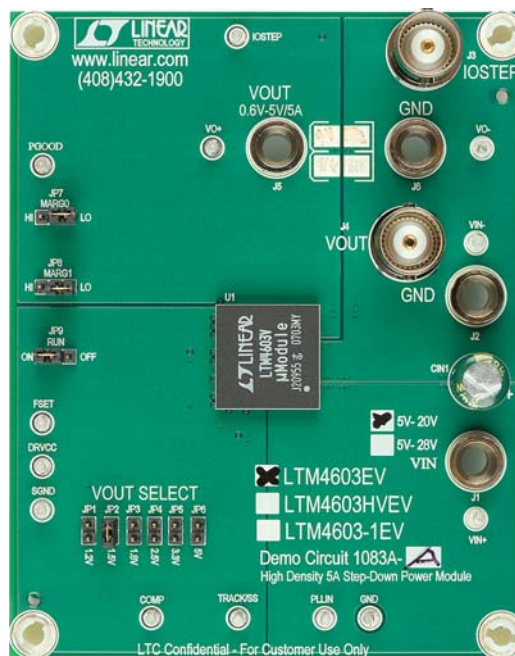
Design files for this circuit board are available at <http://www.linear.com/demo>

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PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Input Voltage Range		4.5V to 20V
Output Voltage V _{OUT}	Jumper Selectable (Open for 0.6V)	1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V; $\pm 2\%$
Maximum Continuous Output Current	Derating is Necessary for Certain V _{IN} , V _{OUT} , and Thermal Conditions	6A _{DC}
Default Operating Frequency		1MHz
External Clock Frequency Range	Refer to Data Sheet for Minimum t _{ON} and t _{OFF} Requirement	700kHz to 1.3MHz

BOARD PHOTO



dc1083aaf

DEMO MANUAL DC1083A-A

QUICK START PROCEDURE

Demonstration circuit DC1083A-A is an easy way to evaluate the performance of the LTM4603EV. Please refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Place jumpers in the following positions for a typical $1.5V_{OUT}$ application:

MARG0	MARG1	RUN	VOUT SELECT
LO	LO	ON	1.5V

2. With power off, preset the load to 0A and V_{IN} supply to be less than 20V. Connect the input power supply, load and meters as shown in Figure 1.
3. Turn on the power at the input. The output voltage should be $1.5V \pm 2\%$.
4. Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters.

5. To measure input and output ripple, please refer to Figure 2 for proper setup.
6. For optional load transient test, apply adjustable pulse signal between IOSTEP CLK and GND pins. Pulse amplitude sets the current step. The pulse signal should have very small duty cycle (<15%) to limit the thermal stress on the transient load circuit. The output transient current can be monitored at BNC connector J3 (10mV/A), the output voltage can be monitored at BNC connector J4.
7. For margining function test, place jumper MARG0 and MARG1 in the configurations shown in the following table, measure the output voltage at J4.

MARG1	MARG0	ΔV_{OUT}
LO	LO	0
LO	HI	+5%
HI	LO	-5%
HI	HI	0

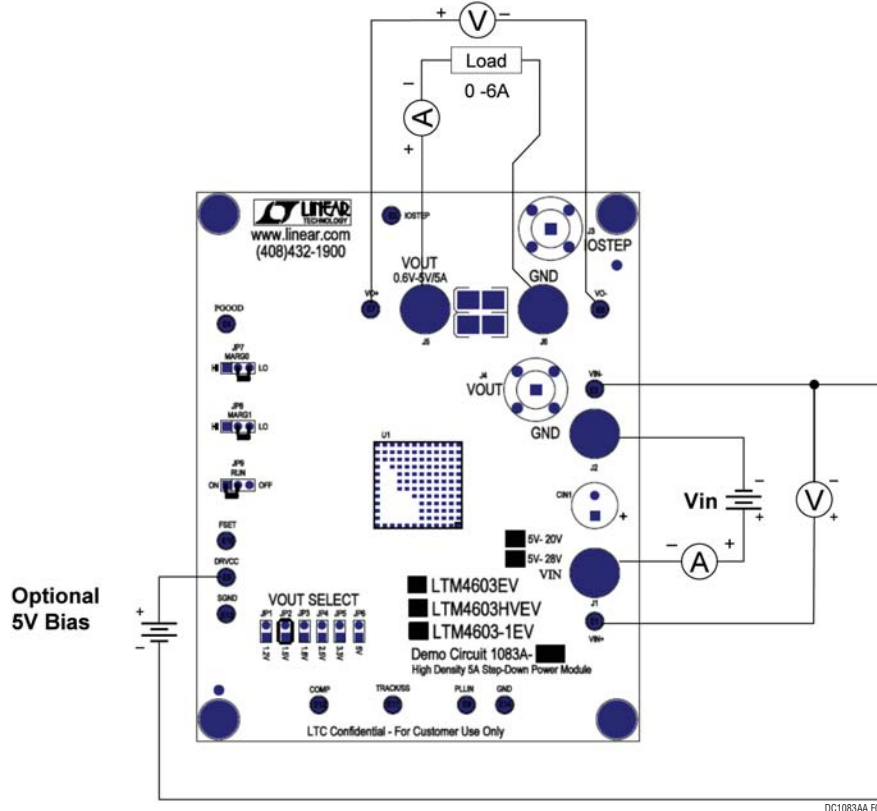


Figure 1. Test Setup of DC1083A-A (DRV_{CC} Bias Supply is Optional)

QUICK START PROCEDURE

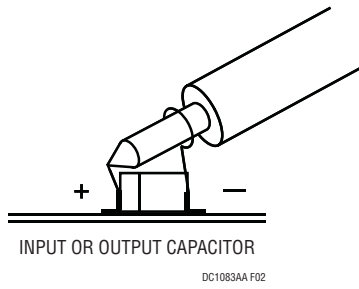


Figure 2. Scope Probe Placements for Measuring Input or Output Ripple

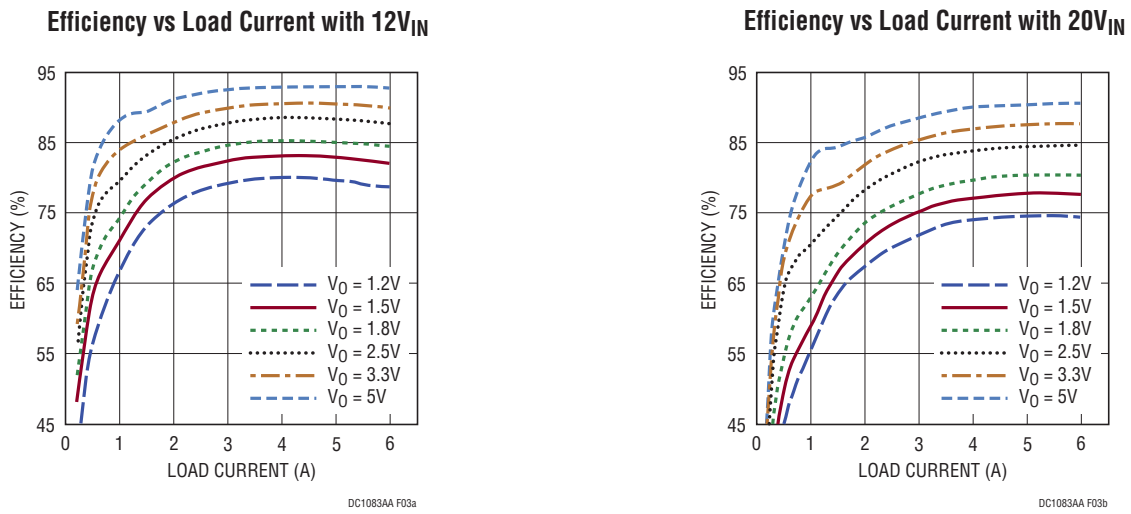
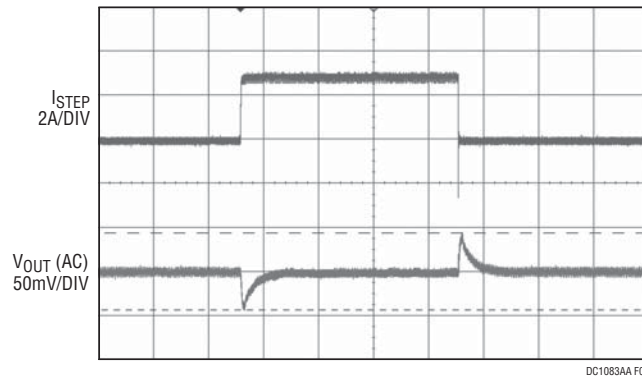


Figure 3. Measured Supply Efficiency with Different V_{IN} and V_{OUT}



$V_{IN} = 12V, V_{OUT} = 1.5V$
 1.5A TO 4.5A LOAD STEP
 $C_{OUT} = 1 \times 10\mu F$ CERAMIC, $1 \times 100\mu F$ CERAMIC

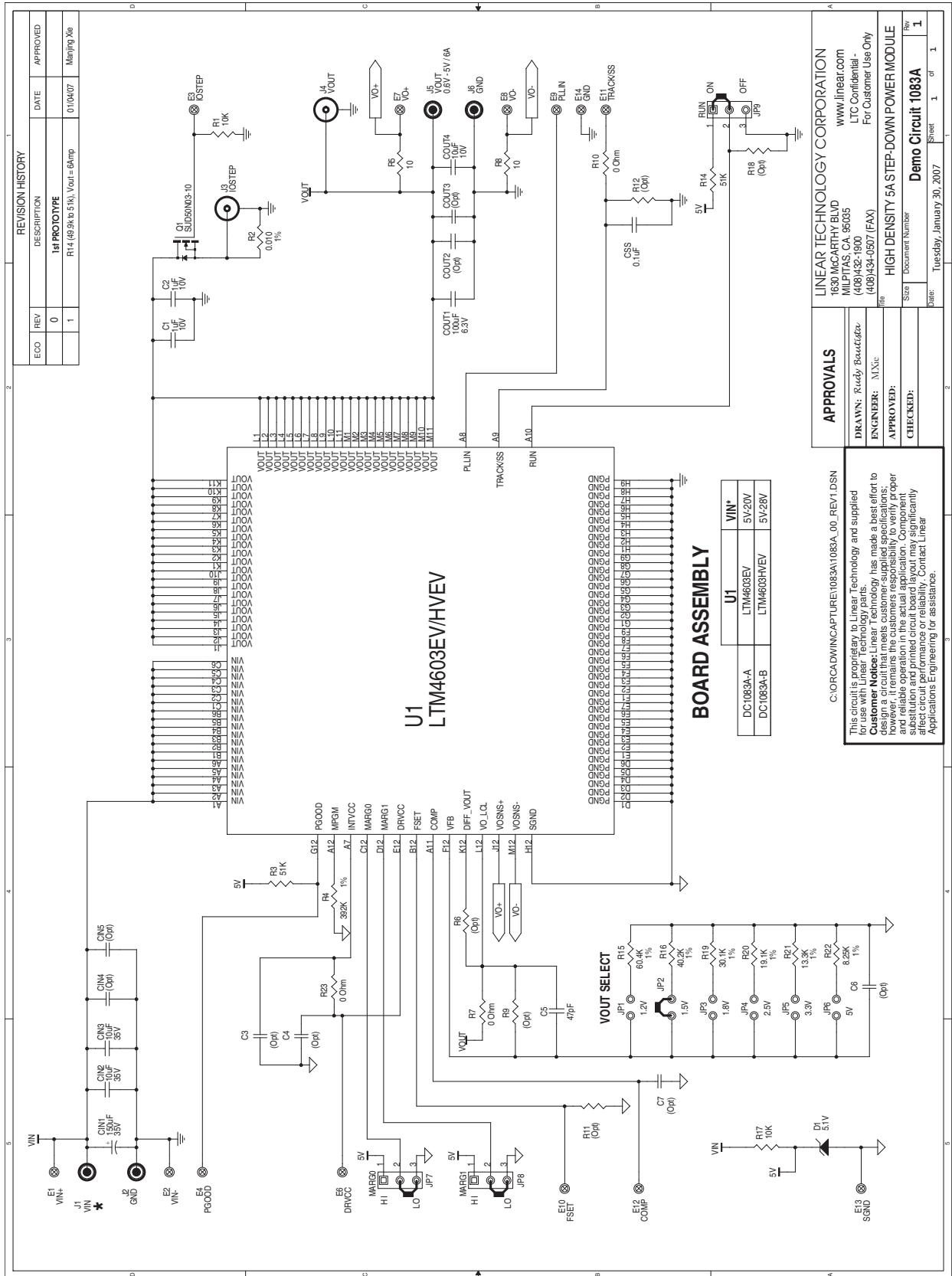
Figure 4. Measured Load Transient Response (3A Step)

DEMO MANUAL DC1083A-A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	CIN2, CIN3	CAP, X7R 10 μ F 35V 20%	TAIYO YUDEN GMK316BJ106ML-T
1	1	COUT1	CAP, X5R 100 μ F 6.3V 20%	TAIYO YUDEN JMK432BJ107MU-T
1	1	COUT4	CAP, X5R 10 μ F 10V 10%	TAIYO YUDEN LMK316BJ106KL-T
1	1	C5	CAP, NPO 47pF 50V 10%	AVX 06035A470KAT1A
1	1	R14	RES, CHIP 51k 0.1W 5%	AAC CR16-513JM
1	1	R4	RES, CHIP 392k 0.1W 1%	AAC CR16-3923FM
1	2	R7, R23	RES, CHIP 0 Ω 1/16W 1A	AAC CJ06-000M
1	1	R16	RES, CHIP 40.2k 0.1W 1%	AAC CR16-4022FM
1	1	U1	μ MODULE REGULATOR	LINEAR TECHNOLOGY CORPORATION LTM4603EV
Additional Demo Board Circuit Components				
1	1	CIN1	CAP, ALUM 150 μ F 35V 10%	SANYO 35ME150WXV+TS (NOW SUNCON 35ME150WXV)
2	0	CIN4, CIN5	CAP, 1206 OPTIONAL	OPTIONAL
3	0	COUT2	CAP, 1812 OPTIONAL	OPTIONAL
4	0	COUT3	CAP, 1210 OPTIONAL	OPTIONAL
5	1	CSS	CAP, X7R 0.1 μ F 16V 20%	AVX 0603YC104MAT2A
6	2	C1, C2	CAP, X5R 1 μ F 10V 10%	TAIYO YUDEN LMK107BJ105KA
7	0	C3, C4, C6, C7	CAP, 0603 OPTIONAL	OPTIONAL
8	1	D1	ZENER DIODE, 5.1V	ON SEMICONDUCTOR MMBZ5231B
9	1	Q1	MOSFET, N-CHANNEL 30V	SILICONIX SUD50N03-10
10	2	R17, R1	RES, CHIP 10k 0.1W 5%	AAC CR16-103JM
11	1	R2	RES, LRC 0.010 0.25W 1%	IRC LRF1206-01-R010-F
12	1	R3	RES, CHIP 51k 0.1W 5%	AAC CR16-513JM
13	2	R8, R5	RES, CHIP 10 0.1W 5%	AAC CR16-100JM
14	0	R6, R9, R11, R12, R18	RES, 0603 OPTIONAL	OPTIONAL
15	1	R10	RES, CHIP 0 Ω 1/16W 1A	AAC CJ06-000M
16	1	R15	RES, CHIP 60.4k 0.1W 1%	AAC CR16-6042FM
17	1	R19	RES, CHIP 30.1k 0.06W 1%	AAC CR16-3012FM
18	1	R20	RES, CHIP 19.1k 0.1W 1%	AAC CR16-1912FM
19	1	R21	RES, CHIP 13.3k 0.1W 1%	AAC CR16-1332FM
20	1	R22	RES, CHIP 8.25k 0.1W 1%	AAC CR16-8251FM
Hardware - for Demo Board Only				
1	13	E1 TO E4, E6 TO E14	TURRET, TESTPOINT	MILL MAX 2308-2
2	6	JP1 TO JP6	JUMPER, 2 PINS 2mm CTRS	SAMTEC TMM-102-02-L-S
3	3	JP7, JP8, JP9	HEADERS, 3 PINS 2mm CTRS	SAMTEC TMM-103-02-L-S
4	4	J1, J2, J5, J6	CONNECTOR, BANANA JACK	KEYSTONE 575-4
5	2	J3, J4	BNC CONNECTOR	CONNEX 112404
6	4	XJP2, XJP7, XJP8, XJP9	SHUNT, 2mm CTRS	SAMTEC 2SN-BK-G
7	4		STAND-OFF, NYLON, 0.50" TALL	KEYSTONE, 8833 (SNAP ON)

SCHEMATIC DIAGRAM



REVISION HISTORY				
ECCO	REV	DESCRIPTION	DATE	APPROVED
	0	1st PROTOTYPE		
	1	R14 (49.9k to 51k), Vout = 64mp	01/04/07	Manning Xie

APPROVALS	
DRAWN:	Rudy Baulezza
ENGINEER:	M.Xie
APPROVED:	
CHECKED:	

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Date:	Tuesday, January 30, 2007
Sheet:	1 of 1

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DEMO MANUAL DC1083A-A

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