DESCRIPTION

Demonstration circuit 1250 is an evaluation board featuring Linear Technology Corporation's LTM9001 16-bit Receiver Subsystem. DC1250 demonstrates good circuit layout techniques and recommended external circuitry for optimal system performance.

DC1250 comes installed with one of Linear Technology's 16-bit LTM9001 amplifier/ADC subsystems. The board includes a wideband input transformer (for evaluation with a single-ended RF signal generator) and output CMOS buffers. **The LTM9001 is also capable of generating LVDS outputs – for evaluation of the part with LVDS outputs, obtain DC1241.** DC1250 plugs into the DC890 Data Acquisition demo board and the output can be easily analyzed with Linear Technology's PScope data processing software, which is available for no charge on our website at http://www.linear.com.

Design files for this circuit board are available. Call the LTC factory.

QUICK START PROCEDURE

Validating the performance of the LTM9001 is simple with DC1250, and requires only an input source, a clock source, a computer, and a lab power supply. Refer to Figure 1 for proper board evaluation equipment setup and follow the procedure below:

1. Connect the power supply as shown in Figure 1. There are on-board low-noise voltage regulators that provide the three supply voltages for the LTM9001. The entire board and all components share a common ground. The power supply should still be a low-noise lab power supply capable of supplying at least 1 Amp.

2. Provide an encode clock to the ADC via SMA connector J3. Use a low-phase-noise clock source such as a filtered RF signal generator or a high-quality clock oscillator. **Obtain DC1216 for a low-phase-noise ADC clock source that can plug directly into DC1250.**

NOTE. Similar to having a noisy input, a high-jitter (phase noise) encode clock will degrade the signal-to-noise ratio (SNR) of the system.

Table 1: DC1250 Connectors and Jumpers

REFERENCE	FUNCTION
J1 (AIN+)	Board Signal Input. Impedance-matched to 50Ω for use with lab signal generators.
J2 (AIN-)	Differential Board Input. **Normally not connected.** See text for differential-input evaluation methods.
J3 (ENC)	Board Clock Input. Impedance-matched to 50Ω. Drive with a low-phase-noise clock oscillator or filtered sine wave signal source.
E1 (EXT REF)	Reference input to adjust the full-scale range of the LTM9001. Connects to the SENSE pin; by default, tied to VDD for internal reference.
JP5 (AMP_EN)	Enables the LTM9001 amplifier. Default is EN.
JP1 (PGA_GAIN)	Selects the input range of LTM9001. Default is LOW (low PGA gain, larger input range)
JP2 (RAND)	Output Randomizer. NORM is default.
JP3 (ADC_SHDN)	Enables the LTM9001 ADC. Default is NORM.
JP4 (DITH)	ADC Internal Dither. Default is OFF.

3. Apply an input signal to the board. DC1250 allows great flexibility in applying input signals (see the section on Applying Input Signals). For best results, use a low distortion, low noise signal generator with sufficient filtering to avoid degrading the performance of the amplifier and ADC.

4. Observe the ADC output with demo circuit DC890, a USB cable, a Windows computer, and Linear Technology's Pscope data processing software.

NOTE. Even a high-quality signal synthesizer will still have noise and harmonics that should be attenuated with a low-pass or band-pass filter. For good-quality high order filters, see TTE, Lark Engineering, or equivalent.

Power Supply
(3.8V-6V @ 1.0A)

Signal Generator HP 8644B or equiv.

BPF

RF Signal Generator (HP 8644B) or other low phase noise clock source (e.g. DC1216)
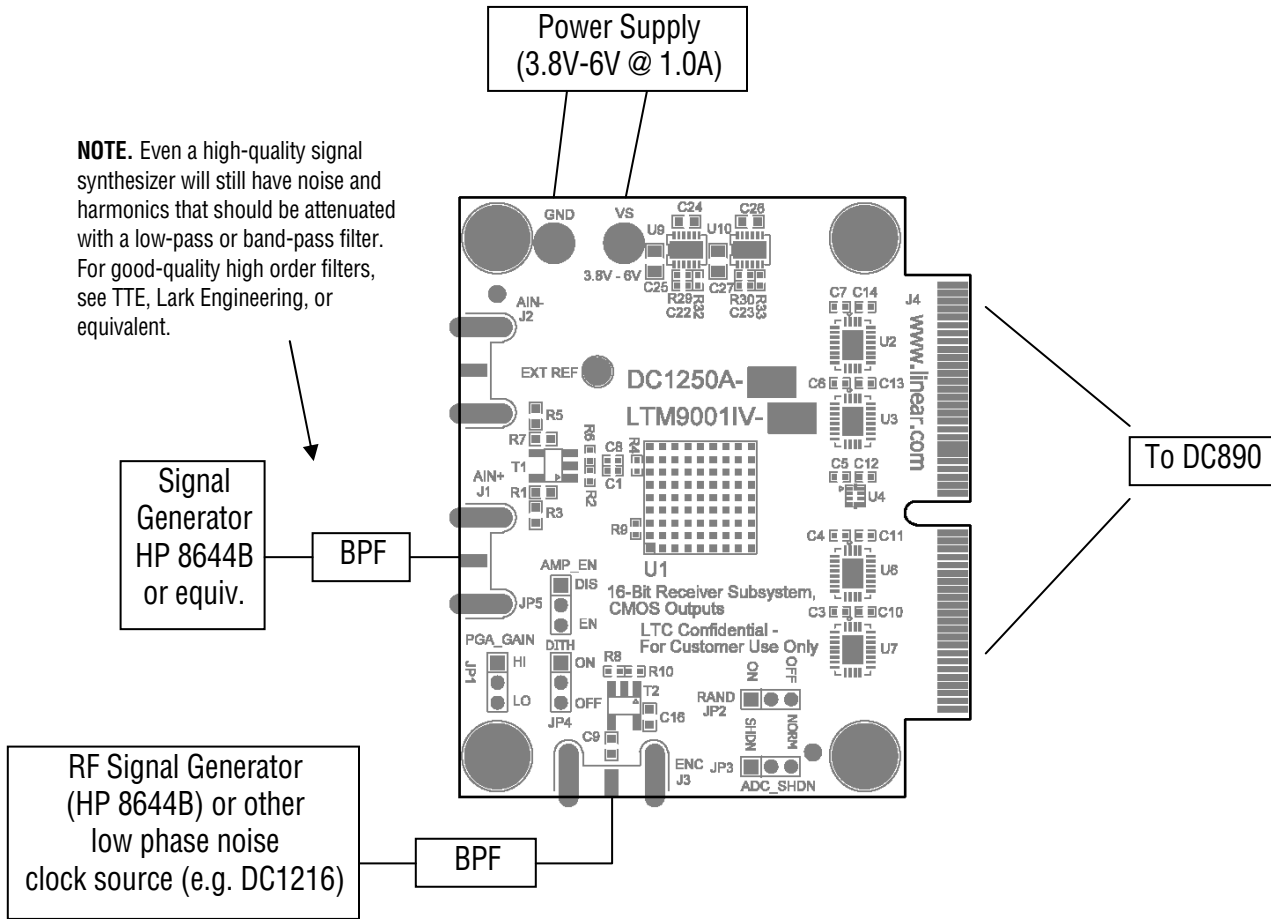
BPF

To DC890

Figure 1. Proper Evaluation Equipment Setup

ADDITIONAL INFORMATION

Although the DC1250 demo board is ready to use on de-livery, it has additional flexibility built in for various types of input networks. Below is some information about con-figuring DC1250 to meet the specific needs of your eval-uation.

APPLYING INPUT SIGNALS

The input network consists of various components de-signed to allow either single-ended or differential inputs, AC-coupled or DC-coupled. Table 2 shows some possi-ble input configurations, and which components to in-stall. LTM9001 is designed for excellent performance with both single-ended and differential input drive, with little difference in distortion performance. When using DC-coupled inputs, the inputs to DC1250 need to be lev-el-shifted to within the input common-mode limits in the datasheet.

Table 2: DC1250 Input Configuration Guide

CONFIGURATION	COMPONENTS NECESSARY
Single-Ended Input AC-Coupled (Default Setup)	No change. Transformer T1 acts as a balun for differential drive.
Single-Ended Input No Transformer AC-Coupled	Remove T1, replace with 0Ω jumpers. May need to install impedance-matching resistor at R4 or R1/R7.
Single-Ended Input No Transformer DC-Coupled	Same as above. Change C1 and C8 to 0Ω jum-pers. Inputs must be within the common-mode voltage limits of LTM9001.
Differential Inputs	Remove R7 and install R5. T1 and C1/C8 can be replaced with 0Ω for DC coupling.

NOTE. When driving the ADC driver with a direct DC-coupled path, increased input bias currents may occur due to the amplifier's input impedance. See the LTM9001 datasheet for more details.

LTM9001 16-BIT RECEIVER SUBSYSTEM

OUTPUT DATA FORMAT

The default output format for DC1250 is demultiplexed CMOS output mode, which alternates the digital outputs coming out of the LTM9001 "A" and "B" channels. The first output word is shifted out of the "A" channel, the second word out of the "B" channel, and so on. Thus each channel is updating at half the data rate. **By default, DC890 and PSCOPE read the board in demultiplexed CMOS mode.**

Removing resistor R19 on the DC1250 would ground the LVDS pin, and the digital outputs would all come out of channel "A" at the full data rate. However, PSCOPE is not currently set up to read the data this way. When using the outputs in full-data-rate mode, you must manually configure PSCOPE (see Figure 2) to 2-channel mode, and ignore the "B" channel display in PSCOPE.

OTHER BOARD CIRCUITRY

Device U5 is an EEPROM that is used by the PScope software to identify the board and apply the correct settings for the data collection.

USING PSCOPE SOFTWARE

PScope, downloadable from Linear Technology's website http://www.linear.com/, processes data from the DC890 FastDAACS board and displays FFT and signal analysis information on the computer screen. The on-board EEPROM U5 should enable automatic board detection and auto-configuration of the software, but if the user wishes to change the settings, they can easily do so.

From the Configure menu in the toolbar, uncheck "Auto-detect Device". The default settings are shown in Figure 2. The LTM9001 also has an output randomizer, which the user needs to select if it is enabled on the board (under a different menu option). The software will automatically un-randomize the output by performing an exclusive-OR with each bit and the LSB.
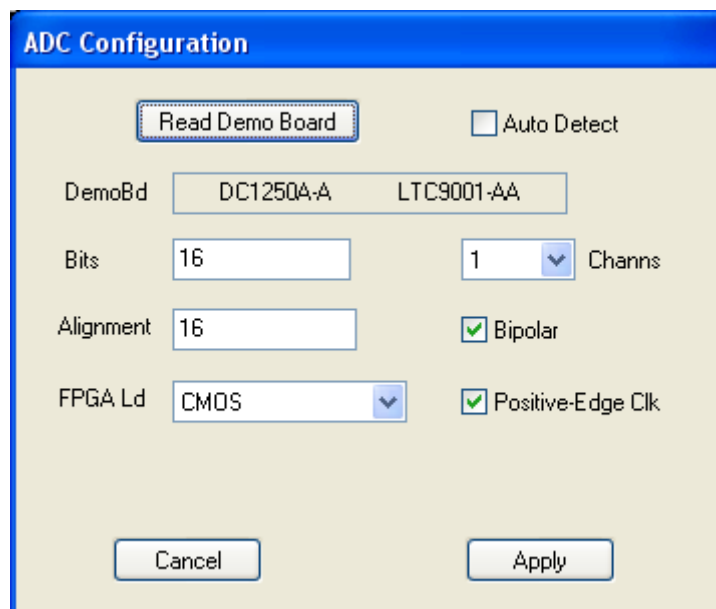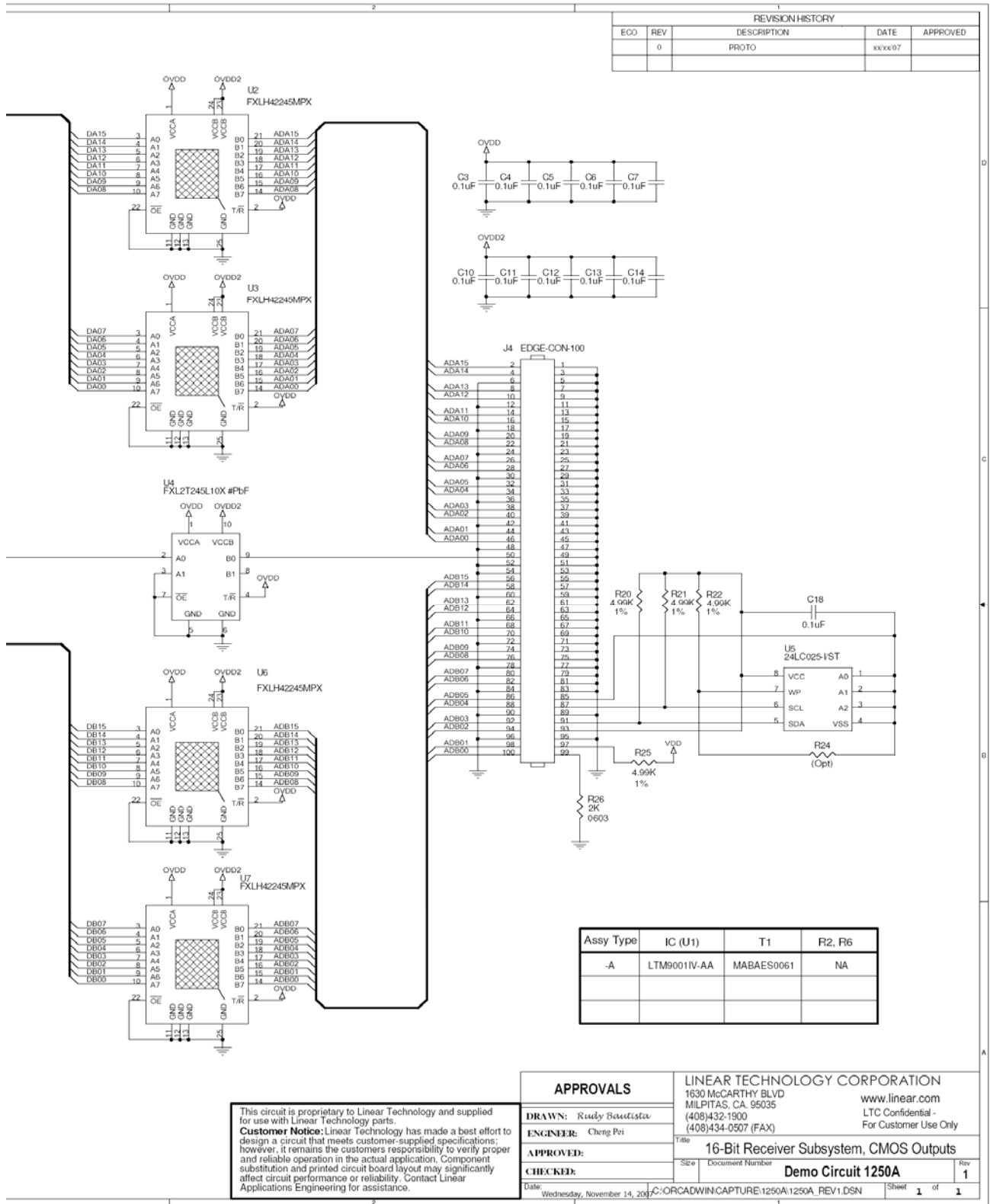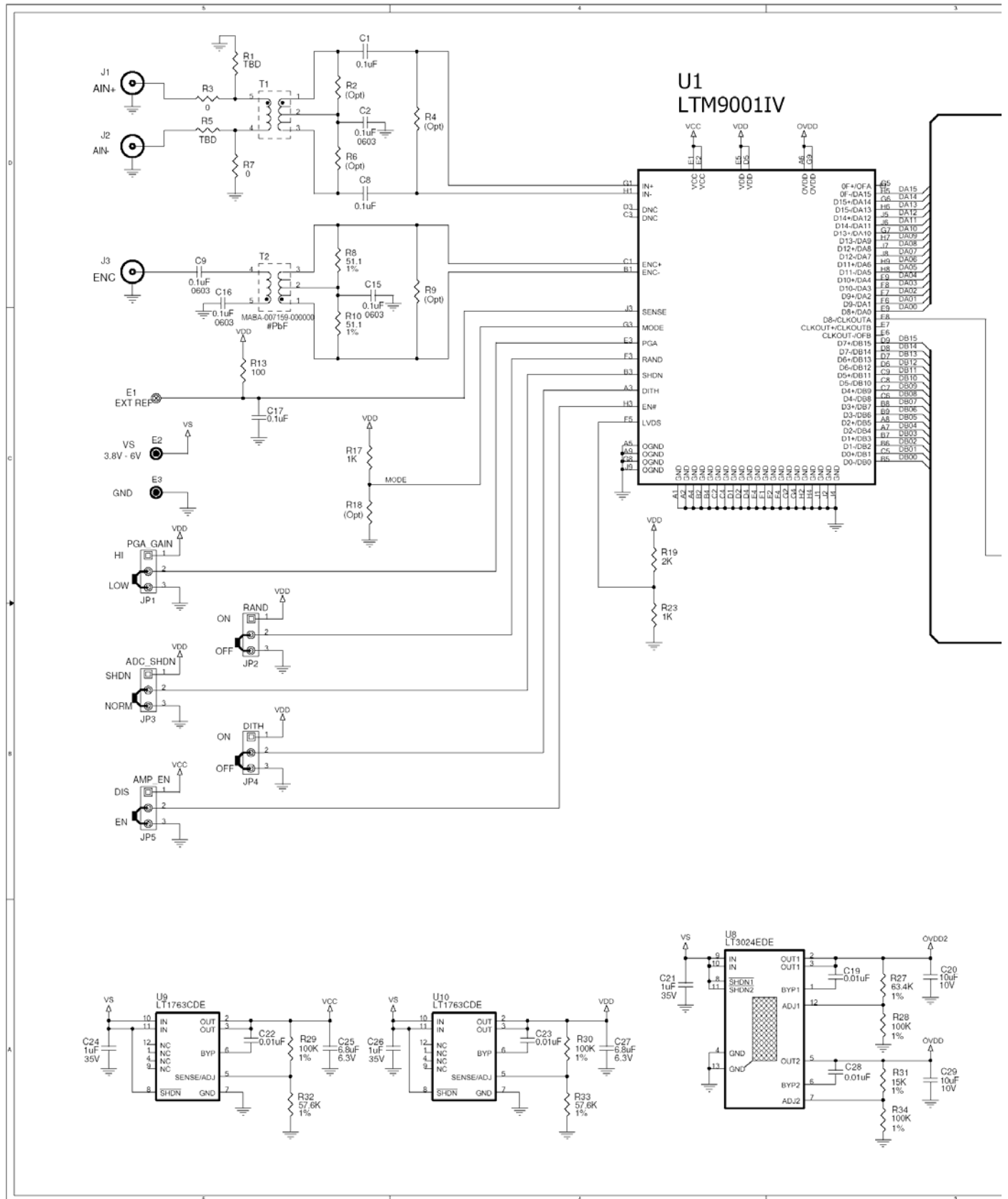

Figure 2. Entering the correct device information for your ADC. Select the correct parameters for the DC1250. Under normal conditions, PSCOPE should automatically recognize the board and adjust the software settings accordingly.

DC1250 Schematic (Separated into 2 pages)

LTM9001 16-BIT RECEIVER SUBSYSTEM

J1 AIN+
J2 AIN-
J3 ENC
E1 EXT REF
VS E2 3.8V - 6V
GND E3

R1 TBD
R3 0
R5 TBD
R7 0
T1
C1 0.1uF
R2 (Opt)
C2 0.1uF 0603
R6 (Opt)
C8 0.1uF
R4 (Opt)

C9 0.1uF 0603
T2
C16 0.1uF 0603
MABA-007159-000000 #PbF
R8 51.1 1%
R10 51.1 1%
C15 0.1uF 0603
R9 (Opt)

R13 100
C17 0.1uF

U1
LTM9001IV
VCC VDD OVDD
IN+
IN-
DNC
DNC
ENC+
ENC-
SENSE
MODE
PGA
RAND
SHDN
DITH
EN#
LVDS
OGND OGND OGND OGND
GND

0F+/OFA
0F-/DA15
D15+/DA14
D15-/DA13
D14+/DA12
D14-/DA11
D13+/DA10
D13-/DA9
D12+/DA8
D12-/DA7
D11+/DA6
D11-/DA5
D10+/DA4
D10-/DA3
D9+/DA2
D9-/DA1
D8+/DA0
D8-/CLKOUTA
CLKOUT+/CLKOUTB
CLKOUT-/OFB
D7+/DB15
D7-/DB14
D6+/DB13
D6-/DB12
D5+/DB11
D5-/DB10
D4+/DB9
D4-/DB8
D3+/DB7
D3-/DB6
D2+/DB5
D2-/DB4
D1+/DB3
D1-/DB2
D0+/DB1
D0-/DB0

DA15 DA14 DA13 DA12 DA11 DA10 DA09 DA08 DA07 DA06 DA05 DA04 DA03 DA02 DA01 DA00
DB15 DB14 DB13 DB12 DB11 DB10 DB09 DB08 DB07 DB06 DB05 DB04 DB03 DB02 DB01 DB00

R17 1K
MODE
R18 (Opt)
R19 2K
R23 1K

PGA_GAIN
HI
LOW
JP1

RAND
ON
OFF
JP2

ADC_SHDN
SHDN
NORM
JP3

DITH
ON
OFF
JP4

AMP_EN
DIS
EN
JP5

U9 LT1763CDE
IN IN OUT OUT NC NC NC NC BYP SENSE/ADJ SHDN GND
C24 1uF 35V
C22 0.01uF
R29 100K 1%
C25 6.8uF 6.3V
R32 57.6K 1%

U10 LT1763CDE
IN IN OUT OUT NC NC NC NC BYP SENSE/ADJ SHDN GND
C26 1uF 35V
C23 0.01uF
R30 100K 1%
C27 6.8uF 6.3V
R33 57.6K 1%

U8 LT3024EDE
IN IN SHDN1 SHDN2 OUT1 OUT1 BYP1 ADJ1 GND GND OUT2 BYP2 ADJ2
C21 1uF 35V
C19 0.01uF
R27 63.4K 1%
C20 10uF 10V
R28 100K 1%
C28 0.01uF
R31 15K 1%
C29 10uF 10V
R34 100K 1%
OVDD2
OVDD

VS VCC VDD

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