LTC4221 Dual Hot Swap Controller/Power Sequencer w/ Dual Speed, Dual Level Fault Protection

## DESCRIPTION

Demonstration circuit DC1355 is a dual hot swap circuit featuring the LTC4221 Dual Hot Swap Controller / Power Sequencer with Dual Speed, Dual Level Fault Protection

DC1355 facilitates evaluation of the LTC4221 performance characteristics including supply ramp-up transients, steady state operation, and overcurrent fault conditions. On board LEDs indicate input supply presence, output state, and power good conditions.

The first LTC4221 channel controls a rail from 2.7 V to 13.5 V and the second one from 1 V to 13.5 V with condition that $\mathrm{V}_{\mathrm{CC} 2} \leq \mathrm{V}_{\mathrm{CC} 1}$.

DC 1355 is assembled to operate with a +12 V rail with 6 A maximum current and a +3.3 V rail with 3.0A maximum current.

## Design files for this circuit board are available. Call the LTC factory.

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## PERFORMANCE SUMMARY Specifications are at $\mathrm{TA}=\mathbf{2 5}^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC} 1}$ | Supply Voltage Channel 1 |  | 2.7 |  | 13.5 | V |
| $\mathrm{V}_{\mathrm{CC} 2}$ | Supply Voltage Channel 2 | $\mathrm{V}_{\mathrm{CC} 2} \leq \mathrm{V}_{\mathrm{CC} 1}$ | 1.0 |  | 13.5 | V |
| $\mathrm{V}_{\mathrm{CC1}}$ (UVL) | Undervoltage Lockout for Channel 1 | $\mathrm{V}_{\mathrm{CC} 1}$ Rising | 2.1 | 2.5 | 2.675 | V |
| $\mathrm{V}_{\text {CC2(UVL) }}$ | Undervoltage Lockout for Channel 2 | $\mathrm{V}_{\mathrm{CC} 2}$ Rising | 0.65 | 0.8 | 0.975 | V |
| $\mathrm{V}_{\text {SENSE(FC) }}$ | SENSEn Threshold Voltage | Channeln Fast Comparator Threshold | 85 | 100 | 115 | mV |
| $\mathrm{V}_{\text {SENSE(SC) }}$ | SENSEn Threshold Voltage | Channeln Slow Comparator Threshold | 20.5 | 25 | 29.5 | mV |
| $\mathrm{V}_{\text {SENSE }}(\mathrm{ACL})$ | SENSEn Voltage at Active Current Limit | $\begin{aligned} & \mathrm{V}_{\mathrm{FBn}}=0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{FBn}}=0.65 \mathrm{~V} \\ & \hline \end{aligned}$ | $\begin{gathered} 4 \\ 20.5 \end{gathered}$ | $\begin{gathered} 9 \\ 25 \end{gathered}$ | $\begin{aligned} & 16 \\ & 29.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| IGATE(UP) | GATEn Output Current | $\mathrm{V}_{\mathrm{ON} 1}=\mathrm{V}_{\mathrm{ON} 1}=2 \mathrm{~V}, \quad \mathrm{~V}_{\mathrm{GATE}}=0 \mathrm{~V}$ | -7 | -9.5 | -120 | uA |
| I GATE(DN) | GATEn Output Current | $\mathrm{V}_{\mathrm{ON} 1}=\mathrm{V}_{\mathrm{ON} 1}=0.6 \mathrm{~V}, \mathrm{~V}_{\mathrm{GATE}}=3.3 \mathrm{~V}$ | 75 | 100 | 125 | uA |
| $\mathrm{I}_{\text {GATE(FSTDN }}$ | GATEn Output Current | UNLO with $\mathrm{V}_{\text {GATEn }}=3.3 \mathrm{~V}$ or FAULT latched with $V_{\text {GATEn }}=3.3 \mathrm{~V}$ |  | 16 |  | mA |
| $\Delta \mathrm{V}_{\text {GATE }}$ | External N-Channel Gate Drive | $\mathrm{V}_{\mathrm{GATEn}}-\mathrm{V}_{\mathrm{CC} 1}$ for $\mathrm{V}_{\mathrm{CC} 1}=2.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC} 2}=1 \mathrm{~V}$ <br> $\mathrm{V}_{\mathrm{GATEn}}-\mathrm{V}_{\mathrm{CC} 1}$ for $\mathrm{V}_{\mathrm{CC} 1}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC} 2}=2.5 \mathrm{~V}$ | $\begin{aligned} & \hline 4.5 \\ & 5 \end{aligned}$ |  | $\begin{aligned} & 13 \\ & 16 \end{aligned}$ | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |

PERFORMANCE SUMMARY Specifications are at $\operatorname{TA}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{V}_{\mathrm{GATEn}}-\mathrm{V}_{\mathrm{CC} 1}$ for $\mathrm{V}_{\mathrm{CC} 1}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC} 2}=3.3 \mathrm{~V}$ $\mathrm{V}_{\mathrm{GATE}} \mathrm{V}_{\mathrm{CC} 1}$ for $\mathrm{V}_{\mathrm{CC} 1}=12 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ |  |  |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\overline{\mathrm{V}} \mathrm{ON(OFF)}$ | ONn Off Threshold | High to Low , GATEn Turns Off by 100uA PullDown | 0.796 | 0.821 | 0.846 | V |
| $\triangle \mathrm{V}_{\mathrm{ON} \text { (OFFHYST) }}$ | ON $n$ Off Threshold Hysteresis |  |  | 30 |  | mV |
| $\mathrm{V}_{\text {ON(RESET }}$ | ON1 Reset Threshold | $\mathrm{V}_{\text {ON1 }}$ Falling | 0.375 | 0.4 | 0.425 | V |
| $\Delta$ <br> $\mathrm{V}_{\mathrm{ON}(\text { RESETHYST }}$ | ON1 Reset Threshold Hysteresis |  |  | 25 |  | mV |
| $\mathrm{V}_{\mathrm{FB}(\mathrm{UV})}$ | FBn Undervoltage Threshold | FBn Falling | 0.605 | 0.617 | 0.629 | V |
| $\mathrm{V}_{\mathrm{FB}(\mathrm{OV})}$ | FBn Overvoltage Threshold | FBn Rising | 0.805 | 0.822 | 0.838 | V |
| IFILTER (UP) | FILTER Pull-Up Current | During Current Fault Condition | -80 | -105 | -132 | $\mu \mathrm{A}$ |
| IFILTER (DN) | FILTER Pull-Down Current | During Normal Cycle | 1.15 | 1.8 | 2.45 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {FILTER(TH) }}$ | FILTER Threshold | Latched Off Threshold, FILTER Rising | 1.18 | 1.24 | 1.30 | V |
| $\triangle \mathrm{V}_{\text {FILTER(HYST) }}$ | FILTER Threshold Hysteresis |  |  | 105 |  | mV |
| ITMR(UP1) | TIMER Pull-Up Current 1 | Initial Timing Cycle | -1.2 | 1.9 | -2.6 | $\mu \mathrm{A}$ |
| ITMR(UP2) | TIMER Pull-Up Current 2 | Start-Up cycle | -15 | -20 | -25 | $\mu \mathrm{A}$ |
| ITMR(FSTDN) | TIMER Pull-Down Current | $\mathrm{V}_{\text {TMR }}=1.5 \mathrm{~V}$, End of Initial Timing Cycle |  | 9 |  | mA |
| $\left.\mathrm{V}_{\text {TMR( }} \mathrm{H}\right)$ | TIMER High Threshold | TMER Rising | 1.172 | 1.234 | 1.27 | V |
| $\mathrm{V}_{\text {TMR(L) }}$ | TIMER Low Threshold | TIMER Falling | 0.1 | 0.4 | 0.5 | V |

## OPERATING PRINCIPLES

The LTC4221 controls two rails with external N channel MOSFETs.
Two independent ON $n$ comparators allow ramping rails up and down separately or simultaneously.
Each channel has two current limit comparators that provide dual level and dual speed overcurrent circuit breaker protection after the start-up period. If any current sense voltage exceeds 100 mV for 1us or 25 mV for the timeout delay, then the FAULT latch is set and both GATE pins are pulled low.
The LTC4221 is suited for low voltage applications such as a hot board insertion and removal and has
a rich set of features to support hot swap application including:

- Overvoltage protection
- FAULT latch setting and resetting and fault state indication
- Adjustable Inrush Current Control
- Adjustable duration for Current Limit before switch is turned off
- Power-good signaling


## QUICK START PROCEDURE

Demonstration circuit 1355 is easy to set up to evaluate the performance of the LTC4221. Refer to Figure 1. for proper measurement equipment setup and follow the procedure below:

1. Place jumpers in the initial position:

JP1 (ON2) Off
JP2 (ON1) Off

JP3 (AUTO RETRY) NO
JP4 (FAULT SIGNAL) NO
2. Adjust +12 V supply output voltage between 10.6 V and 13.0 V . Connect +12 V power supply to the +12 V INPUT and GND turrets and turn it on. Green LED +12V INPUT (D2) should light.
3. Adjust +3.3 V supply output voltage between 2.89 V and 3.67 V . Connect +3.3 V power supply to the +3.3V INPUT and GND turrets and turn it on. Green LED +3.3V INPUT (D6) should light.
4. Place jumpers JP1 and JP2 in the ON positions. Two amber LEDs, PWRGD1 and PWRGD2, should light.
5. Connect electronic or resistive loads to the +12 V and +3.3 V output turrets.
6. Activate both loads with lower than 1 A for each rail. Increase load current, use a current probe or meter and verify circuit breaker threshold level. For the +12 V circuit it should be between 5 A and 7.5 A , for the +3.3 V circuit, between 2.5A and 3.8A. After an overcurrent fault associated power good LED D3 or D4 will be off. To reset FAULT latch turn +12 V supply off and then on.
7. Remove the loads. Turn both +12 V and +3.3 V rails off by placing JP1 and JP2 in the OFF position. Load the +12 V output with a 1500uF capacitor and return jumper headers of the JP1 and JP2 to the ON position. Turn the +3.3 V rail on first and then the +12 V rail. Both rails should be on.
8. Repeat step 7 with a 6000 uF capacitor. In this case only the +3.3 V rail comes up, but +12 V fails.
9. Place the JP3 (AUTO RETRY) in the YES position. Use a current probe to display the +12 V rail current and scope probes to display +12 V and +3.3 V output voltages. Activate both channels and overload +12 V rail. The transient should be similar to that shown in Figure 2.
10. Place JP4 (FAULT SIGNAL) in the YES position and control FAULT pin signal on the FAULT turret. Activate both channels with no load. Slowly increase the +12 V supply output (not higher than 16V). Overvoltage protection should disable both channels when the output voltage is in a range from 13.6 V to 15.0 V and FAULT turret signal drops to low.
11. Activate both channels with no load. Slowly decrease +12 V supply output. The PWRGD1 LED goes off when output is in the range of 10.4 V to 11.3 V .
12. Place JP4 (FAULT SIGNAL) in the YES position and control FAULT pin signal on the FAULT turret. Activate both channels with no load. Slowly increase +3.3 V supply output (not higher than 16V). Overvoltage protection should disable both channels, when the output voltage is in the range of 3.7 V to 3.9 V and FAULT turret signal drops to low.
13. Activate both channels with no load. Slowly decrease +3.3 V supply output. The PWRGD2 LED goes off when output is in a range from 2.76 V to 3.0 V .


Figure 1.

Figure 2.



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