LTC2262-14/-12, LTC2261-14/-12, LTC2260-14/-12, LTC2259-14/-12, LTC2258-14/-12, LTC2257-14/-12, LTC2256-14/-12, 14/12-Bit, 25Msps to 150Msps ADCs

DESCRIPTION

Demonstration circuit 1369A supports a family of 14/12-bit 25Msps to 150Msps ADCs. Each assembly features one of the following devices: LTC2262-14 or LTC2262-12, LTC2261-14, LTC2261-12, LTC2260-14, LTC2260-12, LTC2259-14, LTC2259-12, LTC2258-14, LTC2258-12, LTC2257-14, LTC2257-12, LTC2256-14, LTC2256-12, high speed, high dynamic range ADCs.

Demonstration circuit 1369A supports the LTC2261 family DDR LVDS output mode. This family of ADCs is also supported by demonstration circuit 1370A, which is compatible with CMOS and DDR CMOS output modes.

Several versions of the 1369A demo board supporting the LTC2261 14/12-bit series of A/D converters are listed in Table 1. Depending on the required resolution and sample rate, the DC1369A is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for analog input frequencies from 5MHz to 170MHz. Refer to the data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY (T_A = 25°C)

Table 1

PARAMETER	CONDITION	VALUE
Supply Voltage – DC1369A	Depending on sampling rate and the A/D converter provided, this supply must provide up to 250mA	Optimized for 3.6V 3.5V ↔ 6.0V Min/Max
Analog Input Range	Depending on SENSE Pin Voltage	$1V_{P-P}$ to $2V_{P-P}$
Logic Input Voltages	Minimum Logic High	1.3V
	Maximum Logic Low	0.6V
Logic Output Voltages (Differential)	Nominal Logic Levels (100Ω Load, 3.5mA Mode)	350mV/1.25V Common Mode
	Minimum Logic Levels (100Ω Load, 3.5mA Mode)	247mV/1.25V Common Mode
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Convert Clock Level	Single-Ended Encode Mode (ENC – Tied to GND)	0V to 3.6V
Convert Clock Level	Differential Encode Mode (ENC – Not Tied to GND)	0.2V to 3.6V
Resolution	See Table 1	
Input Frequency Range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Table 2. DC1369A Variants

DC1369A VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1369A-A	LTC2261-14	14-Bit	125Msps	5MHz to 170MHz
1369A-B	LTC2260-14	14-Bit	105Msps	5MHz to 170MHz
1369A-C	LTC2259-14	14-Bit	80Msps	5MHz to 170MHz
1369A-D	LTC2258-14	14-Bit	65Msps	5MHz to 170MHz
1369A-E	LTC2257-14	14-Bit	40Msps	5MHz to 170MHz
1369A-F	LTC2256-14	14-Bit	25Msps	5MHz to 170MHz
1369A-G	LTC2261-12	12-Bit	125Msps	5MHz to 170MHz
1369A-H	LTC2260-12	12-Bit	105Msps	5MHz to 170MHz
1369A-I	LTC2259-12	12-Bit	80Msps	5MHz to 170MHz
1369A-J	LTC2258-12	12-Bit	65Msps	5MHz to 170MHz
1369A-K	LTC2257-12	12-Bit	40Msps	5MHz to 170MHz
1369A-L	LTC2256-12	12-Bit	25Msps	5MHz to 170MHz
1369A-M	LTC2262-14	14-Bit	150Msps	5MHz to 170MHz
1369A-N	LTC2262-12	12-Bit	150Msps	5MHz to 170MHz

Demonstration circuit 1369A is easy to set up to evaluate the performance of the LTC2262 family of A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

Setup

If a DC890 QuikEval™ II Data Acquisition and Collection System was supplied with the DC1369A demonstration circuit, follow the DC890 Quick Start Guide to install the required software and for connecting the DC890 to the DC1369A and to a PC.

DC1369A Demonstration Circuit Board Jumpers

The DC1369A demonstration circuit board should have the following jumper settings as default positions (as per Figure 1):

JP2: PAR/SER: Selects Parallel or Serial programming mode. (Default – Serial)

JP3: Duty Cycle Stabilizer: Enables/Disable Duty Cycle Stabilizer. (Default – Enable)

JP4: SHDN: Enables and disables the LTC2262 (Default – Enable)

Applying Power and Signals to the DC1369A Demonstration Circuit

If a DC890 is used to acquire data from the DC1369A, the DC890 must *first* be connected to a powered USB port or provided an external 6V to 9V *before* applying 3.6V to 6.0V across the pins marked V^+ and GND on the DC1369A. DC1369A requires 3.6V for proper operation. Regulators on the board produce the voltages required for the ADC. The DC1369A demonstration circuit requires up to 250mA depending on the sampling rate and the A/D converter supplied.

The DC890 data collection board is powered by the USB cable and does not require an external power supply unless it must be connected to the PC through an unpowered hub, in which case it must be supplied an external 6V to 9V on turrets G7(+) and G1(–) or the adjacent 2.1mm power jack.

Analog Input Network

For optimal distortion and noise performance the RC network on the analog inputs may need to be optimized for different analog input frequencies. For input frequencies above 170MHz, refer to the LTC2262 data sheet for a proper input network. Other input networks may be more appropriate for input frequencies less that 5MHz.

QUICK START PROCEDURE

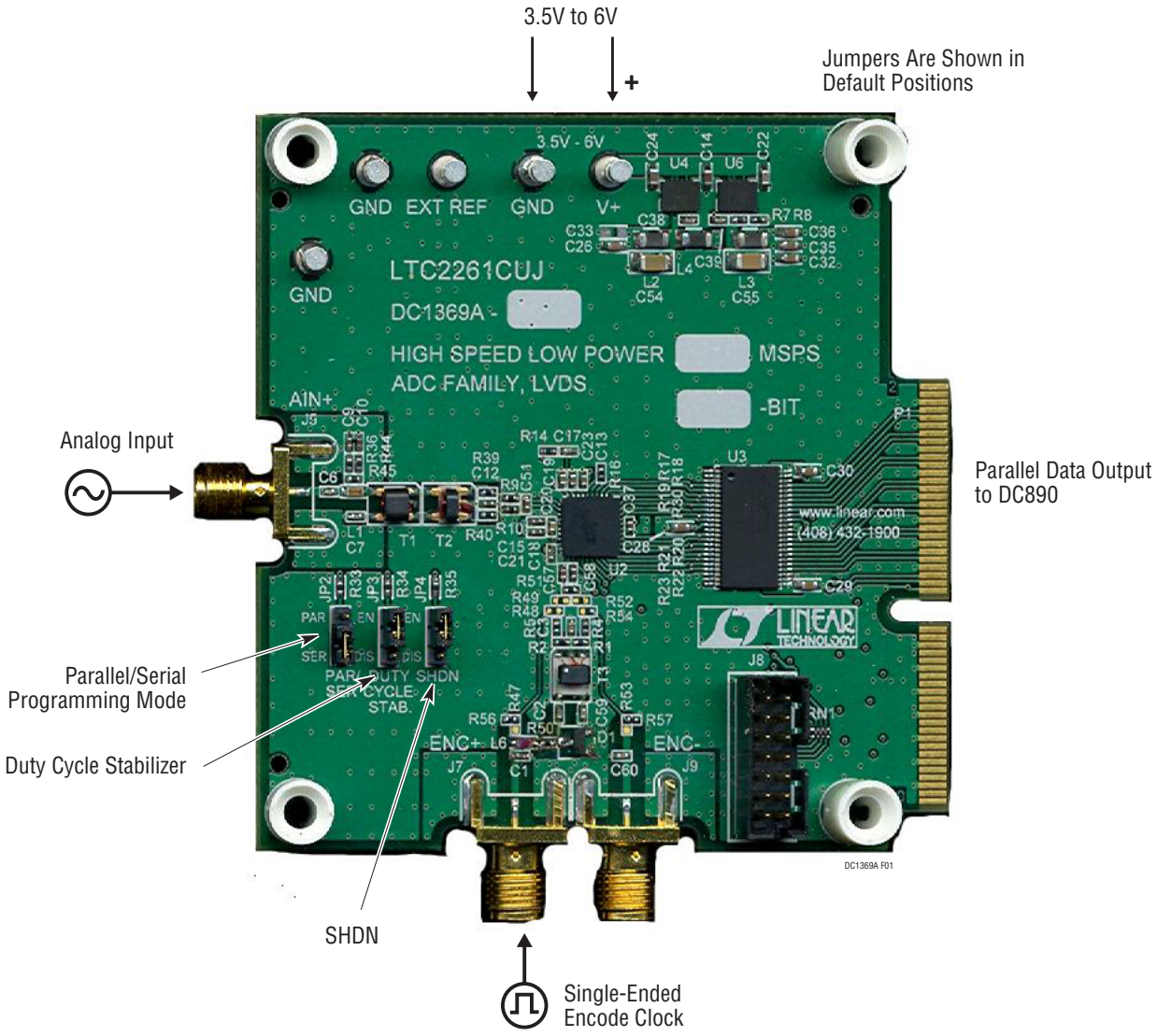


Figure 1. DC1369A Setup

QUICK START PROCEDURE

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR. In the case of the DC1369A a bandpass filter used for the clock should be used prior to the DC1075A.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full-scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and High IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

Encode Clock

NOTE: Apply an encode clock to the SMA connector on the DC1369A demonstration circuit board marked J7. As a default the DC1369A is populated to have a single-ended input.

For the best noise performance, the encode input must be driven with a very low jitter, square wave source. The amplitude should be large, up to $3V_{P-P}$ or 13dBm. When using a sinusoidal signal generator a squaring circuit can be used. Linear Technology also provides demo board DC1075A that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTC2262 family.

Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1369A a bandpass filter used for the clock should be used prior to the DC1075A. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used with TTE bandpass filters for both the clock input and the analog input.

Apply the analog input signal of interest to the SMA connectors on the DC1369A demonstration circuit board marked J5 A_{IN}^{+}. These inputs are capacitive coupled to Balun transformers ETC1-1-13.

An internally generated conversion clock output is available on J1 which could be collected via a logic analyzer, or other data collection system if populated with a SAMTEC MEC8-150 type connector or collected by the DC890 QuikEval II Data Acquisition Board using PScope™ software.

QUICK START PROCEDURE

Software

The DC890 is controlled by the PScope System Software provided or downloaded from the Linear Technology website at http://www.linear.com/software/. If a DC890 was provided, follow the DC890 Quick Start Guide and the instructions below.

To start the data collection software if PScope.exe is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1369A demonstration circuit is properly connected to the DC890, PScope should automatically detect the DC1369A, and configure itself accordingly. If necessary the procedure below explains how to manually configure PScope.

Under the Configure menu, go to "ADC Configuration...." Check the Config Manually box and use the following configuration options (see Figure 2):

Manual Configuration settings:

Bits: 14 (or 12 for 12-bit parts)

Alignment: 14

FPGA Ld: DDR LVDS

Channs: 2

Bipolar: Checked

Positive-Edge Clk: Checked

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the Collect button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC890 Quick Start Guide and in the online help available within the PScope program itself.

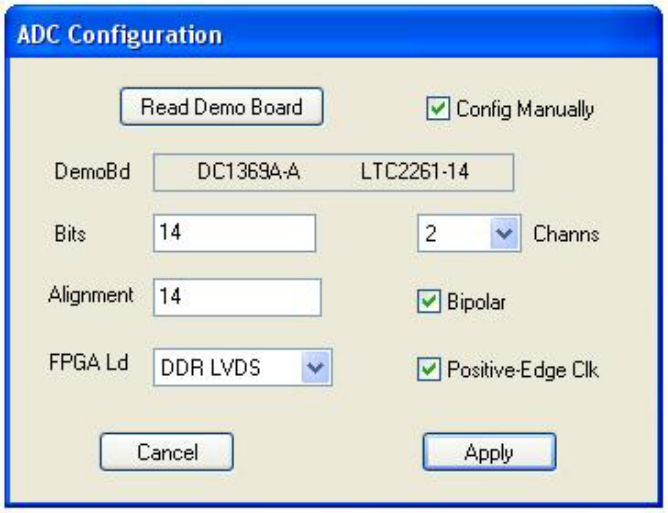


Figure 2. ADC Configuration

QUICK START PROCEDURE

Serial Programming

PScope has the ability to program the DC1369A board serially through the DC890. There are several options available in the LTC2262 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the Set Demo Bd Options icon on the PScope toolbar (Figure 3).

This will bring up the menu shown in Figure 4.

Figure 3. PScope Toolbar

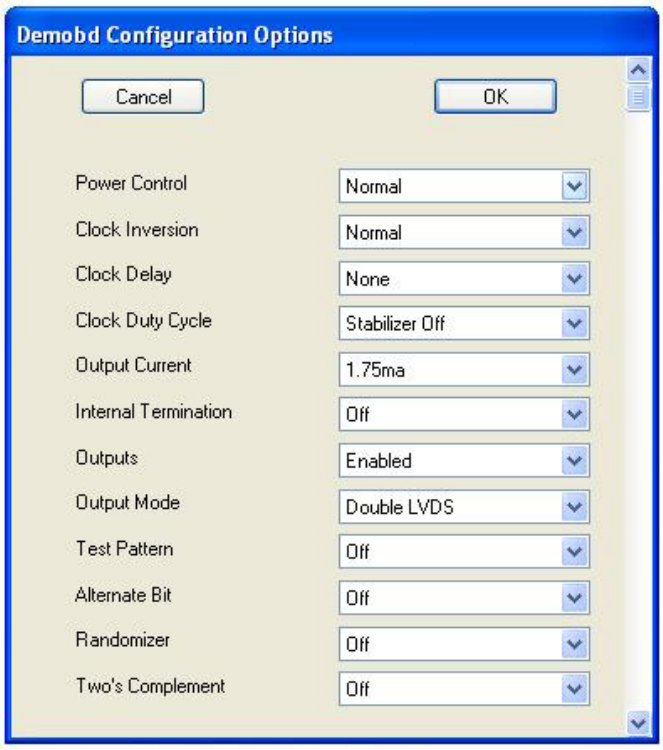


Figure 4. Demo Board Configuration Options

This menu allows any of the options available for the LTC2262 family to be programmed serially. The LTC2262 family has the following options:

Power Control: Selects between normal operation, nap, and sleep modes

- Normal (Default): Entire ADC is powered, and active
- Nap: ADC core powers down while references stay active
- Shutdown: The entire ADC is powered down

Clock Inversion: Selects the polarity of the CLKOUT signal

- Normal (Default): Normal CLKOUT polarity
- Inverted: CLKOUT polarity is inverted

Clock Delay: Selects the phase delay of the CLKOUT signal

- None (Default): No CLKOUT delay
- 45 deg: CLKOUT delayed by 45 degrees
- 90 deg: CLKOUT delayed by 90 degrees
- 135 deg: CLKOUT delayed by 135 degrees

Clock Duty Cycle: Enable or Disables Duty Cycle Stabilizer

- Stabilizer Off (Default): Duty cycle stabilizer disabled
- Stabilizer On: Duty cycle stabilizer enabled

Output Current: Selects the LVDS output drive current

- 1.75mA (Default): LVDS output driver current
- 2.1mA: LVDS output driver current
- 2.5mA: LVDS output driver current
- 3.0mA: LVDS output driver current
- 3.5mA: LVDS output driver current
- 4.0mA: LVDS output driver current
- 4.5mA: LVDS output driver current

QUICK START PROCEDURE

Internal Termination: Enables LVDS Internal Termination

- Off (Default): Disables internal termination
- On: Enables internal termination

Outputs: Enables Digital Outputs

- Enabled (Default): Enables digital outputs
- Disabled: Disables digital outputs

Output Mode: Selects Digital Output Mode

- Full Rate: Full rate CMOS output mode (This mode is not supported by the DC1369A, please use the DC1370)
- Double LVDS (Default): Double data rate LVDS output mode
- Double CMOS: Double data rate CMOS output mode (This mode is not supported by the DC1369A, please use the DC1370)

Test Pattern: Selects Digital Output Test Patterns

- Off (Default): ADC data presented at output
- All Out = 1: All digital outputs are 1
- All Out = 0: All digital outputs are 0
- Checkerboard: OF, and D13-D0 Alternate between 101 0101 1010 0101 and 010 1010 0101 1010 on alternating samples.
- Alternating: Digital outputs alternate between all 1's and all 0's on alternating samples.

Alternate Bit: Alternate Bit Polarity (ABP) Mode

- Off (Default): Disables alternate bit polarity
- On: Enables alternate bit polarity (Before enabling ABP, be sure the part is in offset binary mode)

Randomizer: Enables Data Output Randomizer

- Off (Default): Disables data output randomizer
- On: Enables data output randomizer

Two's Complement: Enables Two's Complement Mode

- Off (Default): Selects offset binary mode
- On: Selects two's complement mode

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1369A demo board.

PARTS LIST

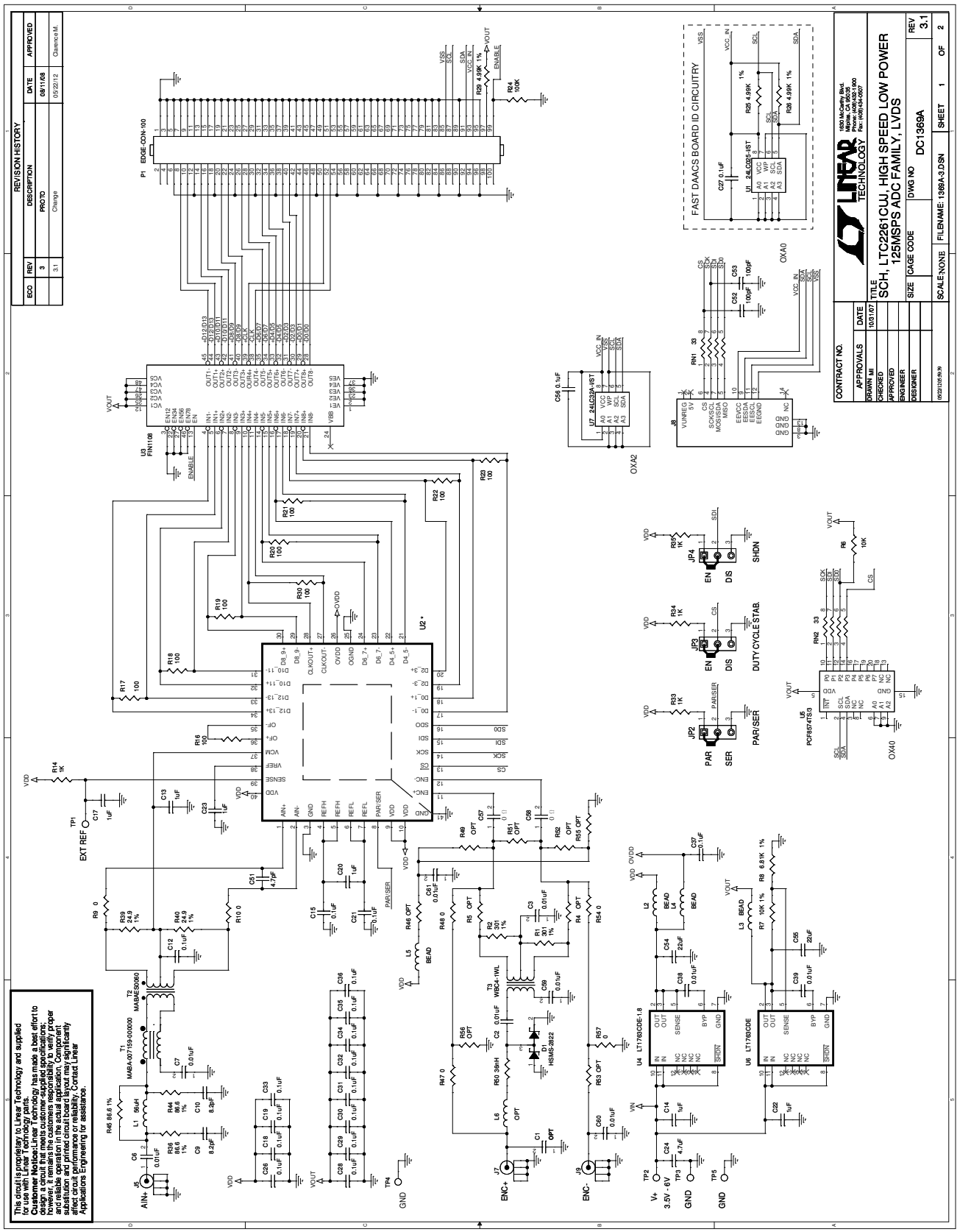
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	1	C1	RES, 0402 150Ω 1% 1/16W	VISHAY CRCW0402150RFKED
2	9	C2, C3, C6, C7, C38, C39, C59-C61	CAP, 0402 0.01uF 10% 16V X7R	AVX 0402YC103KAT
3	2	C10, C9	CAP, 0402 8.2pF 5% 50V COG	AVX 04025A8R2JAT2A
4	6	C12, C15, C18, C19, C21, C37	CAP, 0402 0.1uF 10% 10V X5R	TDK C1005X5R1A104K
5	3	C13, C17, C23	CAP, 0402 1uF 10% 10V X5R	TDK C1005X5R1A105K
6	2	C14, C22	CAP, 0603 1uF 10% 16V X7R	TDK C1608X7R1C105K
7	1	C20	CAP, 0402 1uF 10% 10V X5R	MURATA GRM155R61A105KE15D
8	1	C24	CAP, 0603 4.7uF 20% 6.3V X5R	TDK C1608X5R0J475MT
9	12	C26-C36, C56	CAP, 0603 0.1uF 10% 50V X7R	TDK C1608X7R1H104K
10	1	C51	CAP, 0402 4.7pF +/-0.25pF 50V NPO	AVX 04025A4R7CAT2A
11	2	C53, C52	CAP, 0402 100pf 5% 50V COG	TDK C1005C0G1H101J
12	2	C54, C55	CAP, 1206 22uF 10% 6.3V X5R	AVX 12066D226KAT2A
13	7	R9, R10, R48, R54, R57, C57, C58	RES, 0402 0Ω JUMPER	VISHAY CRCW04020000Z0ED
14	1	D1	DIODE, SCHOTTKY SOT-23	AVAGO HSMS-2822
15	3	JP2, JP3, JP4	HEADER, 3-PIN, 2mm	SAMTEC TMM-103-02-L-S
16	3	J5, J7, J9	CONN, BNC, SMA 50Ω EDGE-LANCH	E.F.JOHNSON, 142-0701-851
17	1	J8	HEADER, 2×7 2mm	MOLEX 87331-1420
18	1	L1	IND, 0603 56uH 5%	MURATA LQP18MN56NG02D
19	3	L2, L3, L4	FERRITE BEAD, 1206	MURATA BLM31PG330SN1L
20	1	L5	IND, 0603 BEAD	?
21	1	L6	IND, 0603 OPTION	OPTION
22	1	P1	EDGE FINGERS ON PCB	PART OF THE PCB
23	2	RN2, RN1	RES ARRAY, 33Ω	VISHAY CRA04SS08333R0JTD
24	2	R1, R2	RES, 0402 301Ω 1% 1/16W	VISHAY CRCW0402301RFKED
25	3	R4, R5, R56	RES, 0402 OPTION	OPTION
26	1	R6	RES, 0402 10kΩ 5% 1/16W	VISHAY CRCW040210K0JNED
27	1	R7	RES, 0402 10kΩ 1% 1/16W	VISHAY CRCW040210K0FKED
28	1	R8	RES, 0402 6.81kΩ 1% 1/16W	YAGEO RC0402FR-076K81L
29	4	R14, R33, R34, R35	RES, 0402 1kΩ 5% 1/16W	VISHAY CRCW04021K00JNTDE3
30	1	R16	RES, 0402 100Ω 5% 1/16W	VISHAY CRCW0402100RJNED
31	8	R17-R23, R30	RES, 0201 100Ω 5% 1/16W	VISHAY CRCW0201100RFNTD
32	1	R24	RES, 0402 100kΩ 5% 1/16W	VISHAY CRCW0402100KJNED
33	3	R25, R26, R29	RES, 0603 4.99kΩ 1% 1/16W	AAC CR16-4991FM
34	3	R36, R44, R45	RES, 0402 86.6Ω 1% 1/16W	VISHAY CRCW040286R6FKED
35	2	R40, R39	RES, 0402 24.9Ω 1% 1/16W	VISHAY CRCW040224R9FKED
36	0	R46, R49, R52, R53, R55	RES, 0402 OPTION	VISHAY CRCW0402101J ?
37	1	R47	RES, 0402 20Ω 1% 1/16W	VISHAY CRCW040220R0FKED
38	1	R50	IND, 36nH	COILCRAFT 0402CS-36NXJB
39	0	R51	RES, 0402 301Ω 1% 1/16W OPTION	VISHAY CRCW0402301RFKED OPTION
40	5	TP1, TP2, TP3, TP4, TP5	TURRETS	MILLMAX 2501-2-00-80-00-00-07-0
41	1	T1	XFMR, 1:1	MACOM MABA-007159-000000
42	1	T2	XFMR, 1:1 CT	M/A-COM MABAES0060/COILCRAFT WBC1-1LB

PARTS LIST

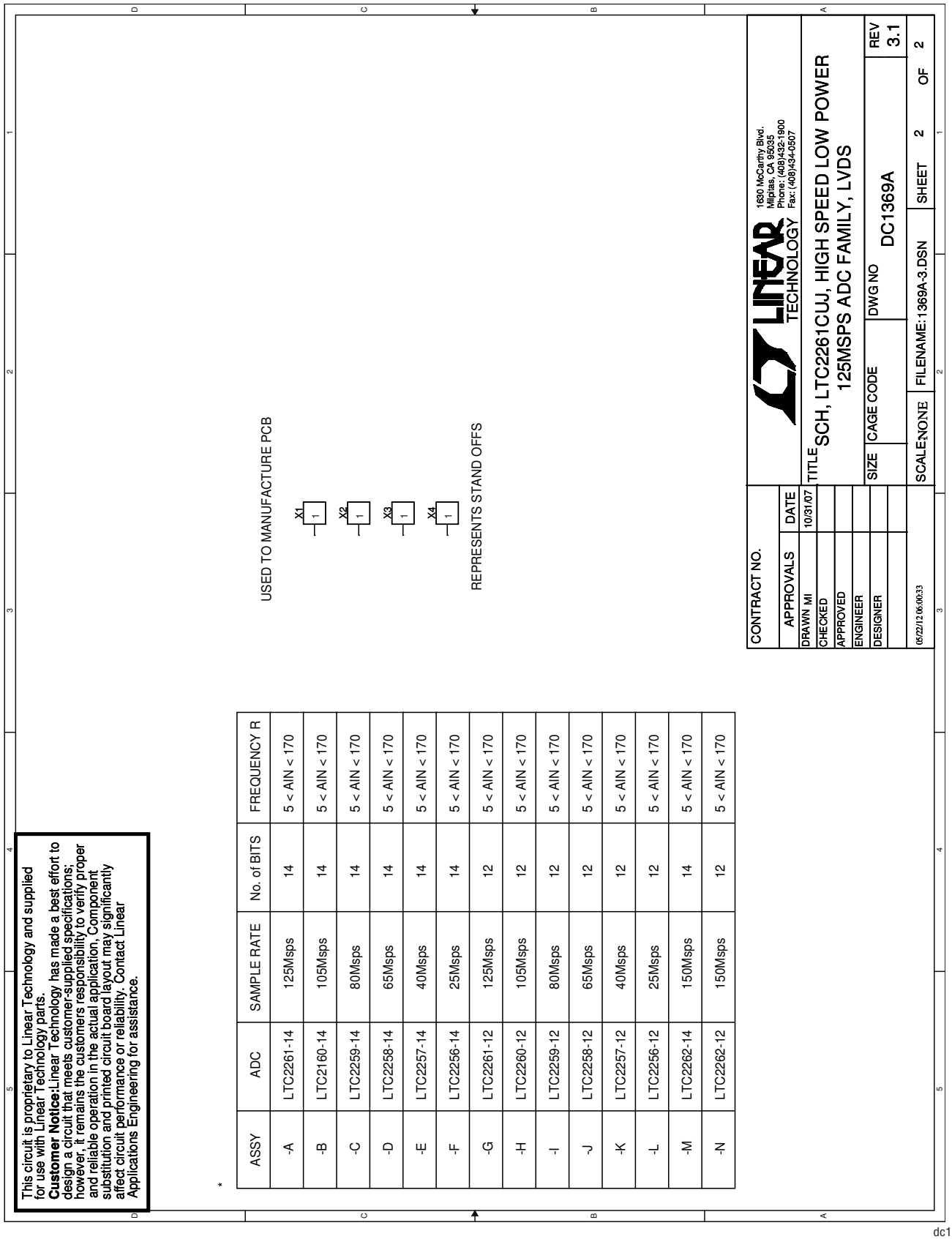
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
43	1	T3	XFMR, 1:4 CT	COILCRAFT WBC4-1WLB
44	1	U1	IC, EEPROM	MICROCHIP TECH. 24LC025-I/ST
45	1	U3	IC, FIN1108	FAIRCHILD FIN1108
46	1	U4	IC, LDO Micropower Regulators	LINEAR TECH. LT1763CDE-1.8
47	1	U5	IC, 8-BIT I/0 EXPANDER	PHILIPS SEMI PCF8574TS/3
48	1	U6	IC, LDO Micropower Regulators	LINEAR TECH. LT1763CDE
49	1	U7	IC, EEPROM	MICROCHIP TECH. 24LC32A-I/ST
50	3	XJP2, XJP3, XJP4	SHUNT, 2mm	SAMTEC 2SN-BK-G
51	4		STANDOFF, SNAP ON	KEYSTONE_8831

See page 2 of the Schematic Diagram for U2.

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



*

ASSY	ADC	SAMPLE RATE	No. of BITS	FREQUENCY R
-A	LTC2261-14	125Msps	14	5 < AIN < 170
-B	LTC2160-14	105Msps	14	5 < AIN < 170
-C	LTC2259-14	80Msps	14	5 < AIN < 170
-D	LTC2258-14	65Msps	14	5 < AIN < 170
-E	LTC2257-14	40Msps	14	5 < AIN < 170
-F	LTC2256-14	25Msps	14	5 < AIN < 170
-G	LTC2261-12	125Msps	12	5 < AIN < 170
-H	LTC2260-12	105Msps	12	5 < AIN < 170
-I	LTC2259-12	80Msps	12	5 < AIN < 170
-J	LTC2258-12	65Msps	12	5 < AIN < 170
-K	LTC2257-12	40Msps	12	5 < AIN < 170
-L	LTC2256-12	25Msps	12	5 < AIN < 170
-M	LTC2262-14	150Msps	14	5 < AIN < 170
-N	LTC2262-12	150Msps	12	5 < AIN < 170

DEMONSTRATION BOARD IMPORTANT NOTICE

Linear Technology Corporation (LTC) provides the enclosed product(s) under the following **AS IS** conditions:

This demonstration board (DEMO BOARD) kit being sold or provided by Linear Technology is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not provided by LTC for commercial use. As such, the DEMO BOARD herein may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including but not limited to product safety measures typically found in finished commercial goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may or may not meet the technical requirements of the directive, or other regulations.

If this evaluation kit does not meet the specifications recited in the DEMO BOARD manual the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY THE SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THIS INDEMNITY, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user releases LTC from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. Also be aware that the products herein may not be regulatory compliant or agency certified (FCC, UL, CE, etc.).

No License is granted under any patent right or other intellectual property whatsoever. **LTC assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or any other intellectual property rights of any kind.**

LTC currently services a variety of customers for products around the world, and therefore this transaction **is not exclusive**.

Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged**.

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Data Conversion IC Development Tools ***category:***

Click to view products by Analog Devices ***manufacturer:***

Other Similar products are found below :

EVAL-AD5063EBZ EVAL-AD5422LFEBZ EVAL-AD7265EDZ EVAL-AD7641EDZ EVAL-AD7674EDZ EVAL-AD7719EBZ EVAL-AD7767-1EDZ EVAL-AD7995EBZ AD9114-DPG2-EBZ AD9211-200EBZ AD9251-20EBZ AD9251-65EBZ AD9255-125EBZ AD9284-250EBZ AD9613-170EBZ AD9627-125EBZ AD9629-20EBZ AD9709-EBZ AD9716-DPG2-EBZ AD9737A-EBZ AD9787-DPG2-EBZ AD9993-EBZ DAC8555EVM ADS5482EVM ADS8372EVM EVAL-AD5061EBZ EVAL-AD5062EBZ EVAL-AD5443-DBRDZ EVAL-AD5570SDZ EVAL-AD7450ASDZ EVAL-AD7677EDZ EVAL-AD7992EBZ EVAL-AD7994EBZ AD9119-MIX-EBZ AD9148-M5375-EBZ AD9204-80EBZ AD9233-125EBZ AD9265-105EBZ AD9265-80EBZ AD9608-125EBZ AD9629-80EBZ AD9648-125EBZ AD9649-20EBZ AD9650-80EBZ AD9765-EBZ AD9767-EBZ ADS8322EVM LM96080EB/NOPB EVAL-AD5445SDZ EVAL-AD5660EBZ