

LTC2268-14/-12,
 LTC2267-14/-12, LTC2266-14/-12, LTC2265-14/-12,
 LTC2264-14/-12, LTC2263-14/-12 12-/14-Bit, 25MSPS to
 125MSPS Dual ADCs

DESCRIPTION

Demonstration circuit 1532 supports a family of 14-/12-bit 25MSPS to 125MSPS ADCs. Each assembly features one of the following devices: LTC2268-14, LTC2268-12, LTC2267-14, LTC2267-12, LTC2266-14, LTC2266-12, LTC2265-14, LTC2265-12, LTC2264-14, LTC2264-12, LTC2263-14, LTC2263-12 high speed, dual ADCs.

The versions of the 1532A demo board are listed in Table 1. Depending on the required resolution and sample rate,

the DC1532 is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for analog input frequencies from 5MHz to 140MHz. Refer to the data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at <http://www.linear.com/demo>

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PERFORMANCE SUMMARY (T_A = 25°C)

| PARAMETER | CONDITIONS | VALUE |
|--|--|---|
| Supply Voltage – DC1532A | Depending on Sampling Rate and the A/D Converter Provided, this Supply Must Provide up to 500mA. | Optimized for 3V [3V \leftrightarrow 6.0V Min/Max] |
| Analog Input Range | Depending on SENSE Pin Voltage | 1V _{P-P} to 2V _{P-P} |
| Logic Input Voltages | Minimum Logic High | 1.3V |
| | Maximum Logic Low | 0.6V |
| Logic Output Voltages (Differential) | Nominal Logic Levels (100 Ω Load, 3.5mA Mode) | 350mV/1.25V Common Mode |
| | Minimum Logic Levels (100 Ω Load, 3.5mA Mode) | 247mV/1.25V Common Mode |
| Sampling Frequency (Convert Clock Frequency) | See Table 1 | |
| Encode Clock Level | Single-Ended Encode Mode (ENC – Tied to GND) | 0V to 3.6V |
| Encode Clock Level | Differential Encode Mode (ENC – Not Tied to GND) | 0.2V to 3.6V |
| Resolution | See Table 1 | |
| Input Frequency Range | See Table 1 | |
| SFDR | See Applicable Data Sheet | |
| SNR | See Applicable Data Sheet | |

QUICK START PROCEDURE

Table 1. DC1532 Variants

| DC1532 VARIANTS | ADC PART NUMBER | RESOLUTION | MAXIMUM SAMPLE RATE | INPUT FREQUENCY |
|-----------------|-----------------|------------|---------------------|-----------------|
| 1532A-A | LTC2268-14 | 14-Bit | 125Msps | 5MHz to 140MHz |
| 1532A-B | LTC2267-14 | 14-Bit | 105Msps | 5MHz to 140MHz |
| 1532A-C | LTC2266-14 | 14-Bit | 80Msps | 5MHz to 140MHz |
| 1532A-D | LTC2265-14 | 14-Bit | 65Msps | 5MHz to 140MHz |
| 1532A-E | LTC2264-14 | 14-Bit | 40Msps | 5MHz to 140MHz |
| 1532A-F | LTC2263-14 | 14-Bit | 25Msps | 5MHz to 140MHz |
| 1532A-G | LTC2268-12 | 12-Bit | 125Msps | 5MHz to 140MHz |
| 1532A-H | LTC2267-12 | 12-Bit | 105Msps | 5MHz to 140MHz |
| 1532A-I | LTC2266-12 | 12-Bit | 80Msps | 5MHz to 140MHz |
| 1532A-J | LTC2265-12 | 12-Bit | 65Msps | 5MHz to 140MHz |
| 1532A-K | LTC2264-12 | 12-Bit | 40Msps | 5MHz to 140MHz |
| 1532A-L | LTC2263-12 | 12-Bit | 25Msps | 5MHz to 140MHz |

Demonstration circuit 1532 is easy to set up to evaluate the performance of the LTC2268 A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow the procedure:

Setup

If a DC1371 QuikEval™ II Data Acquisition and Collection System was supplied with the DC1532 demonstration circuit, follow the DC1371 Quick Start Guide to install the required software and for connecting the DC1371 to the DC1532 and to a PC.

DC1532 Demonstration Circuit Board Jumpers

The DC1532 demonstration circuit board should have the following jumper settings as default positions: (as per Figure 1)

J13: PAR/SER: Selects Parallel or Serial programming mode. (Default – Serial)

Optional Jumpers:

J8: Term: Enables/Disable optional output termination. (Default – Removed)

J5: ILVDS: Selects either 1.75mA or 3.5mA of output current for the LVDS drivers. (Default – Removed)

J14: LANE: Selects either 1 lane or 2 lane output modes (Default – Removed) NOTE: The DC1371 does not support 1 lane operation.

J15: $\overline{\text{SHDN}}$: Enables and disables the LTC2268. (Default – Removed)

J2: WP: Enable/Disables write protect for the EEPROM. (Default – Removed)

Note: Optional jumper should be left open to ensure proper serial configuration.

QUICK START PROCEDURE

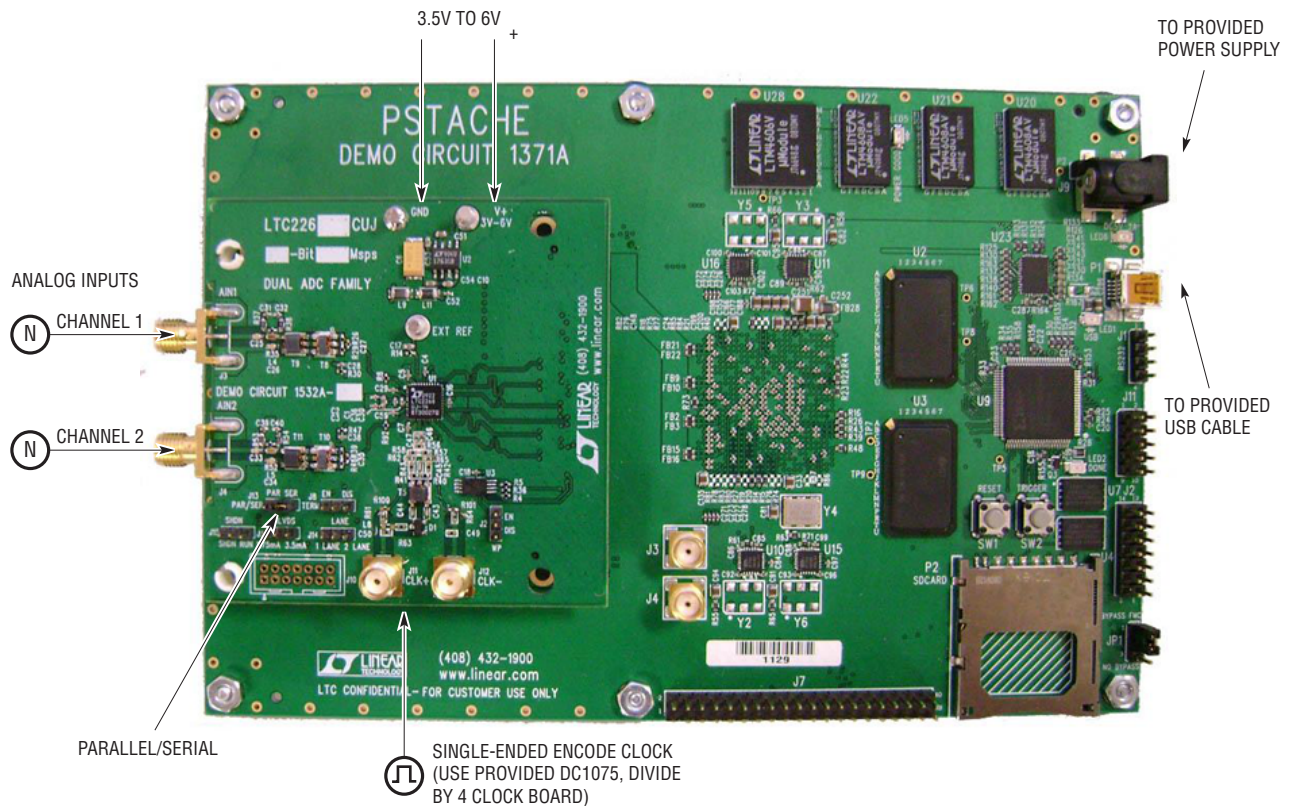


Figure 1. DC1532A Setup

Applying Power And Signals to the DC1532 Demonstration Circuit

The DC1371 is used to acquire data from the DC1532, the DC1371 must FIRST be connected to a powered USB port and have 5V applied power BEFORE applying 3.6V to 6.0V across the pins marked V⁺ and GND on the DC1532. DC1532 requires 3.6V for proper operation.

Regulators on the board produce the voltages required for the ADC. The DC1532 demonstration circuit requires up to 500mA depending on the sampling rate and the A/D converter supplied.

The DC1532 should not be removed, or connected to the DC1371 while power is applied.

Analog Input Network

For optimal distortion and noise performance the RC network on the analog inputs may need to be optimized for different analog input frequencies. For input frequencies above 140MHz, refer to the LTC2268 datasheet for a proper input network. Other input networks may be more appropriate for input frequencies less than 5MHz.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

QUICK START PROCEDURE

If your generator cannot deliver full scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and High IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

Apply the analog input signal of interest to the SMA connectors on the DC1532 demonstration circuit board marked J3 AIN1, J4 AIN2, J6 AIN3, J7 AIN4. These inputs correspond with channels 1-4 of the ADC respectively. These inputs are capacitive coupled to balun transformers ETC1-1-13.

Encode Clock

NOTE: Apply an encode clock to the SMA connector on the DC1532 demonstration circuit board marked J11 CLK+. As a default the DC1532 is populated to have a single-ended input.

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter, square wave source. The amplitude should be large, up to $3V_{P-P}$ or 13dBm. When using a sinusoidal signal generator a squaring circuit can be used. Linear Technology also provides demo board DC1075A that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTC2268.

Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1532 a bandpass filter used for the clock should be used prior

to the DC1075A. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used for both the Clock input and the Analog input.

Digital Outputs

Data outputs, data clock, and frame clock signals are available on J1 of the DC1532. This connector follows the VITA-57/FMC standard, but all signals should be verified when using an FMC carrier card other than the DC1371.

Software

The DC1371 is controlled by the PScope™ System Software provided or downloaded from the Linear Technology website at <http://www.linear.com/software/>.

To start the data collection software if PScope.exe is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1532 demonstration circuit is properly connected to the DC1371, PScope should automatically detect the DC1532, and configure itself accordingly.

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the Collect button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC1371A Quick Start Guide and in the online help available within the PScope program itself.

QUICK START PROCEDURE

Serial Programming

PScope has the ability to program the DC1532 board serially through the DC1371. There are several options available in the LTC2268 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the Set Demo Board Options icon on the PScope toolbar (Figure 3).

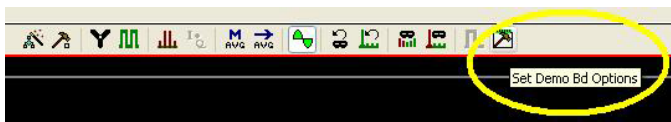


Figure 3. PScope Toolbar

This will bring up the menu shown in Figure 4.

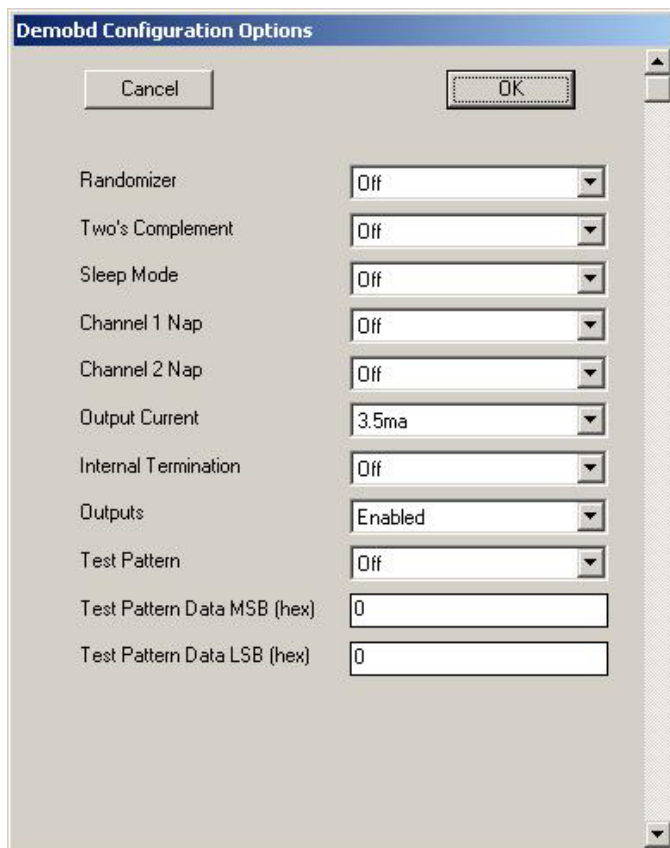


Figure 4: Demo Board Configuration Options

This menu allows any of the options available for the LTC2268 family to be programmed serially. The LTC2268 family has the following options:

Randomizer: Enables Data Output Randomizer

- Off (Default): Disables data output randomizer
- On: Enables data output randomizer

Two's complement: Enables two's complement mode

- Off (Default): Selects offset binary mode
- On: Selects two's complement mode

Sleep Mode: Selects between normal operation, sleep mode

- Off (Default): Entire ADC is powered, and active
- On: The entire ADC is powered down

Channel 1 Nap: Selects between normal operation and putting channel 1 in nap mode

- Off (Default): Channel one is active
- On: Channel one is in nap mode

Channel 2 Nap: Selects between normal operation and putting channel 2 in nap mode

- Off (Default): Channel two is active
- On: Channel two is in nap mode

Output Current: Selects the LVDS output drive current

- 1.75mA (Default): LVDS output driver current
- 2.1mA: LVDS output driver current
- 2.5mA: LVDS output driver current
- 3.0mA: LVDS output driver current
- 3.5mA: LVDS output driver current
- 4.0mA: LVDS output driver current
- 4.5mA: LVDS output driver current

QUICK START PROCEDURE

Internal Termination: Enables LVDS internal termination

- Off (Default): Disables internal termination
- On: Enables internal termination

Outputs: Enables Digital Outputs

- Enabled (Default): Enables digital outputs
- Disabled: Disables digital outputs

Test Pattern: Selects Digital output test patterns. The desired test pattern can be entered into the text boxes provided

- Off (default): ADC input data is displayed
- On: Test pattern is displayed

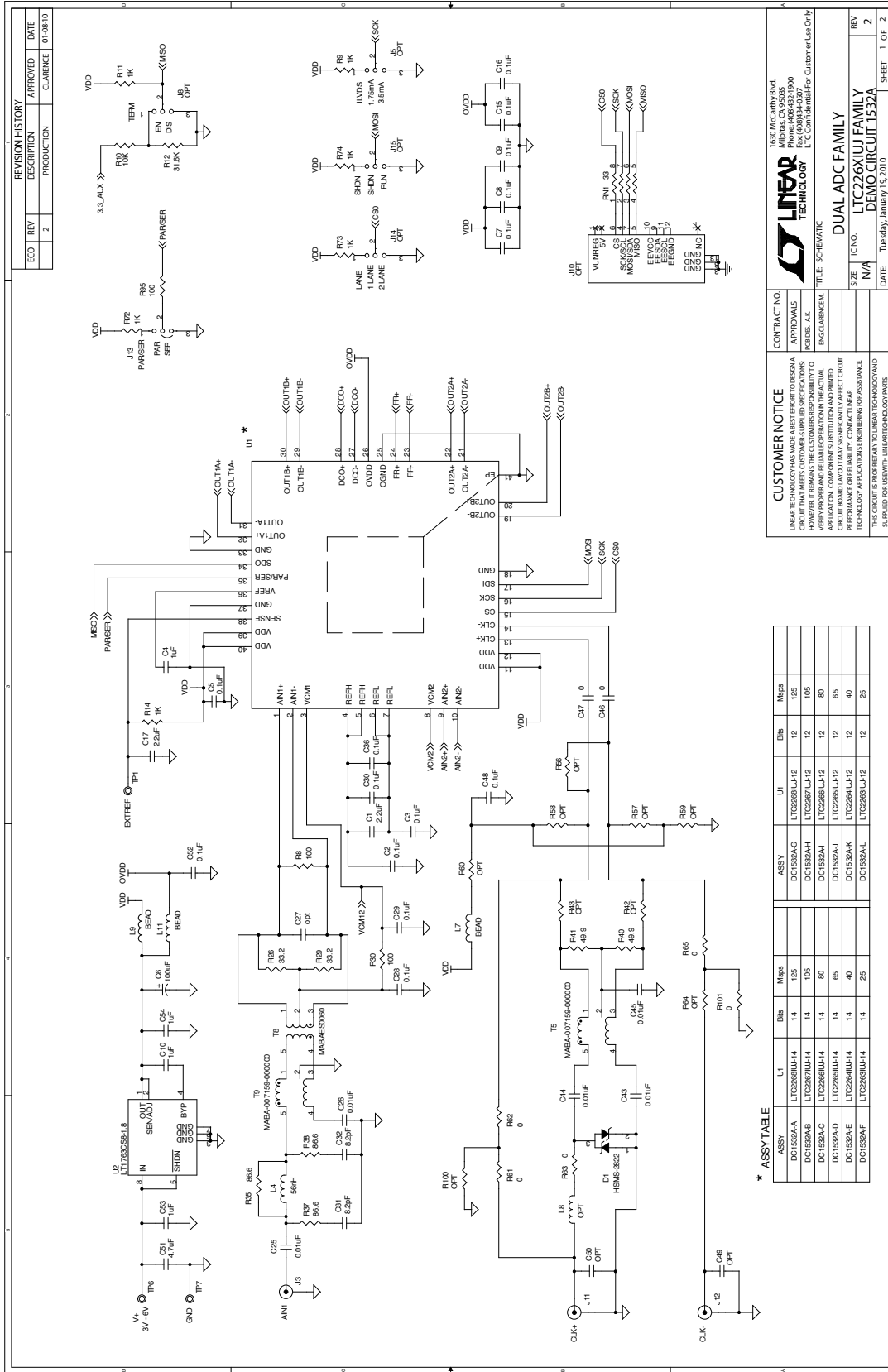
Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1532 demo board

PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|------|-----|--|------------------------------------|-----------------------------------|
| 1 | 2 | C1, C17 | CAP., X5R, 2.2µF, 10V, 20%, 0603 | AVX, 0603ZD225MAT2A |
| 2 | 17 | C2, C3, C5, C7–C9, C15, C16, C18, C28–C30, C36, C38, C48, C52, C59 | CAP., X5R, 0.1µF, 10V, 10%, 0402 | AVX, 0402ZD104KAQ2A |
| 3 | 1 | C4 | CAP., X5R, 1µF, 10V, 10%, 0402 | AVX, 0402ZC105KAT2A |
| 4 | 1 | C6 | CAP., TANT, 100µF, 10%, 6032 | AVX, TAJW107K010R |
| 5 | 3 | C10, C53, C54 | CAP., X7R, 1µF, 10V, 10%, 0603 | AVX, 0603ZC105KAT2A |
| 6 | 4 | C25, C26, C33, C34 | CAP., X7R, 0.01µF, 50V, 10%, 0603 | AVX, 06035C103KAQ2A |
| 7 | 0 | R2, C27, C35, R42, R43, C49, C50, R56, R57, R58, R59, R60, R64, R100 | OPT 0402 | |
| 8 | 4 | C31, C32, C39, C40 | CAP., C0G, 8.2pF, 50V, 5%, 0402 | AVX, 04025A8R2JAT2A |
| 9 | 3 | C43, C44, C45 | CAP., X7R, 0.01µF, 16V, 10%, 0402 | AVX, 0402YC103KAQ2A |
| 10 | 1 | C51 | CAP., X5R, 4.7µF, 6.3V, 20%, 0603 | AVX, 06036D475MAT2A |
| 11 | 1 | D1 | DIODE SCHOTTKY RF SER 15V, SOT-23 | AVAGO, HSMS-2822-TR1G |
| 12 | 1 | J1 | BGA Connector 40 × 10 | SAMTEC, SEAM-40-02.0-S-10-2-A |
| 13 | 6 | J2, J5, J8, J13, J14, J15 | HEADER, 3-Pin, 0.079 Single Row | SAMTEC, TMM-103-02-L-S |
| 14 | 6 | XJ2, XJ5, XJ8, XJ13, XJ14, XJ15 | Shunt, .079" Center | SAMTEC, 2SN-BK-G |
| 15 | 0 | J10, OPT | Header, 2×7PIN, 0.079CC | MOLEX, 87831-1420 |
| 16 | 2 | J4, J3 | CON., SMA 50Ω EDGE-LANCH | E.F. JOHNSON, 142-0701-851 |
| 17 | 2 | J12, J11 | CON., SMA 50Ω Straight Mount | Connex., 132134 |
| 18 | 2 | L4, L5 | Inductor, 56nH, 0603 | Murata, LQP18MN56NG02D |
| 19 | 0 | L7, L8 | OPT | |
| 20 | 2 | L11, L9 | Ferrite Bead, 1206 | Murata, BLM31PG330SN1L |
| 21 | 8 | R1, C46, C47, R61, R62, R63, R65, R101 | RES., CHIP, 0Ω, 0402 | VISHAY, CRCW04020000Z0ED |
| 22 | 1 | RN1 | RES., 2 × 4 Array, CHIP, 33Ω, ISO | VISHAY, CRA06E08333R0JTA |
| 23 | 12 | R4, R5, R10, R36 | RES., CHIP, 10k, 1/16W, 5%, 0402 | VISHAY, CRCW040210K0JNED |
| 24 | | R102–R109 | | |
| 25 | 9 | R8, R30, R47, R92, R95–R99 | RES., CHIP, 100, 1/16W, 5%, 0402 | VISHAY, CRCW0402100RJNED |
| 26 | 6 | R9, R11, R14, R72, R73, R74 | RES., CHIP, 1k, 1/16W, 5%, 0402 | VISHAY, CRCW04021K00JNED |
| 27 | 1 | R12 | RES., CHIP, 31.6k, 1/16W, 1%, 0402 | VISHAY, CRCW040231K6FKED |
| 28 | 4 | R26, R29, R39, R46 | RES., CHIP, 33.2, 1/16W, 1%, 0402 | VISHAY, CRCW040233R2FKED |
| 29 | 2 | R35, R52 | RES., CHIP, 86.6, 1/16W, 1%, 0402 | VISHAY, CRCW040286R6FKED |
| 30 | 4 | R37, R38, R53, R54 | RES., CHIP, 86.6, 1/16W, 1%, 0603 | VISHAY, CRCW060386R6FNED |
| 31 | 2 | R40, R41 | RES., CHIP, 49.9, 1/16W, 1%, 0402 | VISHAY, CRCW040249R9FKED |
| 32 | 8 | R110–R117 | RES., CHIP, 33k, 1/16W, 1%, 0402 | VISHAY, CRCW040233K0FKED |
| 33 | 3 | TP1, TP6, TP7 | Testpoint, Turret, .094" pbf | MILL-MAX, 2501-2-00-80-00-00-07-0 |
| 34 | 3 | T5, T9, T11 | Transformer, MABA-007159-000000 | M/A-COM, MABA-007159-000000 |
| 35 | 2 | T10, T8 | Transformer, MABAES0060 | M/A-COM, MABAES0060 |
| 36 | 1 | U2 | I.C. LT1763CS8-1.8, S08 | LINEAR, LT1763CS8-1.8#TRPBF |
| 37 | 1 | U3 | I.C., Serial EEPROM TSSOP-8 | MICROCHIP, 24LC32A-I/ST |

DEMO MANUAL DC1532

SCHEMATIC DIAGRAM

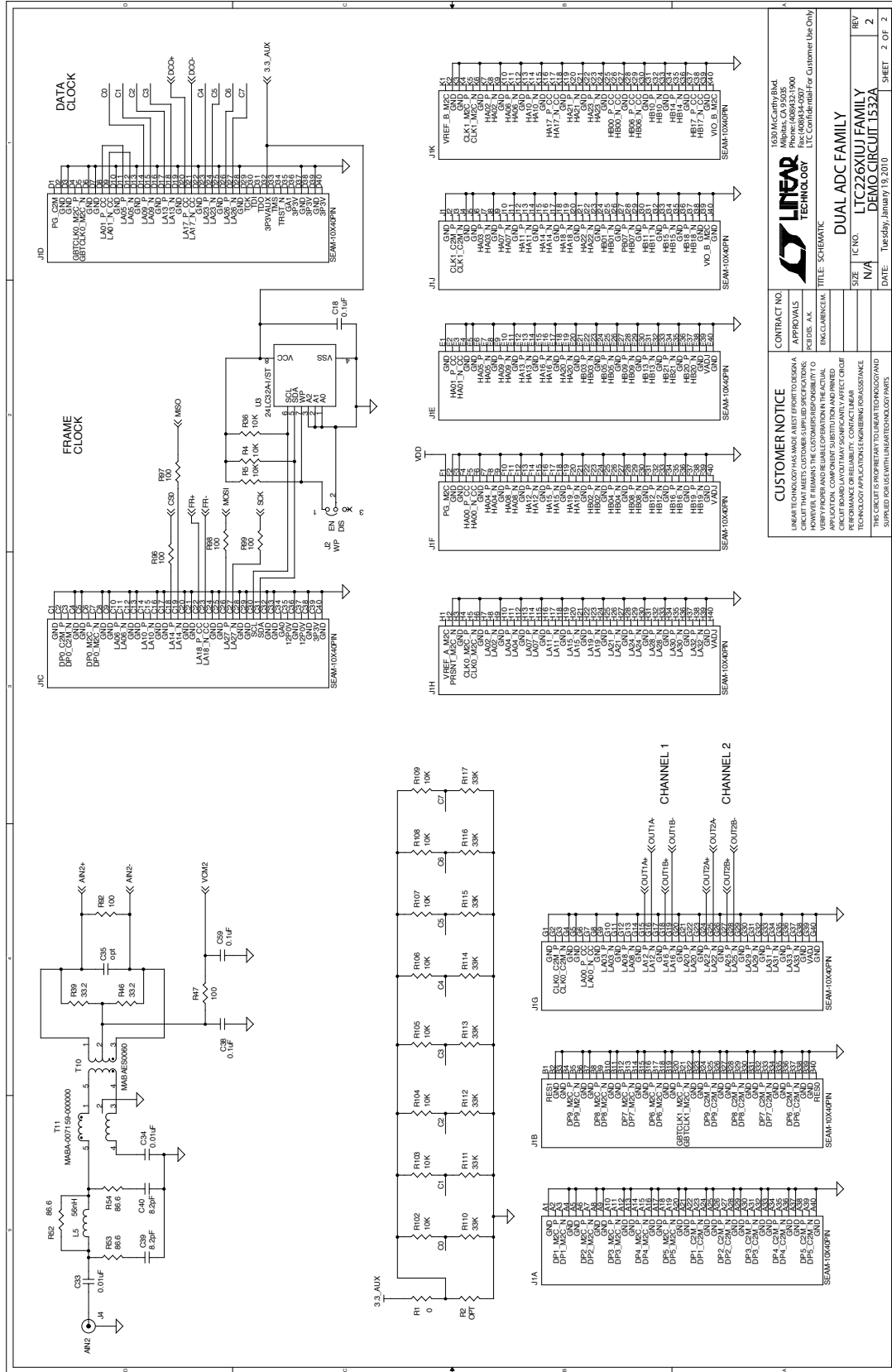


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 DEMO CIRCUIT 1532A

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 SHEET 1 OF 2

SCHEMATIC DIAGRAM



DEMO MANUAL DC1532

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