LTC4365: High Voltage UV, OV and Reverse Supply Protection Controller

DESCRIPTION

Demonstration circuit DC1555B is intended to demonstrate the performance of the LTC4365 High Voltage Undervoltage (UV), Overvoltage (OV) and Reverse Supply Protection Controller.

The LTC4365 protects circuits from input voltages that may be too high, too low or negative. It operates by controlling the gates of two back-to-back connected MOSFETs to keep the output in a safe range. The OV and UV protection levels are adjusted by resistive dividers at the OV and UV pins. Asserting the $\overline{SHDN}$ pin disables the MOSFETs and places the LTC4365 in a low-current shutdown state. The $\overline{FAULT}$ pin is asserted when the Controller is in shutdown mode or when the input voltage is outside of the UV or OV level.

The LTC4365 can withstand DC voltages between –40V and 60V and has a valid operating range of 2.5V to 34V.

The DC1555B includes the LTC4365 Controller, two back-to-back connected power MOSFETs, three jumpers and three LEDs to indicate the input and output voltages and the $\overline{FAULT}$ pin signal.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Board Input Voltage Range		–30		30	V
$V_{IN(UVLO)}$	Input Supply Undervoltage Lockout	V_{IN} Rising	1.8	2.2	2.4	V
I_{VIN}	Input Supply Current	$\overline{SHDN}$ = 0V $\overline{SHDN}$ = 2.5V		10 25	50 150	µA µA
$I_{VIN(R)}$	Reverse Input Supply Current	V_{IN} = –40V, V_{OUT} = 0V		–1.2	–1.8	mA
ΔV_{GATE}	External N-Channel Gate Drive (GATE – V_{OUT})	V_{IN} = V_{OUT} = 5V, I_{GATE} = –1µA V_{IN} = V_{OUT} = 12V to 34V, I_{GATE} = –1µA	3 7.4	3.6 8.4	4.2 9.8	V V
$I_{GATE(UP)}$	External N-Channel Gate Pull-Up current	GATE = V_{IN} = V_{OUT} = 12V	–12	–20	–30	µA
$I_{GATE(FAST)}$	External N-Channel Fast Gate Pull-Down Current	Fast Shutdown, GATE = 20V, V_{IN} = V_{OUT} = 12V	31	50	72	mA
$I_{GATE(SLOW)}$	External N-Channel Gentle Gate Pull-Down Current	Gentle Shutdown, GATE = 20V, V_{IN} = V_{OUT} = 12V	50	90	150	µA
V_{UV}	UV Input Threshold Voltage	UV Falling → ΔV_{GATE} = 0V	492.5	500	507.5	mV
V_{OV}	OV Input Threshold Voltage	OV Rising → ΔV_{GATE} = 0V	492.5	500	507.5	mV
$t_{GATE(FAST)}$	External N-Channel Fast Gate Turn-Off Delay	C_{GATE} = 2.2nF, UV or OV Fault		2	4	µs
t_{FAULT}	OV, UV Fault Propagation Delay	Overdrive = 50mV, V_{IN} = V_{OUT} = 12V		1	2	µs
V_{SHDN}	$\overline{SHDN}$ Input Threshold	$\overline{SHDN}$ Falling to ΔV_{GATE} = 0V	0.4	0.75	1.2	V

OPERATING PRINCIPLES

The LTC4365 monitors the input rail voltage and disconnects downstream circuits when the input voltage is too low, too high or negative. The LTC4365 provides accurate overvoltage and undervoltage comparators to ensure that power is applied to the system only if the input supply is within the allowable voltage window. Reverse supply protection circuit automatically isolates the load from negative input voltages.

During normal operation, a high voltage charge pump enhances the gate of external N-channel power MOSFETs.

The LTC4365 consumes 10µA during shutdown and 125µA while operating.

QUICK START PROCEDURE

Demonstration circuit 1555B is easy to set up to evaluate the performance of the LTC4365. Refer to Figures 1a and 1b for proper measurement equipment setup and follow the procedure below.

Note that the circuit on the DC1555B is optimized for 12V operation; The Si4230 FET limits overvoltage and reverse voltage to 30V and –30V, respectively. Refer to the LTC4365 data sheet for applications optimized for other voltages.

Reverse Voltage Tests (Figure 1a)

1) Set JP1 to EN.

2) Set JP2 and JP3 to CONNECT LED.

3) Connect a power supply across V_{IN} and GND in negative configuration (connect positive rail to GND and negative rail to V_{IN}).

4) Connect voltmeters at the input and output and ammeter in series with supply.

5) Ramp supply down to –30V (referenced to GND).

6) Verify output voltage is between 0V and –0.5V, all LEDs are off, and input current is <1.8mA. (FET leakage or other board leakage paths can pull V_{OUT} slightly negative, but it will be clamped by the internal protection diode.)

7) Ramp supply back to 0V.

Undervoltage/Overvoltage Test (Figure 1b)

8) Reverse the polarity of power supply connection across V_{IN} to GND (connect positive rail to V_{IN} and negative rail to GND).

9) Ramp supply up to 30V and verify green V_{IN} LED, red $\overline{FAULT}$ LED, green V_{OUT} LED, and V_{OUT} according to Table 1 within the various voltage ranges.

10) Ramp supply down from 30V down to 0V and verify green V_{IN} LED, red $\overline{FAULT}$ LED, green V_{OUT} LED, and V_{OUT} according to Table 1.

11) Repeat steps 9 and 10 with 8A load connected across V_{OUT} and GND.

Table 1

V_{IN}	V_{OUT}	V_{IN} LED	V_{OUT} LED	$\overline{FAULT}$ LED
0V to 5.77V	= 0V	Off/Dim/On	Off	On
6.56V to 13.51V	= V_{IN}	On	On	Off
15.47V to 30V	= 0V	On	Off	On

Jumper Test

12) Remove load and set supply to 9V.

13) Move jumpers and verify LEDs according to Table 2.

Table 2

JP1	JP2/JP3	VIN LED	VOUT LED
EN	CONNECT LED	On	On
DIS	CONNECT LED	On	Off
EN	Open	Off	Off

QUICK START PROCEDURE

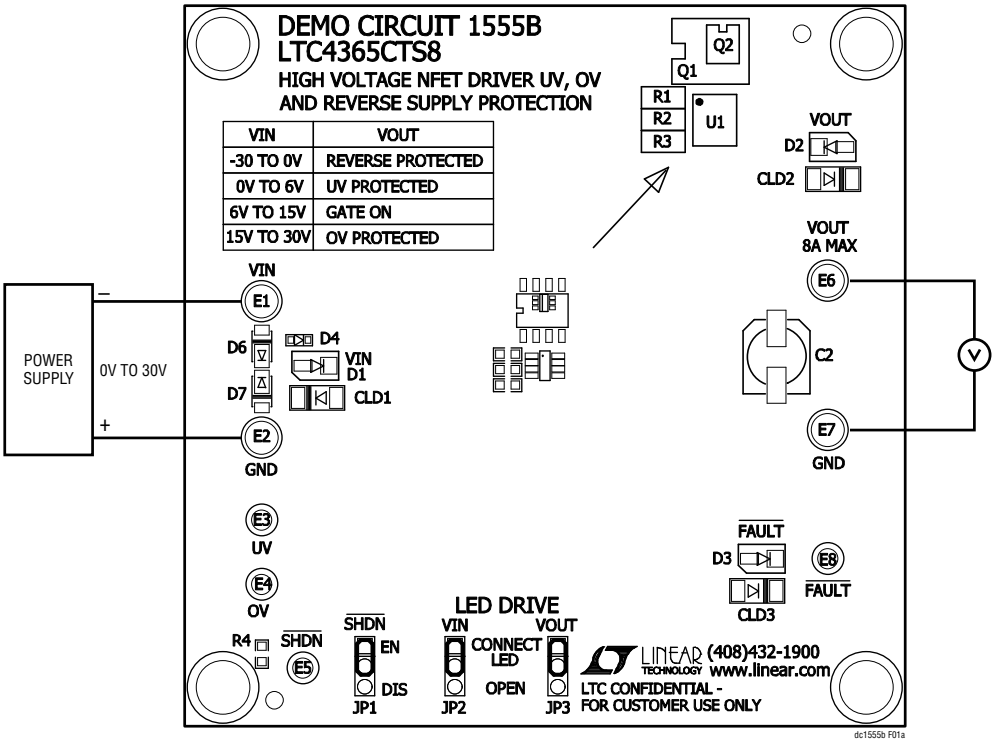


Figure 1a. Reverse Voltage Measurement

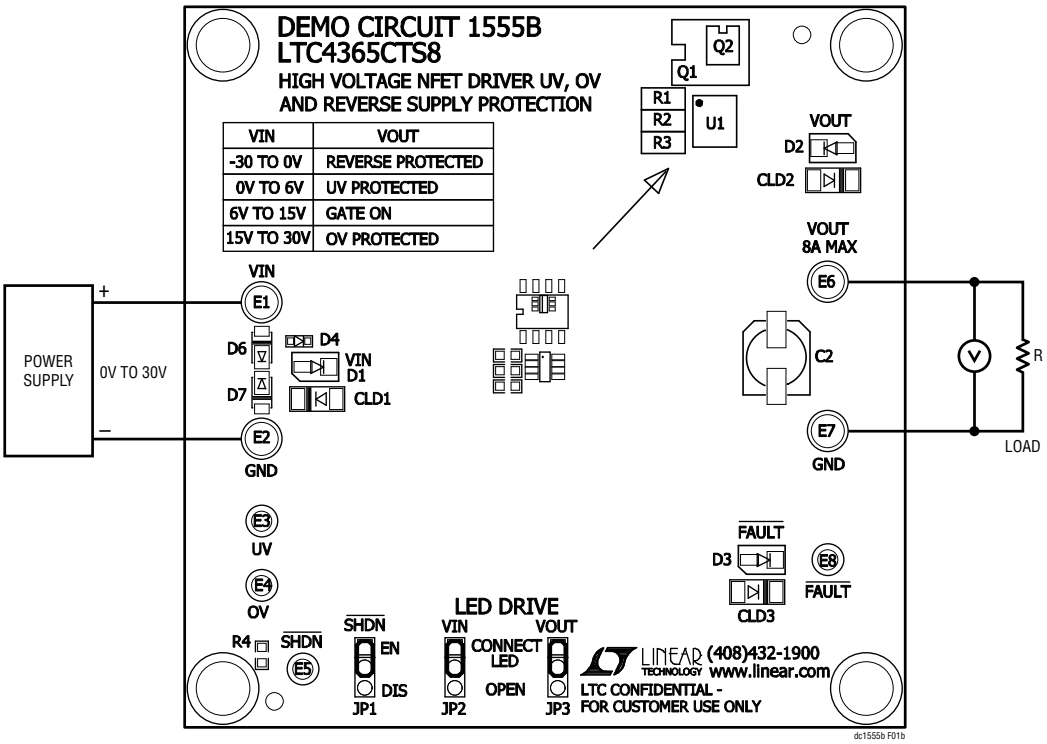
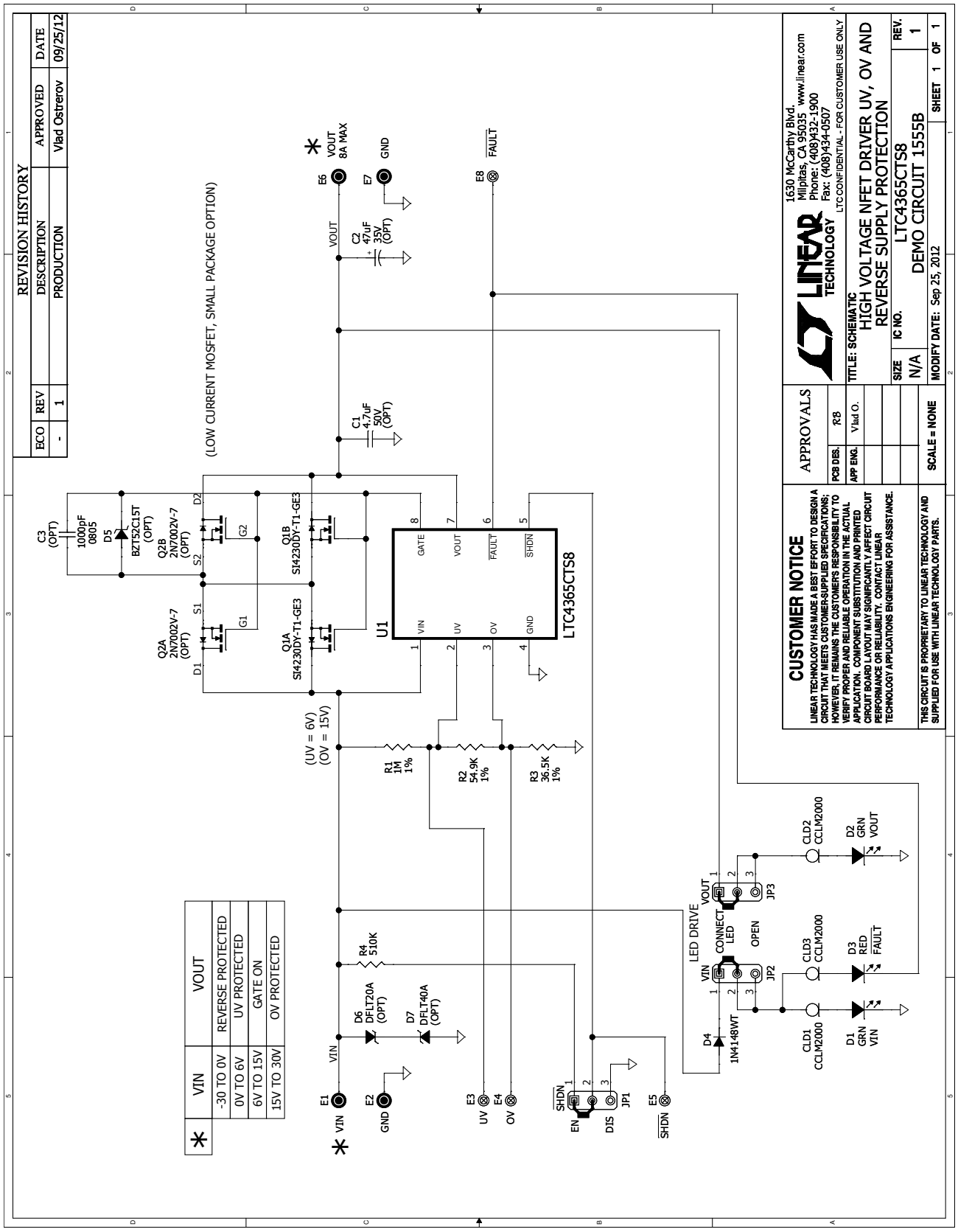


Figure 1b. Undervoltage/Overvoltage Measurement

PARTS LIST

ITEM	QUANTITY	REFERENCE	DESCRIPTION	MANUFACTURERS PART NUMBER
Required Circuit Components				
1	3	CLD1, CLD2, CLD3	Current Limiting, Diode, SOD-80	Central Semi. Corporation, CCLM2000
2	0	C1 (OPT)	Capacitor, X5R, 4.7µF, 50V, 20%, 1210	Taiyo Yuden, UMK325BJ475MM-T
3	0	C2 (OPT)	Capacitor, Alum, 47µF, 35V, 10%, OSCON-CE-6.3	Sanyo, 35CE47AX
4	0	C3 (OPT)	Capacitor, X5R, 10µF, 25V, 10%, 1210	Taiyo Yuden, TMK325BJ106KM
5	2	D1, D2	LED, GRN	Panasonic, LN1351CTR
6	1	D3	LED, RED	Panasonic, LN1251CTR
7	1	D4	Diode, 75V/200mW, SOD-523	Diodes Inc., 1N4148WT
8	0	D5 (OPT)	Zener Diode, 15V, SOD-523	Diodes Inc., BZT52C15T #PbF
9	0	D6 (OPT)	Zener Diode, 20V, POWERDI-123	Diodes Inc., DFLT20A #PbF
10	0	D7 (OPT)	Zener Diode, 40V, POWERDI-123	Diodes Inc., DFLT40A #PbF
11	4	E1, E2, E6, E7	Turret, Testpoint 0.094"	Mill Max 2501-2-00-80-00-00-07-0
12	4	E3, E4, E5, E8	Turret, Testpoint 0.063"	Mill Max 2308-2-00-80-00-00-07-0
13	3	JP1, JP2, JP3	Headers, Sgl. Row, 3 Pins, 2mm Ctrs.	Samtec, TMM-103-02-L-S
14	1	Q1	Dual N-Channel, 30V, SO-8	Vishay, SI4230DY-T1-GE3
15	0	Q2 (OPT)	Dual N-Channel, Low Current, SOT-563	Diodes Inc., 2N7002V-7
16	1	R1 (Bal to #1608A)	Resistor, Chip, 1M, 0.06W, 1%, 0603	Vishay, CRCW06031M00FKEA
17	1	R2	Resistor, Chip, 54.9k, 0.06W, 1%, 0603	Vishay, CRCW060354K9FKEA
18	1	R3	Resistor, Chip, 36.5k, 0.06W, 1%, 0603	Vishay, CRCW060336K5FKEA
19	1	R4	Resistor, Chip, 510k, 0.06W, 5%, 0603	Vishay, CRCW0603510KJNEA
20	1	U1	IC, Over/Under/RevV/RevI Protection, SC8	Linear Technology Corporation, LTC4365CTS8
21	3	XJP1, XJP2, XJP3	Shunt, 2mm Ctrs.	Samtec, 2SN-BK-G
22	4		Stand-Off, Nylon, 0.25" Tall	Keystone, 8831(Snap On)

SCHEMATIC DIAGRAM



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Mailing Address:

Linear Technology

1630 McCarthy Blvd.

Milpitas, CA 95035

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