LTC3388-1/LTC3388-3: 20V High Efficiency Nanopower Step-Down Regulator

DESCRIPTION

Demonstration Circuit DC1658A is a 20V high efficiency nanopower step-down converter featuring the LTC3388-1/LTC3388-3, an ultralow quiescent current step-down regulator. The input current is only 720nA typical at no load while maintaining output voltage regulation. The LTC3388-1/LTC3388-3 is capable of supplying 50mA of load current, and incorporates an accurate undervoltage lockout feature to disable the converter and maintain a low quiescent current state when the input voltage falls below 2.3V. In regulation, the LTC3388-1/LTC3388-3 enter a sleep state in which both input and output quiescent currents are minimal. The buck converter turns on and off as needed to maintain regulation. An additional standby mode disables the buck switching while the output is in regulation for short duration loads requiring low ripple.

Four output voltages are pin selectable with up to 50mA of continuous output current. A power good comparator produces a logic high referenced to V_{OUT} on the PGOOD pin when the converter reaches the programmed V_{OUT}, signaling that the output is in regulation.

The LTC3388EMSE-1/LTC3388EMSE-3 are available in a 10-lead (3mm × 3mm) MSE surface mount package with exposed pad.

Design files for this circuit board are available at http://www.linear.com/demo/DC1658A

PERFORMANCE SUMMARY (T_A = 25°C)

Table 1. LTC3388-1

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range		2.7		20.0	V
V_{OUT} 1.2V	Output Voltage Range	D0 = 0, D1 = 0	1.14	1.2	1.26	V
V_{OUT} 1.5V	Output Voltage Range	D0 = 1, D1 = 0	1.44	1.5	1.56	V
V_{OUT} 1.8V	Output Voltage Range	D0 = 0, D1 = 1	1.737	1.8	1.863	V
V_{OUT} 2.5V	Output Voltage Range	D0 = 1, D1 = 1	2.40	2.5	2.60	V

Table 2. LTC3388-3

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range		2.7		20.0	V
V_{OUT} 2.8V	Output Voltage Range	D0 = 0, D1 = 0	2.688	2.8	2.912	V
V_{OUT} 3.0V	Output Voltage Range	D0 = 1, D1 = 0	2.895	3.0	3.105	V
V_{OUT} 3.3V	Output Voltage Range	D0 = 0, D1 = 1	3.201	3.3	3.399	V
V_{OUT} 5.0V	Output Voltage Range	D0 = 1, D1 = 1	4.82	5.0	5.18	V

OPERATING PRINCIPLE

Refer to the block diagram within the LTC3388-1/LTC3388-3 data sheet for its operating principle.

The LTC3388 is an ultralow quiescent current power supply designed to regulate the output voltage by means of a nanopower high efficiency synchronous buck regulator. See Figure 1 for the LTC3588-1 50mA efficiency versus input voltage curves for the four output voltage settings. Figure 2 is the efficiency curves for the LTC3588-3. The input current is only 720nA typical at no load while maintaining output voltage regulation capable of supplying 50mA of load current.

The LTC3388-1/LTC3388-3 also incorporates an accurate undervoltage lockout feature to disable the converter and maintain a low quiescent current (approximately 400nA), state when the input voltage falls below 2.3V. When the voltage on V_{IN} rises above the UVLO rising threshold, the buck converter is enabled and charge is transferred from the input capacitor to the output capacitor.

The buck regulator uses a hysteretic voltage algorithm to control the output through internal feedback from the V_{OUT} sense pin. The buck converter charges the output capacitor through an inductor to a value slightly higher than the regulation point. It does this by ramping the inductor current up to 150mA through an internal PMOS switch and then ramping down to 0mA through an internal NMOS switch. When the buck converter brings the output voltage into regulation, the LTC3388-1/LTC3388-3 enter a sleep state in which both input and output quiescent currents are minimal. The buck converter turns on and off as needed to maintain regulation.

Two logic pins, EN and STBY, determine the operating mode of the LTC3388-1/LTC3388-3. When EN is high and STBY is low the synchronous buck converter is enabled and will regulate the output if the input is above the programmed output voltage and above the UVLO threshold. If EN is low, the buck converter circuitry is powered to save quiescent current. The internal rail generation circuits are kept alive and the voltages at V_{IN2} and CAP are maintained.

While enabled, the LTC3388-1/LTC3388-3 can be placed in standby mode by bringing STBY high. In standby mode the buck converter is disabled, eliminating the quiescent current used to run the buck circuitry. The PGOOD and sleep comparators are kept alive to maintain the state of the PGOOD pin. The sleep comparator has a lower quiescent current than the PGOOD comparator and when the LTC3388-1/LTC3388-3 is in sleep mode, the PGOOD comparator is shut down and PGOOD is held high. If STBY is driven high with EN low, it will be ignored and will remain in shutdown.

Four output voltages are available by tying the output select pins, D0 and D1, to GND of V_{IN2}. Table 1 shows the four D0/D1 codes and their corresponding output voltages with up to 50mA of continuous output current. The internal feedback network draws a small amount of current from V_{OUT}.

A power good comparator produces a logic high referenced to V_{OUT} on the PGOOD pin when the converter reaches the programmed V_{OUT}, signaling that the output is in regulation. The PGOOD pin will remain Hi-Z until V_{OUT} falls below 92% of the desired regulation voltage. IF PGOOD is high and V_{IN} falls below the UVLO falling threshold, PGOOD will remain high until V_{OUT} falls to 92% of the desired regulation point.

OPERATING PRINCIPLE

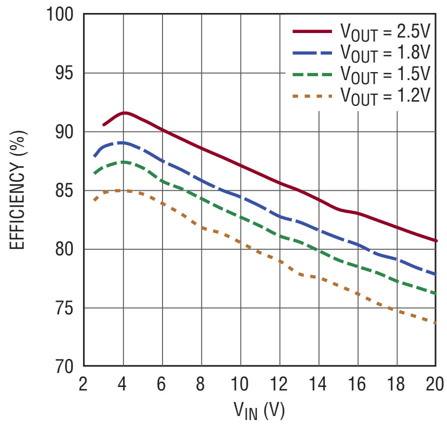


Figure 1. Efficiency vs V_{IN} for I_{LOAD} = 50mA, L = 22µH (LTC3388-1)

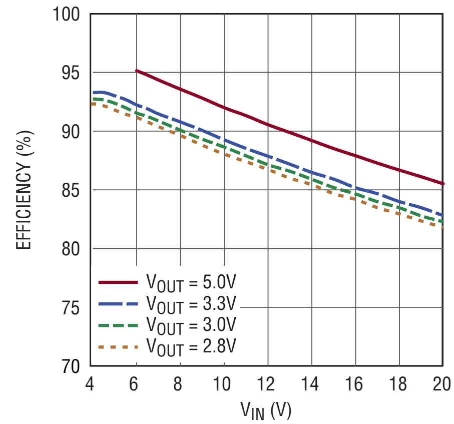


Figure 2. Efficiency vs V_{IN} for I_{LOAD} = 50mA, L = 22µH (LTC3388-3)

QUICK START PROCEDURE

Using short twisted pair leads for any power connections, with all loads and power supplies off, refer to Figure 3 for the proper measurement and equipment setup.

Follow the procedure below:

1. Initial Jumper, PS and LOAD 1 settings:

   JP1 = 0

   JP2 = 1

   JP3 = EN

   JP4 = ON

   JP5 = 1

   PS1 = OFF

   LOAD1 = OFF

2. Turn on PS1 and slowly increase voltage to 2.0V while monitoring the input current. If the current remains less than 5mA, increase PS1 to 6.0V.

3. Set LOAD1 to 50mA. Verify voltage on V_{OUT} is within the V_{OUT} 1.8V/3.3V range in Table 1. Verify that the output ripple voltage is between 50mV and 90mV. Verify that PGOOD is high (V_{OUT}).

4. Set JP1 to 1. Set LOAD1 to 50mA. Verify voltage on V_{OUT} is within the V_{OUT} 2.5V/5.0V range in Table 1. Verify that the output ripple voltage is between 50mV and 110mV.

5. Turn off LOAD1. Set JP4 to STBY. Monitor PGOOD as V_{OUT} decays. PGOOD will go low when V_{OUT} is approximately 2.25V/4.5V.

6. Set JP4 to ON. Set LOAD1 to 50mA. Verify voltage on V_{OUT} is within the V_{OUT} 2.5V/5.0V range in Table 1 and that PGOOD is high.

7. Turn off PS1 and LOAD1.

QUICK START PROCEDURE

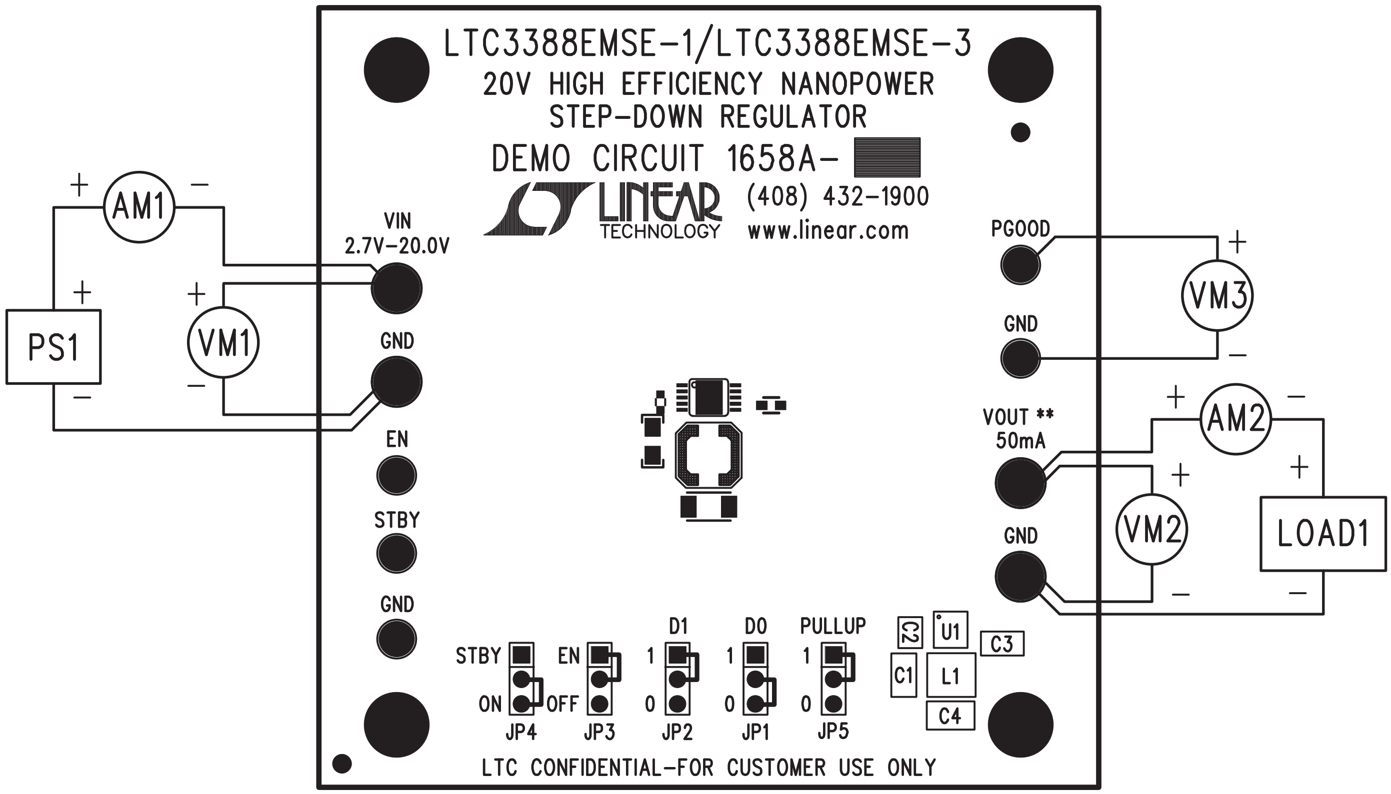
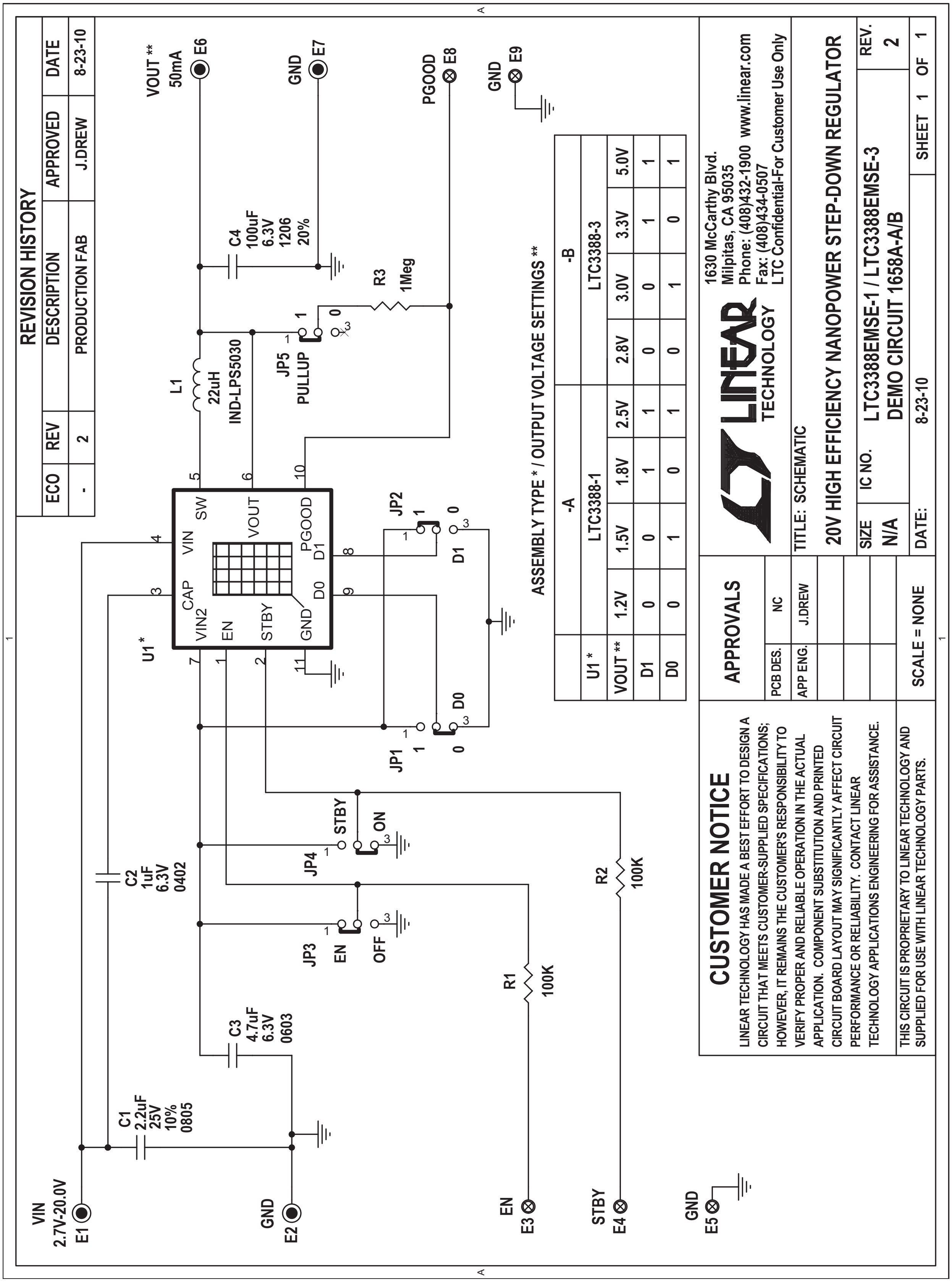


Figure 3. Proper Measurement Equipment Setup

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	C1	CAP, CHIP, X5R, 2.2µF, 10%, 25V, 0805	MURATA, GRM21BR71E22KA73L
2	1	C2	CAP, CHIP, X5R, 1µF, 10%, 6.3V, 0402	TDK, C1005X5R0J105KT
3	1	C3	CAP, CHIP, X5R, 4.7µF, 10%, 6.3V, 0603	TDK, C1608X5R0J475KT
4	1	C4	CAP, CHIP, X5R, 100µF, 20%, 6.3V, 1206	TAIYO YUDEN, JMK316BJ107ML-T
5	1	L1	INDUCTOR, 22µH, 070A, 170mΩ, 5mm × 5mm	COILCRAFT, LPS5030-223MLC
6	0	L1 (OPT)	INDUCTOR, 22µH, 0.70A, 155mΩ, 4.8mm × 4.8mm	WURTH, 744043220
7	2	R1, R2	RES, CHIP, 100k, 1/16W, 1%, 0402	VISHAY, CRCW0402100KFKED
8	1	R3	RES, CHIP, 1MEG, 1/16W, 1%, 0402	VISHAY, CRCW04021M00FKED
9	1 1	U1 (DC1658A-A) U1 (DC1658A-B)	20V HIGH EFFICIENCY NANOPOWER STEP-DOWN REGULATOR 20V HIGH EFFICIENCY NANOPOWER STEP-DOWN REGULATOR	LINEAR TECH., LTC3388EMSE-1 LINEAR TECH., LTC3388EMSE-3
Hardware For Demo Board Only				
1	4	E1, E2, E6, E7	TURRET, 0.09 DIA	MLL-MAX, 2501-2
2	5	E3-E5, E8, E9	TURRET, 0.61 DIA	MLL-MAX, 2308-2
3	5	JP1-JP5	HEADER, 3 PINS, 2mm	SAMTEC, TMM-103-02-LS
4	5	JP1-JP5	SHUNT 2mm	SAMTEC, 2SN-BK-G

SCHEMATIC DIAGRAM



REVISION HISTORY

ECO	REV	DESCRIPTION	APPROVED	DATE
-	2	PRODUCTION FAB	J.DREW	8-23-10

ASSEMBLY TYPE * / OUTPUT VOLTAGE SETTINGS **

	-A				-B			
U1 *	LTC3388-1				LTC3388-3			
VOUT **	1.2V	1.5V	1.8V	2.5V	2.8V	3.0V	3.3V	5.0V
D1	0	0	1	1	0	0	1	1
D0	0	1	0	1	0	1	0	1

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