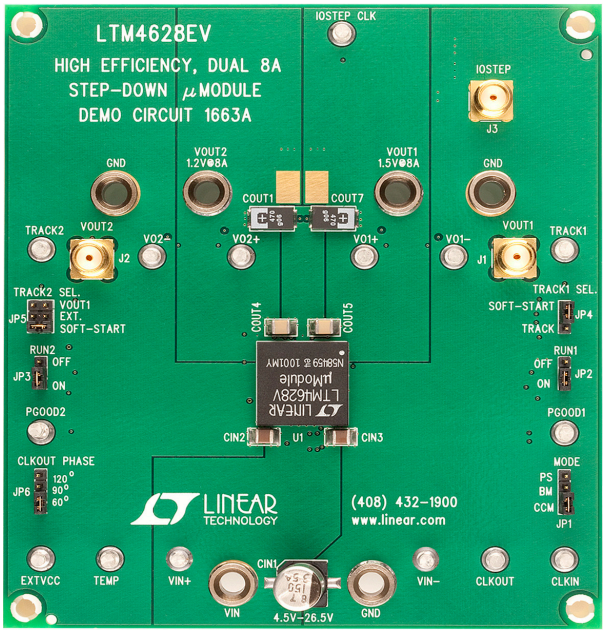
LTM4628EV High Efficiency, Dual 8A Step-Down Power µModule Regulator

DESCRIPTION

Demonstration circuit DC1663A features the LTM®4628EV, the high efficiency, high density, dual 8A output, switch mode step-down power module. The input voltage is from 4.5V to 26.5V. The output voltage is programmable from 0.6V to 5.5V. Output current derating is necessary for certain V_{IN}, V_{OUT}, and thermal conditions. The board operates in continuous conduction mode in heavy load conditions. For high efficiency at low load currents, the MODE jumper (JP1) selects pulse-skipping mode for noise sensitive applications or Burst Mode® operation in less noise sensitive applications. The DC1663A sets the LTM4628EV default switching frequency to 400kHz; however the frequency is resistor programmable from 250kHz up to 780kHz. An internal phase-lock loop allows the module to be synchronized to an external clock. The board allows the user to program how its output ramps up and down through the TRACK/SS pin. The output can be set up to either coincidentally or ratio metrically track with another supply's output. Remote output voltage sensing is available for improved output voltage regulation at the load point. These features and the availability of the LTM4628EV in a compact 15mm × 15mm × 4.32mm LGA package make it ideal for use in many high density point of load regulation applications. The LTM4628 datasheet must be read in conjunction with this demo manual for working on or modifying the demo circuit DC1663A.

Design files for this circuit board are available at http://www.linear.com/demo

BOARD PHOTO



PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Input Voltage Range		4.5V to 26.5V
Output Voltage V_{OUT1}	V_{IN} = 4.5 to 26.5V, I_{OUT1} = 0A to 8A, JP1: CCM	1.5V ± 1.5% (1.4775V to 1.5225V)
Output Voltage V_{OUT2}	V_{IN} = 4.5 to 26.5V, I_{OUT2} = 0A to 8A, JP1: CCM	1.2V ± 1.5% (1.182V to 1.218V)
Per Channel Maximum Continuous Output Current	Derating is Necessary for Certain V_{IN}, V_{OUT} and Thermal Conditions, See Datasheet for Details.	8A
Default Operating Frequency		400kHz
External Clock Synchronous Frequency Range		400kHz to 780kHz
Efficiency of Channel 1	V_{IN} = 5V, V_{OUT1} = 1.5V, I_{OUT1} = 8A, f_{SW} = 400 kHz	87.7% See Figure 2
Efficiency of Channel 2	V_{IN} = 5V, V_{OUT2} = 1.2V, I_{OUT2} = 8A, f_{SW} = 400 kHz	85.5% See Figure 3
Load Transient of Channel 1	V_{IN} = 12V, V_{OUT1} = 1.5V, I_{SETP} = 0A to 4A	See Figure 4
Load Transient of Channel 2	V_{IN} = 12V, V_{OUT2} = 1.2V, I_{SETP} = 0A to 4A	See Figure 5

QUICK START PROCEDURE

Demonstration circuit DC1663A is easy to set up to evaluate the performance of the LTM4628EV. Please refer to Figure 1 for proper measurement equipment setup and the following the procedure:

1. Place jumpers in the following positions for a typical application:

JP1	JP2	JP3	JP4	JP5	JP6
MODE	RUN1	RUN2	TRACK1 SEL.	TRACK2 SEL.	CLKOUT PHASE
CCM	ON	ON	SOFT-START	SOFT-START	60°

2. With power off, connect the input power supply, load and meters as shown in Figure 1. Preset the load to 0A and V_{IN} supply to 12V.
3. Turn on the power supply at the input. The output voltage in channel 1 should be 1.5V ± 1.5% and the output voltage in channel 2 should be 1.2V ± 1.5%.
4. Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, output voltage ripple, efficiency and other parameters. Output ripple should be measured at J1 and J2 with SMA cables. 50Ω termination should be set on the oscilloscope or SMA cables.
5. (Optional) For optional load transient test, apply an adjustable pulse signal between IOSTEP CLK and GND pins. Pulse amplitude (3V to 3.5V) sets the load step current amplitude. The pulse signal should have very small duty cycle (< 10%) to limit the thermal stress on the transient load circuit. The output transient current can be monitored at the SMA connector J3 (15mV/A). Apply the jumper resistors R34 or R35 (on the backside of boards) to apply load transient on channel 1 or channel 2 correspondingly.
6. (Optional) LTM4628 can be synchronized to an external clock signal. Remove the jumper on JP1 and apply a clock signal (0V to 5V, square wave) on the CLKIN test point.
7. (Optional) The outputs of LTM4628 can track another supply. The jumpers JP4 and JP5 allow choosing soft-start or output tracking. If tracking external voltage is selected, the corresponding test points, TRACK1 and TRACK2, need to be connected to a valid voltage signal.
8. (Optional) LTM4628 can be configured for a 2-phase single output at up to 16A on DC1663A. Refer to the schematic for corresponding jumper resistor setup for dual phase single output applications.

QUICK START PROCEDURE

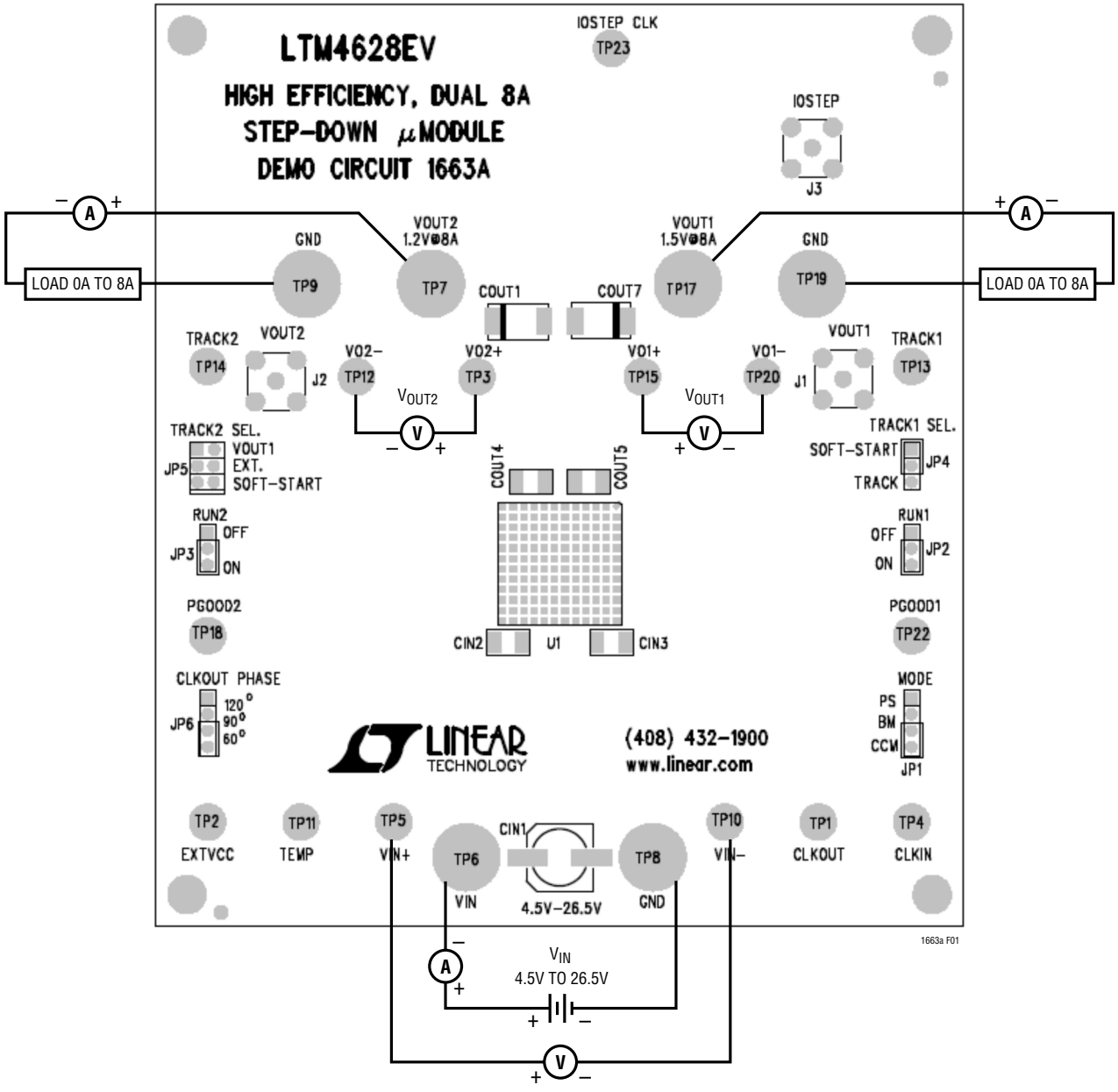


Figure 1. Test Setup of DC1663A

QUICK START PROCEDURE

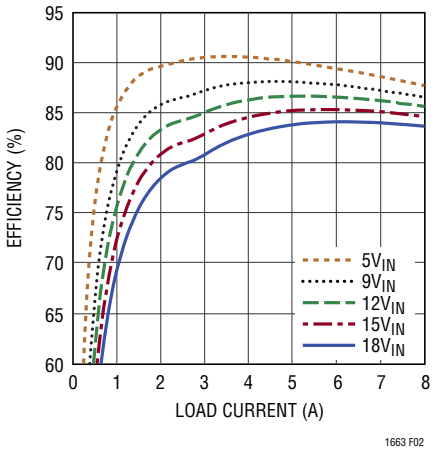


Figure 2. Measured Efficiency on Channel 1 (V_{OUT1} = 1.5V, f_{SW} = 400kHz, Channel 2 Disabled)

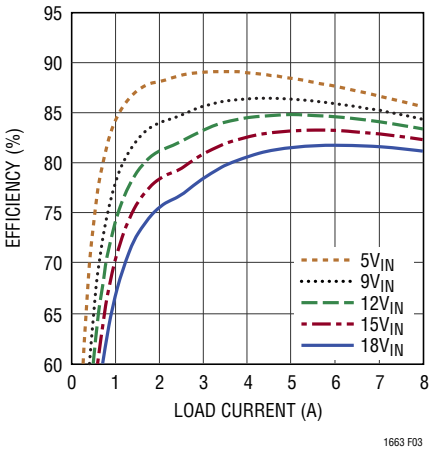


Figure 3. Measured Efficiency on Channel 2 (V_{OUT2} = 1.2V, f_{SW} = 400kHz, Channel 1 Disabled)

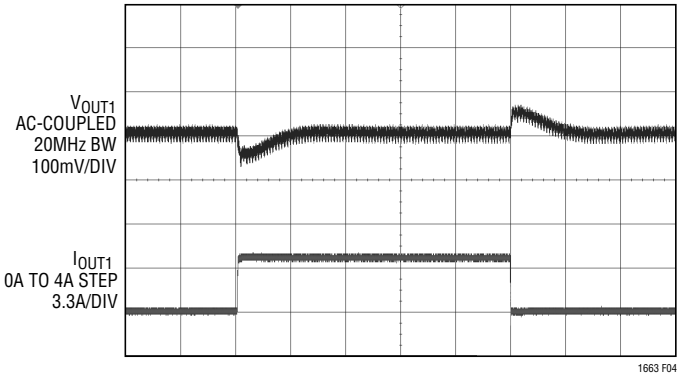


Figure 4. Measured Channel 1 Load Transient (V_{IN} = 12V, V_{OUT1} = 1.5V)

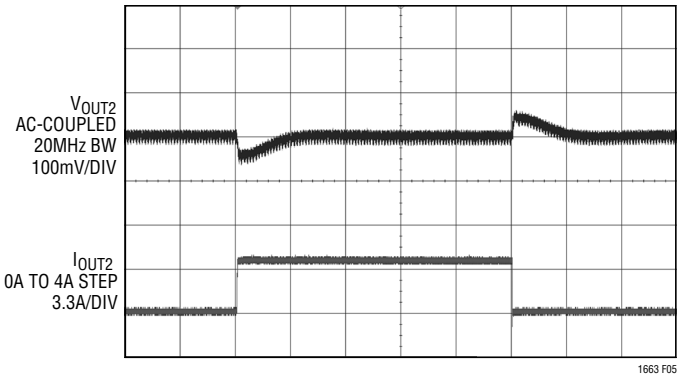


Figure 5. Measured Channel 2 Load Transient (V_{IN} = 12V, V_{OUT2} = 1.2V)

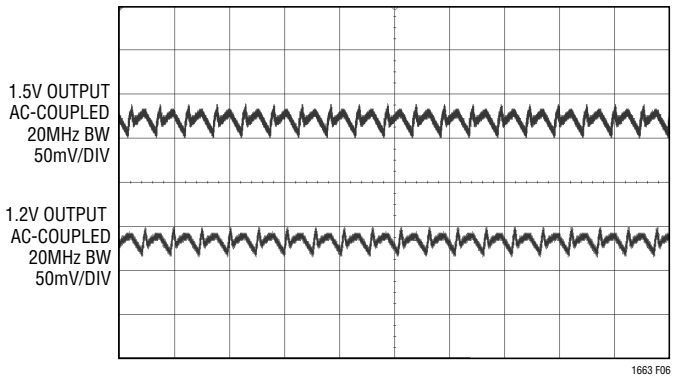
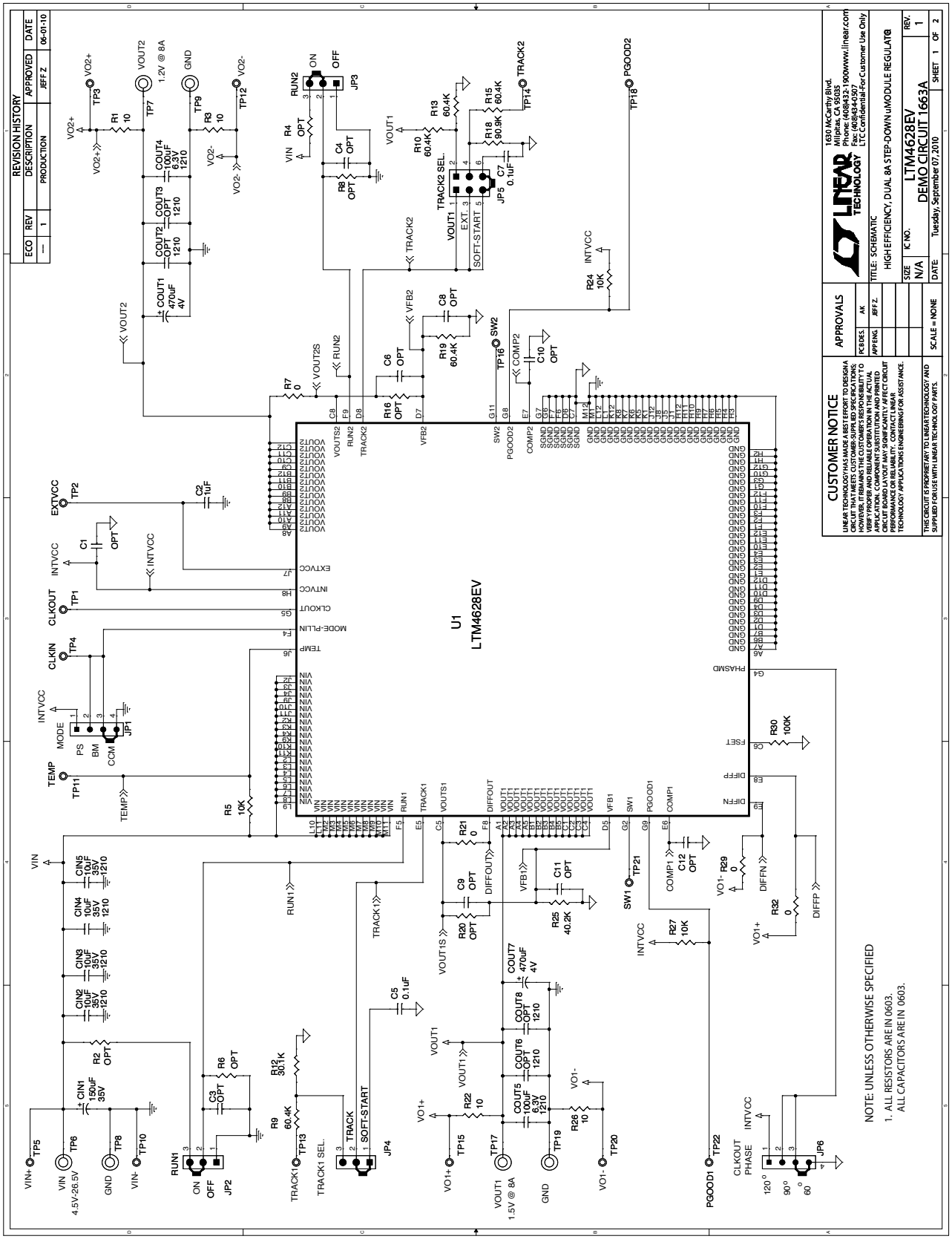


Figure 6. Measured Output Voltage Ripple at 12V Input, 1.5V and 1.2V Output, 8A Per Channel with Standard Demo Circuit Default Setup

PARTS LIST

ITEM	QUANTITY	REFERENCE-DESCRIPTION	DESCRIPTION	MANUFACTURER'S PART NUMBER
Required Circuit Components				
1	4	C_{IN2}, C_{IN3}, C_{IN4}, C_{IN5}	Cap., X5R, 10µF, 35V, 10%, 1210	Murata, GRM32ER6YA106KA12
2	2	C_{OUT1}, C_{OUT7}	Cap., 470µF, 4V, POSCAP, F8	Sanyo, 4TPE470MCL
3	2	C_{OUT4}, C_{OUT5}	Cap., X5R, 100µF, 6.3V, 20%, 1210	AVX, 12106D107MAT2A
4	2	C5, C7	Cap., X5R, 0.1µF, 25V, 10%, 0603	AVX, 06033D104KAT
5	4	R1, R3, R22, R26	Res., Chip, 10, 1%, 0603	NIC, NRC06F10R0TRF
6	1	R19	Res., Chip, 60.4k, 1%, 0603	Vishay, CRCW060360K4FKED
7	1	R25	Res., Chip, 40.2k, 1%, 0603	Vishay, CRCW060340K2FKED
8	1	R30	Res., Chip, 100k, 1%, 0603	Vishay, CRCW0603100KFKED
9	1	U1	IC, High Efficiency Step-Down Module	Linear Technology LTM4628EV
Additional Demo Board Circuit Components				
1	1	C_{IN1}	Cap., 150µF, 35V, Aluminum Electr.,	Sun Electronics, 35CE150AX
2	0	C_{OUT2}, C_{OUT3}, C_{OUT6}, C_{OUT8}	Cap., X5R, 100µF, 6.3V, 20% 1210 Optional	AVX, 12106D107MAT2A Optional
3	0	C1	Cap., X7R, 1µF, 25V,10%, 0805 Optional	AVX, 08053C105KAT2A Optional
4	1	C2	Cap., X7R, 1µF, 25V,10%, 0805	AVX, 08053C105KAT2A
5	0	C3, C4, C6, C8 to C12	Cap., 0603, Optional	Optional
6	0	R2, R4, R6, R8, R16, R20, R40	Res., 0603, Optional	Optional
7	0	R11, R14, R17, R23, R28, R31, R33, R39	Res., Chip, 0, 1%, 0603, Optional	Vishay, CRCW06030000Z0ED, Optional
8	4	R5, R24, R27, R36	Res., Chip, 10k, 1%, 0603	Vishay, CRCW060310K0FKED
9	2	C13, C14	Cap., X7R, 0.01µF, 16V, 10%, 0603	AVX, 0603YC103KAT2A
10	2	C15, C16	Cap., X7R, 1µF, 10V, 10%, 0603	AVX, 0603ZC105KAT
11	4	R7, R21, R29, R32	Res., Chip, 0, 1%, 0603	Vishay, CRCW06030000Z0ED
12	4	R9, R10, R13, R15	Res., Chip, 60.4k, 1%, 0603	Vishay, CRCW060360K4FKED
13	1	R12	Res., Chip, 30.1k, 1%, 0603	Vishay, CRCW060330R1FKED
14	1	R18	Res., Chip, 90.9k, 1%, 0603	Vishay, CRCW060390K9FKED
15	1	R34	Res., Chip, 0.001Ω, 0.5W, 2010	Vishay, WSL20101L000FEA
16	0	R35	Res., 2010, Optional	Optional
17	1	R37	Res., Chip, 0.015Ω, 2W, 2512	Vishay, WSL2512R0150FEA
18	0	R38	Res., 2512, Optional	Optional
19	1	Q1	N-Channel 30-V MOSFET	Vishay, SUD50N03-09P
20	10	TP1 to TP5, TP10 to TP15	Testpoint, Turret, .094" pbf	Mill-Max, 2501-2-00-80-00-00-07-0
21	4	TP18, TP20, TP22, TP23	Testpoint, Turret, .094" pbf	Mill-Max, 2501-2-00-80-00-00-07-0
22	6	TP6, TP7, TP8, TP9, TP17, TP19	Jack Banana	Keystone, 575-4
Hardware - for Demo Board Only				
1	2	JP1, JP6	Header 4 Pin 0.079 Single Row	Samtec, TMM104-02-L-S
2	3	JP2, JP3, JP4	Header 3 Pin 0.079 Single Row	Samtec, TMM103-02-L-S
3	1	J5	Header 3 Pin 0.079 Double Row	Samtec, TMM-103-02-L-D
4	6	XJP1 to XJP6	Shunt, .079" Center	Samtec, 2SN-BK-G
5	3	J1, J2, J3	CON., SMA , PCB, Jack	Amphenol Connex, 132134
6	4	Stand-Off	Stand-Off, Nylon 0.50"	Keystone, 8833 (Snap On)

SCHEMATIC DIAGRAMS



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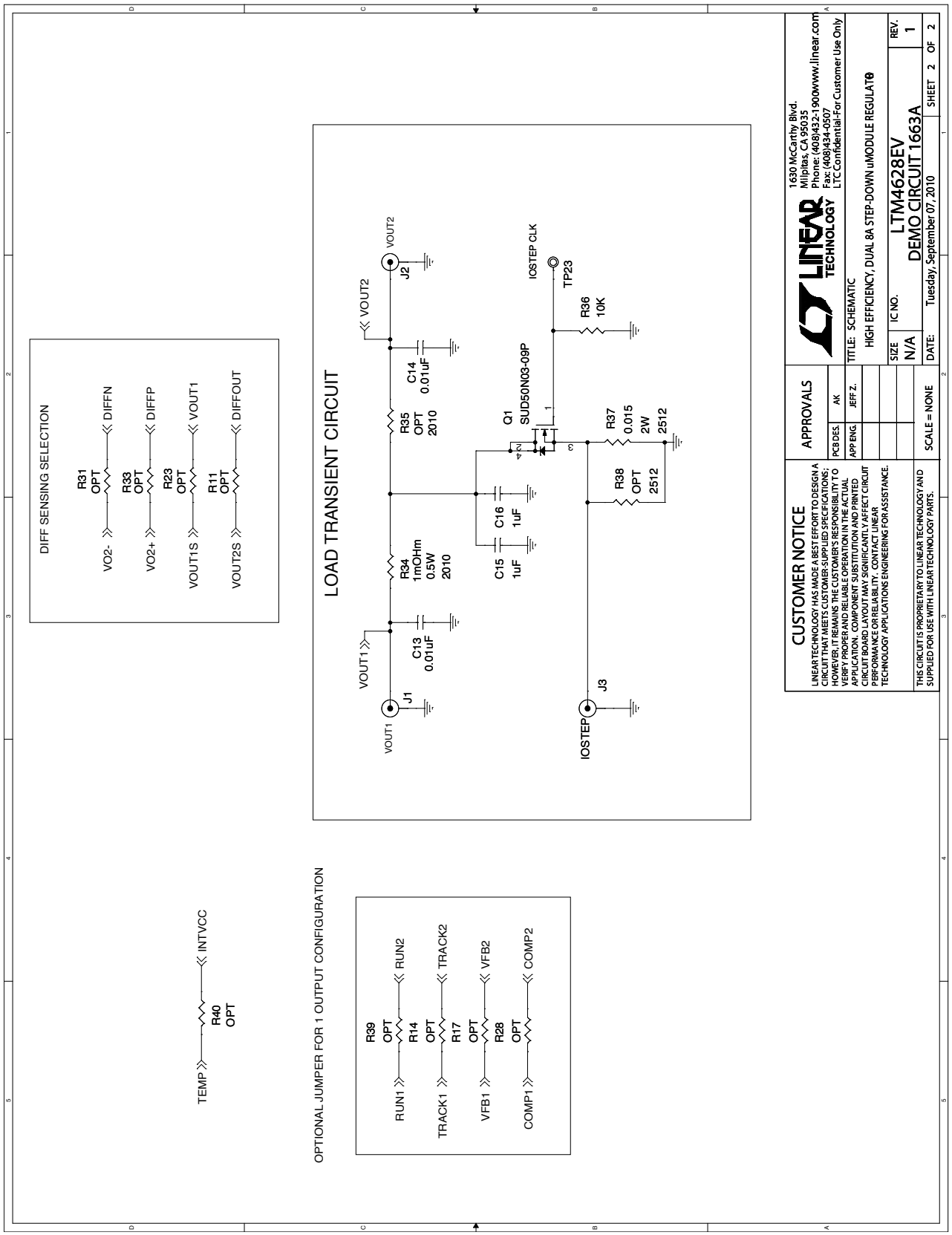

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