# LTM9012
# 14-Bit, 125Msps Quad ADC with Integrated Drivers

## DESCRIPTION

Demonstration circuit DC1732 supports the LTM®9012 high speed, quad ADC modules.

The versions of the 1732B demo board are listed in Table 1. Depending on the required resolution and sample rate, the DC1732 is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for full bandwidth. Refer to the data sheet for proper input networks for different input frequencies.

**Design files for this circuit board are available at http://www.linear.com/demo**



**Table 1. DC1732 Variants**

| DC1732 VARIANTS | ADC PART NUMBER | RESOLUTION | MAXIMUM SAMPLE RATE | INPUT RANGE* |
|---|---|---|---|---|
| 1732B-AB | LTM9012-AB | 14-BIT | 125 Msps | $220mV_{P-P}$ |

*With SENSE pin tied to 1.8V.

## PERFORMANCE SUMMARY ($T_A$ = 25°C)

| PARAMETER | CONDITION | VALUE |
|---|---|---|
| Supply Voltages – DC1732B | Depending on Sampling Rate, This Supply Must Provide Up to 700mA. | 3V to 6V, 5V to 6V |
| Analog Input Range | Depending on SENSE Pin Voltage | $110mV_{P-P}$ to $220mV_{P-P}$ |
| Logic Input Voltages | Minimum Logic High | 1.3V |
| | Maximum Logic Low | 0.6V |
| Logic Output Voltages (Differential) | Nominal Logic Levels (100Ω Load, 3.5mA Mode) | 350mV/1.25V Common Mode |
| | Minimum Logic Levels (100Ω Load, 3.5mA Mode) | 247mV/1.25V Common Mode |
| Sampling Frequency (Convert Clock Frequency) | See Table 1 | |
| Encode Clock Level | Single-Ended Encode Mode ($ENC^-$ Tied to GND) | 0V to 3.6V |
| Encode Clock Level | Differential Encode Mode ($ENC^-$ not Tied to GND) | 0.2V to 3.6V |
| Resolution | See Table 1 | |
| Input Frequency Range | See Table 1 | |
| SFDR | See Applicable Data Sheet | |
| SNR | See Applicable Data Sheet | |

## QUICK START PROCEDURE

Demonstration circuit 1732 is easy to set up to evaluate the performance of the LTM9012 modules. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below. Figure 2 shows the pinout of the analog input header.

### Setup

If a DC1371 data acquisition and collection system was supplied with the DC1732 demonstration circuit, follow the DC1371 quick start guide to install the required software and for connecting the DC1371 to the DC1732 and to a PC.

### DC1732 Demonstration Circuit Board Jumpers

The DC1732 demonstration circuit board should have the following jumper settings as default positions. (as per Figure 1)

J2: PAR/SER: Selects parallel or serial programming mode. (default – serial)

*Optional Jumpers*

J1: Term: Enables/disable optional output termination. (default – removed)

J5: ILVDS: Selects either 1.75mA or 3.5mA of output current for the LVDS drivers. (default – removed)

J3: LANE: Selects either 1-lane or 2-lane output modes (default – removed) NOTE: The DC1371 does not support 1-lane operation.

J4: SHDN: Enables and disables the LTM9012. (default – removed)

J10: WP: Enable/disables write protect for the EEPROM. (default – removed)

Note: optional jumper should be left open to ensure proper serial configuration.

### Applying Power and Signals to the DC1732 Demonstration Circuit

The DC1371 is used to acquire data from the DC1732. The DC1371 must FIRST be connected to a powered USB port and have 5V applied power BEFORE applying DC power to the DC1732. DC1732 requires 3V to 6V at TP1 and 5V to 6V at TP4 for proper operation.

The DC1732 demonstration circuit requires up to 700mA depending on the sampling rate and the A/D converter supplied.

The DC1732 should not be removed, or connected to the DC1371 while power is applied.

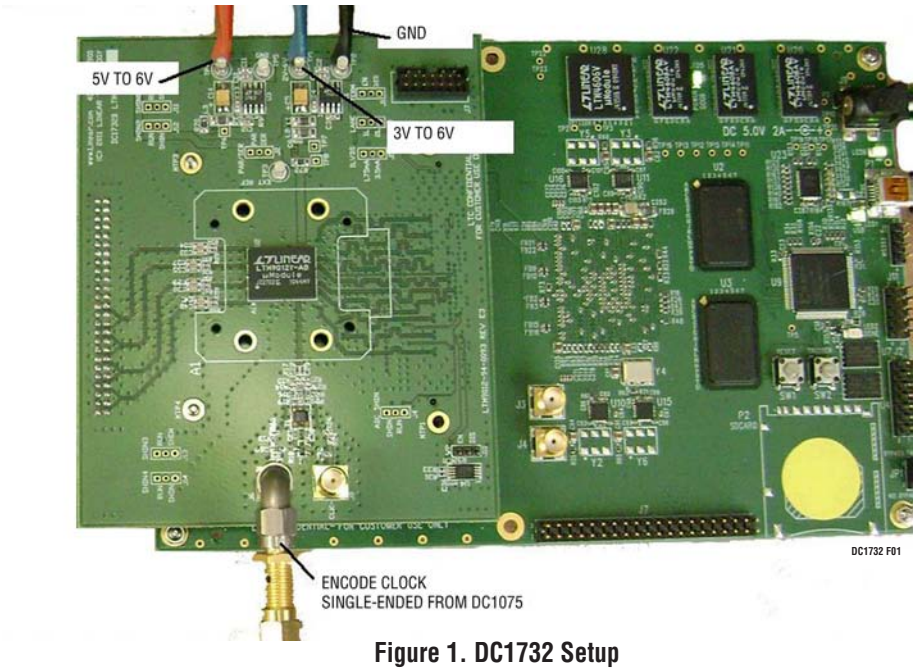



**Figure 1. DC1732 Setup**

## QUICK START PROCEDURE

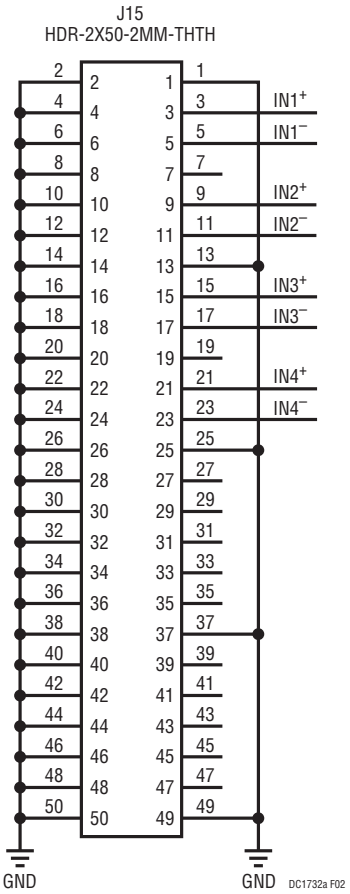



**Figure 2. Pinout for Analog Input Header (J15)**

### Analog Input Network

For optimal distortion and noise performance the RC network on the analog inputs may need to be optimized for different analog input frequencies. For full bandwidth operation, no series RC elements should be used.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full-scale signals without distortion, you may benefit from a medium power amplifier based on a gallium arsenide gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and high IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

Apply the analog input signal of interest to the header on the DC1732 demonstration circuit board marked “J15”. There is access to the eight analog inputs. For a pin out of this header see Figure 2 in this quick start guide, or the attached schematic.

### Encode Clock

NOTE: Apply an encode clock to the SMA connector on the DC1732 demonstration circuit board marked “J11 CLK+”. As a default the DC1732 is populated to have a single-ended input.

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter, square wave source. The amplitude should be large, up to $3V_{P-P}$ or 13dBm. When using a sinusoidal signal generator a squaring circuit can be used. Linear Technology also provides demo board DC1075A that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTM9012.

Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1732 a bandpass filter used for the clock should be used prior to the DC1075A. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used for both the clock input and the analog input.

### Digital Outputs

Data outputs, data clock, and frame clock signals are available on J9 of the DC1732. This connector follows the VITA-57/FMC standard, but all signals should be verified when using an FMC carrier card other than the DC1371.

## QUICK START PROCEDURE

### Software

The DC1371 is controlled by the PScope system software provided or downloaded from the Linear Technology website at http://www.linear.com/software/.

To start the data collection software if "PScope.exe", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1732 demonstration circuit is properly connected to the DC1371, PSCOPE should automatically detect the DC1732, and configure itself accordingly.

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC1371 quick start guide and in the online help available within the PScope program itself.

### Serial Programming

PScope has the ability to program the DC1732 board serially through the DC1371. There are several options available in the LTM9012 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the "Set Demo Bd Options" icon on the PScope toolbar (Figure 3).

This will bring up the menu shown in Figure 4.

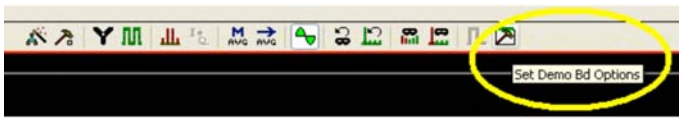



**Figure 3. PScope Toolbar**

This menu allows any of the options available for the LTM9012 family to be programmed serially. The LTM9012 family has the following options:

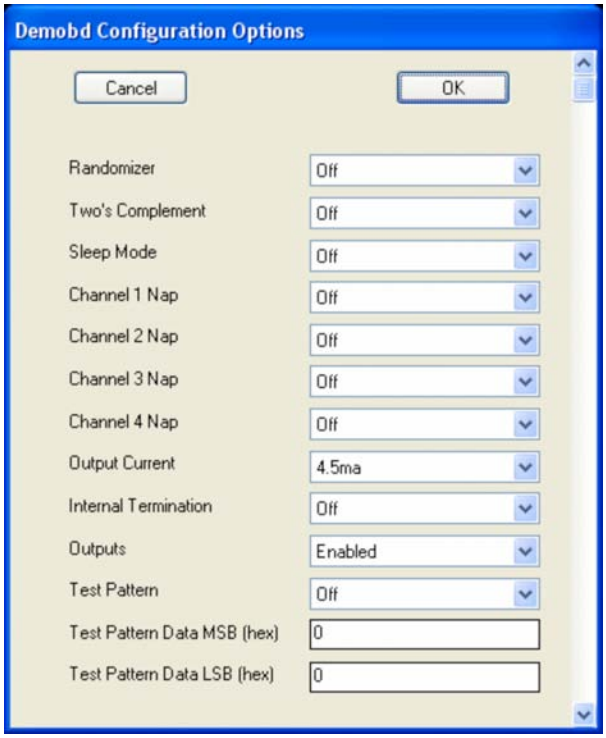



**Figure 4. Demobd Configuration Options.**

**Randomizer:** Enables data output randomizer

Off (default): Disables data output randomizer

On: Enables data output randomizer

**Two's Complement:** Enables two's complement mode

Off (default): Selects offset binary mode

On: Selects two's complement mode

**Sleep Mode:** Selects between normal operation, sleep mode:

Off (default): Entire ADC is powered, and active

On: The entire ADC is powered down.

**Channel 1 Nap:** Selects between normal operation and putting channel 1 in nap mode.

Off (default): Channel 1 is active

On: Channel 1 is in nap mode

## QUICK START PROCEDURE

**Channel 2 Nap:** Selects between normal operation and putting channel 2 in nap mode.

Off (default): Channel 2 is active

On: Channel 2 is in nap mode

**Channel 3 Nap:** Selects between normal operation and putting channel 3 in nap mode.

Off (default): Channel 3 is active

On: Channel 3 is in nap mode

**Channel 4 Nap:** Selects between normal operation and putting channel 4 in nap mode.

Off (default): Channel 4 is active

On: Channel 4 is in nap mode

**Output Current:** Selects the LVDS output drive current

1.75mA (default): LVDS output driver current

2.1mA: LVDS output driver current

2.5mA: LVDS output driver current

3.0mA: LVDS output driver current

3.5mA: LVDS output driver current

4.0mA: LVDS output driver current

4.5mA: LVDS output driver current

**Internal Termination:** Enables LVDS internal termination

Off (default): Disables internal termination

On: Enables internal termination

**Outputs:** Enables digital outputs

Enabled (default): Enables digital outputs

Disabled: Disables digital outputs

**Test Pattern:** Selects digital output test patterns. The desired test pattern can be entered into the text boxes provided.

Off (default): ADC input data is displayed

On: Test pattern is displayed

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1732 demo board.

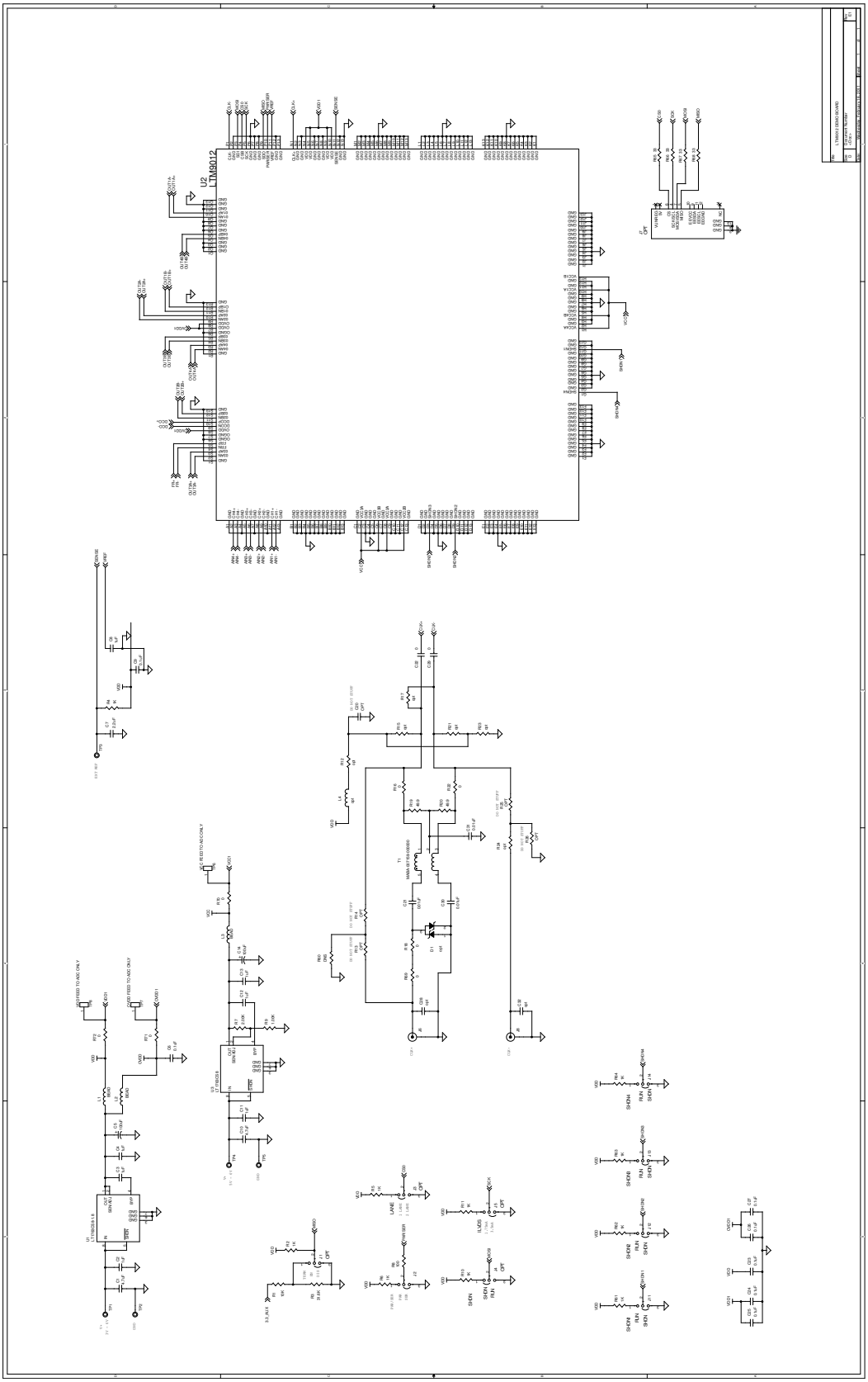
## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|---|---|---|---|---|
| **Required Circuit Components** | | | | |
| 1 | 1 | T1 | BALUN, 1:1, SMT, SM-22 | MACOM MABA-007159-000000 |
| 2 | 6 | C2, C3, C4, C11, C12, C13 | CAP, X5R, 1µF, 10V, 10%, 0603 | AVX 0603ZD105KAT |
| 3 | 1 | C7 | CAP, X5R, 2.2µF, 10V, 10%, 0603 | AVX 0603ZD225KAT |
| 4 | 2 | C5, C14 | CAP, TANT, 100µF, 10V, 10%, C 6032 | VISHAY 293D107X9010C2TE3 |
| 5 | 8 | C33, C34, C35, C37 to C41 | CAP, X7R, 0.01µF, 16V, 10%, 0603 | AVX 0603YC103KAT |
| 6 | 3 | C21, C30, C31 | CAP, X7R, 0.01µF, 16V, 10%, 0402 | AVX 0402YC103KAT |
| 7 | 1 | C8 | CAP, X5R, 1µF, 10V, 10%, 0402 | AVX 0402ZD105KAT |
| 8 | 8 | C6, C9, C23 to C27, C36 | CAP, X5R, 0.1µF, 10V, 10%, 0402 | AVX 0402ZD104KAT |
| 9 | 2 | C1, C10 | CAP, X5R, 4.7µF, 10V, 10%, 0603 | AVX 0603ZD475KAT |
| 10 | 0 | C20, C28, C32 | CAP, DNI, 0402 | OPT |
| 11 | 0 | D1 | DIODE, DNI, SOT-23 | OPT |
| 12 | 1 | J9 | CONNECTOR, FMC MEZZAININE | SAMTEC ASP-134606-01 |
| 13 | 2 | J6, J8 | CONN, SMA 50Ω PC MOUNT, FEMALE | AMPHENOL 132134 |
| 14 | 10 | J1 to J5, J10, J11, J12, J13, J14 | HEADER, 3 × 1, 2mm | SAMTEC TMM-103-02-L-S |
| 15 | 1 | J15 | HEADER, 2 × 25, 2mm | SAMTEC SQT-125-01-F-D |
| 16 | 1 | J7 | HEADER, 2 × 7, 2mm | MOLEX 87831-1421 |
| 17 | 0 | L4 | IND, DNI, 0603 | OPT |
| 18 | 1 | R69 | RES, 0Ω JUMPER, 0603 | VISHAY CRCW06030000Z0ED |
| 19 | 3 | R70, R71, R72 | RES, 0Ω JUMPER, 0805 | VISHAY CRCW08050000Z0ED |
| 20 | 3 | L1, L2, L3 | IND, BEAD, 1206 | MURATA BL31PG330SN1L |
| 21 | 11 | R2, R4, R5, R6, R9, R10, R11, R61 to R64 | RES, 1k, 1%, 1/16W, 0402 | PANASONIC ERJ-2RKF1001X |
| 22 | 1 | R3 | RES, 31.6k, 1%, 1/16W, 0402 | PANASONIC ERJ-2RKF3162X |
| 23 | 8 | R39 to R46 | RES, 33k, 1%, 1/16, 0402 | PANASONIC ERJ-2RKF3302X |
| 24 | 1 | R7 | RES, 1.74k, 1%, 1/16W, 0402 | PANASONIC ERJ-2RKF1741X |
| 25 | 4 | R65, R66, R67, R68 | RES, 33.0, 1%, 1/16W, 0402 | PANASONIC ERJ-2RKF33R0X |
| 26 | 4 | R1, R31, R32, R33 | RES, 10k, 1%, 1/16, 0402 | PANASONIC ERJ-2RKF1002X |
| 27 | 0 | R12 to R15, R17, R21, R23 to R26, R48 to R56, R60 | RES, DNI, 0402 | OPT |
| 28 | 14 | C22, C29, R16, R18, R22, R29, R34, R36, R37, R38, R47, R57, R58, R59 | RES, 0Ω JUMPER, 0402 | VISHAY CRCW04020000Z0ED |
| 29 | 2 | R19, R20 | RES, 49.9, 1%, 1/16, 0402 | PANASONIC ERJ-2RKF49R9X |
| 30 | 5 | R8, R27, R28, R30, R35 | RES, 100, 1%, 1/16, 0402 | PANASONIC ERJ-2RKF1000X |
| 31 | 5 | TP1, TP2, TP3, TP4, TP5 | TURRET, 0.093 | MILL MAX 2501-2-00-80-00-00-07-0 |
| 32 | 1 | U1 | IC, VREG, 1.8V, 500MA, SO8 | LINEAR TECHNOLOGY LT1763CS8-1.8 |

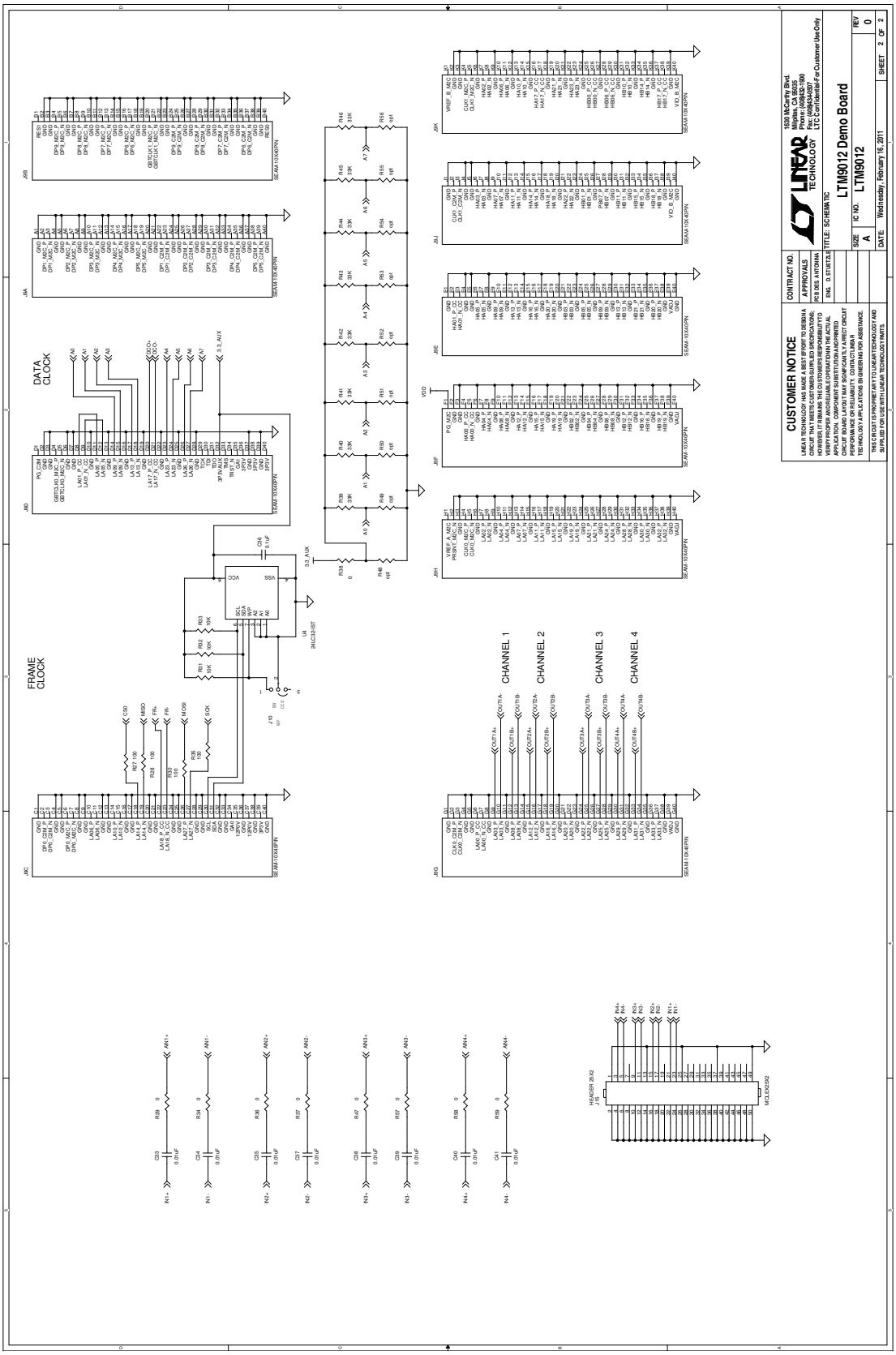
## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|---|---|---|---|---|
| 33 | 1 | U2 | MODULE, LTM9012 | LINEAR TECHNOLOGY LTM9012-AB |
| 34 | 1 | U4 | IC, SERIAL_EEPROM, TSSOP8 | MICROCHIP 24LC32-IST |
| 35 | 1 | U3 | IC, VREG, ADJ, 500MA, SO8 | LINEAR TECHNOLOGY LT1763CS8 |
| 36 | 1 | | STENCIL SET | STENCIL DC1732B |
| 37 | 1 | | FAB, PCB, DC1732B | DEMO CIRCUIT DC1732B |

## SCHEMATIC DIAGRAM



# SCHEMATIC DIAGRAM



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