

LTC3226EUD

2-Cell Supercap Charger With Backup PowerPath Controller

DESCRIPTION

Demonstration circuit DC1735A is a 2-cell supercap charger with a backup PowerPath™ controller, featuring the LTC®3226. It includes a charge-pump supercapacitor charger with programmable output voltage, a low dropout regulator and a power-fail comparator for switching between normal and backup modes. The constant-input current supercapacitor charger is designed to charge two supercapacitors in series to a resistor programmable output voltage from a 2.5V to 5.3V input supply. The charger input current limit is programmable by an external resistor up to 315mA. The internal backup LDO is powered from

the supercapacitors and provides up to 2A peak output current with an adjustable output voltage. When the input supply falls below the resistor programmable power-fail threshold, the LTC3226 automatically enters a backup state in which the supercapacitors power the output through the LDO. The LTC3226 is available in a 16-lead, 3mm × 3mm QFN surface mount package with an exposed pad.

Design files for this circuit board are available at <http://www.linear.com/demo>

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PERFORMANCE SUMMARY Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IN}	Input Voltage Range		2.5		5.5	V
I _{VIN(ILIM)}	Input Current Limit	R _{PROG} = 33.3k		315		mA
V _{STACK}	Supercap Stack Output Voltage	R _{CP1} = 3.83M, R _{CP2} = 1.21M		5.3	5.5	V
V _{MID}	Supercap Midpoint Voltage			2.65	2.75	V

OPERATING PRINCIPLE

The LTC3226 is a 2-cell series supercapacitor charger designed to back up a Li-ion battery or any system rail in the range of 2.5V to 5.3V. Its four principle circuit components are:

1. Dual (1×/2×) charge pump with an integrated balancer and a voltage clamp
2. LDO to supply the load current from the charge stored on the supercapacitors
3. Ideal diode controller to control the gate of the external MOSFET between V_{IN} and V_{OUT}
4. PFI comparator to decide whether to activate the charge pump to charge the supercapacitor stack or to activate the LDO to supply the load when V_{IN} falls below an externally programmed value.

The LTC3226 has two modes of operation: normal and backup. If V_{IN} is above an externally programmable PFI threshold voltage, the part is in normal mode and power flows from V_{IN} to V_{OUT} through the external MOSFET while the internal charge pump charges the supercapacitor stack (see Figure 1). If V_{IN} is below the PFI threshold, the part is in backup mode (see Figure 2). In this mode, the internal charge pump is turned off and the LDO is turned on to supply the load current from the stored charge on the supercapacitor stack.

The device includes three open-drain, output status signals: CAPGOOD, $\overline{\text{PFO}}$ and $\overline{\text{RST}}$. The CAPGOOD pin is an open-drain N-channel MOSFET transistor controlled by a comparator that monitors the voltage on the supercapaci-

dc1735Af

OPERATING PRINCIPLE

tor stack. This pin is pulled to ground until the CPO pin voltage rises within 7.5% of the programmed value. Once the CPO pin is above this threshold, the CAPGOOD pin goes high impedance. The output of the PFI comparator also drives the gate of an open-drain N-channel MOSFET to report the status via the $\overline{\text{PFO}}$ pin. In normal mode the $\overline{\text{PFO}}$ pin is high impedance, but in backup mode the pin is pulled down to ground. The LTC3226 contains a RESET

comparator which monitors V_{OUT} under all operating modes via the RST_FB pin and reports the status via an open-drain NMPS transistor on the $\overline{\text{RST}}$ pin. At any time, if V_{OUT} falls below 7.5% from its programmed value, it pulls the $\overline{\text{RST}}$ pin low almost instantaneously.

However, on the rising edge, the comparator waits 290ms after V_{OUT} crosses the threshold voltage before making the $\overline{\text{RST}}$ high impedance.

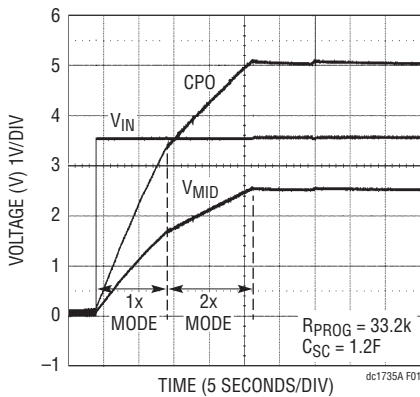


Figure 1. Charge Profile with Equal Value Supercapacitors

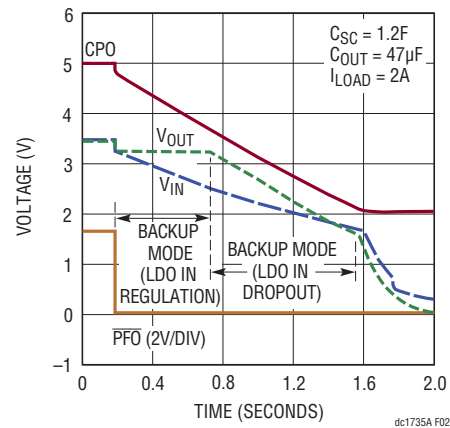


Figure 2. Normal-to-Backup Mode Switchover

QUICK START PROCEDURE

Refer to Figure 3 for the proper measurement equipment setup and jumper settings, and follow the procedure below.

NOTE. When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the V_{IN} or V_{OUT} and GND terminals. See Figure 4 for the proper scope probe technique.

1. Initial jumper, power supply and load settings:

JP1 = EN	Power Supply = OFF
JP2 = 110mA	Load = Off
JP3 = 110mA	Pulse Generator = OFF

2. Connect the power supply to the V_{IN} terminals, turn the power supply on, and increase the voltage to 2V while monitoring the input current. If the input current is less than 5mA, increase the voltage until the point at which $\overline{\text{PFO}}$ goes high. Verify that V_{IN} is between 3.53V and 3.65V, the input current is approximately 320mA, the output voltage is approximately equal to the input voltage and the voltage on the CPO pin is rising.
3. Monitor the voltage on CPO and CAPGOOD. Verify that CAPGOOD goes high when CPO is at 4.6V and that CPO charges between 4.83V and 5.23V. Verify that V_{MID} is one-half of CPO. Verify that $\overline{\text{RST}}$ is high.

QUICK START PROCEDURE

- Turn on the load and increase the current to 2A. Verify that V_{OUT} is within 50mV of V_{IN} .
- Decrease the power supply to 3V and quickly observe that V_{OUT} is between 3.12V and 3.47V, PFI is low, RST is high and the voltage on CPO is falling. Increase V_{IN} to 3.6V and verify that the voltage on CPO starts to rise again. Let the voltage on CPO rise beyond where CAPGOOD goes high.
- Turn off the power supply and observe that V_{OUT} remains between 3.12V and 3.47V for greater than 700ms, and that V_{OUT} then falls, tracking CPO until V_{OUT} reaches 2.4V. Verify that \overline{RST} is low.
- Disconnect the power supply from the V_{IN} terminals, turn down the voltage to 0V and connect the power supply between the CPO and ground terminals. Slowly increase the voltage to 5V and verify that V_{OUT} is between 3.12V and 3.47V. Increase the load on V_{OUT} to 1A. Set up the pulse generator for an output voltage peak of 10V, a pulse with 1ms pulse width and a period of 20ms. Connect the pulse generator to the pulse generator terminals and observe the transient response on the V_{OUT} terminals. Verify that the negative transition of V_{OUT} is less than 75mV and that it recovers within 100 μ s.

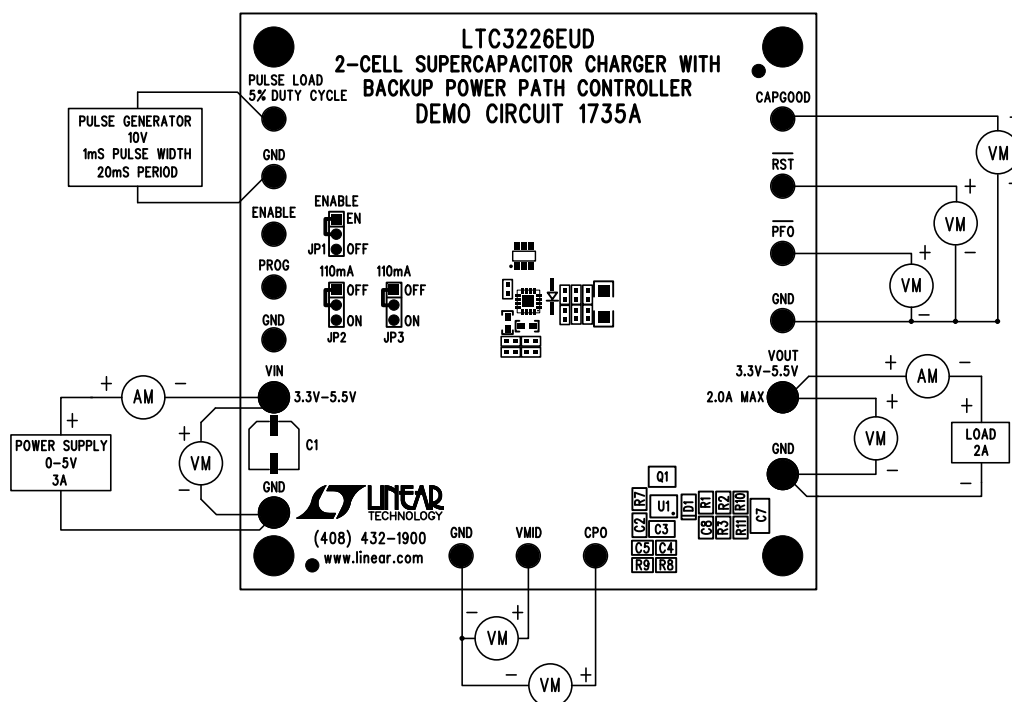
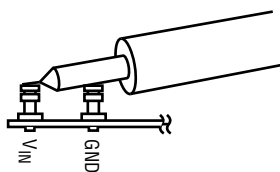


Figure 3. Proper Measurement Equipment Setup for DC1735A



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Figure 4. Measuring Input or Output Ripple

DEMO MANUAL DC1735A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	C2	Cap., Chip, X5R, 4.7 μ F, 10%, 6.3V, 0603	Murata, GRM188R60J475KE19D
2	1	C3	Cap., Chip, X5R, 2.2 μ F, 20%, 10V, 0603	Murata, GRM188R61A225KE34D
3	2	C4, C5	Cap., Chip, X7R, 0.1 μ F, 10%, 16V, 0402	Murata, GRM155R71C104KA88D
4	1	C6	Supercap, 1.2 μ F, 5.5V, 39mm \times 17mm	CAP-XX, HS230F
5	1	C7	Cap., Chip, X5R, 47 μ F, 20%, 6.3V, 1206	Murata, GRM31CR60J476ME19L
7	1	R2	Res., Chip, 210k, 1/16W, 1%, 0402	Vishay, CRCW0402210KFKED
8	1	R3	Res., Chip, 121k, 1/16W, 1%, 0402	Vishay, CRCW0402121KFKED
9	1	R7	Res., Chip, 100k, 1/16W, 1%, 0402	Vishay, CRCW0402100KFKED
10	1	R8	Res., Chip, 3.83M, 1/16W, 1%, 0402	Vishay, CRCW04023M83FKED
11	1	R9	Res., Chip, 1.21M, 1/16W, 1%, 0402	Vishay, CRCW04021M21FKED
12	1	R10	Res., Chip, 255k, 1/16W, 1%, 0402	Vishay, CRCW0402255KFKED
13	1	R11	Res., Chip, 80.6k, 1/16W, 1%, 0402	Vishay, CRCW040280K6FKED
14	1	Q1	MOSFET, -20V, 33m Ω , -5.5A, SUPERSOT-6	Fairchild, FDC604P
15	1	U1	2-Cell Supercapacitor Charger with Backup PowerPath Controller	Linear Technology, LTC3226EUD
Additional Circuit Components				
1	1	C1	Cap., SMD, OSCON, 220 μ F, 20%, 6.3V, 6.3mm \times 6mm	Sanyo, 6VPE220M
2	0	C8 (OPT)	Cap., Chip, 0402	
3	1	D1	SMD, Switching Diode, SOD323	Vishay, 1N4148WS-V-GS08
4	1	R1	Res., Chip, 1M, 1/16W, 1%, 0402	Vishay, CRCW04021M00FKED
5	1	R4	Res., Chip, 10k, 1/16W, 1%, 0402	Vishay, CRCW040210K0FKED
6	3	R5, R6, R16	Res., Chip, 100k, 1/16W, 1%, 0402	Vishay, CRCW0402100KFKED
7	3	R12 to R14	Res., Chip, 475k, 1/16W, 1%, 0402	Vishay, CRCW0402475KFKED
8	1	R15	Res., Chip, 1k, 1/16W, 1%, 0402	Vishay, CRCW04021K00FKED
9	2	R17, R18	Res., Chip, 6.65 Ω , 1/4W, 1%, 1206	Vishay, CRCW12066R65FKED
10	1	Q2	MOSFET, 30V, 65m Ω , 3.5A, SOT-23	Vishay, Si2306BDS
Hardware for Demo Board Only				
1	4	E1, E2, E8, E9	Turret, 0.09 DIA	Mill-Max, 2501-2
2	12	E3 to E7, E10 to E16	Turret, 0.061 DIA	Mill-Max, 2308-2
3	3	JP1 to JP3	Header, 3 Pins, 2mm	Samtec, TMM-103-02-L-S
4	3	JP1 to JP3	Shunt 2mm	Samtec, 2SN-BK-G
5	4		Stand-Off, Nylon, 0.375" Tall (Snap On)	Keystone, 8832 (Snap On)

SCHEMATIC DIAGRAM

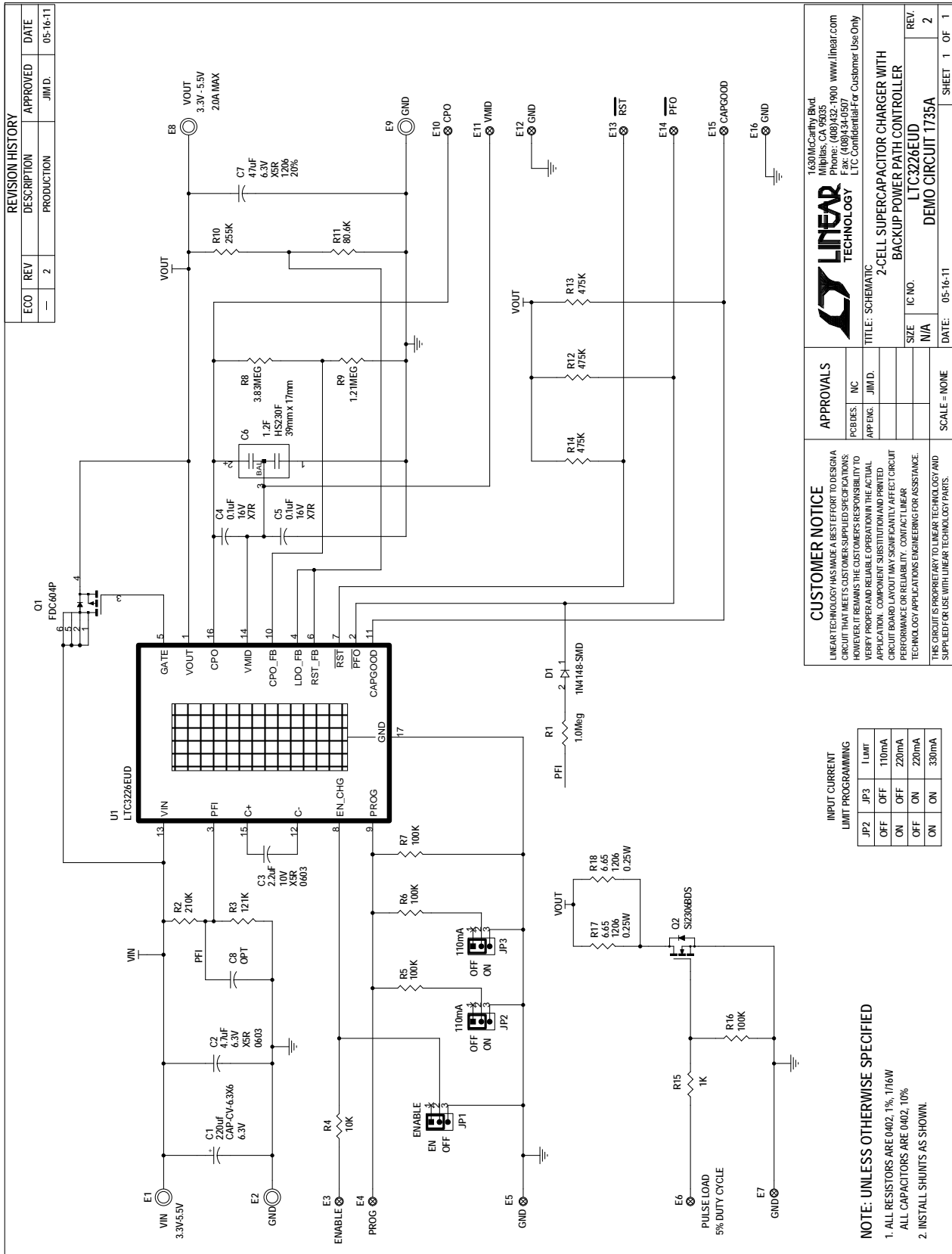


Figure 5. Demo Circuit Schematic

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

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