LTM2881: Isolated RS485/RS422 µModule Transceiver + Power

DESCRIPTION

Demonstration circuit 1746A is an isolated RS485/RS422 µModule® transceiver + power featuring the LTM®2881. The demo circuit is a 2500V_{RMS} galvanically isolated RS485/RS422 transceiver interface. The demo circuit features an EMI optimized circuit configuration and printed circuit board layout. All components are integrated into the µModule transceiver. The demo circuit operates from a single external supply on V_{CC}. The part generates the output voltage V_{CC2} and communicates all necessary signaling across the isolation barrier using LTC's isolator µModule technology.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Input Supply Range	LTM2881-5 LTM2881-3	4.5 3.0	5 3	5.5 3.6	V V
V_{CC2}	Output Voltage	I_{LOAD} = 0mA to 100mA, DE = 0V	4.7	5		V
f_{MAX}	Maximum Data rate	$\overline{SLO}$ = V_{CC2}	20			Mbps
V_{IORM}	Maximum Working Insulation Voltage	GND to GND2	560 400			V_{DC} V_{RMS}
	Common Mode Transient Immunity		30			kV/µs

OPERATING PRINCIPLES

The LTM2881 contains an isolated DC/DC converter, delivering power to V_{CC2} at 5V from the input supply, V_{CC}. Isolation is maintained by the separation of GND and GND2 where significant operating voltages and transients can exist without affecting the operation of the LTM2881. The logic side ON pin enables or shuts down the LTM2881. RS485/RS422 signaling is controlled by the logic inputs DE, DI, TE and $\overline{RE}$. Connection to the transceiver pins (A, B, Y and Z) allows full- or half-duplex operation on the isolated side of the demo circuit. A full-/half-duplex switch is included on the demo circuit to ease setting the system configuration. The $\overline{SLO}$ pin configures the slew rate of the driver output pins Y and Z.

Data is transmitted out the driver pins Y and Z from the input DI with DE set on. Data is received through the difference in A and B to the output RO with $\overline{RE}$ set on.

The demo circuit has been designed and optimized for low RF emissions. To this end some features of the LTM2881 are not available for evaluation on the demo circuit. The logic supply voltage, V_L, is tied to V_{CC} on the demo circuit. All control signals are selectable by jumper programming only, including ON, $\overline{RE}$, DE, TE and $\overline{SLO}$. The spare logic channel D_{IN} to D_{OUT} is not available.

OPERATING PRINCIPLES

EMI mitigation techniques used include the following:

1. Four layer PCB, allowing for isolated side to logic side 'bridge' capacitor. The bridge capacitor is formed between an inner layer of floating copper which overlaps the logic side and isolated side ground planes. This structure creates two series capacitors, each with approximately 0.008" of insulation, supporting the full dielectric withstand rating of $2500V_{RMS}$. The bridge capacitor provides a low impedance return path for injected currents due to parasitic capacitances of the LTM2881's signal and power isolating elements.
2. Discrete bridge capacitors (C3, C4) mounted between GND2 and GND. The discrete capacitors provide additional attenuation at frequencies below 400MHz. Capacitors are safety rated type Y2, manufactured by Murata, part # GA342QR7GF471KW01L.
3. Board/ground plane size has been minimized. This reduces the dipole antenna formed between the logic side and isolated side ground planes.
4. Top signal routing and ground floods have been optimized to reduce signal loops, minimizing differential mode radiation.
5. Common mode filtering is integrated into the input pin header and output DB9 connector. Filtering helps to reduce emissions caused by conducted noise and minimizes the effects of cabling to common mode emissions.
6. A combination of low ESL and high ESR decoupling is used. A low ESL ceramic capacitor is located close to the module minimizing high frequency noise conduction. High ESR tantalum capacitors are included to minimize board resonances and prevent voltage spikes due to hot plugging of the input supply voltage.

EMI performance is shown in Figure 1, measured using a gigahertz transverse electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, "Testing and Measurement Techniques—Emission and Immunity Testing in Transverse Electromagnetic Waveguides".

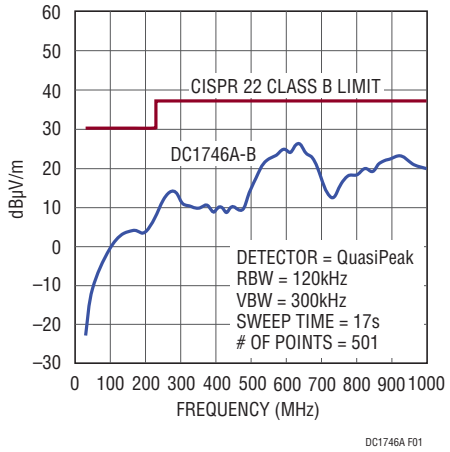


Figure 1. DC1746A Radiated Emissions

QUICK START PROCEDURE

Demonstration circuit 1746A is easy to set up and evaluate the performance of the LTM2881. Refer to Figure 2 for proper measurement equipment setup and follow the procedure below.

NOTE: When measuring the input or output voltage ripple or high speed signals, care must be taken to avoid a long ground lead on the oscilloscope probe.

1. Install jumpers in following positions: (all are default except JP5 and SW1)

   JP1 ON

   JP2 ON

   JP3 ON

   JP4 ON

   JP5 OFF

   SW1 HALF DUPLEX

2. With power off, connect the input power supply to V_{CC} and GND on pin header J1.

3. Turn on the power at the input.

   NOTE: Make sure that the input voltage does not exceed 6V.

4. Check for the proper output voltage. V_{CC2} = 5V, this can be measured between probe points V2 and C.

5. Once the proper output voltage is established, connect a function generator to pin DI and set to square wave with a low of 0V, high = V_{CC}. Set frequency to 10MHz (20Mbps). Enable output of function generator.

6. Connect oscilloscope to pin RO and observe 10MHz waveform. This demonstration shows data that is transmitted from DI, loops back through half-duplex connection, and out of RO.

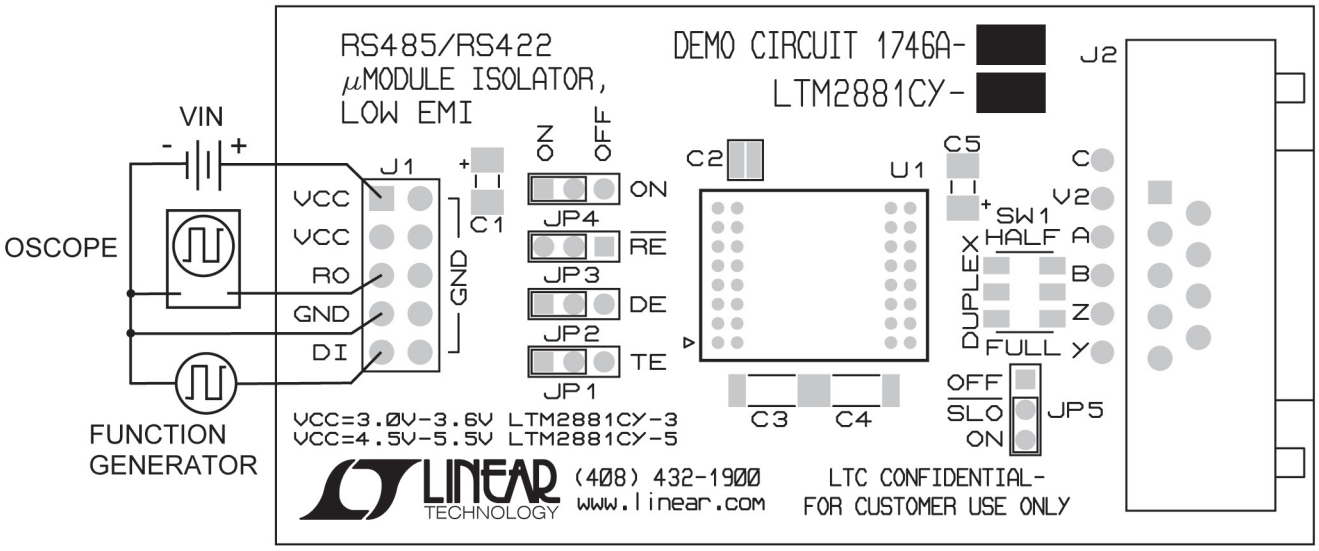
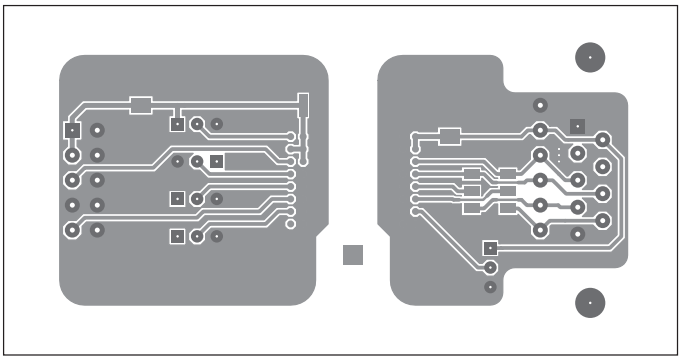
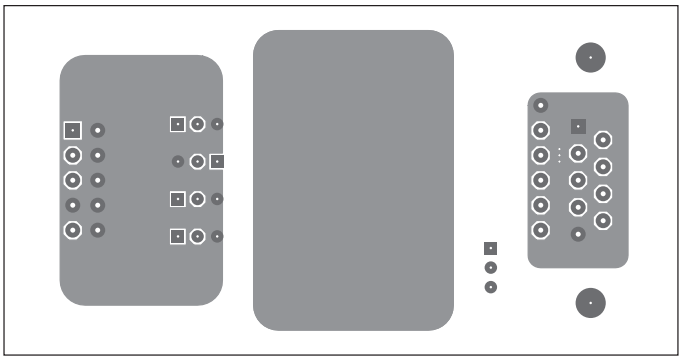


Figure 2. Demo Board Setup

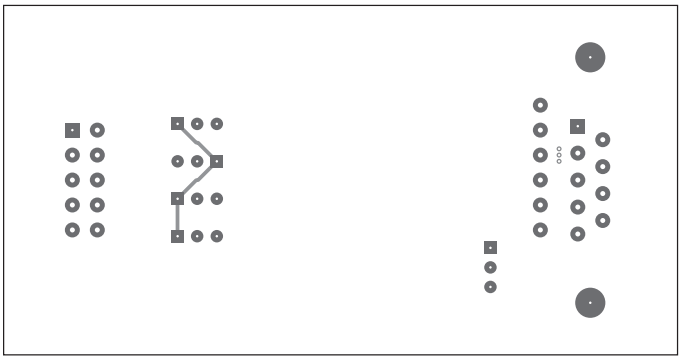
PCB LAYOUT



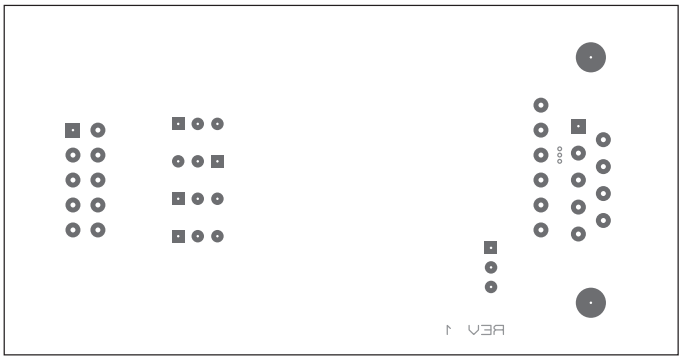
Layer 1. Top Layer



Layer 2. Ground Plane



Layer 3. Signal Layer

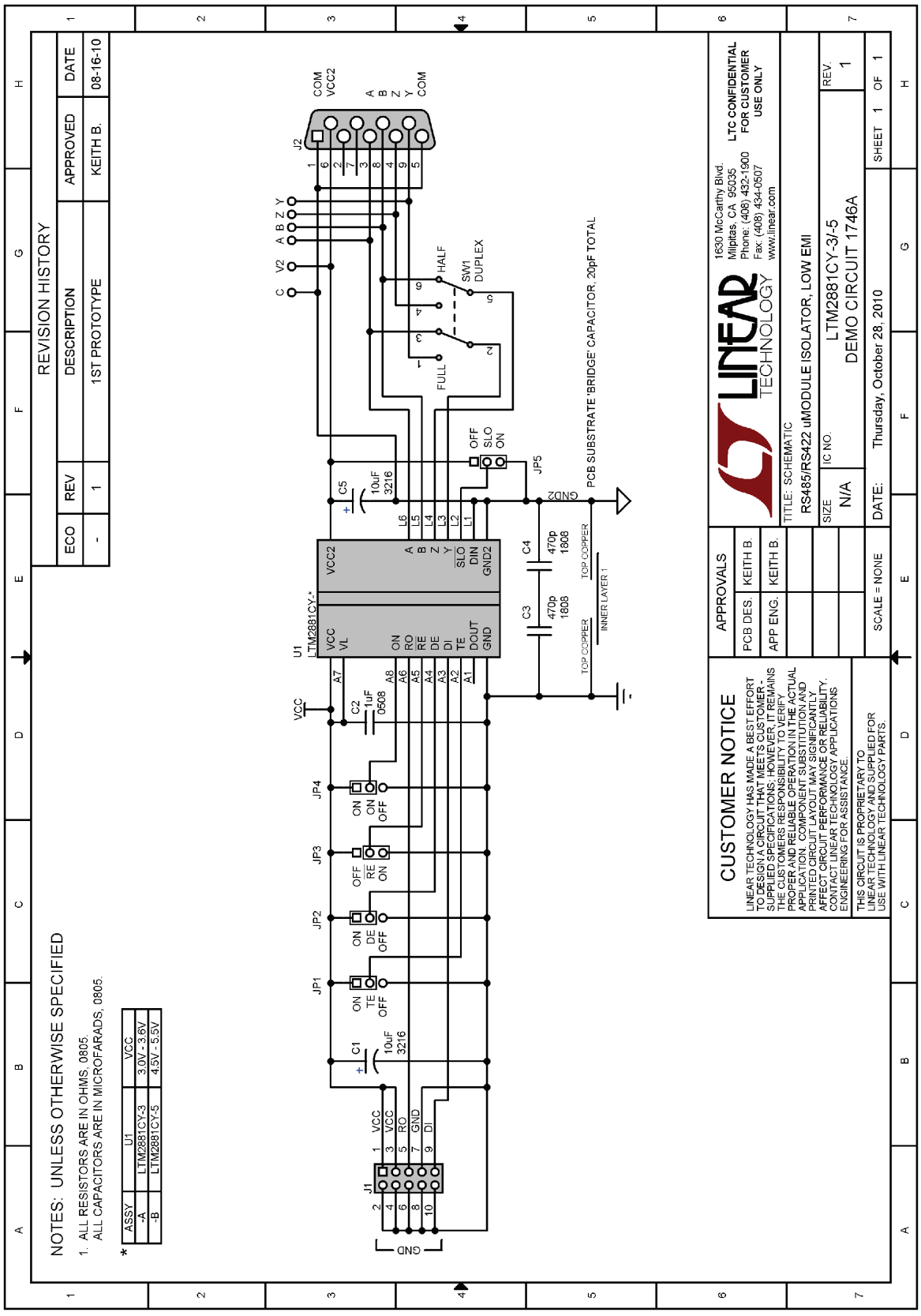


Layer 4. Bottom Layer

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	U1	I.C., LTM2881CY-3	LINEAR LTM2881CY-3#PBF
			I.C., LTM2881CY-5	LINEAR LTM2881CY-5#PBF
Hardware/Components (For Demo Board Only)				
2	2	C1, C5	CAP., TANT 10µF 10V 20% TAJA	AVX TAJA106M010RNJ
3	1	C2	CAP., CER 1µF 10V 20% 0508	MURATA LLL219R71A105MA01L
4	2	C3, C4	CAP., CER 470pF 250V_{AC} 10% 1808	MURATA GA342QR7GF471KW01L
5	1	J1	0.1" DOUBLE ROW HEADER, 5 × 2 PIN	SAMTEC TSW-105-22-G-D
6	1	J1	0.1" FERRITE PLATE, 5 × 2 HOLE	FAIR RITE 2644247101
7	1	J2	CON, FILTERED, DSUB 9-PIN	KOBICONN 152-3609
8	5	JP1-5	2mm SINGLE ROW HEADER, 3-PIN	SAMTEC TMM-103-02-L-S
9	5	JP1-5	SHUNT	SAMTEC 2SN-BK-G
10	1	SW1	SWITCH, DPDT, SMD	COPAL CAS-220TA

SCHEMATIC DIAGRAM



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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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