LTC1418 (200ksps) 14-Bit A/D Converter Demo Board

DESCRIPTION

The LTC®1418 is a 4µs, 200ksps sampling A/D converter that draws 15mW. The LTC1418 demo board provides the user with a way to evaluate the LTC1418 A/D converter. The LTC1418 is equipped to handle serial or parallel data transfer. The demo board allows the user to select the desired interface. In addition, the LTC1418 demo board is intended to illustrate the layout and bypassing techniques required to obtain optimum performance from this part. The LTC1418 demo board is designed to be easy to use and requires only ±7V to ±15V supplies, a conversion-start signal and an analog input signal (single-ended or differential). As shown in the Board Photo, the LTC1418 is a very space-efficient solution for A/D users. Combining a 14-bit A/D, sample-and-hold and reference in a single SO package allows all the data acquisition circuitry, including the bypass capacitors, to be placed in an area of only 0.22 inch^2 when operating on split supplies and only 0.2 inch^2 with single-supply operation.

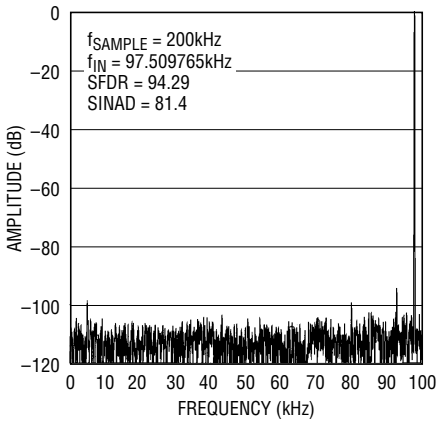
This manual shows how to use the demo board. Included are timing diagrams, power supply requirements and analog input range information. Additionally, a schematic, parts list, drawings and dimensions of all the PC board layers are included. An explanation of the layout and bypass strategies used in this board is also included, so that anyone designing a PC board using the LTC1418 will be able to get the maximum performance from the device. The LTC1418 and its demo board are intended for, but not limited to, signal acquisition and processing, high resolution and industrial data acquisition applications and battery-powered equipment, especially those that benefit from a ±2.048V input range. **Gerber files for this circuit board are available. Call the LTC factory.**

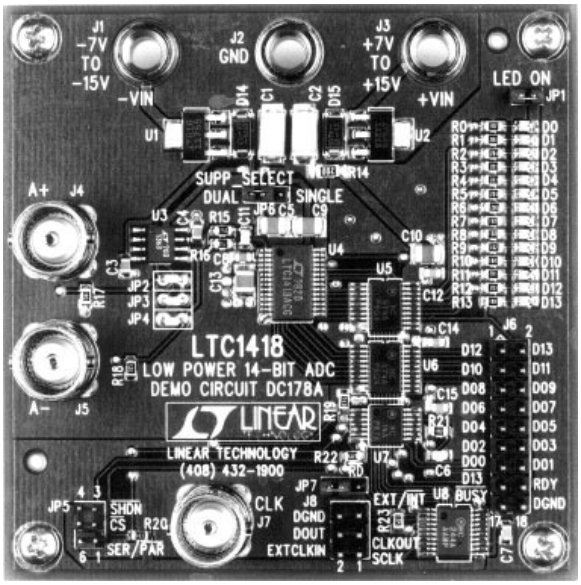
Some key features of this demo board include:

- Proven 200ksps 14-bit ADC surface mount layout
- Actual ADC footprint is only 0.22 inch^2 including bypass capacitors
- 81.5dB SINAD and –94dB THD with a 100kHz full-scale sine wave input

TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

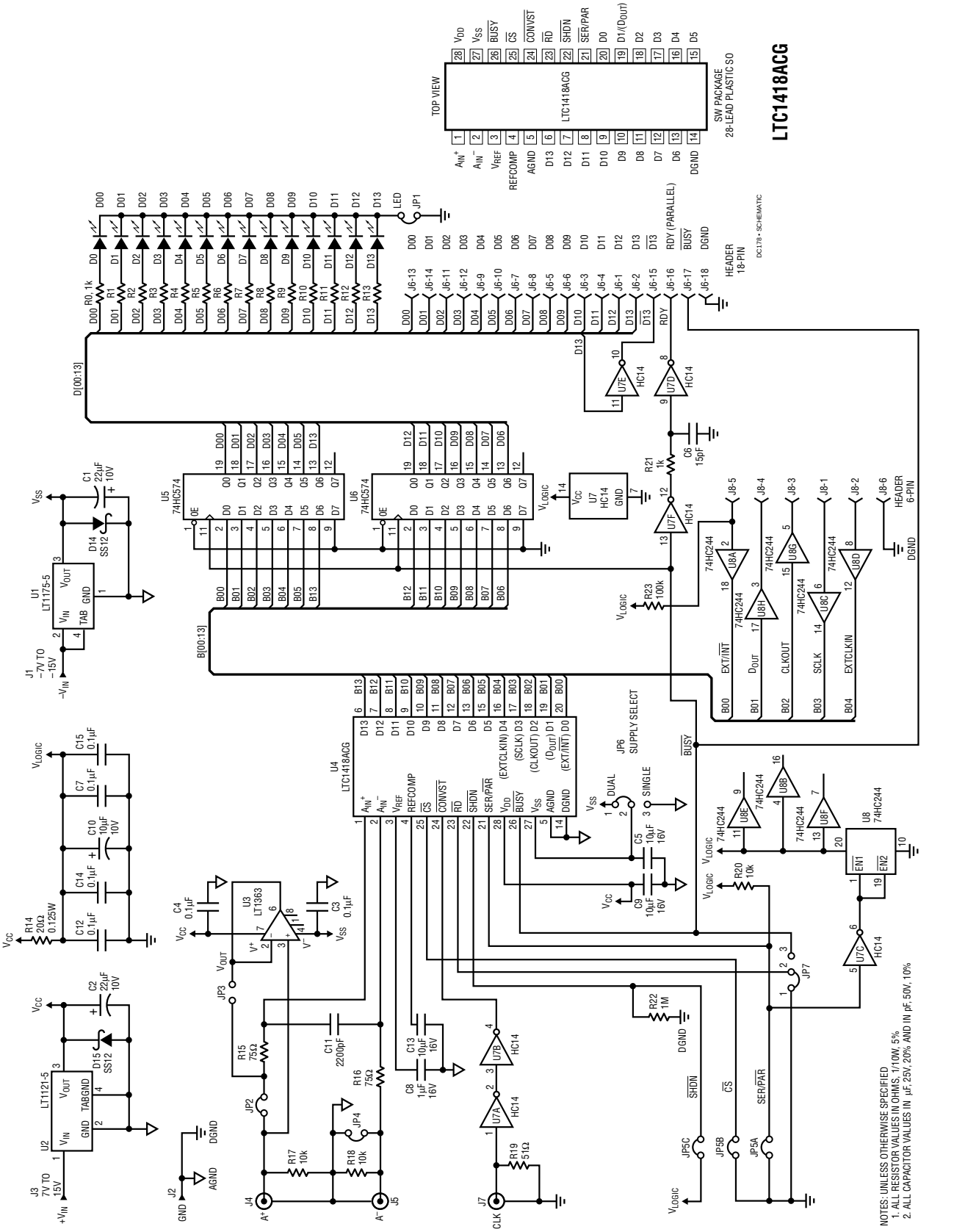
4096 Point FFT of LTC1418 Demo Board





PACKAGE AND SCHEMATIC DIAGRAMS

LTC1418 Demonstration Board Features Analog Input Signal Buffer, 200ksps Parallel and Serial Data Output 14-Bit ADC, Data Latches and LED Binary Data Display. Latched Conversion Data is Available on the 18-Pin Header, J6



PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1, C2	2	TAJC226M010R	22µF 10V 20% Tantalum Capacitor	AVX	(803) 946-0690
C3, C4, C7, C12, C14, C15	6	08053C104MAT1A	0.1µF 25V 20% X7R Capacitor	AVX	(803) 946-0362
C5, C9, C10, C13	4	1210YG106ZAT1A	10µF 16V Y5V Capacitor	AVX	(803) 946-0362
C6	1	08055A150KAT1A	15pF 50V 10% NPO Capacitor	AVX	(803) 946-0362
C8	1	0805YG105ZAT1A	1µF 16V Y5V Capacitor	AVX	(803) 946-0362
C11	1	08053A222KAT1A	2200pF 25V 10% NPO Capacitor	AVX	(803) 946-0362
D0-D13	14	SML-LX0805SRC-TR	2.1V 15mA Super Red SMT Led	Lumex	(847) 359-2790
D14, D15	2	SS12-PKG11	20V 1A SMA Schottky Diode	General Inst	(516) 847-3000
J1-J3	3	575-4	Standard Banana Jack Connector	Keystone	(718) 956-8900
J4, J5, J7	3	112404	50Ω PCB-Vertical BNC Connector	CONNEX	(805) 378-6464
J6	1	3201S-18G1	0.100cc 18-Pin 2-Row Header Connector	COMM CON	(818) 301-4200
J8	1	3201S-06G1	0.100cc 3-Pin 2-Row Header Connector	COMM CON	(818) 301-4200
JP1	1	2802S-02-G2	2mm 2-Pin Jumper	COMM CON	(818) 301-4200
JP2-JP4	3	JL-100-25-T	0.100cc 22-AWG Wire Jumper	Samtec	(800) 726-8329
JP5	1	2202S-06-G2	2mm 3-Pin 2-Row Jumper	COMM CON	(818) 301-4200
JP6, JP7	2	2802S-03-G2	2mm 3-Pin Jumper	COMM CON	(818) 301-4200
R0-R13, R21	15	CR10-102J-M	1k 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R14	1	CR18-200J-M	20Ω 1/8W 5% Chip Resistor	TAD	(800) 508-1521
R15, R16	2	CR10-750J-M	75Ω 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R17, R18, R20	3	CR10-510J-M	10k 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R19	2	CR10-510J-M	51Ω 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R22	1	CR10-510J-M	1M 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R23	1	CR10-510J-M	100k 1/10W 5% Chip Resistor	TAD	(800) 508-1521
U1	1	LT1175CST-5	–5V SO-8 IC Regulator	LTC	(408) 432-1900
U2	1	LT1121CST-5	5V SOT-223 IC Regulator	LTC	(408) 432-1900
U3	1	LT1363CS8	SO-8 IC Op Amp	LTC	(408) 432-1900
U4	1	LTC1418ACG	14-Bit SOL-28 IC ADC	LTC	(408) 432-1900
U5, U6	2	MC74HC574ADT	MSOP-20 IC Octal D Flip Flop	Motorola	(800) 441-2447
U7	1	MC74HC14ADT	MSOP-14 IC Hex Inverter Schmitt	Motorola	(800) 441-2447
U8	1	MC74HC244ADT	MSOP-20 IC Octal Buffer	Motorola	(800) 441-2447
	6	CCIJ2MM-138-G	2mm SHUNT	COMM CON	(818) 301-4200
	4		#4-40 1/4" SCREW	Any	
	4		#4-40 1/2" Nylon Hex STANDOFF	Keystone	(718) 956-8900
	2	CCIJ335-138-G	0.100cc SHUNT	COMM CON	(818) 301-4200

OPERATION

OPERATING THE BOARD

Powering the Board

To use the demo board, apply ±7V to ±15V at 200mA to the banana jacks J1 and J3 and 0V (GND) to J2. Be careful to observe the correct polarity. Onboard regulators provide ±5V to the LTC1418. An LT®1121-5 regulator (U2) provides 5V for analog and digital circuitry and the MC79L05 regulator (U1) provides –5V for the A/D and buffer.

The Analog Input

The LTC1418 has a unique feature not found on previous ADCs: differential inputs with good common mode rejection from DC to over 5MHz. Although this feature is

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extremely valuable for rejecting noise and measuring differential signals, the board can also be used to evaluate the LTC1418 in single-ended mode (with the "–" input grounded). A simple jumper selection at JP4 allows evaluation in either mode.

Differential (bipolar) analog signals are applied to the LTC1418 demo board using BNC connectors J4 (noninverting + input) and J5 (inverting – input). The analog signal input range is ±2.048V when operating on ±5V and 0V to 4.096V when using a single 5V supply.

The LTC1418 A_{IN}^+ (noninverting) and A_{IN}^- (inverting) inputs have a common mode range of V_{SS} to V_{DD}. The full-scale differential between the signals applied to A_{IN}^+ and A_{IN}^- is ±2.048V. For example, when a 1.5V signal is applied to the A_{IN}^- input, the negative-to-positive full-scale input range of A_{IN}^+ is –0.548V to 3.548V, corresponding to an output code of 10 0000 0000 0000 to 01 1111 1111 1111.

The demo board is delivered with jumpers JP2 and JP4 closed and jumper JP6 set for dual supply. This configures the board for a ±2.048V input signal centered around ground and applied to J4 (A_{IN}^+). For unipolar inputs (0V to 4.096V) set JP6 to single-supply and open JP4.

The board includes a recommended lowpass filter (R15, R16 and C11) across the differential inputs. With the component values shown, the cutoff frequency (f_S) is:

$$\frac{1}{2\pi(150\Omega)(0.0022\mu F)} = 482kHz$$

These values can be altered to meet other circuit and input-signal requirements. For lower bandwidth input signals, increase the value of C11. For undersampling applications that take advantage of the input circuitry's wide bandwidth, decrease the capacitance of C11.

The best way to observe the performance of the LTC1418 is to drive it directly from a low impedance signal source. However, since some applications involve high output impedance sources, the board also has provisions for an onboard LT1363 high speed operational amplifier. The LT1363, operating as a noninverter buffer, provides the LTC1418 with a fast settling, low impedance signal that allows the input voltage to fully settle before starting a conversion. The buffer is recommended if the source impedance of the input signal is greater than 930Ω. The LT1363 demonstrates how to properly drive the LTC1418. When using the LT1363, open JP2 and close JP4 and JP3.

Optimum performance is achieved using a signal source that has low output impedance, is low noise and has low distortion. Signal generators, such as the B & K Type 1051 Sine Generator, give excellent results. Further, this generator can be configured to operate referenced to a master clock signal, as shown in Figure 1.

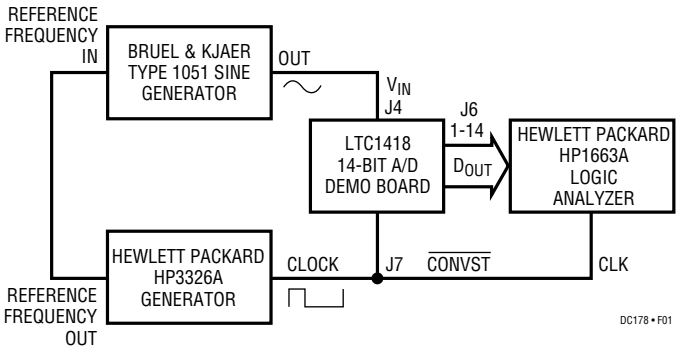

Figure 1. Typical Setup for LTC1418 Demo Board

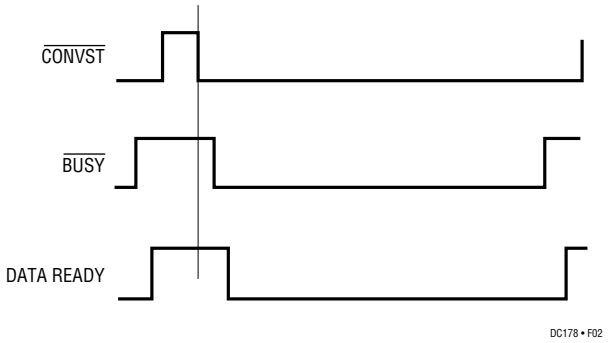

Figure 2. Timing Diagram

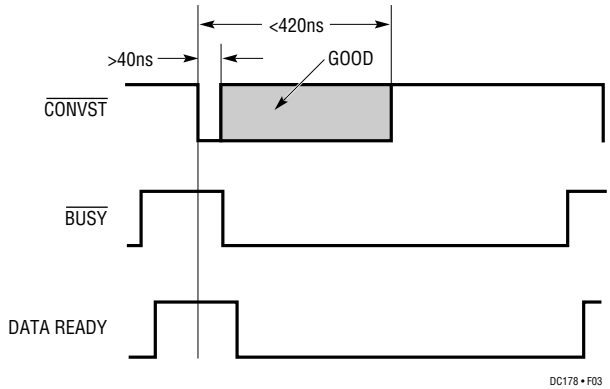

Figure 3. Alternative Timing Diagram

OPERATION

Applying the Conversion Start Signal

A conversion is initiated by a falling edge on the $\overline{\text{CONVST}}$ input (BNC J7). The $\overline{\text{CONVST}}$ input uses TTL or CMOS levels. As shown in Figure 2, $\overline{\text{CONVST}}$ should remain low until the conversion is completed or returned high within 420ns of the negative-going edge, as shown in Figure 3. During a conversion, transitions on the $\overline{\text{CONVST}}$ input can cause errors in the conversion data.

DATA OUTPUT INTERFACE

The LTC1418 features a versatile data interface that connects to a parallel or serial data bus. The SER/$\overline{\text{PAR}}$ pin configures the LTC1418 for the desired interface. The SER/$\overline{\text{PAR}}$ pin is accessed through jumper JP5A. For onboard control, shorting JP5A applies a logic low to the SER/$\overline{\text{PAR}}$ pin, configuring the LTC1418 for parallel data. Opening JP5A applies a logic high to the SER/$\overline{\text{PAR}}$ pin through R20, which is connected to 5V. This logic high reconfigures the LTC1418's data outputs for a serial bus, changing the function of Pin 16 through Pin 20 from parallel data outputs to a serial data interface. The remaining data outputs are placed in a high impedance state. Select the desired interface by opening JP5A and applying the appropriate logic level to JP5A, Pin 2. The SER/$\overline{\text{PAR}}$ logic signal source must be able to sink current to ground through a 10k resistor (R20). The data outputs of either configuration are active only when a logic low is applied to the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ pins. The data outputs are in a high impedance state for any other logic combination on the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ pins. Table 1 is a summary of the configurations and connections for the four serial modes. Figures 4 through 7 are timing diagrams for the serial interface. Refer to the LTC1418 data sheet for more details on the serial interface modes.

PARALLEL INTERFACE

Applying a logic low to the SER/$\overline{\text{PAR}}$ pin configures the LTC1418 for a parallel data bus. The LTC1418's pins 20 through 15 and pins 13 through 6 correspond to parallel bits D0 to D5 and D6 to D13. These data bits are found on J6, Pin 1 through Pin 14, along with an end of conversion signal (RDY) on Pin 16. For performing an AC test using FFTs that require unsigned binary, the MSB is inverted and available on J6, Pin 15 (D13).

SERIAL INTERFACE

Serial Data Output During a Conversion

In the two modes that follow, the serial data, beginning with the MSB, is present on D_{OUT} (Pin 19 on the LTC1418 and Pin 4 on J8) during the conversion. Since the $\overline{\text{BUSY}}$ signal is a logic low during conversions, it can serve as a frame signal in applications using DSPs.

Table 1. Serial Data Mode Configuration and Connection Summary

	Data During Conversion		Data After Conversion	
Inputs/Outputs	Internal Conversion and Serial Data Clocks	External Conversion and Serial Data Clocks	Internal Conversion and External Serial Data Clocks	External Conversion and Serial Data Clocks
EXT/$\overline{\text{INT}}$	Short J8-5 to J8-6	J8-5 Open	Short J8-5 to J8-6	J8-5 Open
SCLK Signal	Short J8-1 to J8-3		Apply External Clock Source to J8-1	
$\overline{\text{RD}}$	Short JP7-2 to JP7-3		Apply External Read Signal to JP7-2 Leave JP7-1 and JP7-3 Unconnected	
EXTCLKIN		Apply External Clock Source to J8-2		Apply External Clock Source to J8-2
CLKOUT	Present on J8-3		Present on J8-3	
$\overline{\text{CONVST}}$ Signal	Apply to J7			
D_{OUT}	Present on J8-4			
$\overline{\text{BUSY}}$	Present on J6-17			
SER/$\overline{\text{PAR}}$	Open JP5A For Serial Operation			
$\overline{\text{CS}}$	Close JP5B			
$\overline{\text{SHDN}}$	Close JP5C			

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Internal Conversion and Serial Data Shift Clocks

The mode shown in Figure 4 uses the LTC1418's internal conversion clock signal to shift out the conversion result on the D_{OUT} pin. This mode uses the least wiring (just four lines, $\overline{CONVST}$, $\overline{BUSY}$, CLKOUT and D_{OUT}) and requires no external clocks. The D_{OUT} pin's output state (high impedance or active) is controlled by $\overline{BUSY}$'s logic state. While $\overline{BUSY}$ is a logic low, the serial data is shifted out on the D_{OUT} pin (J8, Pin 4). The LTC1418 is configured for this mode by making the following connections:

SER/$\overline{PAR}$ = V_{LOGIC} (open JP5A)

$\overline{CS}$ = GND (close JP5B)

$\overline{SHDN}$ = V_{LOGIC} (close JP5C)

EXT/$\overline{INT}$ = GND (short J8-5 to J8-6)

SCLK = CLKOUT (short J8-1 to J8-3)

$\overline{RD}$ = $\overline{BUSY}$ (connect JP7-2 to JP7-3)

$\overline{CONVST}$ signal is applied to J7

CLKOUT is on J8-3

D_{OUT} is on J8-4

$\overline{BUSY}$ is on J6-17

External Conversion and Serial Data Shift Clocks

The mode shown in Figure 5 uses an external clock signal to clock conversions and serial data. As in the previous mode, this mode also uses the least wiring (just four lines, $\overline{CONVST}$, $\overline{BUSY}$, EXTCLKIN and D_{OUT}). The D_{OUT} pin's output state (high impedance or active) is controlled by $\overline{BUSY}$'s logic state. While $\overline{BUSY}$ is a logic low, the serial data is shifted out on the D_{OUT} pin (J8, Pin 4). The LTC1418 is configured for this mode by making the following connections:

SER/$\overline{PAR}$ = V_{LOGIC} (open JP5A)

$\overline{CS}$ = GND (close JP5B)

$\overline{SHDN}$ = V_{LOGIC} (close JP5C)

EXT/$\overline{INT}$ = V_{LOGIC} (nothing connected to J8-5)

SCLK = EXTCLKIN (short J8-1 to J8-2)

$\overline{RD}$ = $\overline{BUSY}$ (connect JP7-2 to JP7-3)

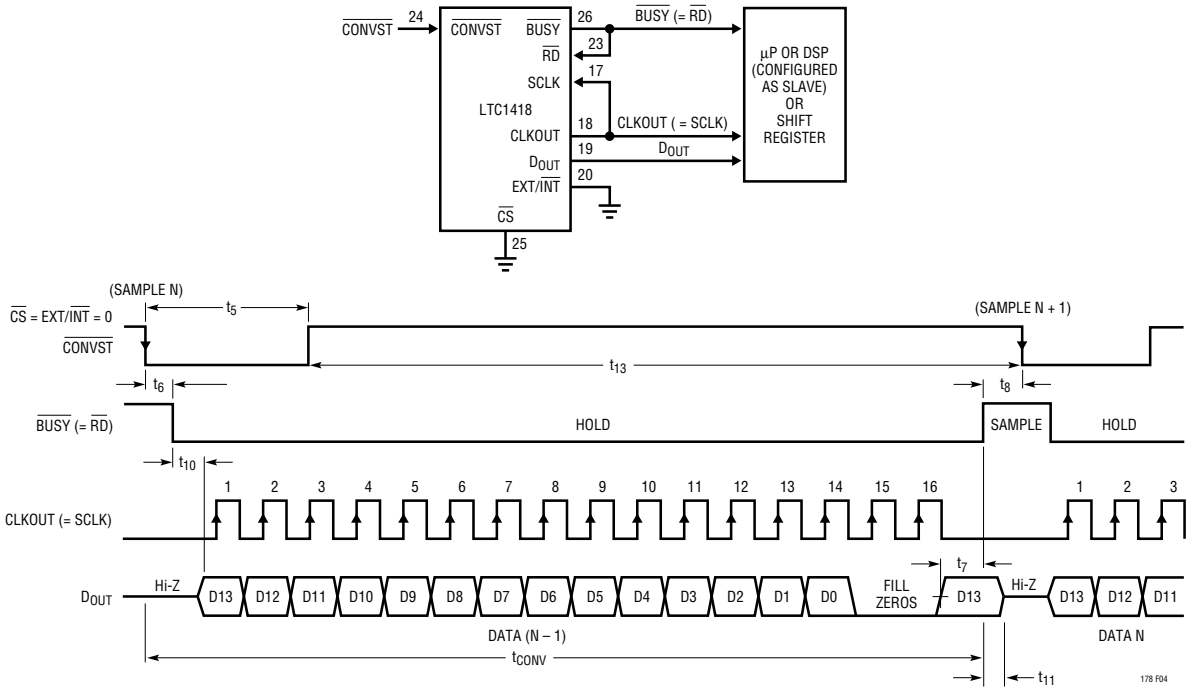

Figure 4. Internal Conversion Clock Selected. Data Transferred During Conversion Using the ADC Clock Output as a Master Shift Clock (SCLK Driven from CLKOUT).

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$\overline{CONVST}$ signal is applied to J7

EXTCLKIN = signal from external clock source

D_{OUT} is on J8-4

$\overline{BUSY}$ is on J6-17

Serial Data Output After Conversion

The two serial modes that follow potentially offer the best AC performance because error-producing switching noise is eliminated during conversion, since external clocks are inactive. In these modes, the serial data is available on D_{OUT} (Pin 19 on the LTC1418 and Pin 4 on J8) after the conversion is completed. It begins with the MSB and can be shifted out anytime after the $\overline{BUSY}$ signal's logic low to logic high transition. The $\overline{RD}$ signal must be a logic low while clocking the data. It can serve as a frame signal in applications using DSPs.

Internal Conversion Clock and External Data Clock

The mode shown in Figure 6 uses the internal clock signal for conversions and an external clock to shift the serial data. This mode adds just one more line to the serial interface ($\overline{BUSY}$, $\overline{RD}$, CLKOUT and D_{OUT}). The LTC1418 is configured for this mode by making the following connections:

SER/$\overline{PAR}$ = V_{LOGIC} (open JP5A)

$\overline{CS}$ = GND (close JP5B)

$\overline{SHDN}$ = V_{LOGIC} (close JP5C)

EXT/$\overline{INT}$ = GND (short J8-5 to J8-6)

SCLK = signal from external serial shift-clock source (applied to J8-1)

$\overline{RD}$ = external $\overline{RD}$ signal source is applied to JP7-2 (remove any shorts from JP7)

$\overline{CONVST}$ signal is applied to J7

D_{OUT} is on J8-4

$\overline{BUSY}$ is on J6-17

External Conversion Clock and External Data Clock

The mode shown in Figure 7 uses an external clock signal to clock conversions and serial data. Although this mode has the most serial interface connections, it is also the

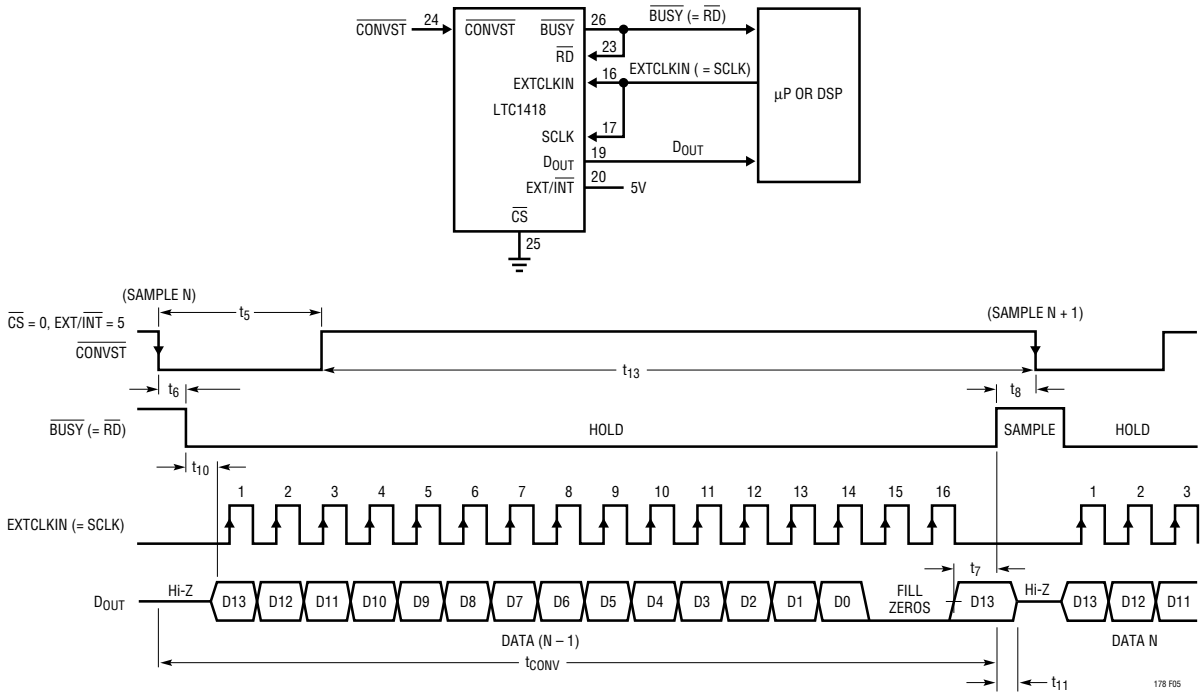

Figure 5. External Conversion Clock Selected. Data Transferred During Conversion Using the External Clock (External Clock Drives Both EXTCLKIN and SCLK).

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most versatile and flexible. By using two separate clocks (one clocks the conversion and another clocks the serial data), the conversion speed can be optimized for an application's requirements (source impedance, bandwidth, power dissipation, etc). The speed of the serial data can be set to what is needed by the processor, independent of the conversion clock. Conversely, this mode can be simplified by using the same clock signal for the conversion and data retrieval. This mode uses $\overline{BUSY}$, $\overline{RD}$, EXTCLKIN, CLKOUT and D_{OUT}. The LTC1418 is configured for this mode by making the following connections:

SER/$\overline{PAR}$ = V_{LOGIC} (open JP5A)

$\overline{CS}$ = GND (close JP5B)

$\overline{SHDN}$ = V_{LOGIC} (close JP5C)

EXT/$\overline{INT}$ = V_{LOGIC} (nothing connected to J8-5)

SCLK = signal from external serial shift-clock source (applied to J8-1)

$\overline{RD}$ = external $\overline{RD}$ signal source is applied to JP7-2 (remove any shorts from JP7)

$\overline{CONVST}$ signal is applied to J7

EXTCLKIN = signal from external conversion clock signal source (applied to J8-2)

D_{OUT} is on J8-4

$\overline{BUSY}$ is on J6-17

Reading the Output Data

The ADC's parallel data outputs are buffered by the two 74HC574 latches and are available on connector J6. The latches drive the LEDs and connector J6. In a practical circuit, latches are not required unless the ADC is tied to a noisy data bus. (Refer to the LTC1418 data sheet for details on different digital interface modes.)

The output data format of the LTC1418 is two's complement. The data can be converted to offset binary by using $\overline{D13}$ (J6-15) instead of D13. Offset binary is used when an FFT is to be performed on the sampled data. A Data Ready line (J6, Pin 16) is provided to latch the D_{OUT} word. D_{OUT} is valid on the rising edge of Data Ready. Two ground lines

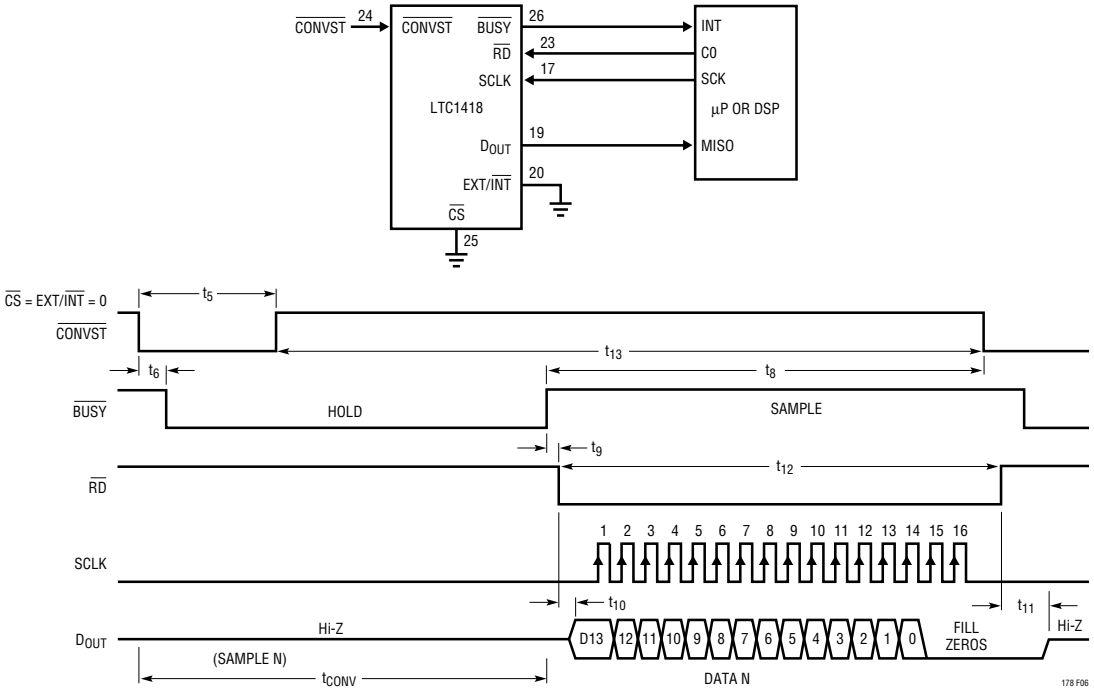

Figure 6. Internal Conversion Clock Selected. Data Transferred After Conversion Using an External SCLK. $\overline{BUSY}$↑ Indicates End of Conversion

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are provided on the connector and should be connected to the receiving system's ground.

The LTC1418 D_{OUT} word can be acquired with a logic analyzer. Conversion data can be stored on a disk and easily transferred to a PC by using a logic analyzer that has a PC compatible floppy drive (such as an HP1663A). Once the data is transferred to a PC, use programs such as MathCAD or Excel to calculate FFTs. Use the FFTs to obtain LTC1418 AC specifications, such as signal-to-noise ratio and total harmonic distortion.

LEDs D0 to D13 provide a visual display of the LTC1418 digital output word. D0 and D13 display the logic state of the LSB and MSB, respectively. Remove jumper JP1 to disable the LEDs, reducing supply current consumption up to 37mA.

Driving $\overline{CS}$, $\overline{RD}$ and $\overline{SHDN}$ Pins

Jumpers for $\overline{SHDN}$, $\overline{RD}$ and $\overline{CS}$ (JP5A to JP5C) are shorted for normal operation. The jumpers can be removed and these lines externally driven if desired. See the LTC1418 data sheet for details on driving these lines.

LAYOUT

A well-designed printed circuit board layout incorporating the LTC1418 uses separate analog and digital ground planes. Except for connecting them near U4's Pin 24, completely isolate the ground planes from each other. Additionally, they should not overlap if they are on different printed circuit board layers. Connecting the LTC1418 analog (AGND) and digital (DGND) pins to the analog ground plane ensures the lowest noise operation.

The demonstration board layout (section titled "PCB Layout and Film") shows the best way to configure and connect the ground planes. To ensure maximum ground plane efficiency, especially for the analog ground plane, it is important to minimize plane-breaking traces.

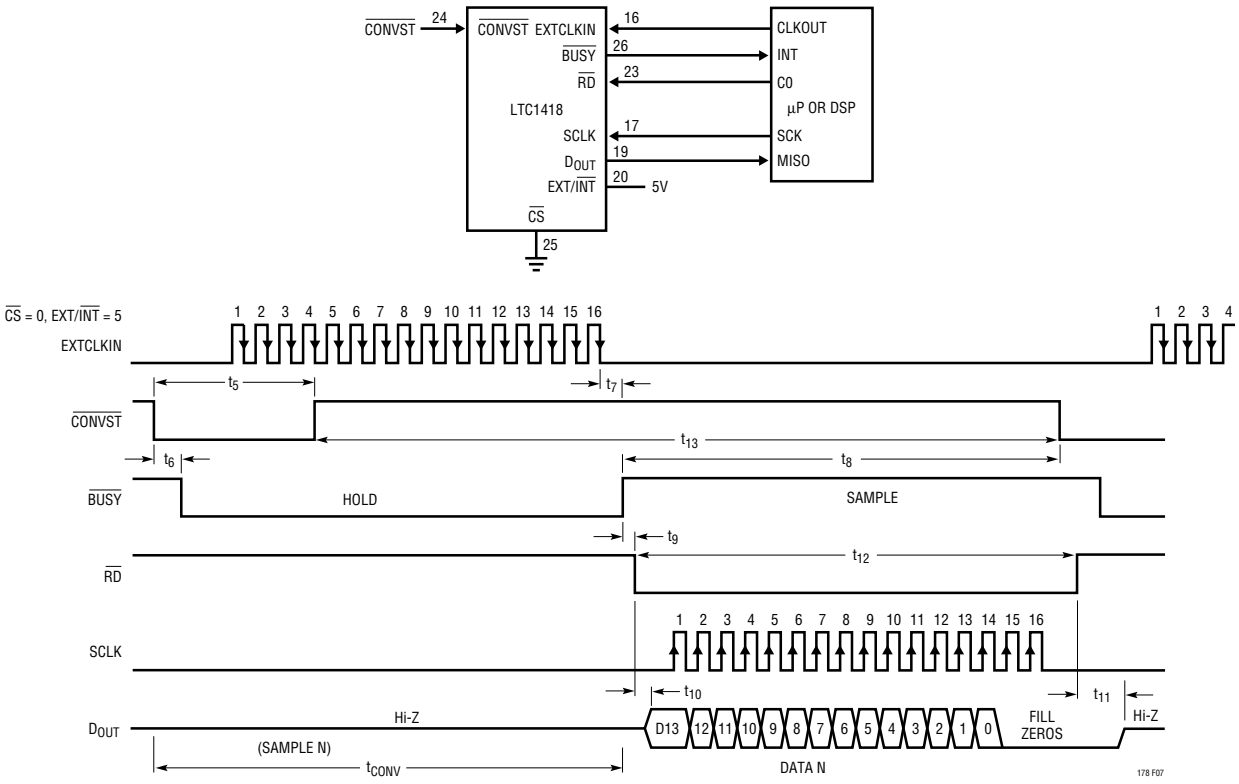


Figure 7. External Conversion Clock Selected. Data Transferred After Conversion Using an External SCLK. $\overline{BUSY}\uparrow$ Indicates End of Conversion

POWER SUPPLY CONNECTIONS AND BYPASSING

Analog and digital positive supply pins, AV_{DD} and DV_{DD} respectively, are connected at the device and to the 5V supply with a single trace. The negative supply pin (V_{SS}) is connected to the –5V supply. The best performance is achieved by careful attention to proper bypassing. Bypass V_{DD} to the analog ground plane with a 10µF monolithic ceramic capacitor. Bypass V_{SS} to the analog ground plane with its own 10µF monolithic ceramic capacitor.

The internal voltage reference requires a 10µF monolithic ceramic capacitor connected between the REFCOMP pin and the analog ground plane. This bypass capacitor is necessary because the LTC1418 internal reference requires a bypass capacitor of at least 1µF for stable operation. Reference noise can be reduced even further by using a 1µF monolithic ceramic capacitor connected between the V_{REF} pin and the analog ground plane.

As with all high accuracy, high resolution circuits, the best performance is achieved by minimizing the lead length of the bypass capacitors.

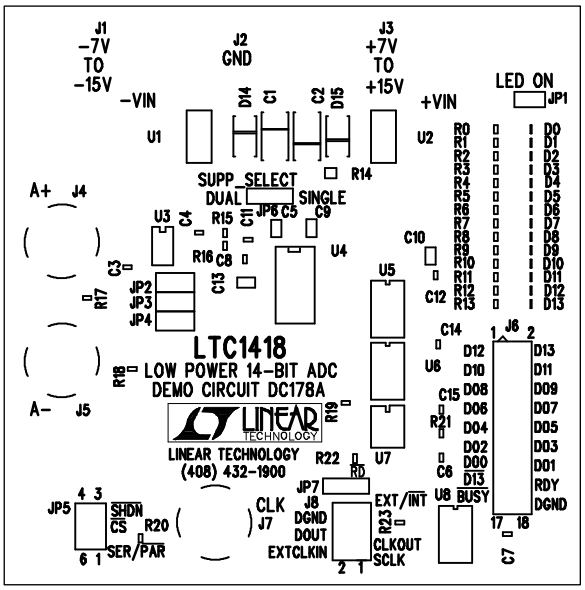
Table 2. Functional Description of User Configurable Jumpers

JUMPER	JUMPER NAME	JUMPER CONNECTION
JP1	LED Enable	Shorting Enables LED Operation. Opening Disables LED Operation
JP2	A_{IN}^+	Shorted for Unbuffered Operation. Open When Using the Noninverting Input Buffer. See JP3
JP3	Noninverting Input Buffer Bypass	Open for Normal Operation. Short for Buffered Input Signals and Open JP2
JP4	A_{IN}^-	Shorted for Single-Ended Operation. Open for Differential Input Signals
JP5A	SER/$\overline{PAR}$	Shorted for Parallel Interface Operation. Open for Serial Interface Operation.
JP5B	$\overline{CS}$	Shorted for Normal Operation. Open to Externally Drive the $\overline{CS}$ Pin.
JP5C	$\overline{SHDN}$	Shorted for Normal Operation. Open to Externally Drive the $\overline{SHDN}$ Pin with a Logic Low for Shutdown Mode or with a Logic High for Normal Operation.

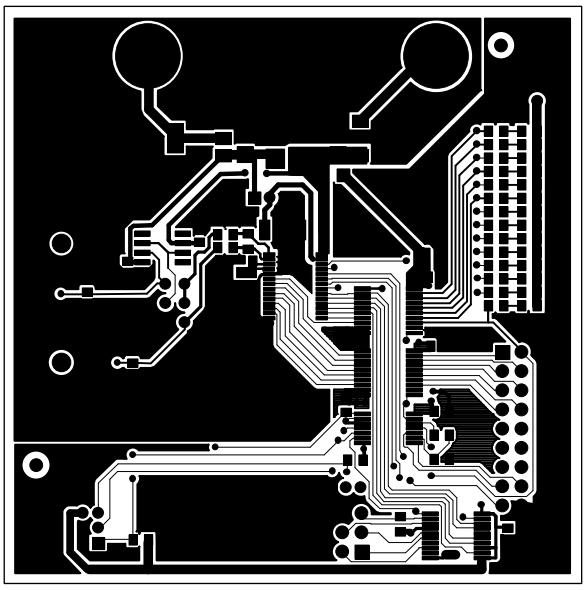
Table 3. Input and Output Pin Functional Description

INPUT/OUTPUT PIN	FUNCTION
E1	AGND (Mounting Hole)
E2	DGND (Mounting Hole)
E3	DGND (Mounting Hole)
E4	DGND (Mounting Hole)
J1	Negative Supply Voltage: –7V to –15V at 100mA
J2	Supply Ground
J3	Positive Supply Voltage: 7V to 15V at 100mA
J4	A_{IN}^+, Noninverting Input: ±2.5V, Referenced to A_{IN}^-. Input Voltage Range: V_{SS} to AV_{DD} (DV_{DD}).
J5	A_{IN}^-, Inverting Input: ±2.5V, Referenced to A_{IN}^+. Input Voltage Range: V_{SS} to AV_{DD} (DV_{DD}).
J6-1	D12
J6-2	D13 (MSB)
J6-3	D10
J6-4	D11
J6-5	D08
J6-6	D09
J6-7	D06
J6-8	D07
J6-9	D04
J6-10	D05
J6-11	D02
J6-12	D03
J6-13	D00
J6-14	D01
J6-15	$\overline{D13}$ (MSB)
J6-16	RDY Output (Parallel End of Conversion)
J6-17	Digital Ground
J6-18	$\overline{BUSY}$
J7	Convert Start: 0V to 5V

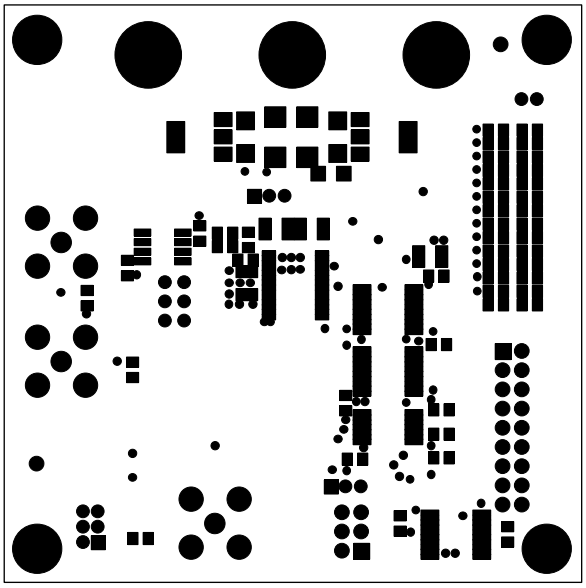
PCB LAYOUT AND FILM



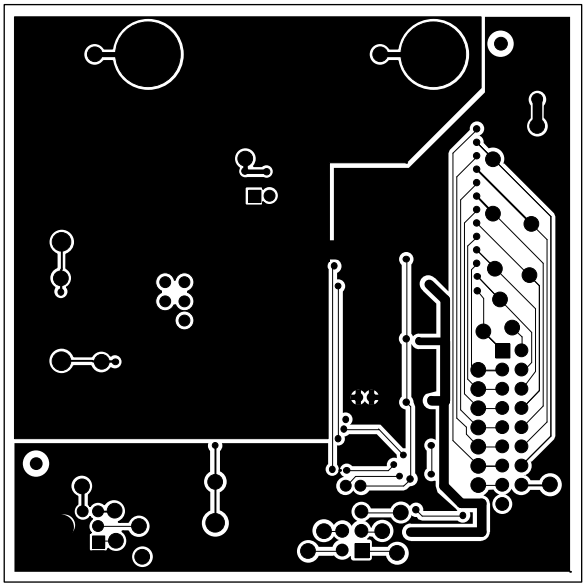
Component Side Silkscreen



Component Side

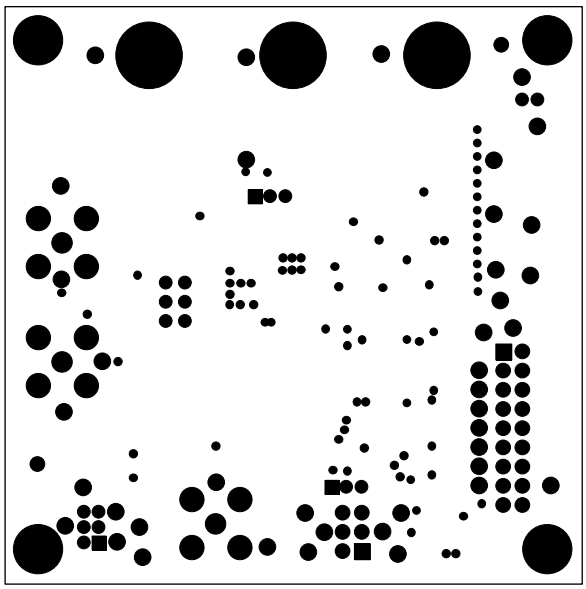


Component Side Soldermask

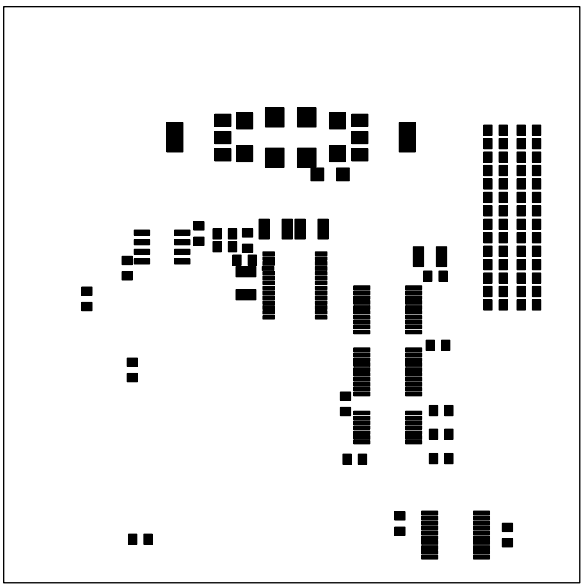


Solder Side

PCB LAYOUT AND FILM

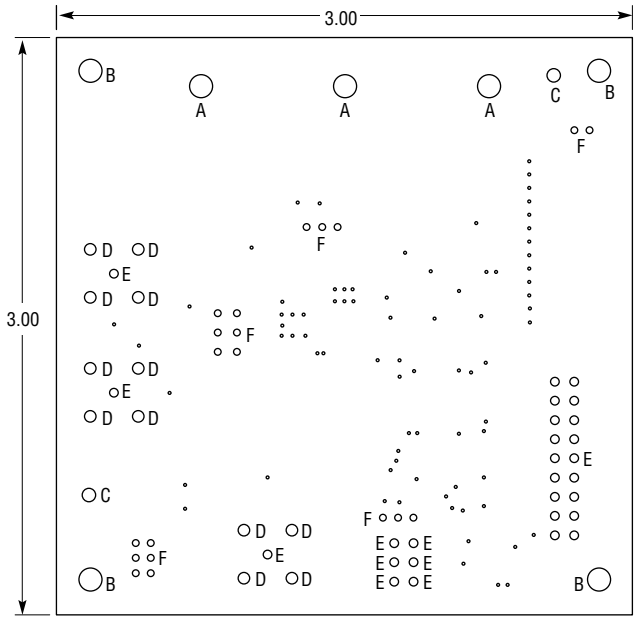


Solder Side Soldermask



Pastemask

PC FAB DRAWING



NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIALS: FR4 OR EQUIVALENT EPOXY, 2 OZ COPPER CLAD
   THICKNESS 0.062 ±0.006 TOTAL OF 2 LAYERS
2. FINISH: ALL PLATED HOLES 0.001 MIN/0.0015 MAX COPPER PLATE
   ELECTRODEPOSITED TIN-LEAD COMPOSITION
   BEFORE REFLOW, SOLDER MASK OVER BARE COPPER (SMOBC)
3. SOLDER MASK: BOTH SIDES USING LPI OR EQUIVALENT
4. SILKSCREEN: USING WHITE OR NONCONDUCTIVE EPOXY INK
5. ALL DIMENTIONS IN INCHES

SYMBOL	DIAMETER	NUMBER OF HOLES
A	0.210	3
B	0.120	4
C	0.070	2
D	0.060	12
E	0.045	27
F	0.035	20
UNMARKED	0.015	78
TOTAL HOLES		146

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