

LTC2756

Serial 18-Bit SoftSpan I_{OUT} DAC

DESCRIPTION

Demonstration circuit 1792A features the LTC2756 18-bit SoftSpan™, I_{OUT} DAC. The digital interface is a simple, 4-wire Serial Peripheral Interface (SPI) interface, augmented with separate CLEAR and LDAC pins that reset the output to zero and load the DAC code, respectively. This device features six output ranges: 0V to 5V, 0V to 10V, ±5V, ±10V, ±2.5V, and -2.5V to 7.5V. These ranges are programmable through the SPI interface or through

separate span control pins if SoftSpan operation is not needed. Voltage input offset and gain adjustment pins facilitate trimming of residual DC errors without impacting the excellent temperature stability of this device.

Design files for this circuit board are available at <http://www.linear.com/demo>

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BOARD PHOTO

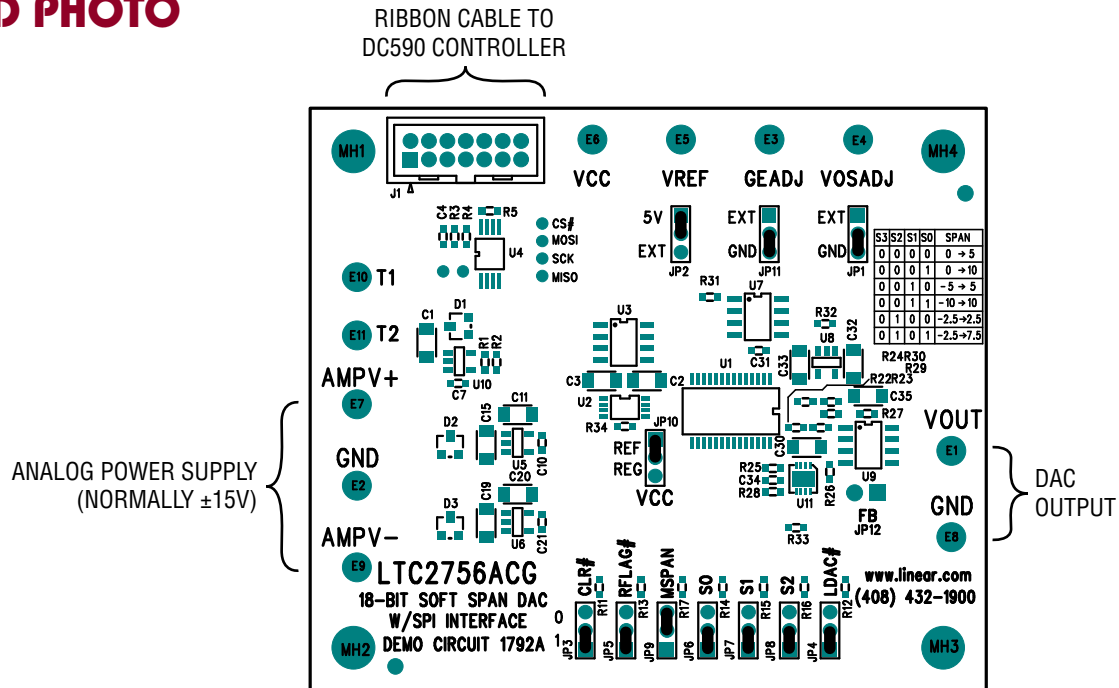


Figure 1. Connection Diagram

QUICK START PROCEDURE

Connect a low noise ±15V power supply to the AMPV⁺ and AMPV⁻ turret posts at the left side of the DC1792A board. Connect J1 to a DC590 USB serial controller using the supplied 14-conductor ribbon cable. Connect DC590 to a host PC with a standard USB A/B cable. Run the evaluation software supplied with the DC590, or download it from www.linear.com/software. The correct control panel will be loaded automatically, shown in

Figure 2. The software automatically sets the LTC2756 outputs according to the entries in the control panel. A square wave option is available to test settling time. MSPAN jumper should be set to 0 if software span control is desired. Setting MSPAN high (1) causes the S2, S1, S0 pins to set the span according to the table printed on the board, and the corresponding span should be selected in software to ensure that the calculated DAC code is correct.

dc1792af

QUICK START PROCEDURE

Additional software documentation may be available from the Help menu item, as features may be added periodically.

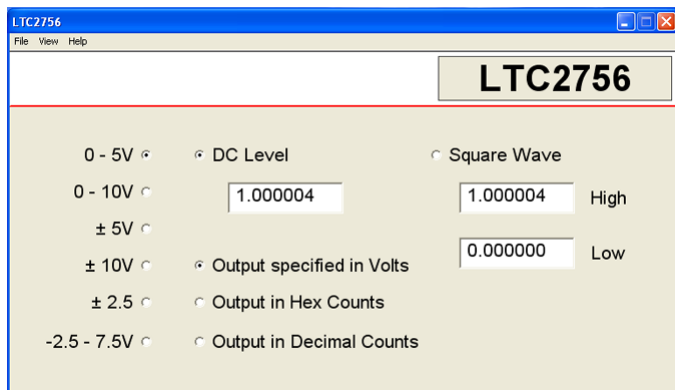


Figure 2. Software Screenshot

HARDWARE SET-UP

Jumpers

MSPAN: Manual Span Control Pin. MSPAN is used to configure the LTC2756 for operation in a single, fixed output range. If MSPAN is 1 (high) it will be configured for single span use. If MSPAN is low it will be set through the QuikEval™ Software. Default position is 0 (low).

S0, S1, S2: Used to set the fixed output range if MSPAN is 1 (high).

Table 1. MSPAN Configuration

S2	S1	S0	SPAN
0	0	0	0V to 5V
0	0	1	0V to 10V
0	1	0	±5V
0	1	1	±10V
1	0	0	±2.5V
1	0	1	-2.5V to 7.5V

GEADJ: Gain Adjust Pin. If no adjustments are required, select GND. Selecting EXT. connects the pin to the turret allowing external adjustment to null gain error or compensate for reference errors.

VOSADJ: Offset Adjustment Selection for DAC. If no offset adjustment is required, select GND. Selecting EXT connects the offset pin to the turret allowing external adjustment of offset.

V_{CC}: Select source for 5V V_{CC} supply. Set to 5V for supply by onboard LTC6655 reference (recommended). Set to REG to be supplied by regulated supply from DC590 Controller and remove the jumper to supply externally.

V_{REF}: Select source for reference. Set to 5V to use onboard LTC6655 reference or select EXT to drive externally through the V_{REF} jumper.

CLR: Asynchronous Clear Input. Tie to 0 to set all DAC outputs to 0V.

LDAC: Asynchronous DAC Load Input. Tie to 0 to update all DACs if _CS is high.

RFLAG: Reset Flag Output. Remove jumper and probe middle pin for RFLAG status.

Analog Connections (Turret Posts)

V_{OUT}: DAC Voltage Output.

V_{REF}: DAC Reference Voltage. If the onboard LTC6655 reference is selected, the voltage may be measured at these points. If a remote reference is selected, then an external reference must be applied to these points.

VOSADJ: DAC offset adjust input, use only if VOSA jumper set to EXT. Nominal input range is ±5V, which will provide ±2048LSB of offset adjustment.

GEADJ: Gain Adjust Pin. This voltage control pin can be used to null gain error or to compensate for reference errors. The gain error change expressed in LSB is the same for any output range. Nominal range is ±5V, which will provide ±2048LSB of gain adjustment.

Power and Ground Connections

Analog Power: AMPV⁺, AMPV⁻, and GND turret posts are the analog supplies for the onboard DAC amplifiers. These should be connected to a well regulated, low noise ±15V power supply.

V_{CC}: Connection to V_{CC}. See schematic and description for V_{CC} jumper.

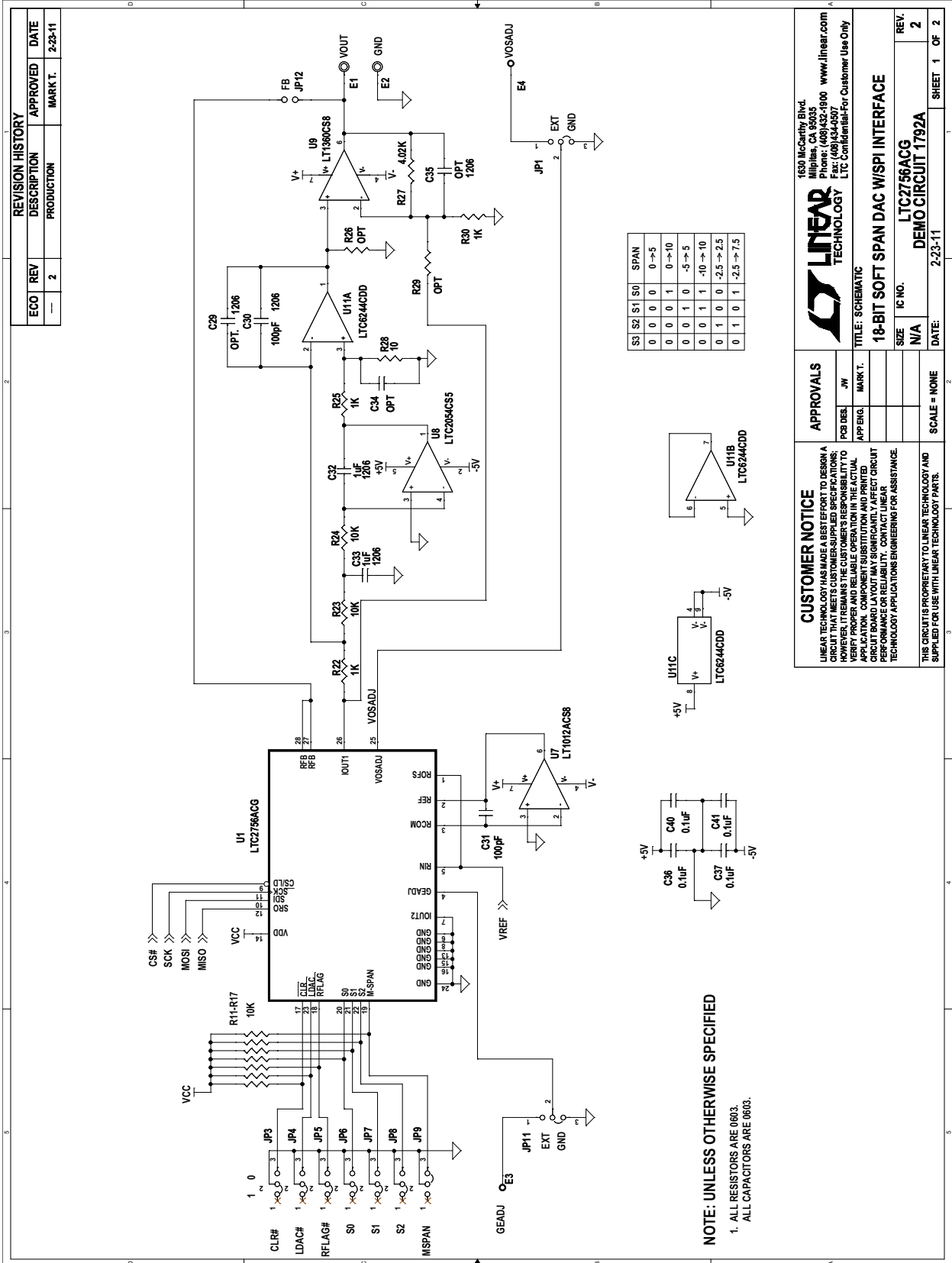
Grounding: Separate power and signal grounds are provided. Signal GND is the turret closest to V_{OUT}, use this for measurement ground and output return. Power GND is between AMPV⁺ and AMPV⁻ turrets.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	11	C1, C2, C3, C5, C6, C11, C13, C15, C18, C19, C20	CAP, X7R, 10µF, 10V, 20% 1206	TDK, C3216X5R1A106M
2	5	C4, C36, C37, C40, C41	CAP, X7R, 0.1µF, 10V, 10% 0603	AVX, 0603ZC104KAT2A
3	3	C7, C10, C21	CAP, X7R, 0.01µF, 10V, 10% 0603	AVX, 0603ZC103KAT2A
4	0	C34(OPT.)	CAP, 0603	
5	1	C31	CAP, COG, 100pF, 10V, 10% 0603	AVX, 06033A101KAT2A
6	0	C29, C35(OPT.)	CAP, 1206	
7	1	C30	CAP, COG, 100pF, 10V, 10% 1206	AVX, 1206ZC101KAT
8	2	C32, C33	CAP, X7R, 1µF, 10V, 10% 1206	AVX, 1206ZC105KAT2A
9	3	D1, D2, D3	DIODE, BAT54C, SOT23	DIODE/ZETEX, BAT54CTA
10	1	J1	CONNECTOR, HD2X7-079	MOLEX, 87831-1420
11	11	JP1-JP11	3-PIN 0.079 SINGLE ROW HEADER	SAMTEC, TMM103-02-L-S
12	14	XJP1-XJP11	SHUNT, .079" CENTER	SAMTEC, 2SN-BK-G
13	1	JP12	0.1" JUMPER SHUNT, SOLDER DOWN	SAMTEC, JL-100-25-T
14	1	R1	RES., CHIP, 88.7k, 1/16W, 1% 0603	VISHAY, CRCW060388K7KFEA
15	1	R2	RES., CHIP, 10.0k, 1/16W, 1% 0603	NIC, NRC06F1002TRF
16	3	R3, R4, R5	RES., CHIP, 4.99k, 1/16W, 1% 0603	NIC, NRC06F4991TRF
17	3	R22, R25, R30	RES., CHIP, 1k, 1/16W, 5% 0603	VISHAY, CRCW06031K00JNEA
18	9	R11-R17, R23, R24	RES., CHIP, 10k, 1/16W, 5% 0603	NIC, NRC06J1002TRF
19	0	R26, R29, R31-R34(OPT.)	RES., CHIP, 0603	
20	1	R27	RES., CHIP, 4.02k, 1/16W, 1% 0603	VISHAY, CRCW06034K02KFEA
21	1	R28	RES., CHIP, 10, 1/16W, 5% 0603	VISHAY, CRCW060310R0JNEA
22	11	E1-E11	Turret, Testpoint	MILL-MAX, 2308-2-00-44
23	1	U1	IC., LTC2756ACG, SSOP28	LINEAR, LTC2756ACG#TRPBF
24	1	U2	IC., LTC6655CHMS8-5, MSOP-8	LINEAR, LTC6655CHMS8-5#TRPBF
25	0	U3(OPT)	IC., SO-8	
26	1	U4	IC., 24LC025, TSSOP-8	MICROCHIP, 24LC025 I /ST
27	1	U5	IC., LT1761ES5-5, SOT23-5	LINEAR, LT1761ES5-5#TRPBF
28	1	U6	IC., LT1964ES5-5, SOT23-5	LINEAR, LT1964ES5-5#TRPBF
29	1	U7	IC., LT1012ACS8, SO-8	LINEAR, LT1012ACS8#TRPBF
30	1	U9	IC., LT1360CS8, SO-8	LINEAR, LT1360CS8#TRPBF
31	1	U8	IC., LTC2054CS5, TSOT23-5	LINEAR, LTC2054CS5#TRPBF
32	1	U10	IC., LT1761ES5-BYP, SOT23-5	LINEAR, LT1761ES5-BYP#TRPBF
33	1	U11	IC., LTC6244CDD, 8-PIN 3 × 3, DD	LINEAR, LTC6244CDD#TRPBF
34	4	MH1-MH4	STAND-OFF, NYLON 0.25"	KEYSTONE, 8831(SNAP ON)

DEMO MANUAL DC1792A

SCHEMATIC DIAGRAM



REVISION HISTORY		
ECO	REV	DESCRIPTION
---	2	PRODUCTION

APPROVED	DATE
MARK.T.	2-23-11

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LINEAR TECHNOLOGY

APPROVALS

FCB DES.	JW	MARK.T.

TITLE: SCHEMATIC
 18-BIT SOFT SPAN DAC WSPI INTERFACE

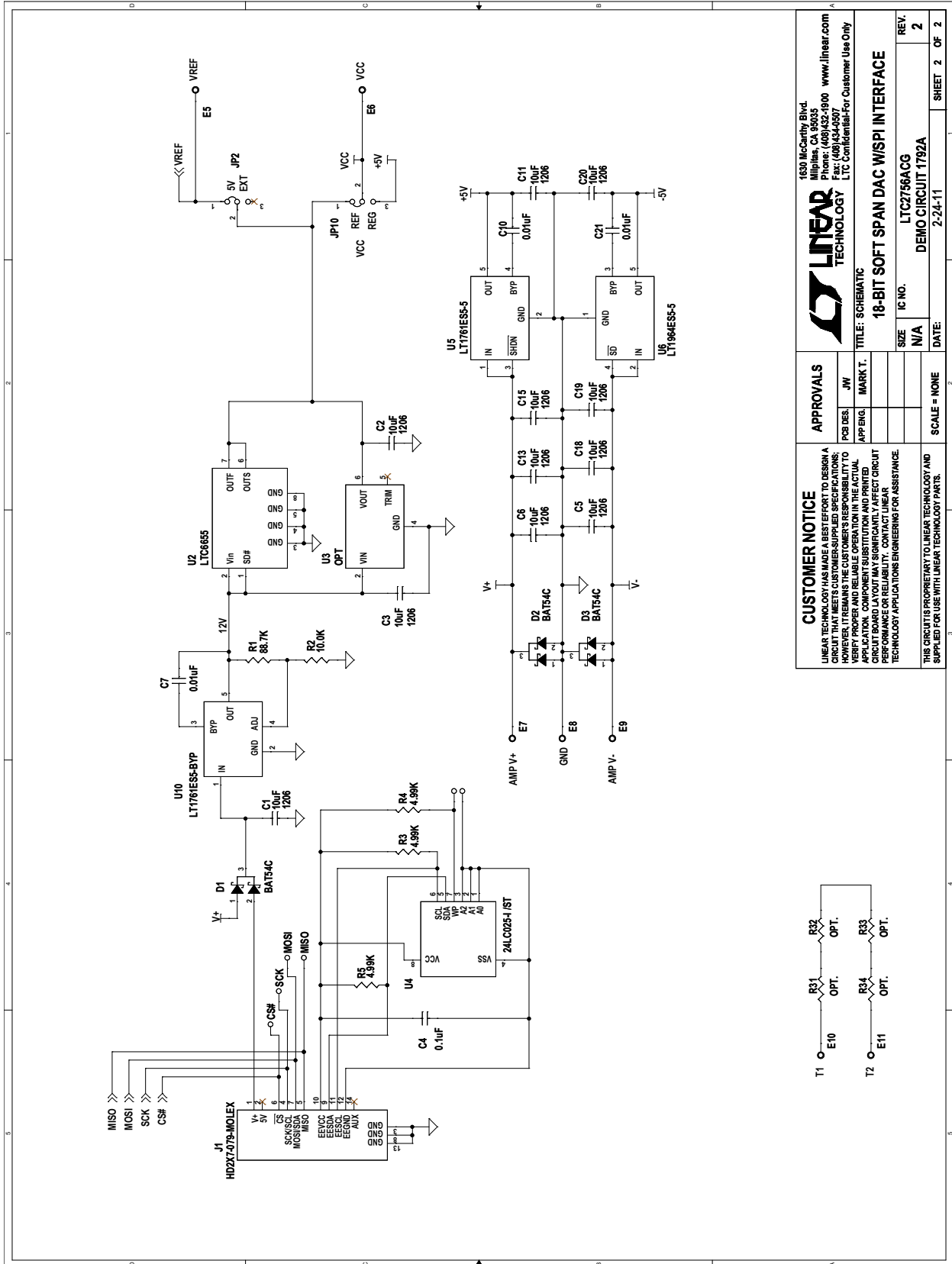
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N/A	LTC2756ACG	2

SCALE = NONE
 DATE: 2-23-11
 SHEET 1 OF 2

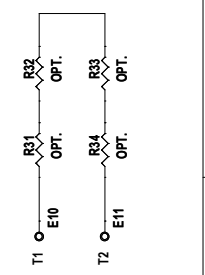
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		2-24-11	SHEET 2 OF 2



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DEMO MANUAL DC1792A

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