

## DESCRIPTION

Demonstration Circuit DC2064A is a bidirectional cell balancer using two LTC<sup>®</sup>3300-1 ICs to achieve active cell balancing of up to 12 Li-Ion batteries. The board uses the LTC6803-2 multi-cell addressable battery stack monitor to measure cell voltages and two LTC3300-1 ICs to provide active cell balancing. The demonstration circuit uses a two window GUI developed for the DC2064A. One window is a modified version of the GUI for the LTC6803-2 and also contains a tab to control the LTC3300-1 ICs through the DC590B USB Serial controller and the second window

reports the status of the LTC3300-1 devices. All the functions of the LTC6803-2 GUI are supported except that cell balancing is achieved through the LTC3300-1 ICs by transferring charge from one to six batteries per LTC3300-1 to the stack or from the stack to one to six batteries per LTC3300-1.

**Design files for this circuit board are available at <http://www.linear.com/demo/DC2064A>**

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## PERFORMANCE SUMMARY

Specifications are at  $T_A = 25^\circ\text{C}$

Battery Voltage Range	3.2V to 4.5V (2.5V to 4.5V)*
Stack Voltage	60V Max
Average Battery Balancing Charge Current (12 Cell)	2.6A (Typ) (4A)*
Average Battery Balancing Discharge Current (12 Cell)	2.4A (Typ) (3.6A)*
Average Battery Balancing Charge Current (6 Cell)	2.2A (Typ) (3.3A)*
Average Battery Balancing Discharge Current (6 Cell)	2.4A (Typ) (3.6A)*
Balancing Efficiency	92% (Typ)

\*The battery voltage range may be expanded to 2.5V-4.5V by changing resistor  $R_{TONS}$  to 19.1k and resistor  $R_{TONP}$  to 29.4k. The demo board's average balancing current is adjustable up to 4A by scaling and installing new values of RS1A and RS1B through RS12A and RS12B.

## BOARD PHOTO

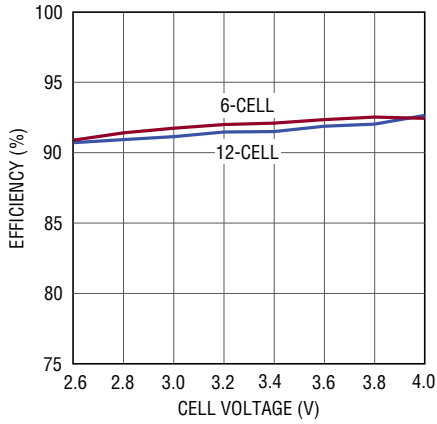


dc2064afa

# DEMO MANUAL DC2064A

## DESCRIPTION

Power Stage Discharge Efficiency



Power Stage Charge Efficiency

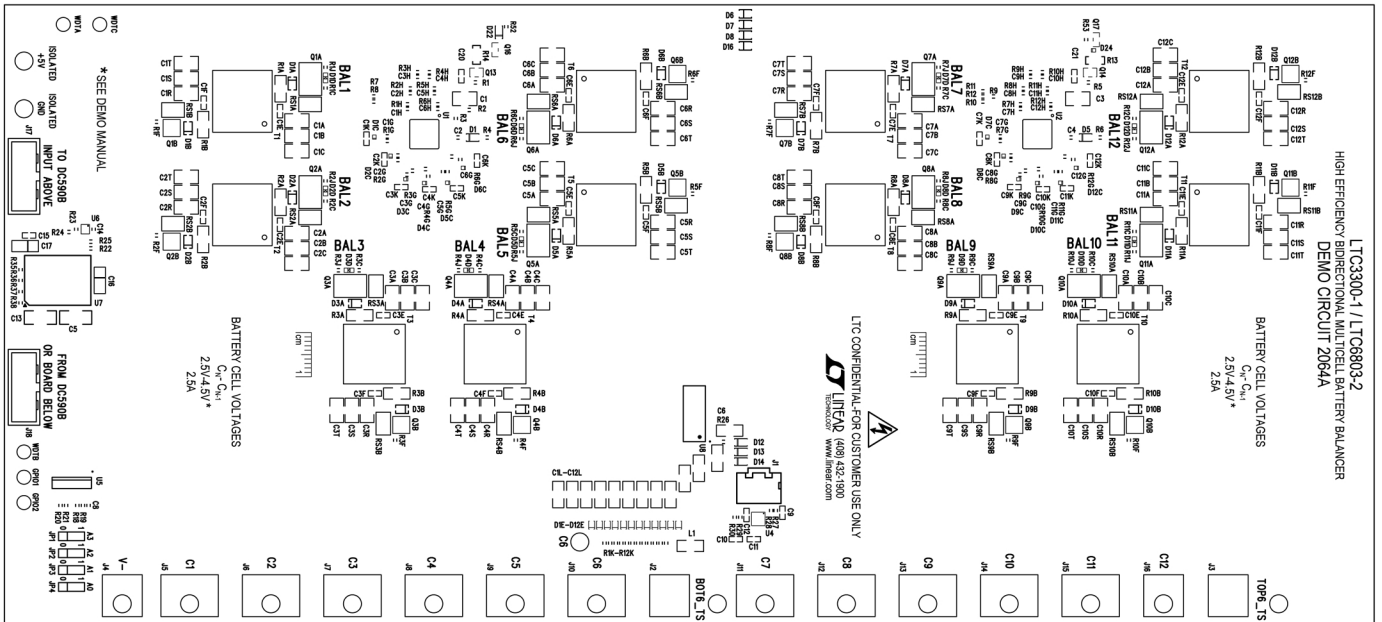
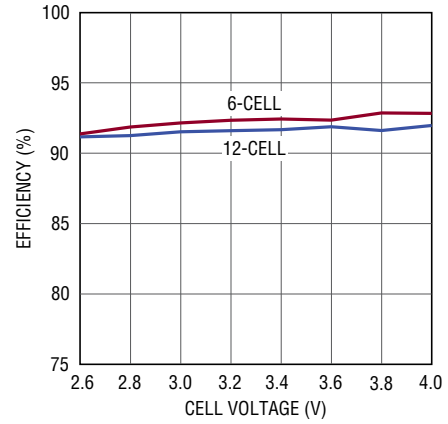


Figure 1. DC2064A Size 5.5" × 12.2"

## OPERATING PRINCIPLE

Operation of the LTC6803-2 is detailed in the LTC6803-2 data sheet and the operation of the DC2064A GUI is similar to the DC1652A GUI except additional functionality was added to control the LTC3300-1 balancing devices. Refer to the Quick Start Guide for the DC1652B for operation of the LTC6803-2 GUI. The DC2064A has a two window GUI, one window based on the DC1652A GUI to control the LTC6803-2 with a tab to control the LTC3300-1 for battery balancing and the second window to display the status of the LTC3300-1 based on the command and status registers read from the LTC3300-1.

The LTC3300-1 active balancer is a power stage control IC. The LTC3300-1 does not have a balancer algorithm built into it. The determination of the balancing times and directions are performed at a system level and conveyed to the LTC3300-1 through its SPI interface. The LTC3300-1 only accepts battery charge or discharge commands.

Charge is transferred to/from a cell (battery) from/to the stack, a series connection of adjacent cells, through a flyback converter that is operating in boundary mode.

During discharge of a cell, the current in the primary of a coupled inductor transformer with a turns ratio of 1:2, ramps up to 6.25A at which point the primary switch turns off. The charge in the primary inductor is transferred to the secondary inductor which is connected across the 12-cell pack. This pack current then passes through the series connected cells thus distributing the charge equally across each cell. When charging a cell, the current, in the secondary of the coupled inductor transformer, ramps up to 3.125A at which point the secondary switch turns off. The charge in the secondary inductor is transferred to the primary inductor which is connected across the cell. The secondary current is drawn from the series connected cells thus removing charge equally across each cell. The efficiency through the flyback converter is  $\approx 92\%$ .

## QUICK START PROCEDURE

The demonstration circuit is set up per Figure 29 to evaluate the performance of the DC2064A bidirectional cell balancer using the LTC3300-1.

**Caution: BOT6\_TS and TOP6\_TS turrets must not be allowed to float and must be connected to their respective top of stack-battery terminal.**

Using short twisted-pair leads for any power connections, refer to Figure 29 for the proper measurement and equipment setup. The DC2064A will support a system of 4 to 12 batteries.

### Recommended Cell Connection Sequence

The recommended cell connection sequence is to connect the  $V^-$  connection first followed by connecting cells 1 through cell 12. Disconnection of the cells should follow this sequence in the reverse order with the  $V^-$  connection being removed last. Connecting the  $V^-$  connection first and removing last is recommended because the  $V^-$  connection is the ground reference for the circuitry within the demo board. After connecting the  $V^-$ , all other cell connection sequence is less critical as long as the cell circuit capacitances are matched as they are in the demo board.

Following the recommended cell connection removes the possibility of excessive voltage on any of the lower cells due to an imbalance in cell circuit capacitance.

Follow the procedure outlined in the DC1835A Quick Start Guide for general use of the modified LTC6803-2 GUI window. The 4-bit board ID code that is set by the A0 through A3 jumpers on the DC2064A must match the board Address box in the LTC6803-2 GUI window shown in Figure 2 for each board in the system.



Figure 2. Board Address Box

## QUICK START PROCEDURE

The Voltage Comparator box must be turned off and the VREF must remain on during balancing. Set window by using the Up/Down arrows to the right of the box. See Figure 3.

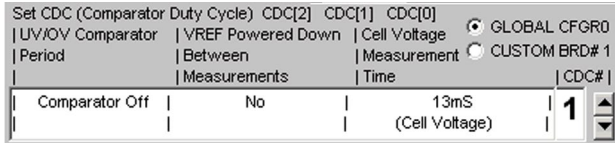


Figure 3. Voltage Comparator Box

The DC2064A GUI periodically checks for OV and UV measured on the cells when balancing. To avoid the program from suspending balancing from an OV or UV measurement during normal operation, the OV and UV values must be entered in the VOV and VUV text boxes on the LTC6803-2 tab shown in Figure 4.

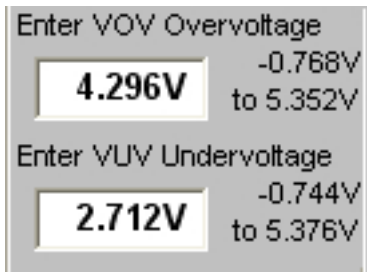


Figure 4. VOV and VUV text boxes

Once this is done, Click the WRITE CONFIG button and verify that the configuration was set correctly by clicking the READ CONFIG.



Figure 5. Write Configuration Box

Click the START CELL VOLT button followed by the READ CELL VOLT to verify that the batteries are connected and that the LTC6803-2 can read the battery voltages.

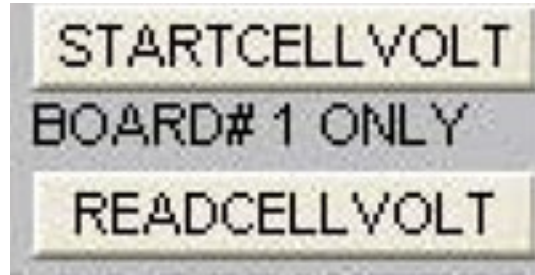


Figure 6. Start Cell Voltage Read Box

To access the LTC3300-1 screen, click on the LTC3300-1 tab in the upper left of the LTC6803-2 GUI window.



Figure 7. LTC3300-1 Screen Select Box

Within this window you can manually select which cells are to be discharged by clicking the cell's DISCHARGE button and which cells are to be charged by clicking the cell's CHARGE button.

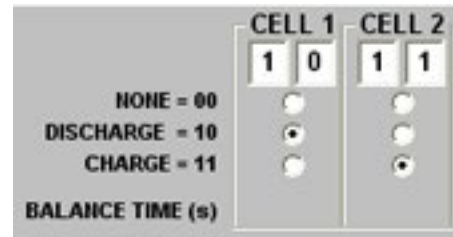


Figure 8. Balance Mode Select Boxes

To write this configuration, the WRITE button followed by the SEND button must be clicked. To enable the balancers, the EXECUTE button followed by the SEND button must be clicked. To pause the cell balancers, the SUSPEND button is clicked followed by clicking the SEND button. This will turn off all balancers until the EXECUTE button is clicked followed by clicking the SEND button. This will resume the previous settings of the cell charge/discharge settings.

## QUICK START PROCEDURE



Figure 9. Write/Execute Command Box

To change any of the settings “on the fly”, a new charge/discharge setting is entered using the respective CHARGE and DISCHARGE buttons followed by clicking the WRITE button followed by the SEND button and then the EXECUTE button followed by the SEND button. To disable any cell from operating, the cell’s NONE button must be clicked in the balance mode box followed by clicking the WRITE button followed by the SEND button and then the EXECUTE button followed by the SEND button.

The LTC3300-1 GUI allows the user to program the balancer to charge or discharge each cell for a specific amount of time. The LTC3300-1 is a power stage control IC. The determination of the balancing times and directions are done at the System level and conveyed to the LTC3300-1 through its SPI communications port. In order to perform a timed balance, the TIMED BALANCE check shown in Figure 10 must be selected to have access to the timed balance controls as shown in Figure 27.



Figure 10. TIMED BALANCE Check Box

To do this, select the DISCHARGE or CHARGE button for the desired cell, then enter the time in seconds into the cells “BALANCE TIME” text box. Press the enter key on the key board or select another button in the GUI to load the time. When all the desired balance actions and times have been entered, select the “Balance Cells” START button to start the balancing sequence.

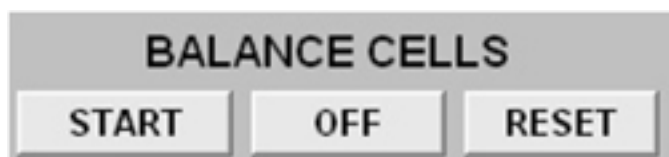


Figure 11. Balance Cells Start Box

The START button will display PAUSE. The balancing algorithm will first turn off all cells, then set all cells to be balanced. The cells will run until the first cell(s) have elapsed their balance time. At this time all cell balancing is suspended, the completed cell’s balancing action is set to “None”, the remaining times to balance are recalculated, then the remaining cells continue to balance until the next cell(s) have completed. This sequence continues until all of the balance times have elapsed.

Selecting the PAUSE button while the balancer is running, will shut off the active cell and pause the timer. The START button now displays CONTINUE. Selecting the CONTINUE button again will start the active cell balancing and continue the timer. After the last cell has completed balancing, all the cells are turned off. The START button will again display START. Selecting the RESET button will reset all the cell actions and times to the previous entered settings.

The LTC3300 STATUS window displays the status of all LTC3300-1 ICs in the system. This GUI is updated every time the LTC3300-1 status or command registers are read. When the balancer timer is running, the command register is read after each execute command is sent.

## QUICK START PROCEDURE

### Cell Balancer Efficiency Measurements:

Figure 30 shows the proper connections for measuring the efficiency of a cell balancer. The secondary of the cell balancer connects to the top of stack. This connection needs to be to an isolated power source through a current sensing resistor (0.10Ω). Cells 1 through 6 are connected to the BOT6\_TS turret with its return path the V- turret while Cells 7 through 12 are connected to the TOP6\_TS turret with its return path the C6 turret. The primary side connections of the cell balancers are connected to a string of batteries that simulate the battery stack. Cell 1 is a 2-wire connection that connects the positive node, through a current sensing resistor (0.01Ω), to the C1 turret, and the negative node to the V- turret. Remote sense connections for power sources with remote sensing capabilities should be connected to the C1 and V- respectively. All other connections of the simulated string of batteries connect their positive node, through a current sensing resistor (0.01Ω), to respective turrets. Cell voltage measurements should be made across the C(x) and C(x - 1) turrets of the respective cells. Stack voltage measurements should be made at the BOT6\_TS and TOP6\_TS turrets and their return path turret.

To calculate cell balancer efficiency use the expressions below:

### Cells 1-6

#### Charge Mode

$$\text{Efficiency}_{11} = \frac{Vm_1 \cdot Vm_2 \cdot 10}{Vm_3 \cdot Vm_4} \cdot 100\%$$

#### Discharge Mode

$$\text{Efficiency}_{11} = \frac{Vm_3 \cdot Vm_4}{Vm_1 \cdot Vm_2 \cdot 10} \cdot 100\%$$

### Cells 7-12

#### Charge Mode

$$\text{Efficiency}_{11} = \frac{Vm_5 \cdot Vm_6 \cdot 10}{Vm_7 \cdot Vm_8} \cdot 100\%$$

#### Discharge Mode

$$\text{Efficiency}_{11} = \frac{Vm_7 \cdot Vm_8}{Vm_5 \cdot Vm_6 \cdot 10} \cdot 100\%$$

### Cell Balancer Performance Measurements:

Table 2 through Table 5 present the typical operational data for a 12-cell and 6-cell balancer in both Discharge and Charge modes. The cell voltages were 3.6V and measurements of Cell Current, Stack Current, Operating Frequency were taken and transfer Efficiency was calculated from the data. Figure 12 through Figure 15 are actual in circuit waveforms taken on Cell 1 and Cell 7 while operating in both modes. The waveforms present voltage on the primary side and secondary side MOSFET's drain to source voltage and the primary side and secondary side current sense inputs to the LTC3300-1.

Figures 16 through 19 are cell and stack currents taken over a range of cell voltages from 2.6V to 4.0V. The RTONP and RTONS resistors for these graphs were set for 2.6V cell voltage operation. All cells were set to the cell voltage under test. The slight negative slope in current at higher voltages is due to the increased operating frequency and the circuit delays and dead time becoming a higher percent-age of the operating period.

# QUICK START PROCEDURE

## 12 Cell Discharge

Table 2. Typical 12 Cell Discharge Data

Cell I (A)	Stack I (A)	Frequency (kHz)	Efficiency
2.444	0.188	127.7	92.21%

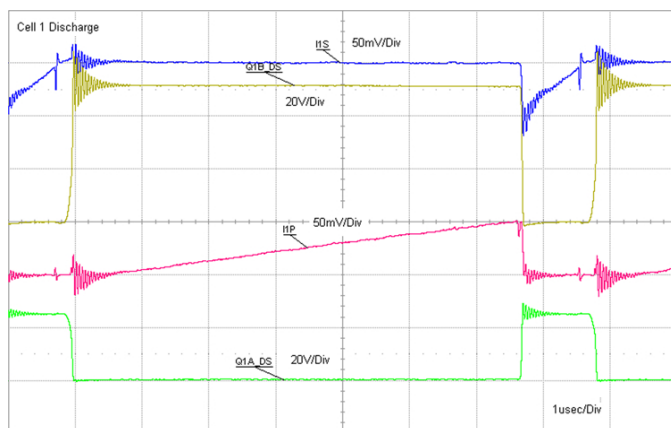


Figure 12. 12 Cell Discharge Waveforms

## 6 Cell Discharge

Table 4. Typical 6 Cell Discharge Data

Cell I (A)	Stack I (A)	Frequency (kHz)	Efficiency
2.448	0.277	126.1	92.33%

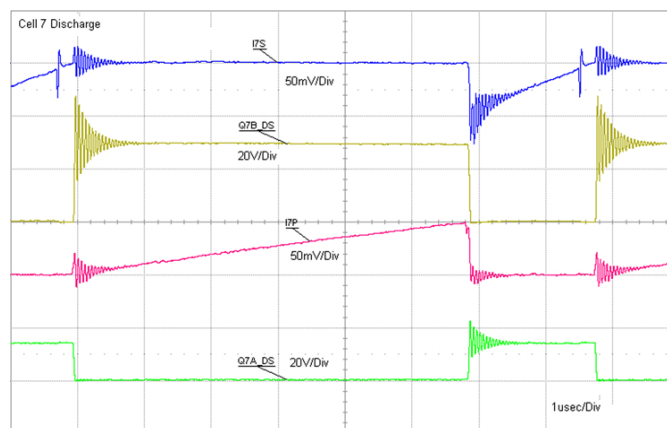


Figure 14. 6 Cell Discharge Waveforms

## 12 Cell Charge

Table 3. Typical 12 Cell Charge Data

Cell I (A)	Stack I (A)	Frequency (kHz)	Efficiency
2.601	0.237	149.1	91.71%

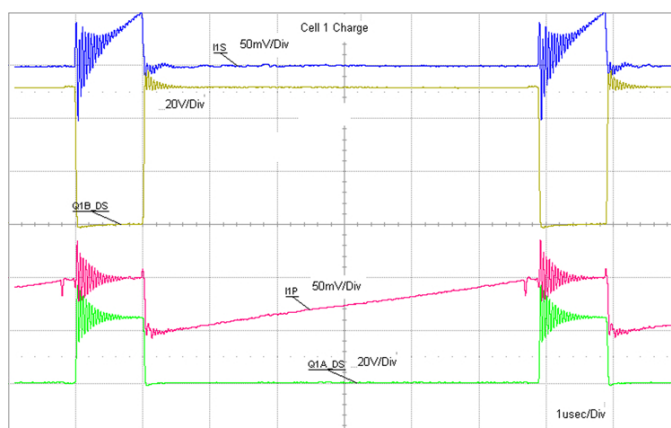


Figure 13. 12 Cell Charge Waveforms

## 6 Cell Charge

Table 5. Typical 6 Cell Charge Data

Cell I (A)	Stack I (A)	Frequency (kHz)	Efficiency
2.219	0.399	133.1	92.72%

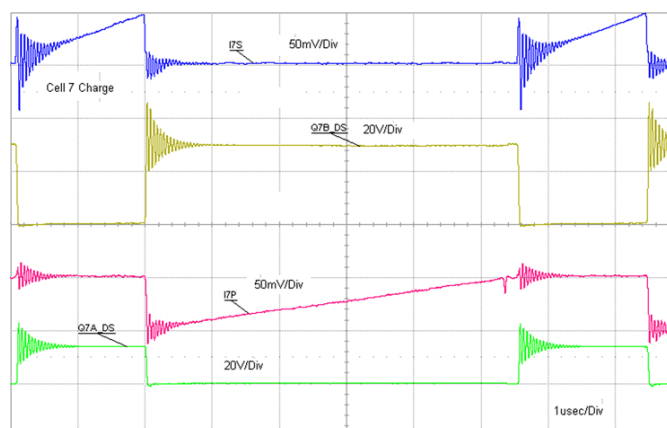


Figure 15. 6 Cell Charge Waveforms

## QUICK START PROCEDURE

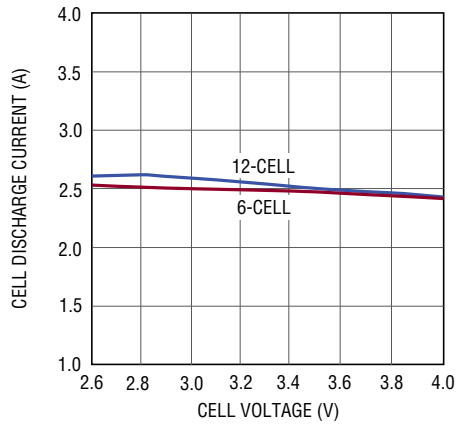


Figure 16. Cell Discharge Current

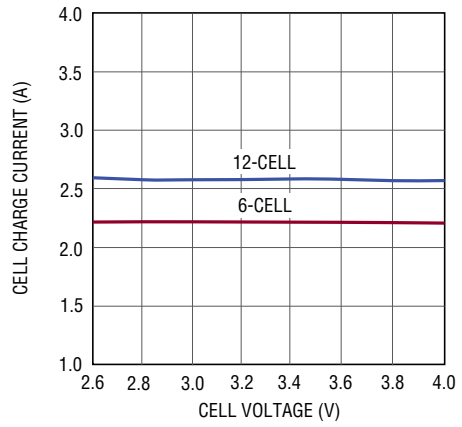


Figure 18. Cell Charge Current

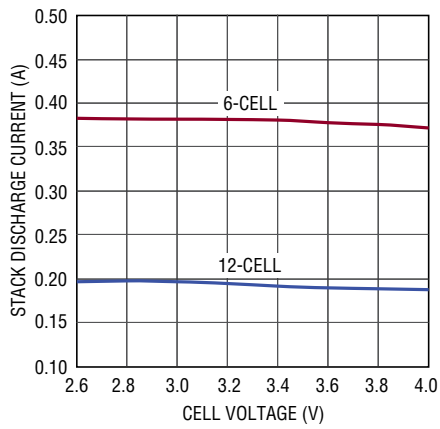


Figure 17. Stack Discharge Current

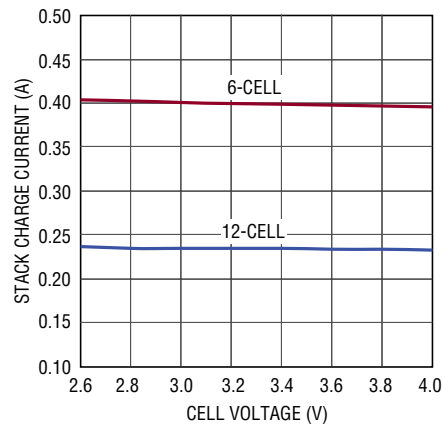


Figure 19. Stack Charge Current



## QUICK START PROCEDURE

### Two Board Setup and Operation:

As a result of communication latency to the PC, the system only supports two series DC2064A boards

When connecting two DC2064A boards together, the interface cables must be connected in sequence as shown in Figure 20 to avoid large inrush currents. The DC590B

must be connected to the PC USB port and the bottom DC2064A board first and then the top DC2064A board may be connected.

The 24 cells should be interconnected to allow balancing between the two 12-cell stacks, as shown in Figure 21.

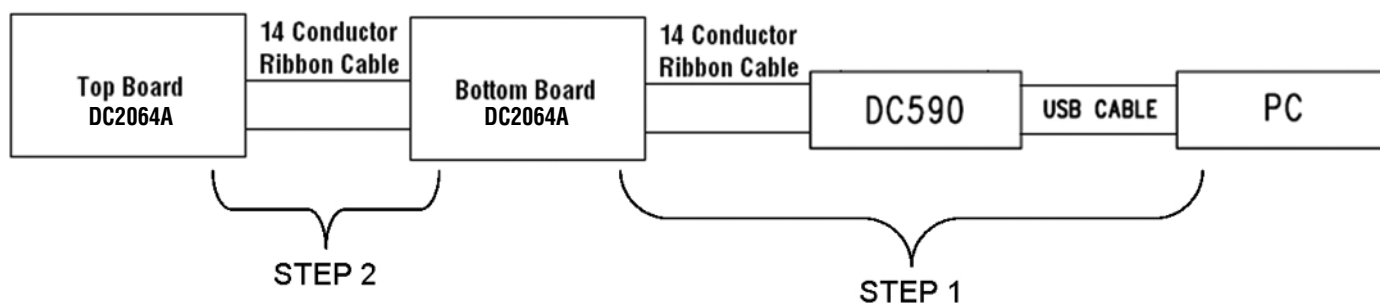


Figure 20. Two DC2064A SPI Connection Sequence

**QUICK START PROCEDURE**

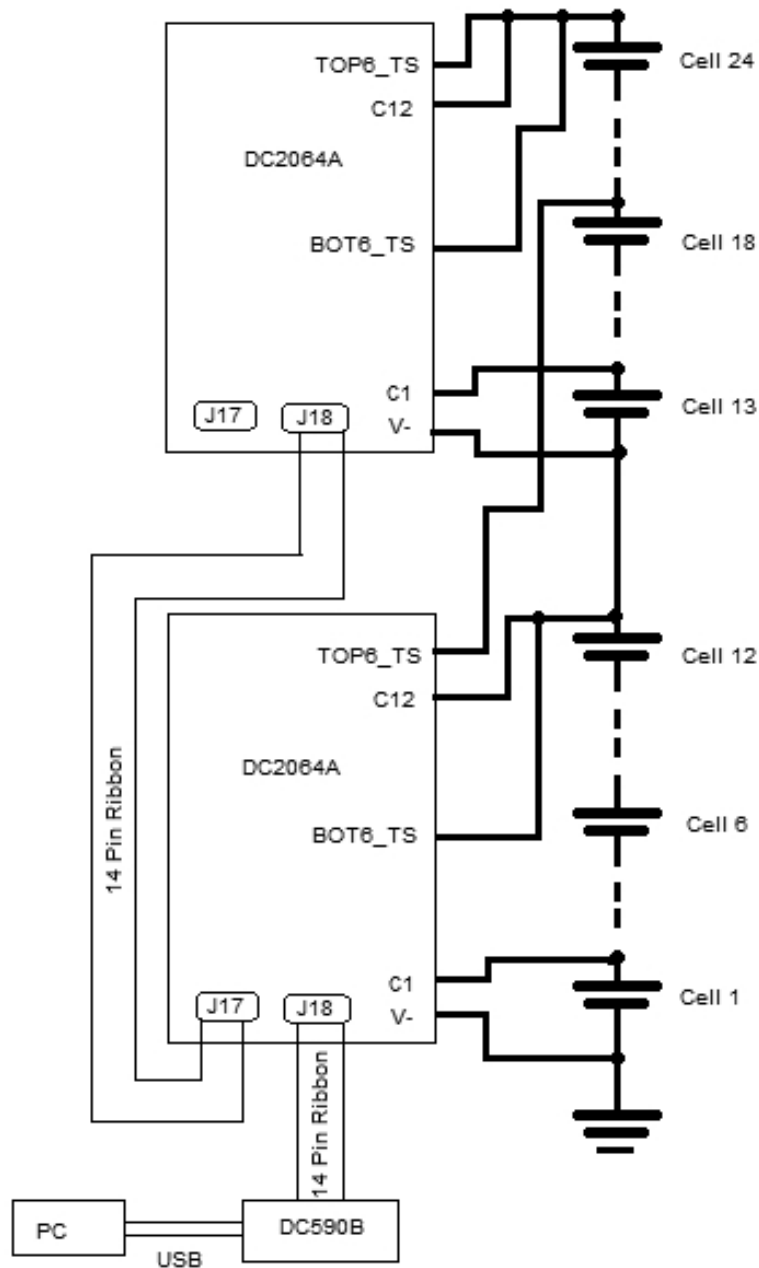


Figure 21. 24 Cell Interconnected Stacks

## QUICK START PROCEDURE

On the LTC6803-2 tab on the DC2064A GUI, the Number of Boards in the System drop down box will need to be changed to 2. Make sure the address for each board in the Hex Address box matches the address set by the A0 to A3 jumpers on the respective DC2064A board. The board selection buttons on the bottom left side of the GUI highlight which board is selected in maroon, as shown and the set hexadecimal address is displayed under each board. To change the hexadecimal address on the GUI, select the board to change by clicking on the appropriate board selection number and then select the correct address in the Hex Address Box.

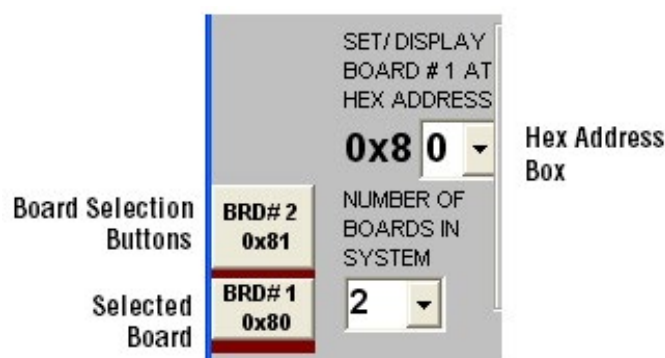


Figure 22. DC2064A GUI Board Selection Controls

To set up the charge and discharge actions for each LTC3300, the appropriate board must be selected first and then the commands for each LTC3300-1 can be selected and written to the LTC3300-1 tab. When all the desired actions are selected and written to the four LTC3300-1 ICs, then a single execute command will send an execute command to both boards simultaneously provided the Broadcast Execute/Suspend button is selected as shown in Figure 23.



Figure 23. Broadcast Execute/Suspend Tab

## Additional Circuitry

Additional circuitry has been added to increase the robustness of the design for fault insertions.

## Cell 6 Wire Disconnection

A 10A 200V Schottky diode has been added for a high current path when the connection between battery cells is broken when a battery stack load is present. The 200V reverse voltage rating of the diode was selected to minimize the reverse leakage current at a battery voltage of 4.2V. The 10A current rating was selected for its low forward voltage drop which will minimize the current in the parallel diode within the LTC3300-1 as well as surviving the fusing current of the 7A fuses on the DC2064A.

Two overvoltage detection circuits have been added to the design that will sense an overvoltage condition on Cell 6 and Cell 7 when a disconnection of the Cell 6 wire connection between battery Cell 6+ and battery Cell 7- of the battery stack occurs. When Cell 6 is being discharged and other cells controlled by the U1, the lower LTC3300-1, and U2, the upper LTC3300-1 are operational, an overvoltage can occur on Cell 7. The overvoltage on Cell 7 will shut down the operation of Cell 7-Cell 12 but Cell 1-Cell 6 will continue to operate. The overvoltage sensing circuit Q15, D21, D23 and R51 will turn off the operations of Cell 1-Cell 6 through the internal overvoltage protection circuit within the LTC3300-1 of U1.

A similar event occurs when Cell 6 is operating in the Charge Mode and the Cell 6 connection from the board to the battery is lost. The overvoltage on Cell 6 will shut down the operation of Cell 1-Cell 6 but Cell 7- Cell 12 will continue to operate. The overvoltage sensing circuit Q16, D22, D24 and R52 will turn off the operations of Cell 7-Cell 12 through the internal overvoltage protection circuit within the LTC3300-1 of U2.

## QUICK START PROCEDURE

### Cell Bypass Capacitors

The DC2064A contains bypass capacitors from the cell connections and the stack connections. These capacitors have a dual function of smoothing the high triangular current wave before the current travels down the inter-connecting wires to the cells and they also help balance the voltage between cells when hot-plugging cells in a random order. The RMS current rating of these capacitors is a critical parameter for these bypass capacitors as well as their physical size. These high triangular current waveforms produce an RMS current that passes through the capacitors which result in an internal heat rise. Larger physical size MLCC capacitors have higher RMS current rating due to their greater surface area to dissipate the heat rise. The capacitance of MLCC capacitors decreases with applied voltage and this must be taken into account when selecting the capacitance value. If a connection is lost during balancing, the differential voltage seen by the LTC3300-1 power circuit on each side of the break may increase or decrease in depending on whether the power stage is charging or discharging and where the break occurred. The worst-case scenario is when the balancers on each side of the break are active and balancing in opposite directions. Here the differential voltage will increase rapidly on one side and decrease rapidly on the

other. The LTC3300-1 contains an overvoltage protection comparator which monitors the cell voltage and will shut down all balancers before the differential voltage on any cell input reaches the maximum absolute voltage rating.

Each cell node must have an equivalent capacitance across it to prevent an overvoltage condition when randomly connecting cells to the LTC3300-1 battery balancer circuit. In addition to the smoothing capacitors across each balancer power circuit, there are capacitors across the Cx pins of the LTC3300-1 to reduce high frequency noise on these pins and capacitors across adjacent cells to act as a reservoir of charge for the cell's MOSFET gate driver circuits. These reservoir capacitors must also be of equal value to maintain the balancing of voltage and a capacitor of 2x the value of the reservoir capacitor must be connected between C1 and V<sup>-</sup> of the lowest LTC3300-1 and from the top cell to the cell below it to insure an equal voltage across all cells when the battery stack is initially connected. Figures 25 and 26 detail these capacitor connections and their values. The reservoir capacitors must be large compared to the capacitors across the Cx pins to force the MOSFET gate charging current to flow through the reservoir capacitors. An effective 10:1 ratio between these cell capacitors was selected when considering that a capacitor across two cells would result in a 5:1 ratio.

# QUICK START PROCEDURE

The screenshot displays the GUI for the LTC3300-1-LTC6803-2 BMS. It features a grid of 12 cell voltage readouts (CELL1-CELL12) with 'READ Only' checkboxes and 'Mask'/'DCC' options. A 'BOARD' indicator shows '1'. The 'CONFIGURATION REGISTERS' section shows 'E1 00 00 00 00 00' for both read and write operations. A 'LEGEND' indicates 'THERMAL SD!' and 'DANGER!' flags. The 'SET VOLTAGE LIMITS' section shows 'VUV' limits at -0.768V and -0.744V. The 'SET I/O MODE CFGR0' section has several checked options like 'WDTB STATUS bit7' and 'GPIO1 bit5'. The 'SELF TEST START A/D' section includes 'CELL VOLT', 'OPEN WIRE', and 'TEMP' options. A 'PACKET ERROR CODE' section shows '49 | CE | D7 == D7'. The bottom right contains 'DCC PERMITTED' and 'START CELL hold DCC' buttons. A status bar at the bottom shows 'LTC3300-1' and 'LTC6803-2-4\_GUI\_V06'.

Figure 24. DC2064A LTC6803-2 Setup Screen

## QUICK START PROCEDURE

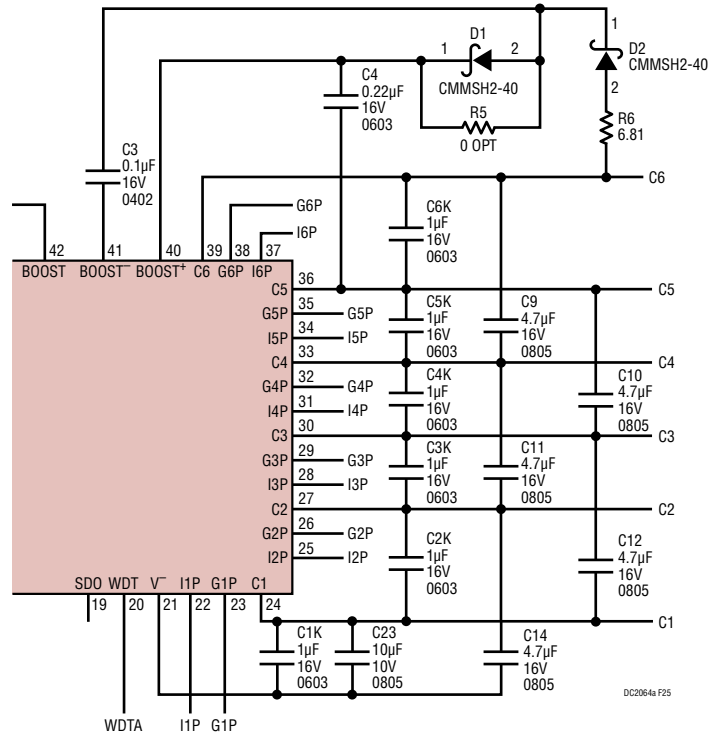


Figure 25. Bypass Capacitors on Lowest LTC3300-1

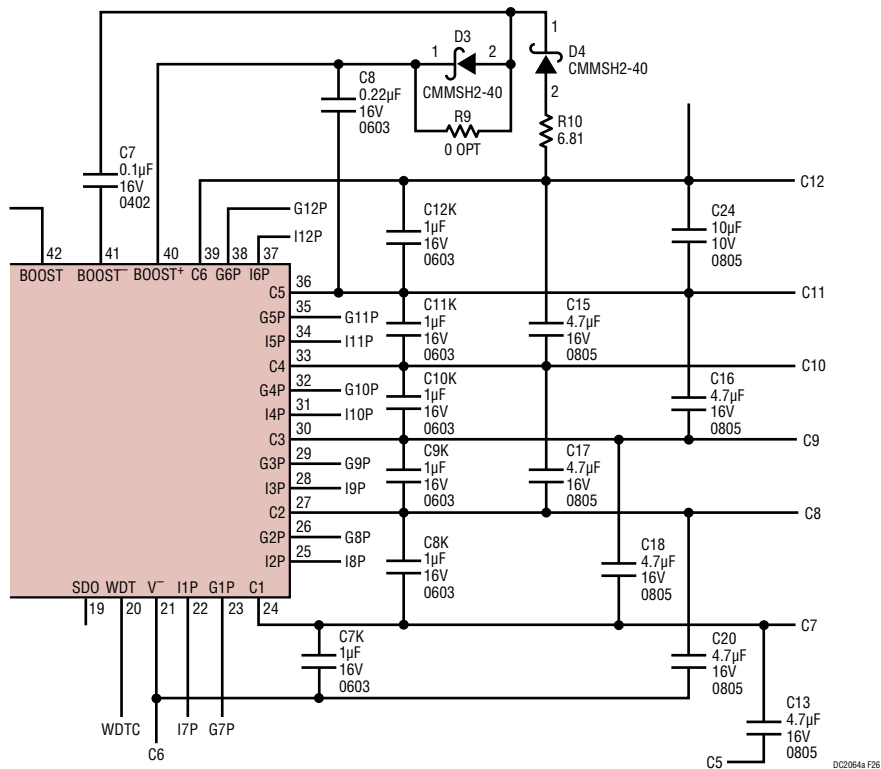


Figure 26. Bypass Capacitors on the Top LTC3300-1

# QUICK START PROCEDURE

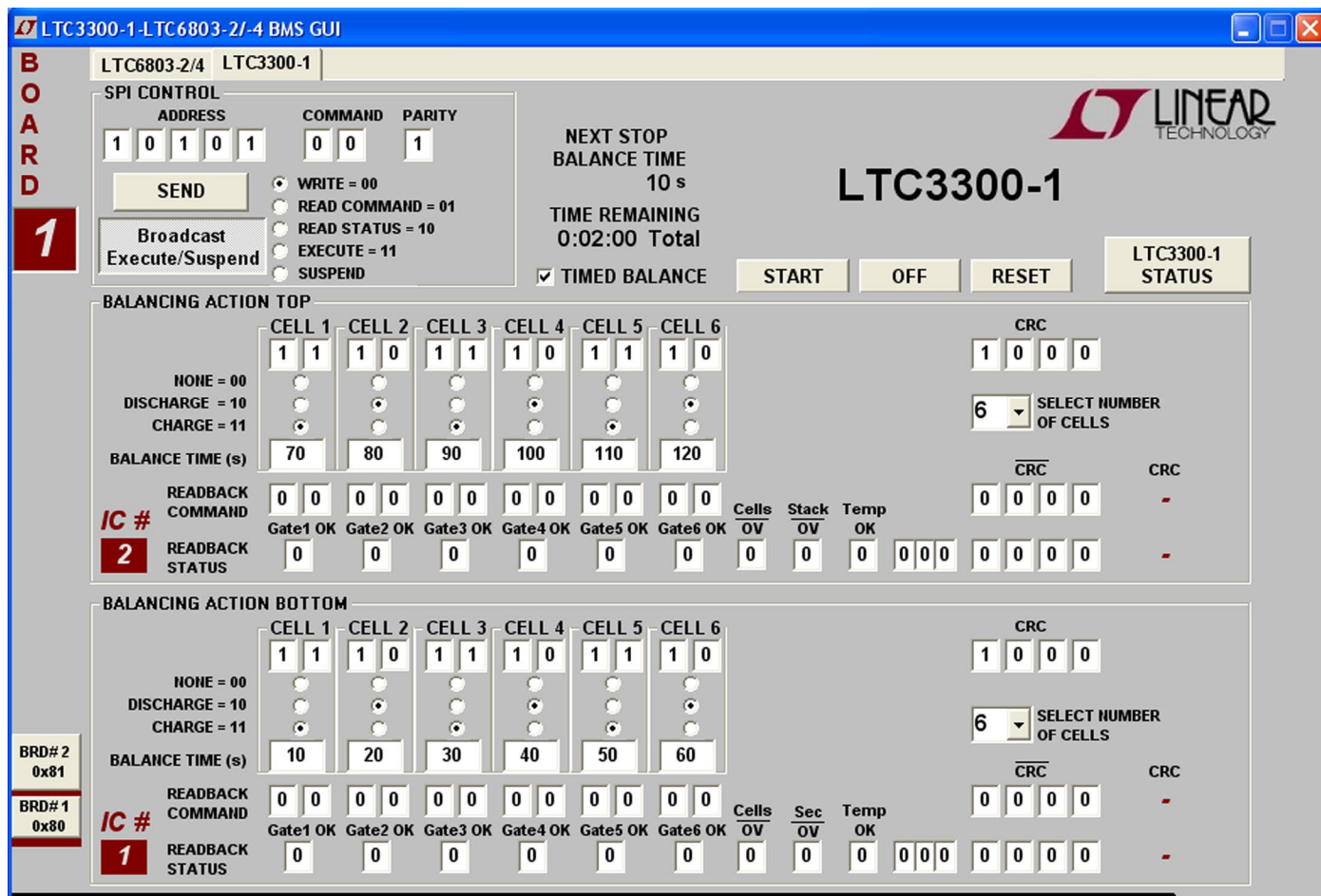


Figure 27. DC2064A LTC3300-1 Setup Screen with Timed Balance Controls

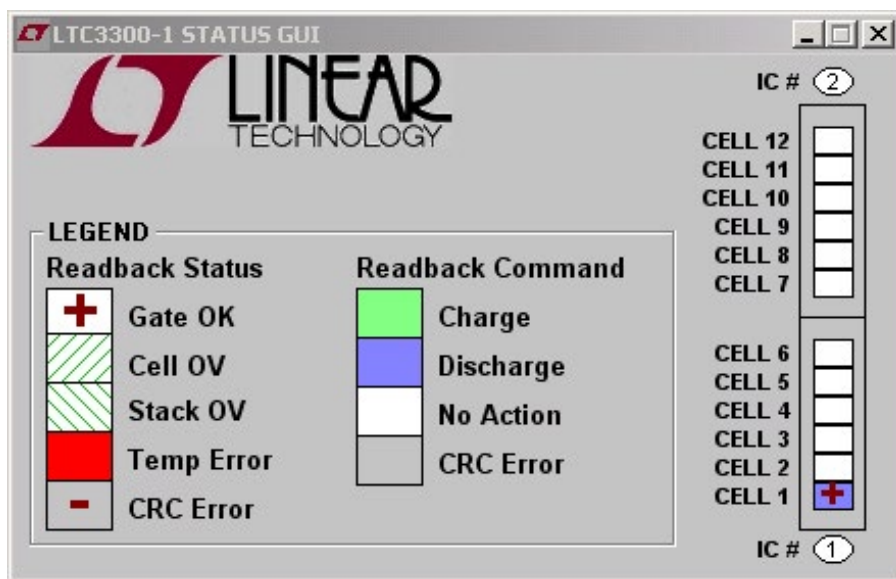


Figure 28. DC2064A LTC3300-1 Status GUI Screen

## QUICK START PROCEDURE

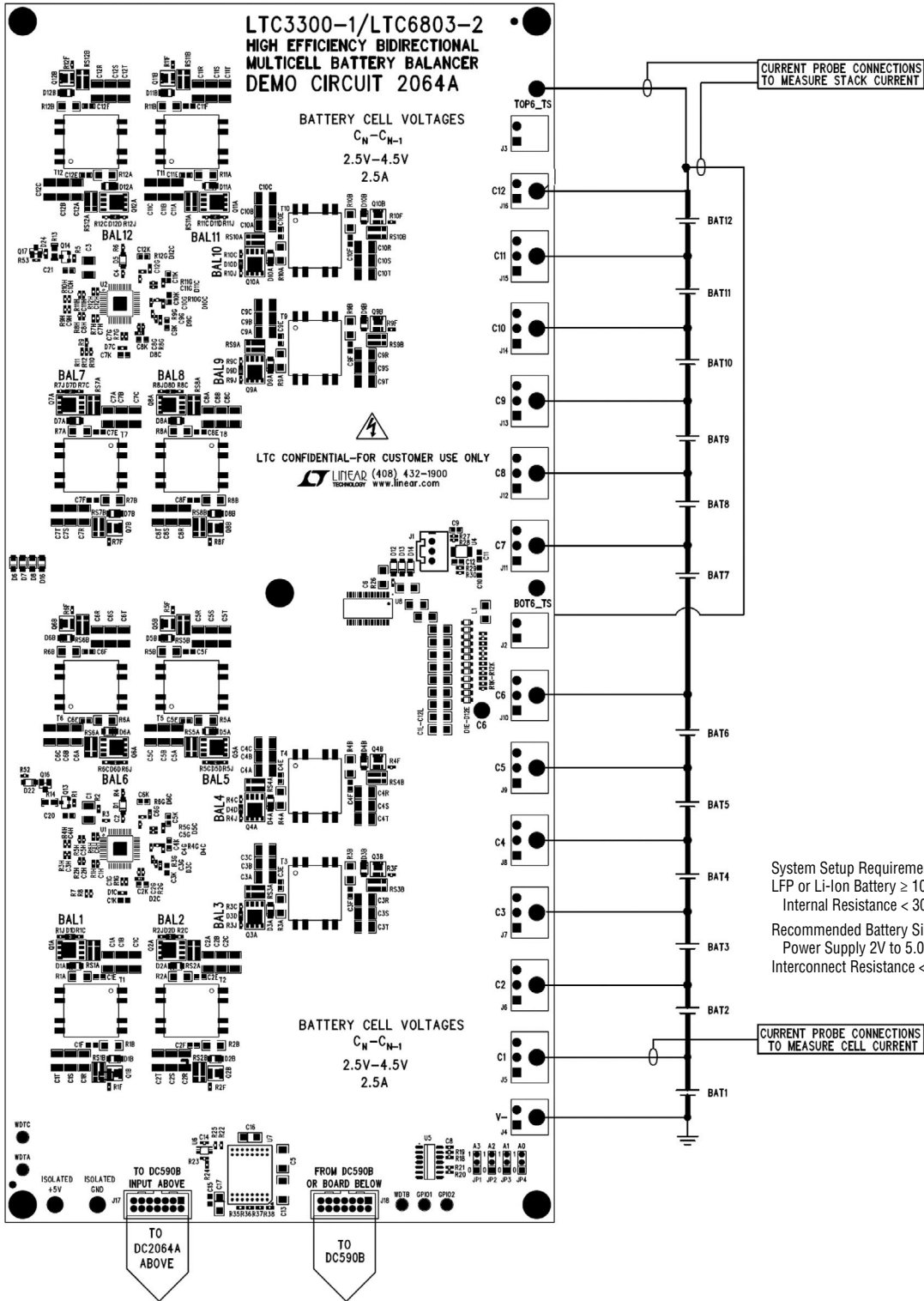
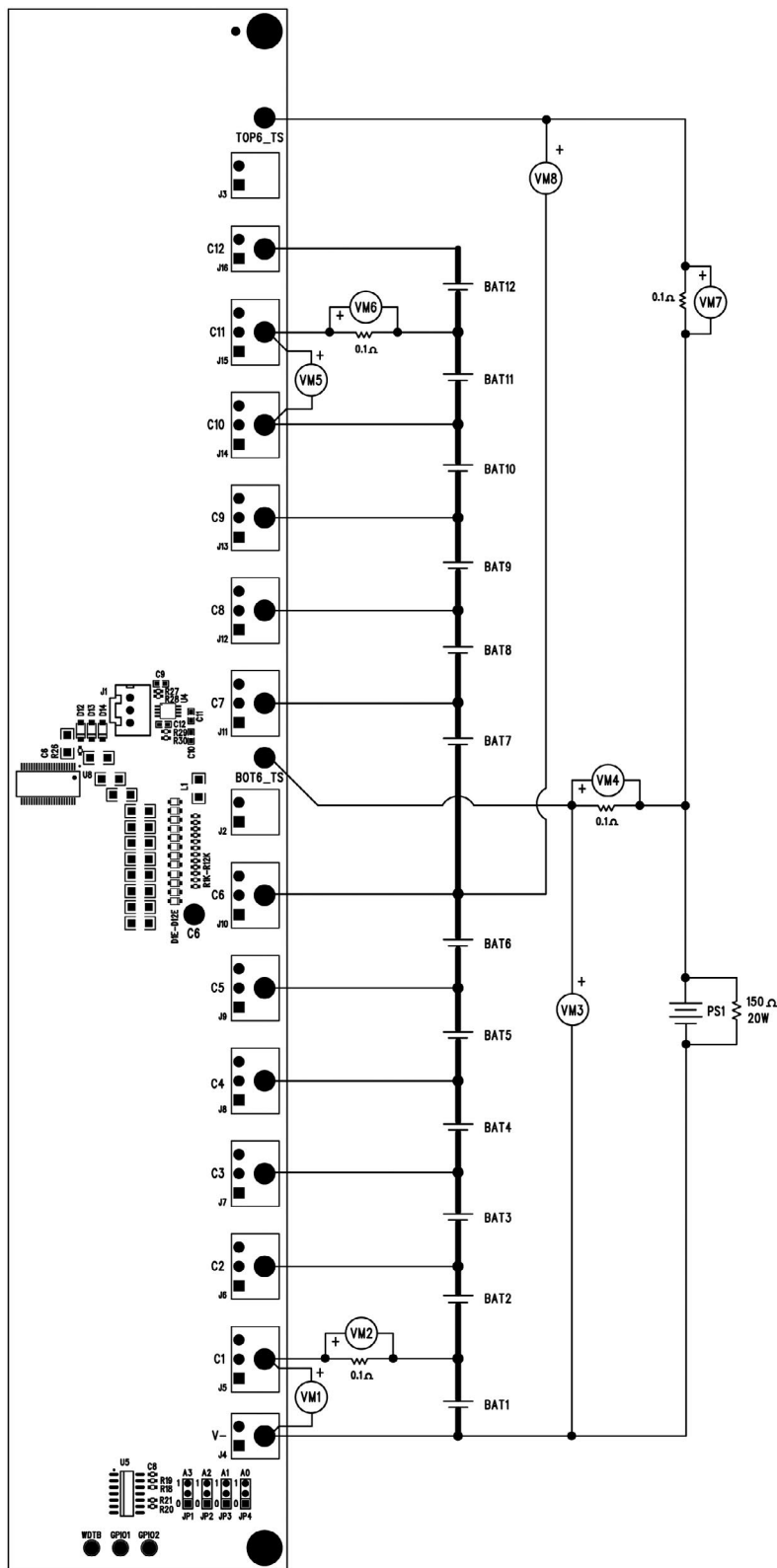


Figure 29. Proper Measurement Equipment Setup for Bidirectional Cell Balancer

Note: All connections from equipment should be Kelvin connected directly to the Board Pins which they are connected to on this diagram and any input, or output, leads should be twisted pair, where possible.



**QUICK START PROCEDURE**

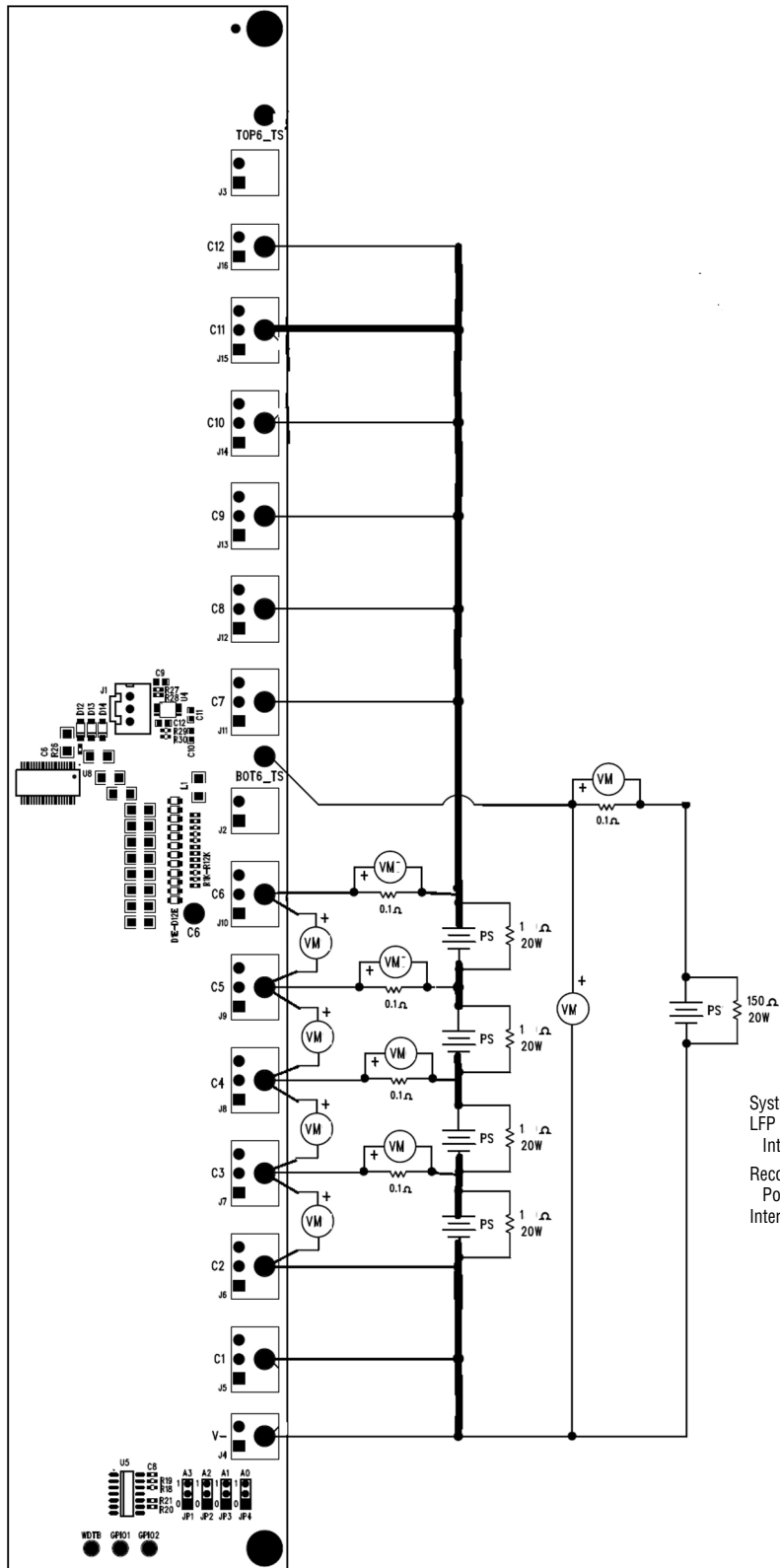


System Setup Requirements:  
 LFP or Li-Ion Battery ≥ 10Ahr  
 Internal Resistance < 30mΩ

Recommended Battery Simulator:  
 Power Supply 2V to 5.0 V ±10A  
 Interconnect Resistance < 25mΩ

Figure 30. Proper Equipment Setup for Cell Balancer Efficiency Measurements

## QUICK START PROCEDURE



System Setup Requirements:  
 LFP or Li-Ion Battery ≥ 10Ahr  
 Internal Resistance < 30mΩ  
 Recommended Battery Simulator:  
 Power Supply 2V to 5.0 V ±10A  
 Interconnect Resistance < 25mΩ

Figure 31. Proper Equipment Setup for Minimum Number of Cell Efficiency Measurements

QUICK START PROCEDURE

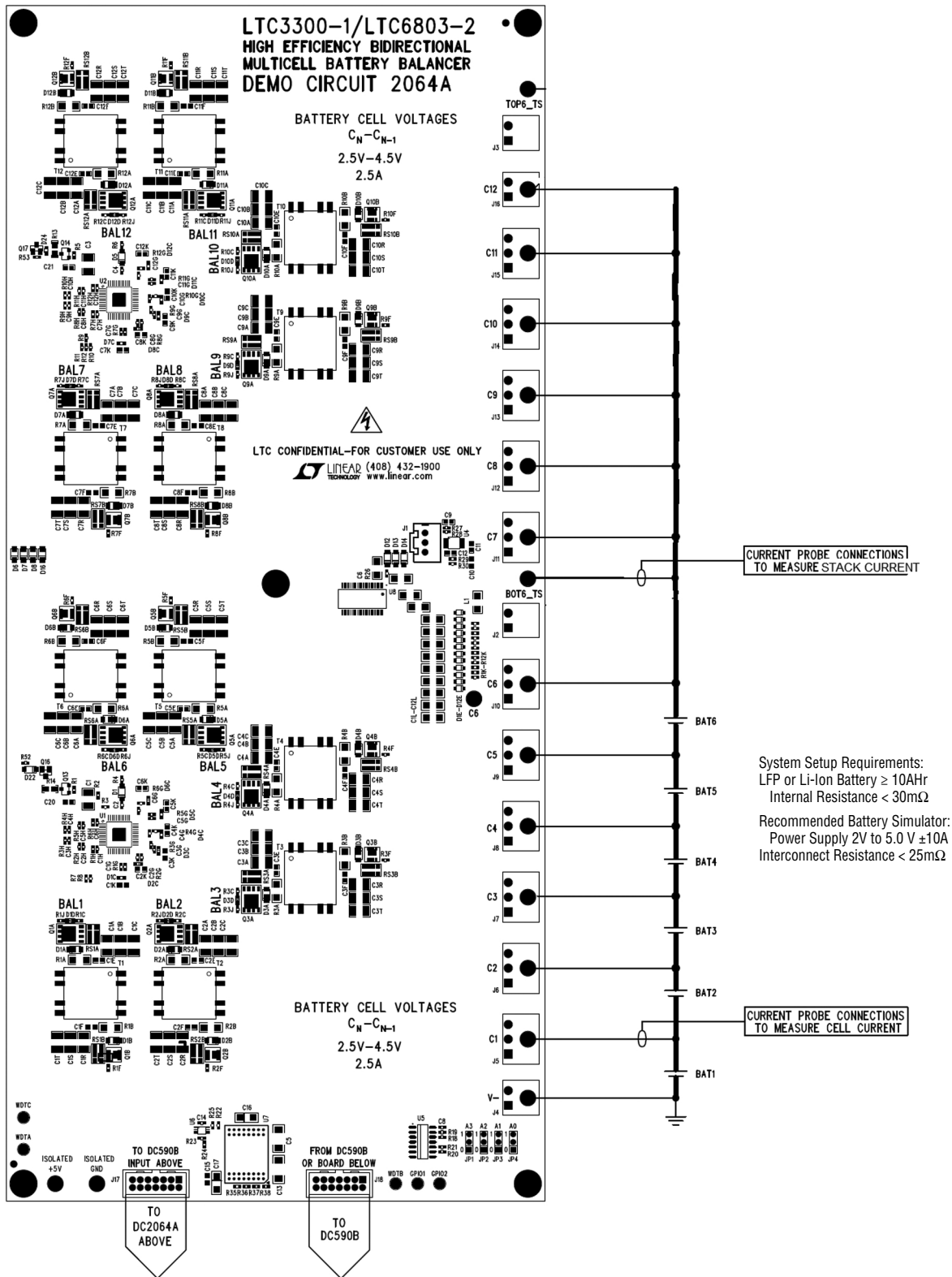


Figure 32. Configuring the Board for Six Batteries

## QUICK START PROCEDURE

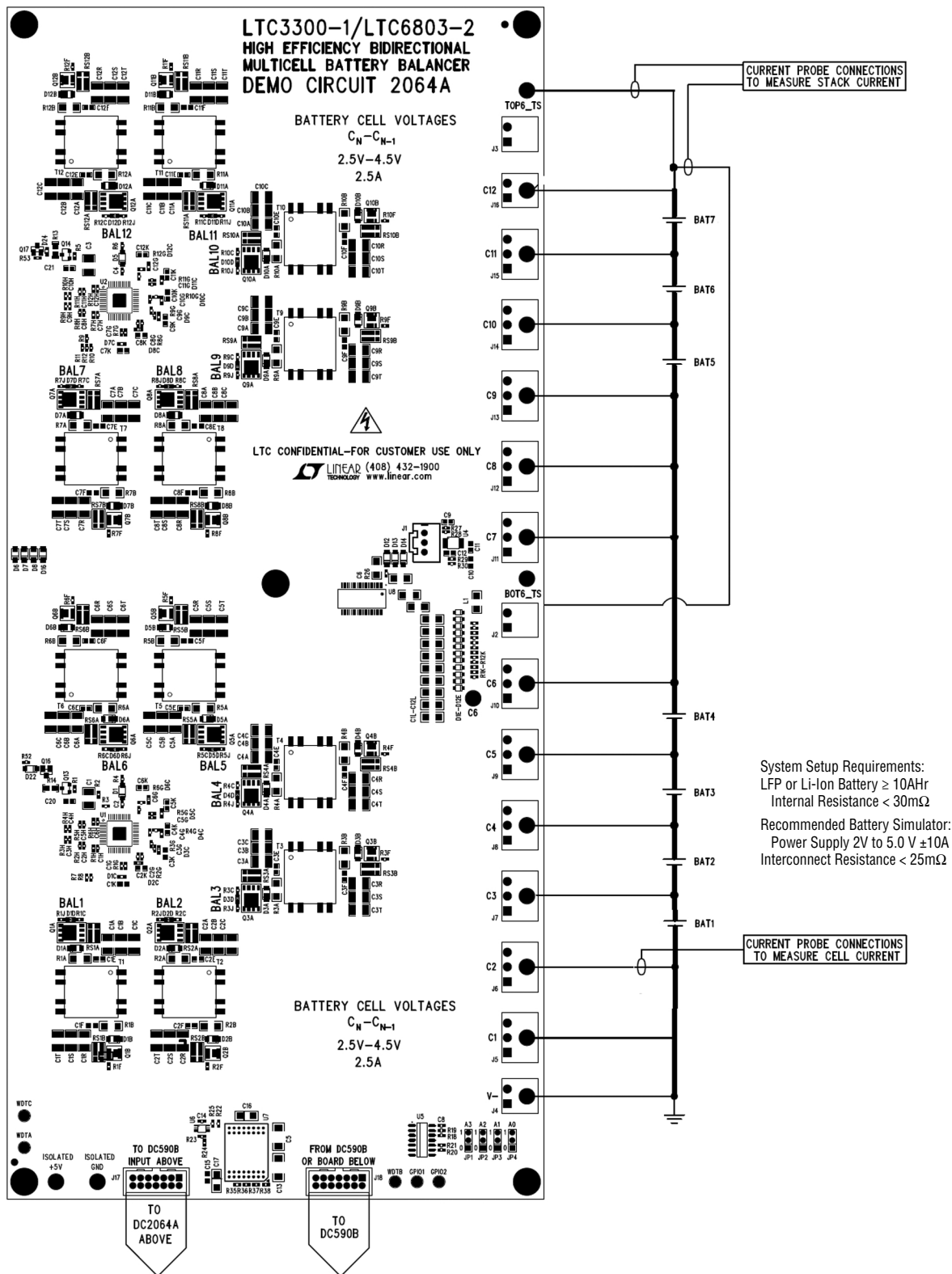


Figure 33. Configuring the Board for Seven Batteries

QUICK START PROCEDURE

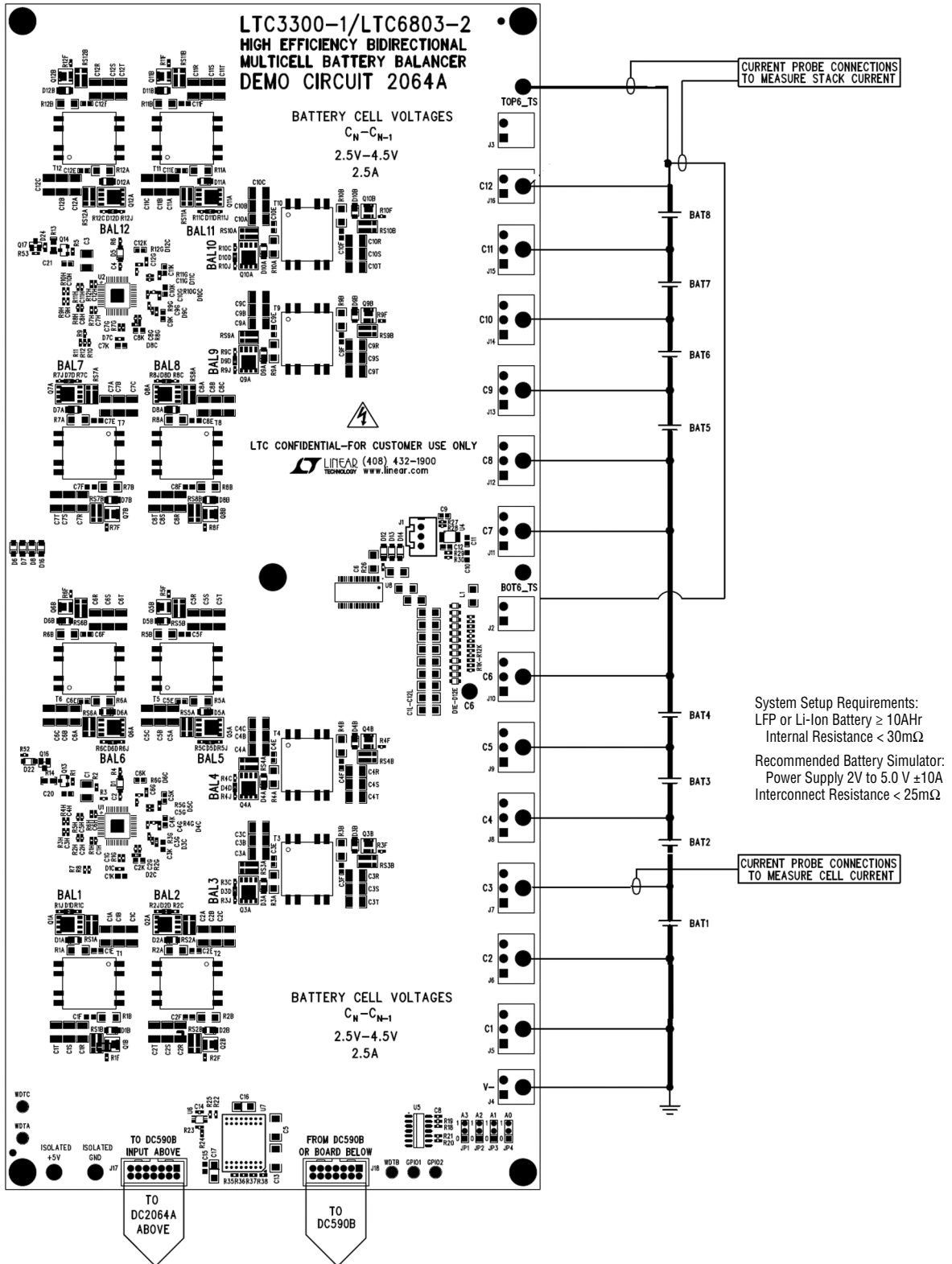


Figure 34. Configuring the Board for Eight Batteries

## QUICK START PROCEDURE

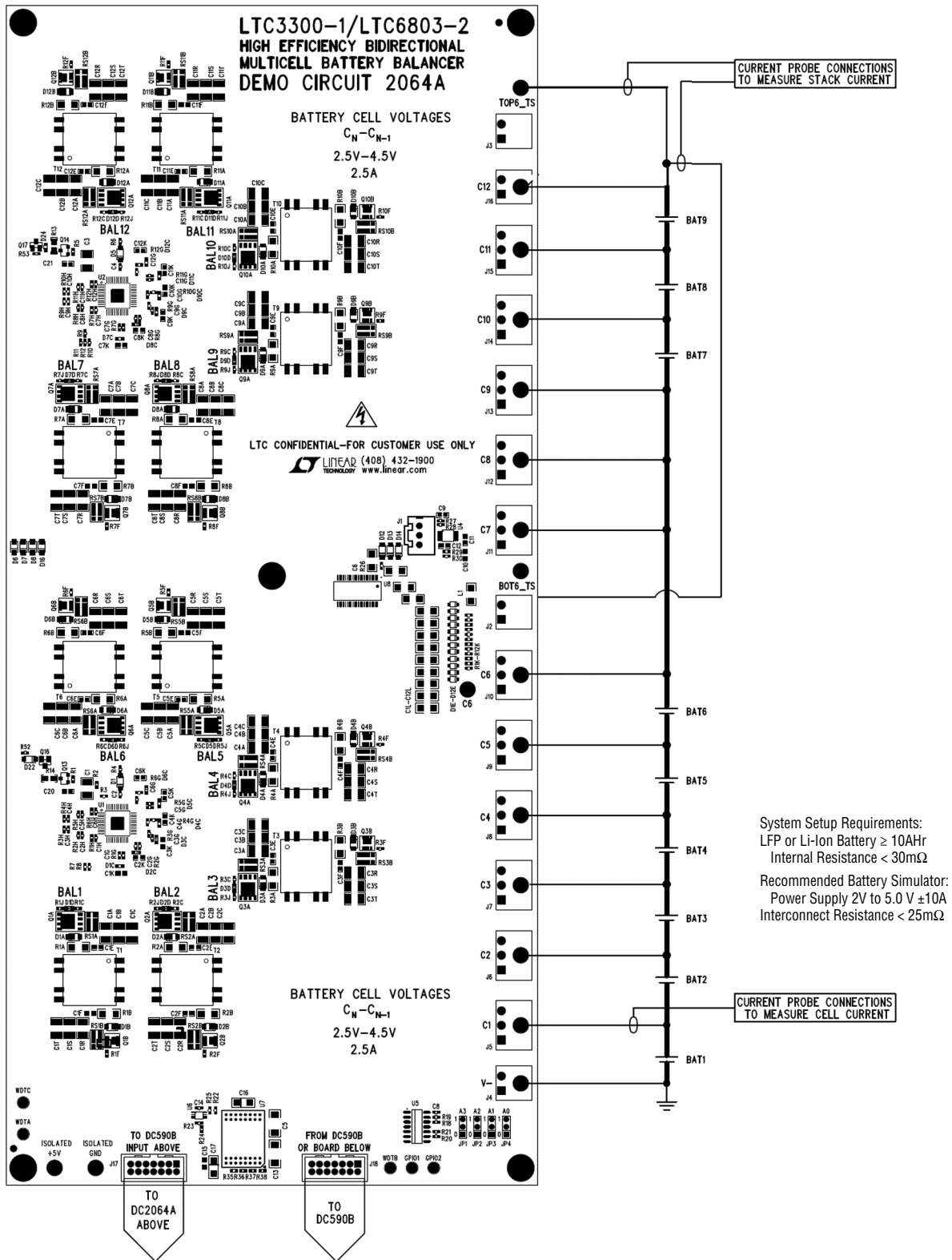


Figure 35. Configuring the Board for Nine Batteries

QUICK START PROCEDURE

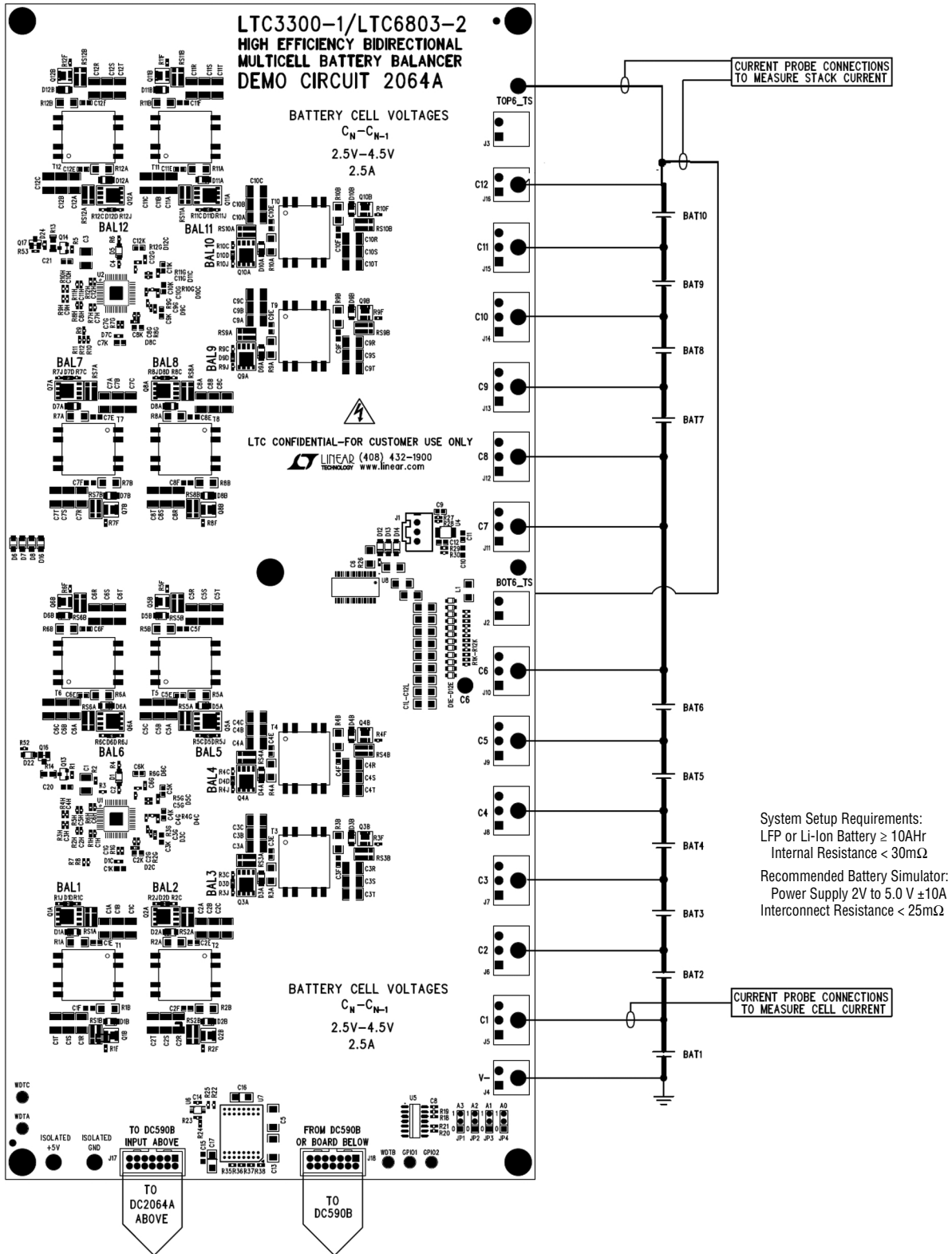


Figure 36. Configuring the Board for Ten Batteries

# DEMO MANUAL DC2064A

## QUICK START PROCEDURE

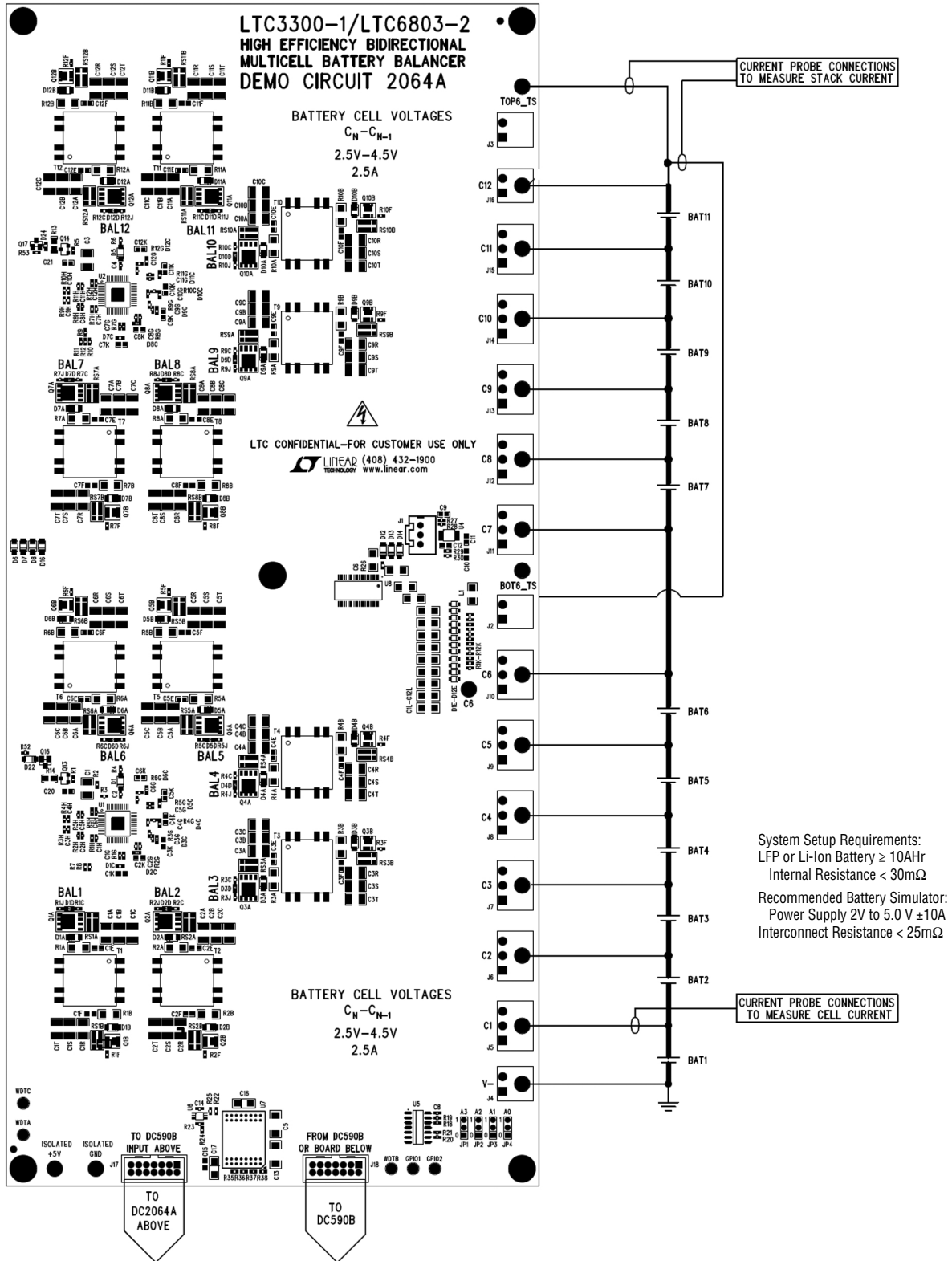


Figure 37. Configuring the Board for Eleven Batteries



**SCHEMATIC DIAGRAMS**

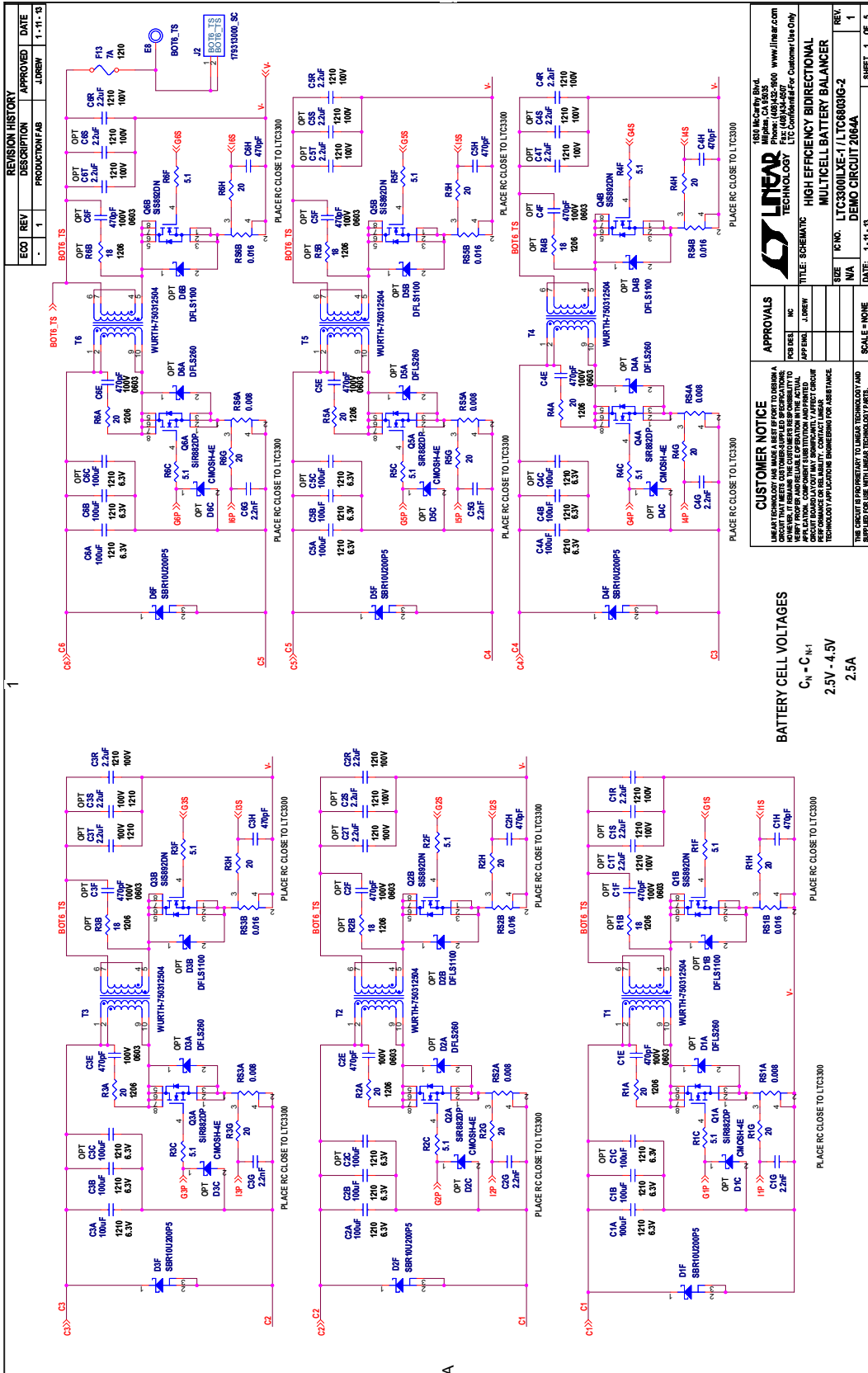
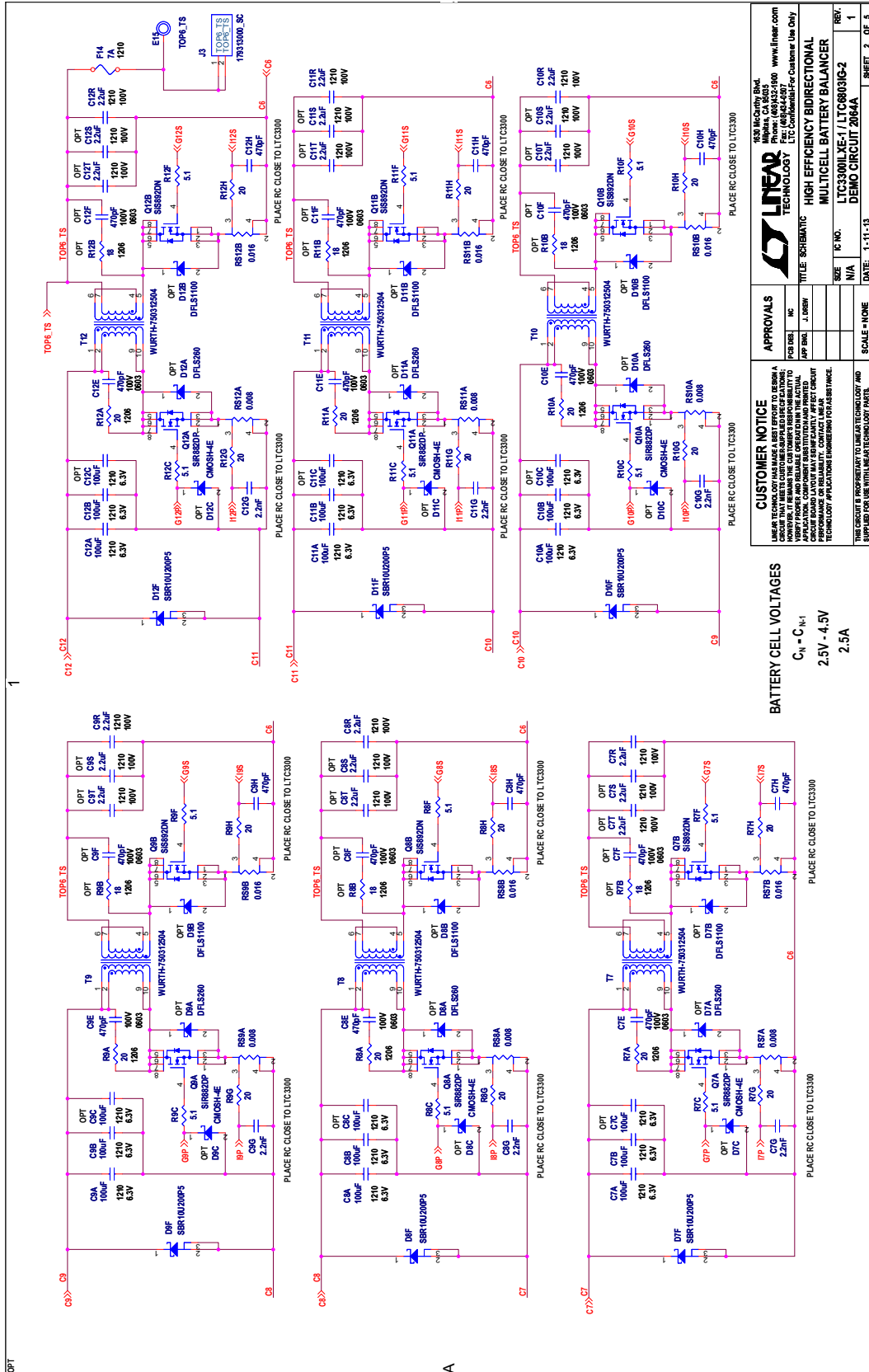


Figure 38. Schematic Diagram Page 1

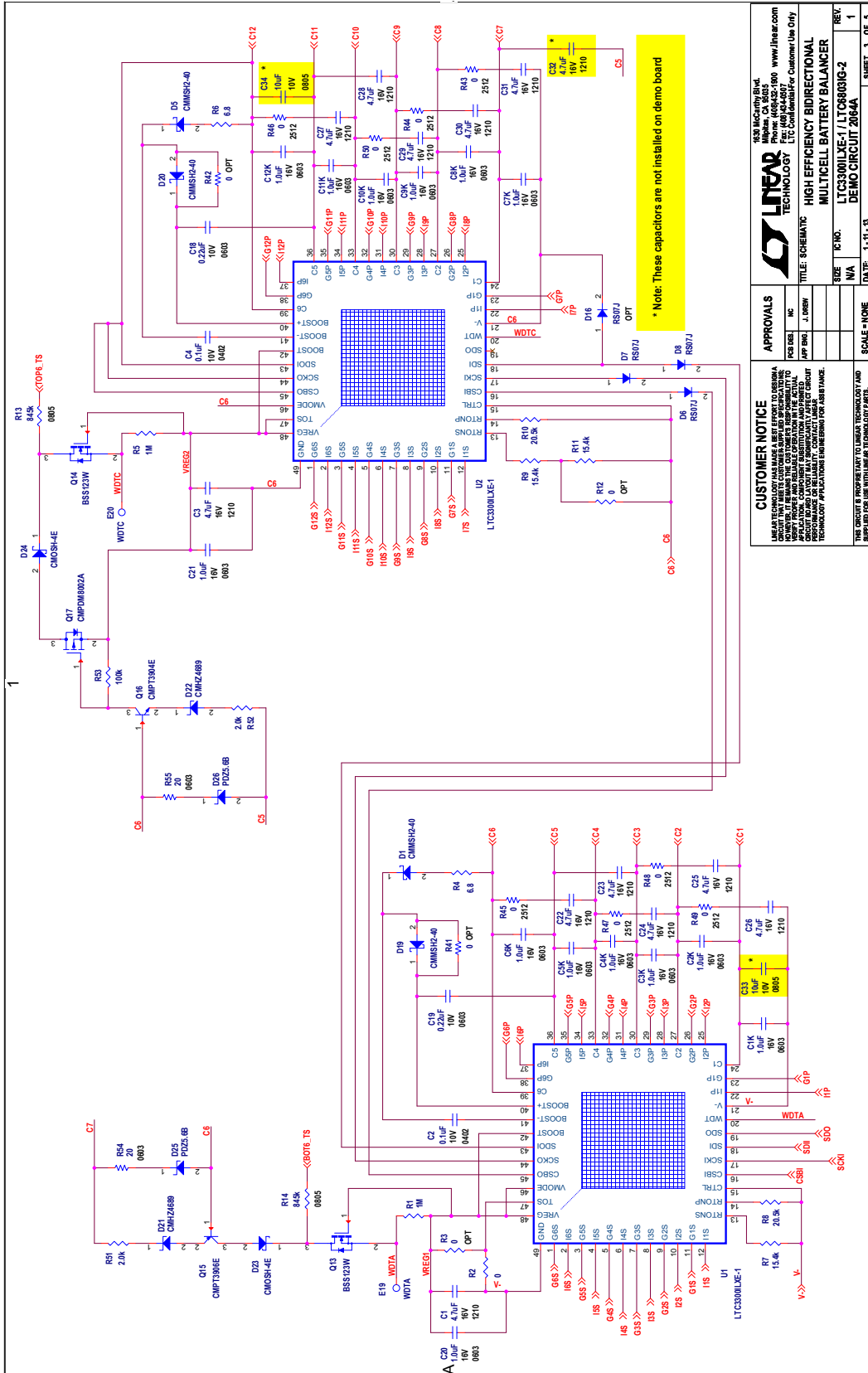
## SCHEMATIC DIAGRAMS



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1351 Massachusetts Ave. Mableton, GA 30148 Phone: (404) 821-7400 Fax: (404) 821-7401 www.linear.com		TITLE: SCHEMATIC IC NO.: LTC3300LXLE-1/LTC8603G-2 DEMO CIRCUIT 2064A	
SCALE: NONE		REV. 1	SHEET 2 OF 5

Figure 39. Schematic Diagram Page 2

**SCHEMATIC DIAGRAMS**



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 J. OSBY

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**High Efficiency Bidirectional Multicell Battery Balancer**

REV. 1  
 DATE: 1-11-13  
 SHEET: 3 OF 5

Figure 40. Schematic Diagram Page 3

SCHEMATIC DIAGRAMS

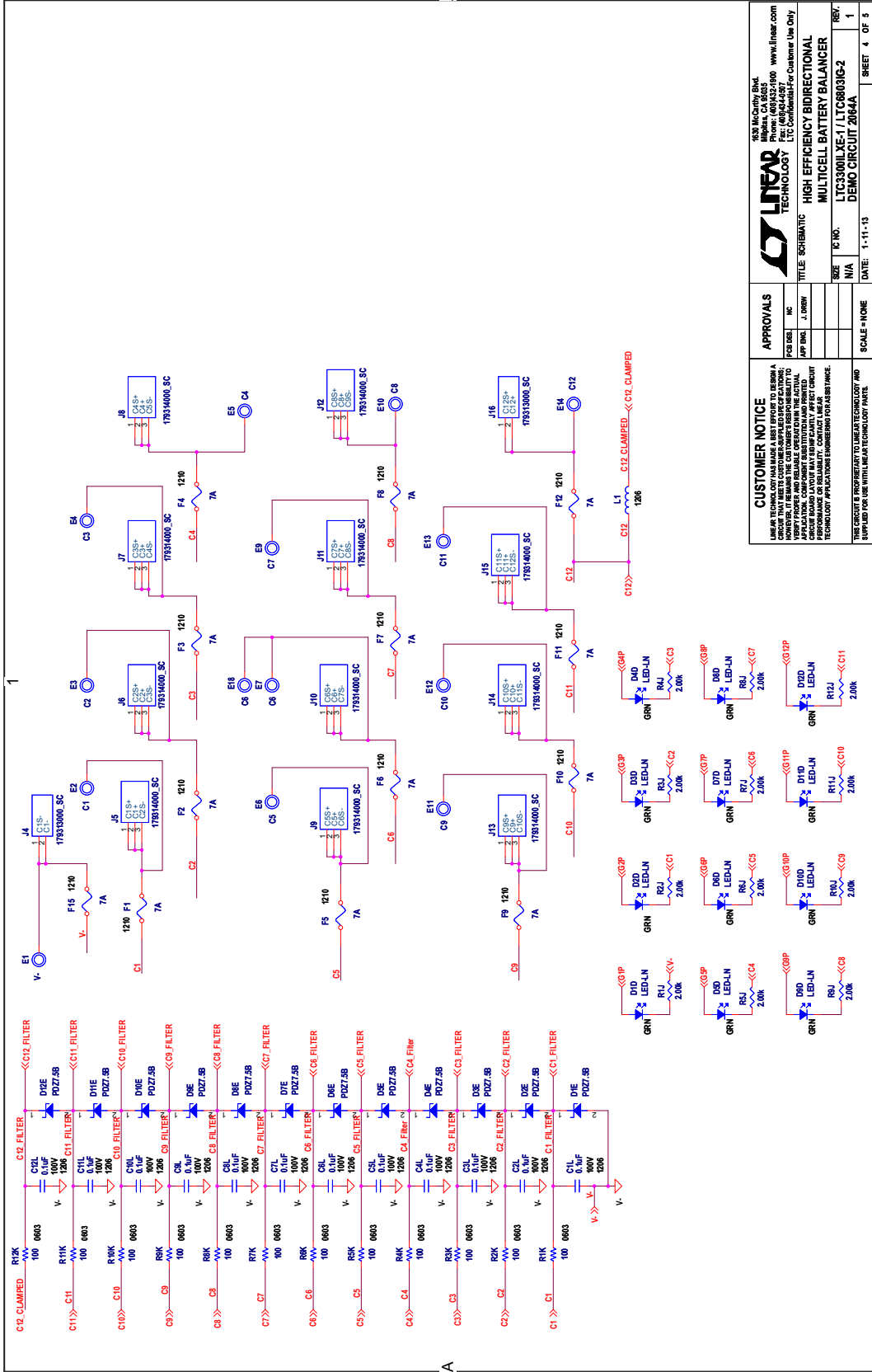
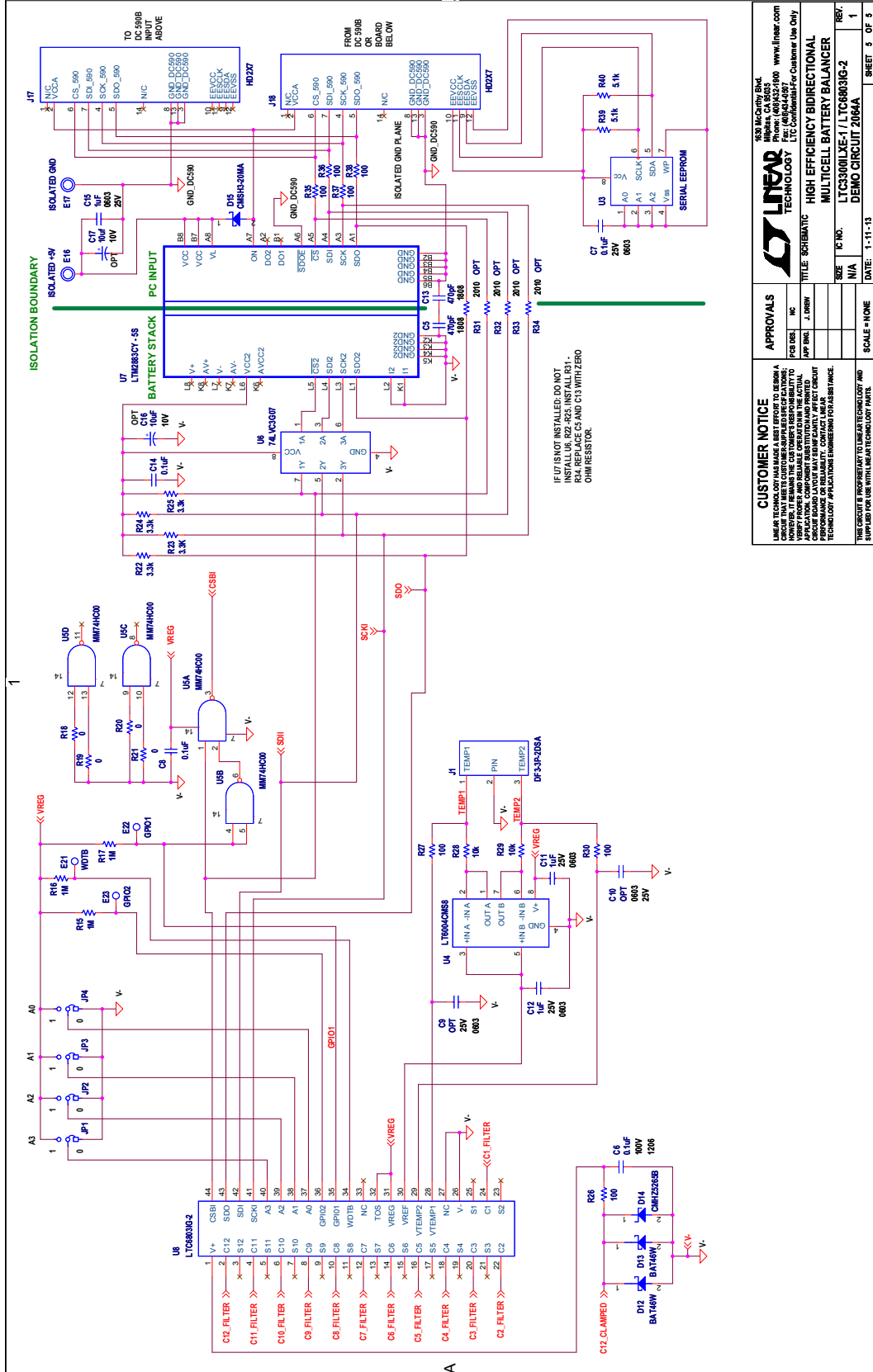


Figure 41. Schematic Diagram Page 4

**SCHEMATIC DIAGRAMS**



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THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.		SCALE	SCALE
<b>LINEAR TECHNOLOGY</b>		DATE: 1-11-13	
930 MCCOY BLVD MILPITAS, CA 95035 Phone: (408) 242-1400 www.linear.com		SHEET 5 OF 5	
<b>LINEAR TECHNOLOGY</b>		LTC3300LXE-1/LTC6803G-2	
HIGH EFFICIENCY BIDIRECTIONAL MULTICELL BATTERY BALANCER		REF: 1	
TITLE: SCHEMATIC		REV: 1	
APP: SDA, J. DREW		REV: 1	
PCB DES: J. DREW		REV: 1	
DATE: 1-11-13		REV: 1	
SCALE: NONE		REV: 1	

Figure 42. Schematic Diagram Page 5

# DEMO MANUAL DC2064A

## PCB LAYOUT

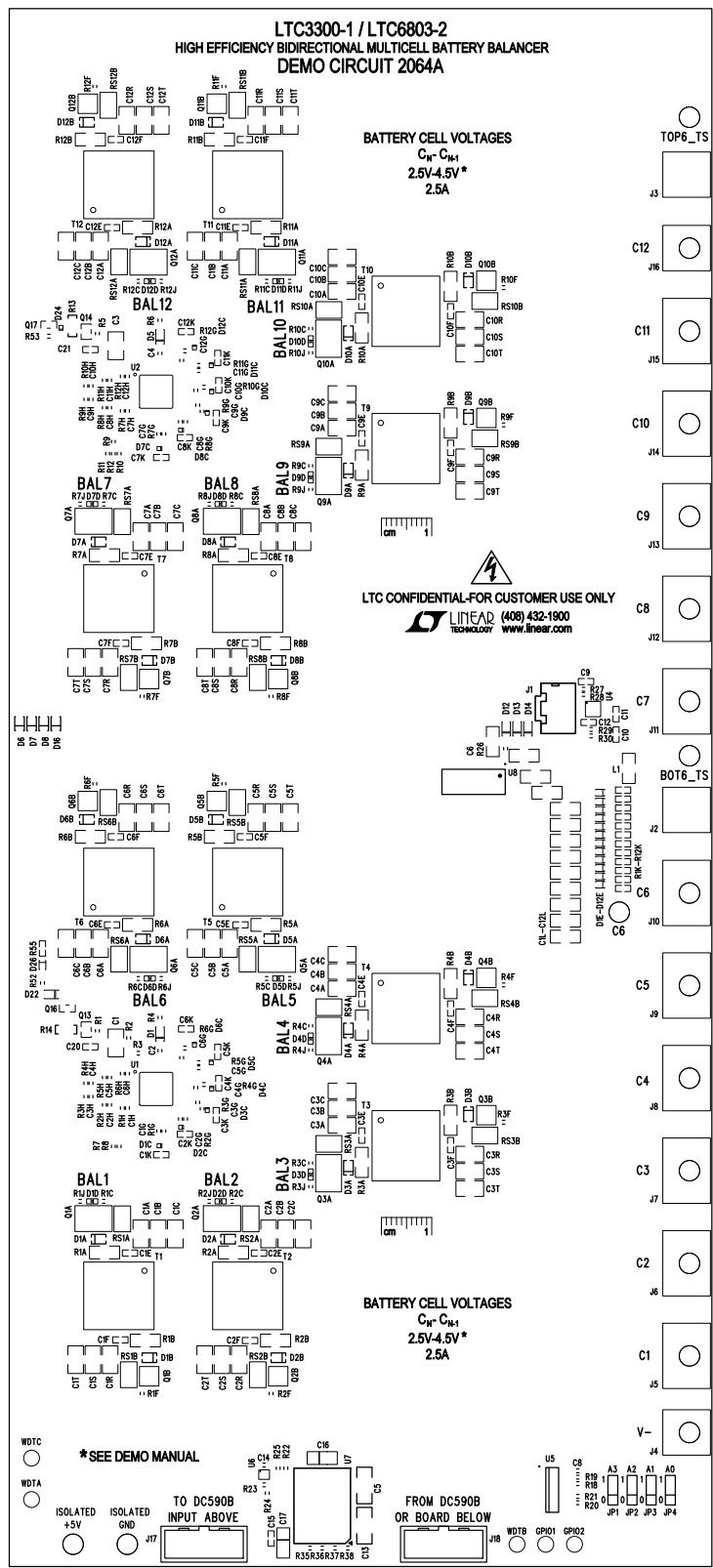


Figure 43. Top Silk Screen

PCB LAYOUT

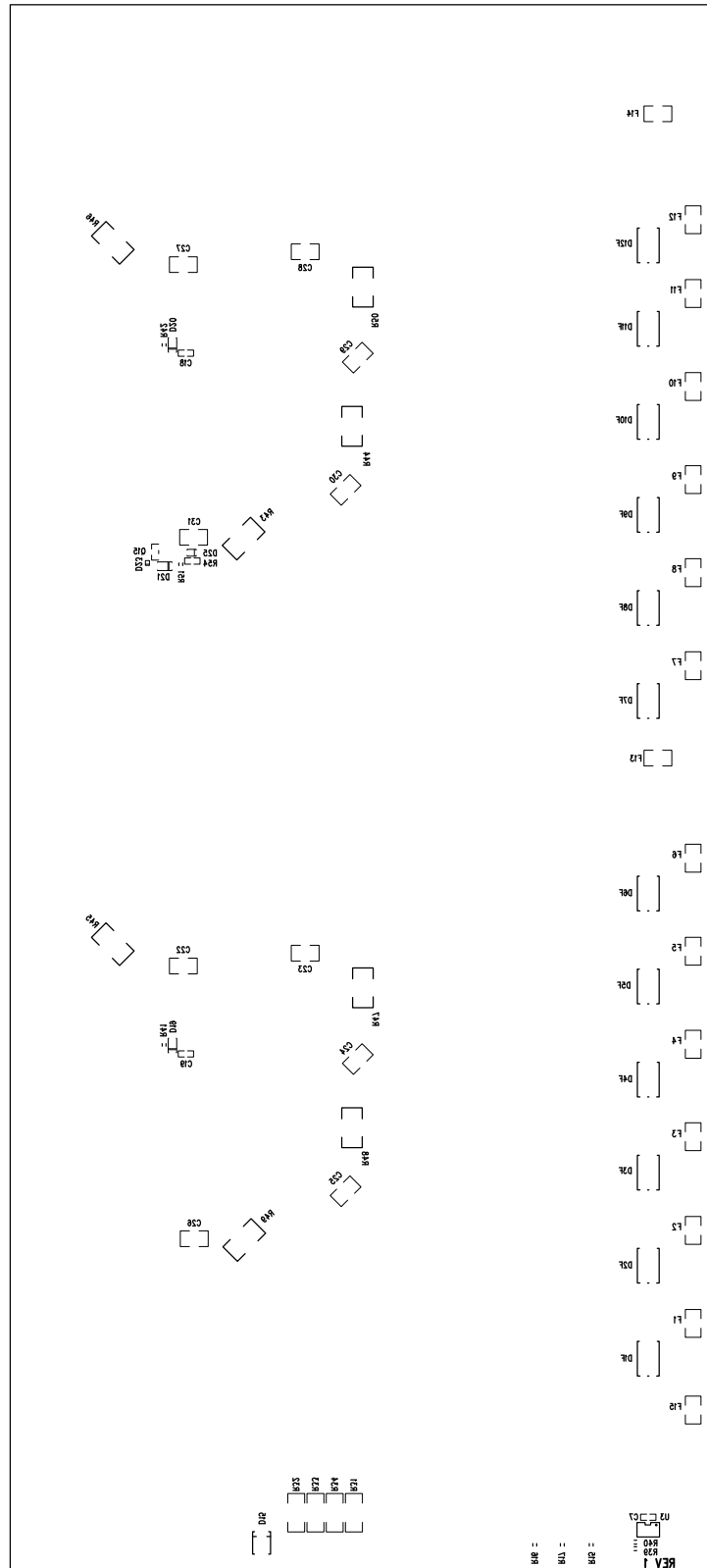


Figure 44. Bottom Silk Screen

PCB LAYOUT

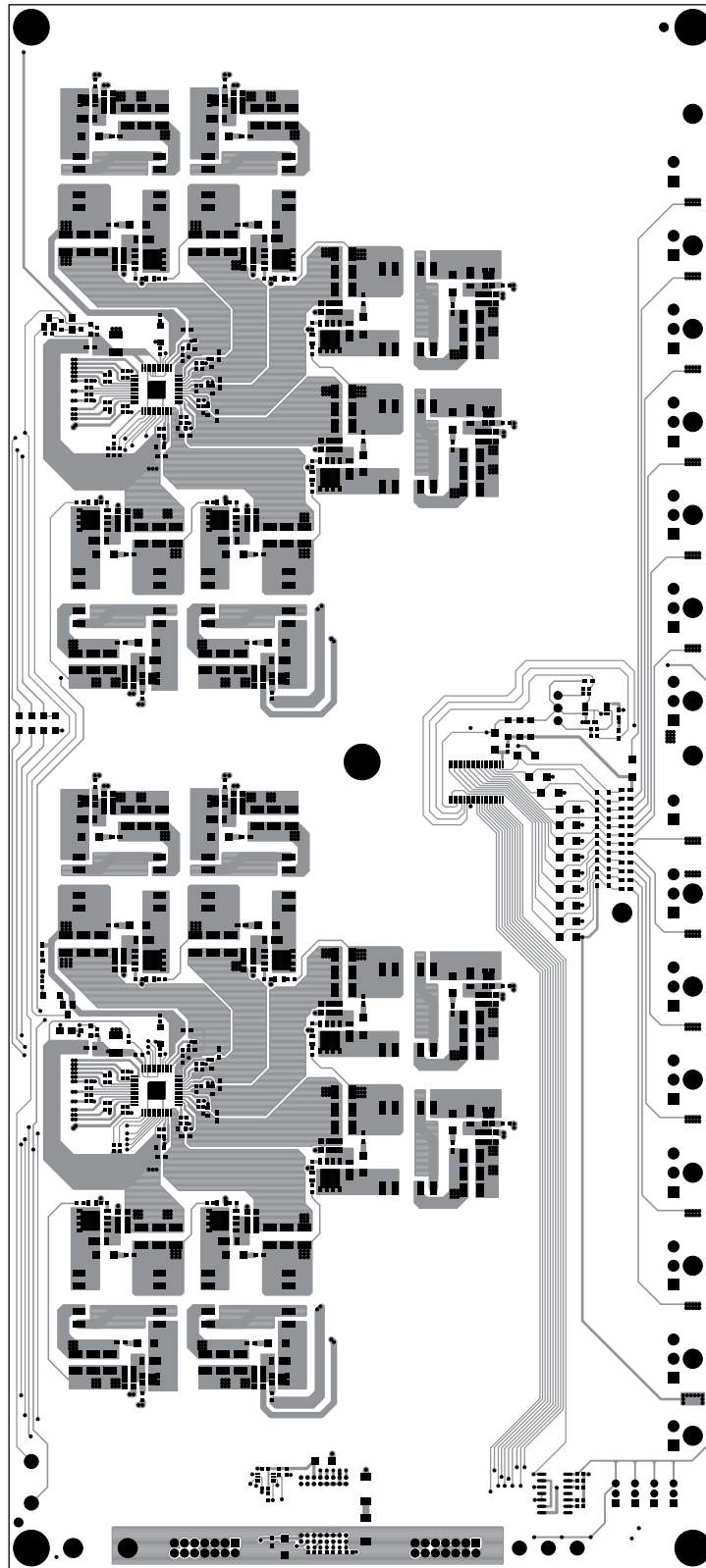


Figure 45. Layer 1



PCB LAYOUT

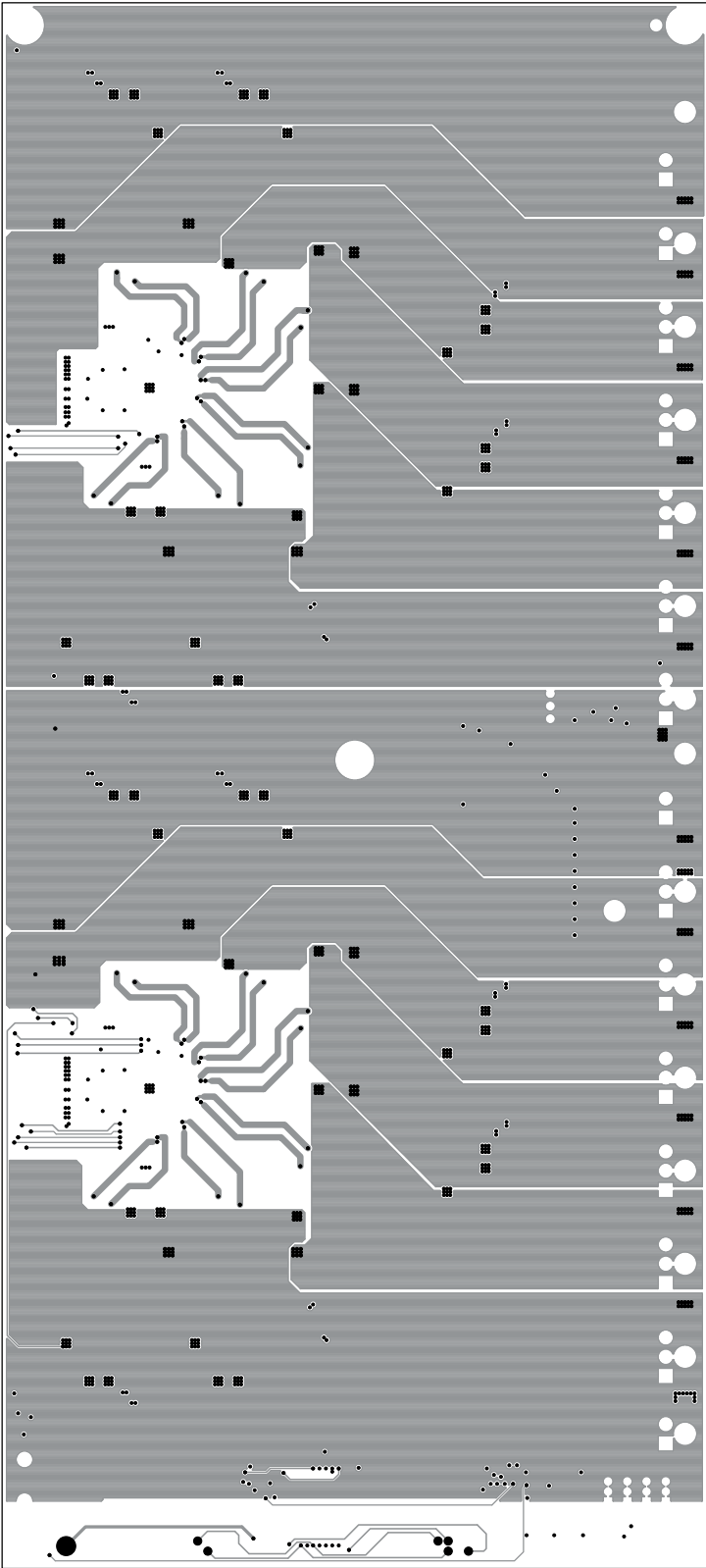


Figure 46. Layer 2

**PCB LAYOUT**

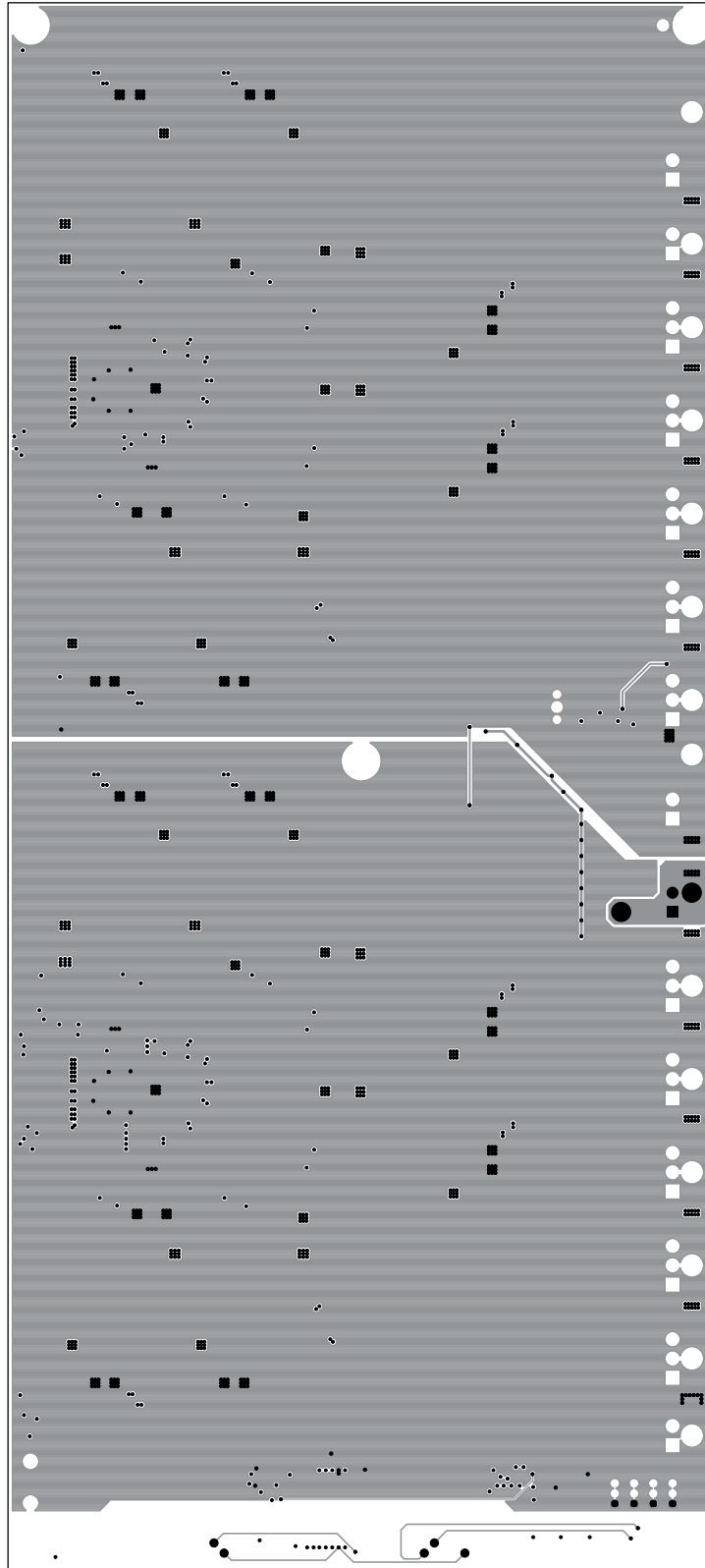


Figure 47. Layer 3

PCB LAYOUT

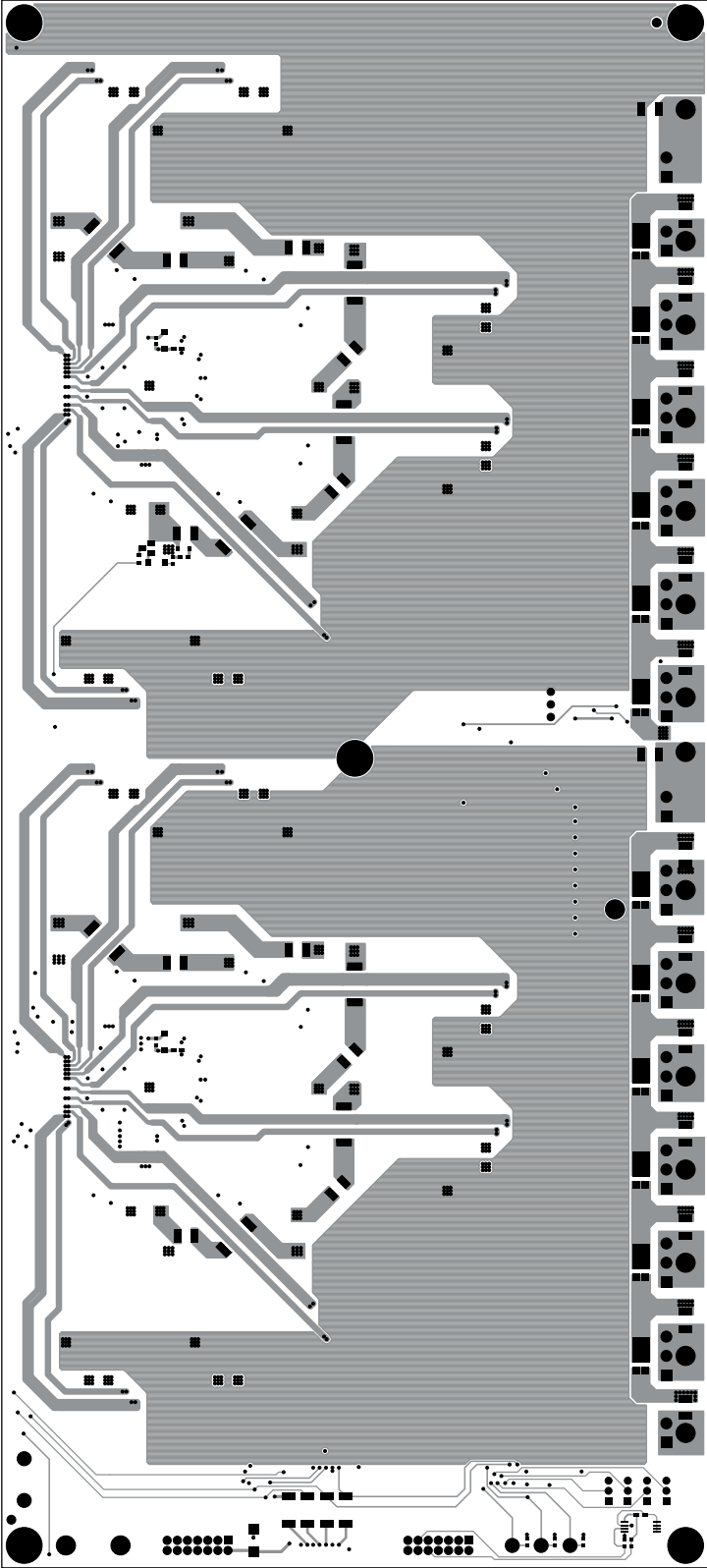


Figure 48. Layer 4

# DEMO MANUAL DC2064A

## PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
<b>Required Circuit Components</b>				
1	24	C1A-C12A, C1B-C12B	CAP.,X5R, 100µF, 6.3V,10%, 1210	MURATA, GRM32ER60J107ME20L
2	12	C1G-C12G	CAP.,X7R, 2200pF, 50V, 10% 0402	MURATA, GRM155R71H222KA01D
3	12	C1H-C12H	CAP.,X7R, 470pF, 50V, 10% 0402	MURATA, GRM155R71H471KA01D
4	12	C1R-C12R	CAP.,X7R, 2.2µF, 100V,10%, 1210	TDK, C3225X7R2A225K
5	14	C1K-C12K, C20,C21	CAP.,X7R, 1.0µF, 16V,10%, 0603	MURATA, GRM188R71C105KA12D
6	4	C2, C4, C8, C14	CAP, X7R, 0.1µF, 16V, 10% 0402	MURATA, GRM155R71C104KA88D
7	1	C7	CAP.,X7R, 0.1µF, 25V,10%, 0603	AVX, 06033C104KAT2A
8	3	C11, C12, C15	CAP.,X5R, 1µF, 25V,10%, 0603	TDK, C1608X5R1E105K
9	2	C18, C19	CAP.,X7R, 0.22µF, 10V,10%, 0603	MURATA, GRM188R71A224KA01
10	2	D23, D24	SMD, SCHOTTKY, SOD523	CENTRAL SEMI, CMOSH-4E
11	4	D1, D5, D19,D20	SMD, SCHOTTKY, SOD-123F	CENTRAL SEMI, CMMSH2-40
12	3	D6, D7, D8	SMD, SILICON SWITCHING DIODE	VISHAY, RS07J
13	12	D1E-D12E	DIODE, ZENER, 7.5V, 400MW, SOD323	NXP, PDZ7.5B.115
14	2	D12, D13	SMD, SCHOTTKY, 200MW, 100V, SOD-12	DIODES INC, BAT46W
15	1	D14	SMD, SILICON ZENER, 62V	CENTRAL SEMI, CMHZ5265B
16	1	D15	SMD, SCHOTTKY	CENTRAL SEMI, CMSH3-20MA
17	2	D21, D22	DIODE, ZENER, 5.1V,SOD-123	CENTRAL SEMI, CMHZ4689
18	2	D25, D26	DIODE, ZENER, 5.6V, 400MW, SOD323	NXP, PDZ5.6B.115
19	12	D1F-D12F	DIODE, SUPER BARRIER RECTIFIER, 10A, POWERDI5	DIODES INC, SBR10U200P5
20	24	R1C-R12C, R1F-R12F	RES,CHIP, 5.1Ω, 1/16W, 5%, 0402	VISHAY, CRCW04025R10JNED
21	2	R4, R6	RES,CHIP, 6.8Ω, 1/16W, 5%, 0402	VISHAY, CRCW04026R80JNED
22	24	R1G-R12G, R1H-R12H	RES,CHIP,20Ω,1/16W,5%,0402	VISHAY, CRCW040220R0JNED
23	7	R26, R27, R30, R35-R38	RES,CHIP,100Ω,1/16W,5%,0402	VISHAY, CRCW0402100R0JNED
24	5	R1, R5, R15-R17	RES,CHIP, 1.00M, 1/16W, 5%, 0402	VISHAY, CRCW04021M00JNED
25	2	R13, R14	RES, CHIP, 845k, 1/8W, 1%, 0805	VISHAY, CRCW0805845KFKEA
26	3	R7, R9, R11	RES, CHIP, 15.4k, 1/16W, 1%, 0402	VISHAY, CRCW040215K4FKED
27	2	R8, R10	RES, CHIP, 20.5k, 1/16W, 1%, 0402	VISHAY, CRCW040220K5FKED
28	2	R51, R52	RES,CHIP,2.0k,1/16W,5%,0402	VISHAY, CRCW04022K00JNED
29	2	R39, R40	RES, CHIP, 5.1k, 1/16W, 5%, 0402	VISHAY, CRCW04025K10JNED
30	2	R28, R29	RES, CHIP, 10.0k, 1/16W, 5%, 0402	VISHAY, CRCW040210K0JNED
31	1	R53	RES, CHIP, 100k, 1/16W, 5%, 0402	VISHAY, CRCW0402100KJNED
32	2	R54, R55	RES, CHIP, 20Ω, 1/16W, 5%, 0603	VISHAY, CRCW060320R0JNED
33	12	RS1A-RS12A	RES, CHIP, 8mΩ, 1W, 1%, 1206	SUSUMU, PRL1632-R008-F-T1
34	12	RS1B-RS12B	RES, CHIP, 16mΩ, 1W, 1%, 1206	SUSUMU, PRL1632-R016-F-T1
35	12	Q1A-Q12A	MOSFET, 100V, 0.0087Ω, 60A, POWERPAK-S08	VISHAY, SiR882DP-T1-GE3
36	12	Q1B-Q12B	MOSFET, 100V, 0.058Ω, 25A, POWERPAK-1212-8	VISHAY, SiS892DN-T1-GE3
37	2	Q13,Q14	MOSFET, 100V, 10Ω, SOT-323	DIODES INC, BSS123W-7-F
38	1	Q15	TRANSISTOR,PNP, 60V SOT-23	CENTRAL SEMI, CMPT3906E
39	1	Q16	TRANSISTOR, NPN, 60V SOT-23	CENTRAL SEMI, CMPT3904E
40	1	Q17	MOSFET, P-CHAN, 50V, 4Ω,SOT-23	CENTRAL SEMI, CMPDM8002A
41	12	T1-T12	TRANSFORMER, 1:1, 3.0µH, 10.8A	WURTH, 750312504
42	2	U1,U2	IC, SMT, BIDIRECTIONAL BATTERY BALANCER	LINEAR, LTC3300LXE-1#PBF
43	1	U3	IC, EEPROM 2KBIT, 400KHZ, 8TSSOP	MICROCHIP TECH. 24LC025-I/ST
44	1	U4	IC, SMT, OP AMP	LINEAR, LT6004IMS8#PBT
45	1	U5	IC, GATE NAND QUAD 2-PIN 14-SO	FAIRCHILD, MM74HC00M
46	1	U8	IC, SMT, BATTERY MONITOR	LINEAR, LTC6803IG-2#PBF

## PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
<b>Components and Hardware for Demo Board Only</b>				
1	12	C1E-C12E	CAP.,X7R, 470pF, 100V,10%, 0603	AVX, 06031C471KAT2A
2	12	C1, C3, C22-C31	CAP.,X7R, 4.7µF, 16V,20%, 1210	TDK, C3225X7R1C475M
3	13	C1L-C12L, C6	CAP., X7R, 0.1µF, 100V, 10%, 1206	AVX, 12061C104KAT2A
4	2	C5, C13	CAP., X7R, 470pF, 250VAC, 10%, 1808	MURATA, GA342QR7GF471KW01L
5	12	D1D-D12D	LED, GREEN CLEAR 0603 SMD	LITE-ON, LTST-C190KGKT
6	15	F1-F15	FUSE, 7A, FAST, SMD, 1206	COOPER BUSSMANN, 3216FF7-R
7	1	L1	IND, FERRITE CHIP 33Ω, 6A, 1206	MURATA, BLM31PG330SN1L
8	12	R1A-R12A	RES, CHIP, 20Ω, 1/4W, 5%, 1206	VISHAY, CRCW120620R0JNEA
9	12	R1K-R12K	RES, CHIP, 100Ω, 1/16W, 5%, 0603	VISHAY, CRCW0603100RJNED
10	4	R22-R25	RES, CHIP, 3.3k, 1/16W, 5%, 0402	VISHAY, CRCW04023K30JNED
11	8	R43-R50	RES, CHIP, 0Ω, 2512	VISHAY, CRCW25120000Z0EG
12	12	R1J-R12J	RES, CHIP, 2.0k, 1/16W, 5%, 0402	VISHAY, CRCW04022K00JNED
13	18	E1-E18	TP, TURRET, 0.094", PBF	MILL-MAX, 2501-2-00-80-00-00-07-0
14	5	E19-E23	TURRET, 0.061 DIA	MILL-MAX, 2308-2-00-80-00-00-07-0
15	2	J17, J18	CONN, HEADER, 14POS 2mm VERT GOLD	MOLEX 87831-1420
16	1	J1	CONN, HEADER, 3POS, 2.5mm STR TIN	HIROSE, DF1EC-3P-2.5DSA(05)
17	1	J1 (MATE)	CONN, RECEPT HOUSING, 3POS 2.5mm	HIROSE, DF1E-3S-2.5C
18	3	J1 (MATE CONTACT)	CONTACT, SOCKET, CRIMP 20-22AWG, TIN	HIROSE, DF1E-2022SCF
19	4	JP1-JP4	HEADER, 3PINS, 2mm	SAMTEC, TMM-103-02-L-S
20	4	JP1-JP4	SHUNT 2mm	SAMTEC, 2SN-BK-G
21	1	U6	IC, SMT, TRIPLE BUFFER	TI, SN74LVC3G07DCTR
22	1	U7	IC, SMT, 5V, SPI ISOLATER _ODULE	LINEAR, LTM2883CY-5S#PBF
23	5	MH1-MH5	STAND-OFF, NYLON, 0.500" TALL (SNAP ON)	KEYSTONE, 8833 (SNAP ON)
<b>Optional Components</b>				
1	0	C1C-C12C	CAP., X5R, 100µF, 6.3V, 10%, 1210	MURATA, GRM32ER60J107ME20
2	0	C1F(OPT)-C12F(OPT)	CAP., X7R, 470pF, 100V, 10%, 0603	AVX, 06031C471KAT2A
3	0	C1S-C12S, C1T-C12T	CAP., X7R, 2.2µF, 100V, 10%, 1210	TDK, C3225X7R2A225K
4	0	C5, C13	RES, CHIP, 0Ω, 2010	VISHAY, CRCW20100000Z0EF
5	0	C9(OPT), C10(OPT)	CAP, OPT, 25V, 0603	
6	0	C16, C17	CAP., TANT, 10µF, 10V, 20%. 1206	AVX, TAJA106M010RNJ
7	0	D1A-D12A	SMD, SCHOTTKY BARRIER RECTIFIER 2A, 60V, PWRD123	DIODES INC, DFLS260
8	0	D1B-D12B (OPT)	SMD, SCHOTTKY BARRIER RECTIFIER, 1A, 100V, PWRD123	DIODES INC, DFLS1100-7
9	0	D1C-D12C (OPT)	SMD, SCHOTTKY, SOD-523	CENTRAL SEMI, CMOSH-4E
10	0	D16(OPT)	SMD, SILICON SWITCHING DIODE	VISHAY, RS07J
11	0	R1B-R12B (OPT)	RES, CHIP, 18Ω, 1/4W, 5%, 1206	VISHAY, CRCW120618R0JNEA
12	0	R3, R12, R41, R42 (OPT)	RES, CHIP, 0Ω, 0402	VISHAY, CRCW04020000Z0ED
13	0	R31-R34 (OPT)	RES, CHIP, 0Ω, 2010	VISHAY, CRCW20100000Z0EF
14	0	J2-J4, J16 (OPT)	HEADER, 1x2, 2-PIN, 3.81mm, 90 DEG	WEIDMULLER, 1793130000
15	0	J2(OPT) (MATE)	SOCKET, 1x2, 2-PIN, 3.81mm, 180 DEG	WEIDMULLER, 1792770000
16	0	J5-J15 (OPT)	HEADER, 1x3, 3-PIN, 3.81mm, 90 DEG	WEIDMULLER, 1793140000
17	0	J5-J15 (OPT)	SOCKET, 1x3, 3-PIN, 3.81mm, 180 DEG	WEIDMULLER, 1792780000

# DEMO MANUAL DC2064A

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