LTM4642IY
20V_{IN}, DUAL 4A or SINGLE 8A DC/DC µMODULE REGULATOR

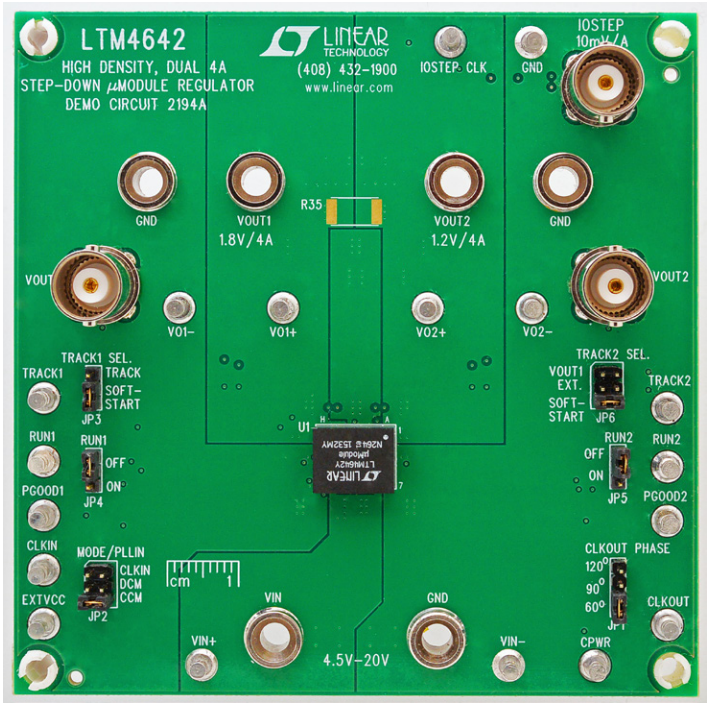
DESCRIPTION

Demonstration circuit of DC2194A features the LTM®4642IY, the wide input voltage, high efficiency and power density, dual 4A or single 8A DC/DC step-down µModule regulator. The step-down regulator operates from an input voltage range of 4.5V to 20V (or 2.5V min. with 5V external bias voltage at CPWR) and provides an adjustable output voltage range from 0.6V to 5V at 4A load current per channel. The part is capable of operating in dual phase single output, delivers up to 8A load current with interleaved two phases at 180 degrees. Differential output voltage sensing is available on Channel 1 for applications requiring more accurate output load regulation. A user-selectable mode input is provided to allow users to trade off ripple noise for light load efficiency: Discontinuous Mode (DCM) of operation delivers higher efficiency at light load while Continuous Conduction Mode (CCM) is preferred for noise sensitive applications. The mode pin can also be used to sync the switching frequency to an external clock. Programmable switching frequency range is from 600kHz to 1400kHz with a ±30% synchronization capture range. Constant on time, valley current mode control architecture and integrated internal control loop compensation allow very fast transient response to line and load changes while maintaining loop stability.

It is recommended to read the data sheet and demo manual of LTM4642 prior using or making any changes to DC2194A.

Design files for this circuit board are available at http://www.linear.com/demo/DC2194A

BOARD PHOTO



PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	VALUE
Dual Phase Dual Output Configuration (Default)		
Input Voltage Range		4.5V to 20V
Input Voltage Range		2.5V to 20V (with External CPWR Bias Supply)
Default Output Voltage V_{OUT1} V_{OUT2}	V_{IN} = 4.5V to 20V I_{LOAD} = 0A to 4A f_{SW} = 800kHz	1.8V ±1.5% 1.2V ±1.5%
Default Switching Frequency	Programmed Frequency with an External Resistor from FREQ Pin to SGND	800kHz ±10%
Maximum Continuous Output Current I_{OUT} per Channel (Dual Phase Dual Outputs)	V_{IN} = 4.5V to 20V f_{SW} = 800kHz	4A
Output Voltage Ripples (Peak-to-Peak) $V_{OUT1,P-P}$ $V_{OUT2,P-P}$ (Dual Phase Dual Outputs)	V_{IN} = 12V f_{SW} = 800kHz V_{OUT1} = 1.8V at I_{OUT1} = 4A V_{OUT2} = 1.2V at I_{OUT2} = 4A C_{OUT} = 1x150µF + 1x22µF per Channel	$V_{OUT1,P-P}$ = 27mV (Figure 8a) $V_{OUT2,P-P}$ = 17mV (Figure 8b)
Dynamic Load Transient Response $V_{OUT1,P-P}$ $V_{OUT2,P-P}$ (Dual Phase Dual Outputs)	V_{IN} = 12V f_{SW} = 800kHz Mode = CCM V_{OUT1} = 1.8V, I_{OUT_STEP} = 2A to 4A V_{OUT2} = 1.2V, I_{OUT_STEP} = 2A to 4A C_{OUT} = 1x150µF + 1x22µF per Channel	$V_{OUT1,P-P}$ = 86mV (Figure 7a) $V_{OUT2,P-P}$ = 67mV (Figure 7b)
Efficiency (Dual Phase Dual Outputs)	V_{IN} = 12V f_{SW} = 800kHz V_{OUT1} = 1.8V at I_{OUT1} = 4A V_{OUT2} = 1.2V at I_{OUT2} = 4A	Channel 1: 87.8% (Figure 4) Channel 2: 84.2% (Figure 4)
Thermal Performance (Dual Phase Dual Outputs)	V_{IN} = 12V f_{SW} = 800kHz V_{OUT1} = 1.8V at I_{OUT1} = 4A V_{OUT2} = 1.2V at I_{OUT2} = 4A T_A = 25°C, No Forced Airflow/Heat Sink	57.2°C Peak Temperature (Figure 11a)

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	VALUE
Dual Phase Single Output Configuration (Optional)		
Input Voltage Range		4.5V to 20V
Input Voltage Range		2.5V to 20V (with External CPWR Bias Supply)
Default Output Voltage V_{OUT}	V_{IN} = 4.5V to 20V I_{LOAD} = 0A to 8A f_{SW} = 800kHz	1.8V ±1.5%
Default Switching Frequency	Programmed Frequency with External Resistor from FREQ Pin to SGND	800kHz ±10%
Maximum Continuous Output Current I_{OUT} (Dual Phase Single Output)	V_{IN} = 4.5V to 20V f_{SW} = 800kHz	8A
Output Voltage Ripples (Peak-to-Peak) $V_{OUT,P-P}$ (Dual Phase Single Output)	V_{IN} = 12V f_{SW} = 800kHz V_{OUT} = 1.8V at I_{OUT} = 8A C_{OUT} = 1x100µF + 1x47µF per channel	$V_{OUT,P-P}$ = 10mV (Figure 10a)
Dynamic Load Transient Response $V_{OUT,P-P}$ (Dual Phase Single Output)	V_{IN} = 12V f_{SW} = 800kHz Mode = CCM V_{OUT} = 1.8V, I_{OUT_STEP} = 4A to 8A C_{OUT} = 1x100µF + 1x47µF per Channel	$V_{OUT,P-P}$ = 138mV (Figure 9b)
Efficiency (Dual Phase Single Output)	V_{IN} = 12V f_{SW} = 800kHz Mode = CCM V_{OUT} = 1.8V at I_{OUT} = 8A	87.9 % (Figure 6)
Thermal Performance (Dual Phase Single Output)	V_{IN} = 12V f_{SW} = 800kHz V_{OUT} = 1.8V at I_{OUT} = 8A T_A = 25°C, No Forced Airflow/Heat Sink	59.2°C Peak Temperature (Figure 12a)

QUICK START PROCEDURE

Demonstration circuit DC2194A is easy to set up to evaluate the performance of the LTM4642. Please refer to Figure 1 for proper measurement equipment setup and follow the procedures below:

1. With power off, connect the input power supply at V_{IN} (J4) and GND (J5)
2. Connect the first load between V_{OUT1} (J6) and GND (J7) for Channel 1, connect the second load between V_{OUT2} (J8) and GND (J3) for Channel 2. Preset all the loads to 0A.
3. Connect the DMMs at the input (E4 and E5) to monitor input voltage. Connect DMMs at V_{O1}+ (E6) and V_{O1}– (E7), V_{O2}+ (E11) and V_{O2}– (E9) to monitor DC output voltages. These output voltage test points are Kelvin sensed directly across C_{OUT1} for Channel 1 and C_{OUT4} for Channel 2 to provide accurate measurement of output voltages. Do not apply load current to any of the above test points to avoid damage to the regulator. Do not connect the ground leads of scope probes to V_{O1}– and V_{O2}–.
4. Turn on the power supply at the input. Measure and make sure the input supply voltage is 12V. Place the RUN 1 (JP4) and RUN2 (JP5) in the "ON" position. The output voltage should be 1.8V ±1.5% for Channel 1 and 1.2 ±1.5% for Channel 2.
5. Once the input and output voltages are properly established, adjust the input voltage between 4.5V and 20V and the loads within the operating range of 0A to 4A max per channel. Observe the output voltage regulation, output voltage ripples, switch node waveform, load transient response and other parameters. Refer to Figure 2 for proper output voltage ripple measurement.

   NOTE 1: To measure the input/output voltage ripple properly, do not use the long ground lead on the oscilloscope probe. See Figure 2 for the proper scope probe placement technique. Short, still leads need to be soldered to the (+) and (–) terminals of an output capacitor. The probe's ground ring needs to touch the (–) lead and the probe tip needs to touch the (+) lead.
6. DC2194A provides convenient on board BNC terminals to accurately measure output ripples of Channel 1 and Channel 2. Connect short BNC cables from V_{OUT1}, V_{OUT2} to the scope inputs (Scope probe ratio 1:1, AC coupling) to observe output voltage ripples.
7. DC2194A provides an optional onboard load transient circuit to measure ΔV_{OUT} peak-to-peak deviation during rising or falling dynamic load transient. The simple load step circuit consisting of a 30V N-channel power MOSFET in series with a 10mΩ, 1W,1% current sense resistor. The MOSFET is configured as a voltage control current source (VCCS) device, therefore the output current step and its magnitude is created and controlled by adjusting the amplitude of the applied input voltage step at the gate of the MOSFET. Use a function generator to provide a voltage pulse between IOSTEP CLK (E17) and GND (E18); the input voltage pulse should be set at the frequency less than 10Hz and maximum duty cycle of less than 5% to avoid excessive thermal stress on the MOSFET device. The output current step is measured directly across the 10mΩ current sense resistor and monitored by connecting a BNC cable from IOSTEP to the input of the oscilloscope (scope probe ratio 1:1, DC coupling), the equivalent voltage to current scale is 10mV/1A. The load step current slew rate dI/dt can be set by adjusting the rising time and fall time of the input voltage pulse.

   The default load step circuit is connected to V_{OUT1} but can be used for V_{OUT2} by simply removing the zero Ohm jumper R27 and stuffing it at the position of R28 and vice versa. Repeat Step 7 to perform load step transient evaluation for Channel 2.

QUICK START PROCEDURE

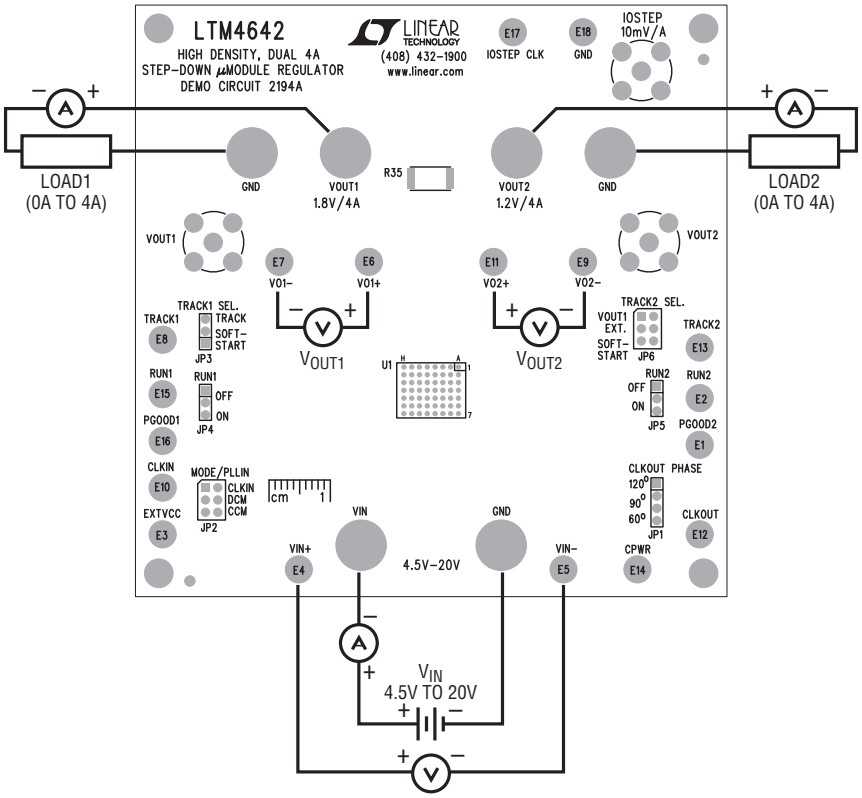


Figure 1. Proper Measurement Equipment Setup

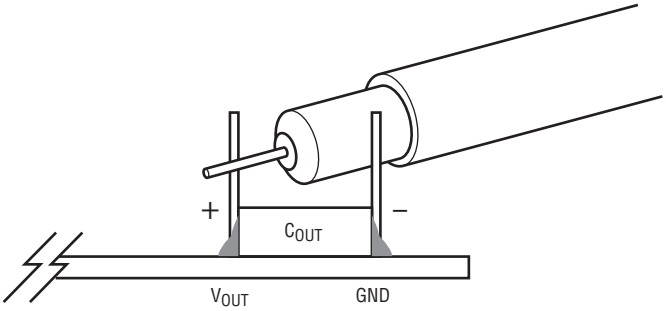


Figure 2. Scope Probe Placement for Measuring Input or Output Voltage Ripple

QUICK START PROCEDURE

8. To program other output voltages for Channel 1 or Channel 2, insert correct values of the bottom feedback resistors (Table 1).

   These values are calculated based on a typical feedback reference voltage of 0.6V and fixed internal top feedback resistor of 60.4kΩ.

Table 1. Bottom Resistive Divider Values (1%) for Setting Typical Output Voltages

V_{OUT} (V)	1.0	1.2	1.5	1.8	2.5	3.3	5.0
R_{BOT} (kΩ)	90.9	60.4	40.2	30.1	19.1	13.3	8.25

* NOTE 2: LTM4642 has been internally compensated for most of input, output voltages and frequency ranges. However, to obtain the best efficiency, thermal and load transient response performance when selecting output voltages different than the demo board default set voltages, the following parameters need to be optimized accordingly: input voltages, switching frequency, output capacitors and optional external compensation values (Feedforward Capacitors: C1, C12 and C_{COMP}: C3, C11). Please refer to Table 2 for more details.

Table 2. Suggested Optimized Switching Frequency for Typical Input and Output Voltages

V_{IN} (V)	3.3V	5.0V	5V	12V	12V	12V	20V	20V	20V
V_{OUT} (V)	1V 1.2V 1.5V 1.8V	1V 1.2V 1.5V 1.8V	1.8V 2.5V 3.3V	1.0V 1.2V	1.5V 1.8V 2.5V	2.5V 3.3V 5.0V	1V 1.2V	1.5V 1.8V	2.5V 3.3V 5.0V
f_{SW} (kHz)	600	650	800	650	800	1000 1200	650	800	1000 1200
R5 (kΩ) R_freq	68.1	66.5	49.9	66.5	49.9	39.2 32.4	66.5	49.9	39.2 32.4

Differential Output Voltage Sensing

The LTM4642 includes an internal low offset, high input impedance, unity gain, high bandwidth differential amplifier for applications that require true remote sensing. This feature allows users to accurately sense the output voltage across the output capacitor at the load point in a widely distributed power system where power trace's parasitic voltage drops are always presented. The differential amplifier's output is internally connected to the error amplifier's inverting input. $V_{OUTS1}+$ and $V_{OUTS1}-$ are Kelvin connected directly across C_{OUT1} on DC2194A.

(Optional) Output Voltage Tracking

TRK/SS1 and TRK/SS2 allow users to program output voltage supply tracking during start-up or shutdown while operating several voltage supply rails at the same time. Channel 1 is configured as a master and Channel 2 is a slave channel on DC2194A. Coincident tracking mode can be implemented by connecting TRK/SS2 of the slave channel to the mid-point of an additional resistive divider (R19, R20) to the master channel's output voltage. The ratio of this divider is identical to that of the slave's channel feedback divider. In this tracking mode, output voltage of the master channel must be higher than the output voltage of the slave channel. The rising time of the output voltage can be adjusted by changing the soft start capacitor's values of the master channel. Coincident tracking mode can be activated by inserting JP6 between Pin 1 and 2 of TRACK2 SEL and performing start-up/shutdown by releasing RUN1 from GND and pulling RUN1 to GND accordingly. Tracking mode can be observed by monitoring V_{OUT1}, V_{OUT2} and FB1, FB2 using scope probes. The same method can be used to configure V_{OUT1} or V_{OUT2} tracking an external supply voltage by inserting JP3 (TRK1 SEL) to TRACK or JP6 (TRK2 SEL) to EXT, applying an external voltage supply at TRACK1 (E8) or TRACK2 (E13) and repeating start-up/shutdown test to evaluate the tracking function of the regulator. Ratiometric tracking mode can be achieved by connecting TRK/SS2 to FB1. Ratiometric tracking mode can save two resistors while coincident tracking mode offers better voltage regulation. It is optional for users to determine the most appropriate tracking method for the power supply design.

(Optional) External Frequency Synchronization

The MODE/PLLIN pin can be used to synchronize the internal oscillator clock frequency to the external clock signal. Place JP2 (MODE/PLLIN) to CLKIN, apply an external clock at CLKIN (E10) to vary the switching frequency within ±30% of the set frequency. The external clock input high threshold is 2V typical, while the input low threshold is 0.5V.

QUICK START PROCEDURE

(Optional) Lower the Default Current Limit Setting for Channel 1

The default current limit setting for Channel 1 is 7A peak current limit with VRNG1 tied to $INTV_{CC}$. DC2194A provides an option to lower the peak current limit setting for Channel 1 (applications that required lower peak current limit to effectively protect the power devices during temporary output overloaded condition or output shorted circuit) by adjusting the DC voltage level at VRNG1. An external resistive divider from $INTV_{CC}$ can be used to set the voltage on VRNG pin between 1V to 0.6V, lower the VRNG1 voltage than 1V resulting in a lower maximum sense voltage and peak current limit.

(Optional) Operation with Low V_{IN} Range ($2.5V \le V_{IN} \le 4.5V$)

LTM4642 is equipped with CPWR pin, allowing V_{IN} to operate down to V_{IN} = 3.3V typical. CPWR pin is the main input power to the control IC and can be disconnected from the default V_{IN} supply voltage (Remove R13) and tied to an external 5V bias supply voltage at E14. If the DC bias supply voltage for CPWR is less than 5.3V, DRV_{CC} can also be tied to this pin by stuffing R15 = 0Ω. Since the RUN pins of Channel 1 and Channel 2 are directly tied to V_{IN}, pull up resistors at the RUN pins (R9, R23) should be re-calculated and inserted to make sure the part can start up at low V_{IN}. A good value to start with is 115kΩ using internal RUN pin pull-down resistor of 100k, RUN Pin On threshold of 1.1V min. to 1.3V max and RUN pin absolute max voltage of 6V. Care should be taken by not exceeding maximum voltage rating on $DRV_{CC}/INTV_{CC}$ pin when operating in this mode. Refer to Table 2. for recommended optimized switching frequency while operating at low V_{IN} voltage range.

(Optional) Operation with $EXTV_{CC}$

$EXTV_{CC}$ pin is available for optional external 5V bias supply to power $INTV_{CC}/DRV_{CC}$. The advantage of using $EXTV_{CC}$ is to shut down the internal LDO powered from V_{IN}, turn on the internal $EXTV_{CC}$ switch and directly source the external 5V bias supply to power $INTV_{CC}/DRV_{CC}$, therefore improving overall efficiency and reducing temperature rise of the part, especially at high input voltage range. An onboard turret (E3) is available for $EXTV_{CC}$ with a minimum of 4.7µF decoupling ceramic capacitor to PGND. Do not exceed the maximum rated voltage for $EXTV_{CC}$ and make sure V_{IN} is powered up before applying $EXTV_{CC}$.

(Optional) Dual Phase Single Output Circuit Configuration:

DC2194A can be configured as dual phase single output to provide up to 8A total load current.

The following simple modification is required: (Channel 1 is master, Channel 2 is slave). Please refer to Table 3 for more details.

Table 3. Dual Phase Single Output Circuit Configuration

	PIN NAME	CONNECTIONS	MODIFIED COMPONENTS
1	V_{OUT1} V_{OUT2}	Tie V_{OUT1}, V_{OUT2} together.	Stuff R35 = 0Ω and short the exposed copper pads at V_{OUT1}, V_{OUT2} on the bottom layer of the board .
2	FB2	Tie to $INTV_{CC}$ to disable the EA of the slave channel.	Remove FB2 bottom divider resistor (R17) and stuff R26 = 0Ω.
3	COMP2	Left open or externally tied to COMP1.	Remove C11.
4	RUN1 RUN2	Tie RUN1, RUN2 together.	Stuff R25 = 0Ω, R9 = 115kΩ, remove R23.
5	TRSK/SS2	Left open.	Remove JP6.
6	PHASMD	Tie to SGND or FLOAT: set phase interleaved 180° between CH1 and CH2.	JP1 = SNGD or FLOAT.
7	PGOOD2	Left open.	Remove R12.

QUICK START PROCEDURE

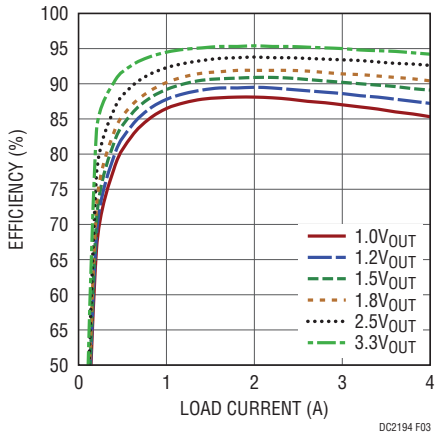


Figure 3. Measured Efficiency at $5V_{IN}$, 800kHz, Dual Phase Dual Outputs

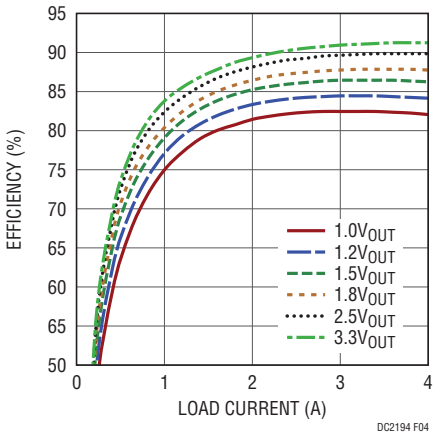


Figure 4. Measured Efficiency at $12V_{IN}$, 800kHz, Dual Phase Dual Outputs

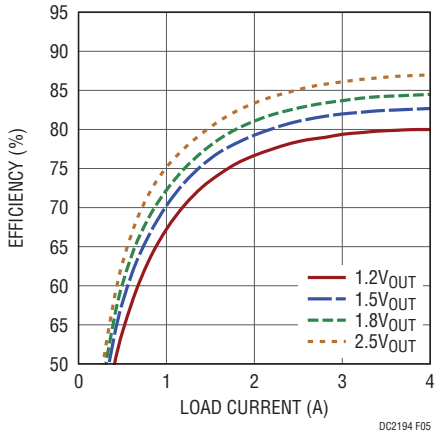


Figure 5. Measured Efficiency at $20V_{IN}$, 800kHz, Dual Phase Dual Outputs

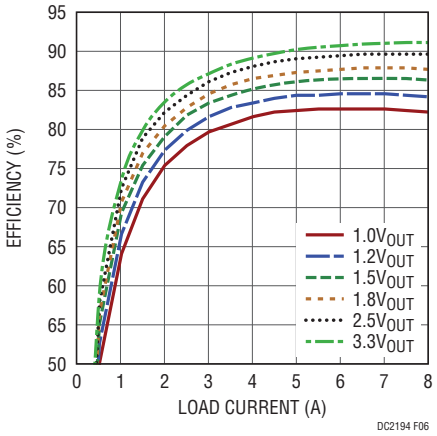
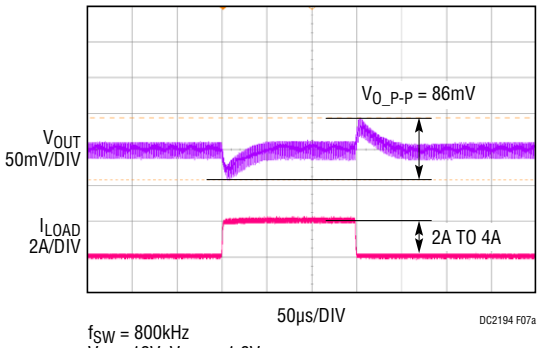
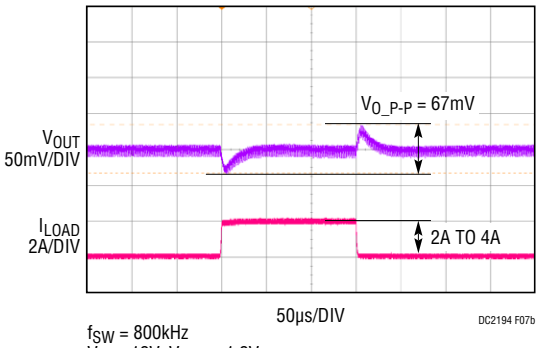


Figure 6. Measured Efficiency at $12V_{IN}$, 800kHz, Dual Phase Single Output



f_{SW} = 800kHz
V_{IN} = 12V, V_{OUT} = 1.8V
I_{LOAD} STEP = 2A TO 4A AT 2A/µs
C_{OUT_POSCAP} = 1×150µF/4V/7mΩ
$C_{OUT\_CERAMIC}$ = 1×22µF/10V/X7R/1206
C_{FF} = 220pF

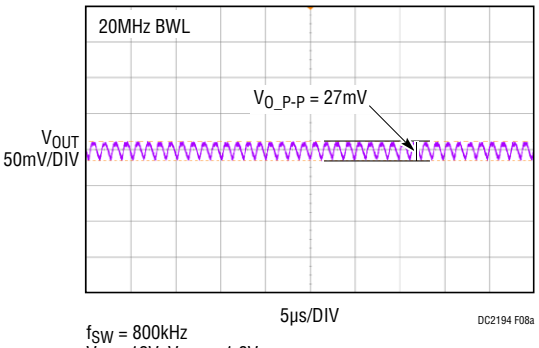
Figure 7a. Load Transient Response (CH1) Dual Phase Dual Outputs



f_{SW} = 800kHz
V_{IN} = 12V, V_{OUT} = 1.2V
I_{LOAD} STEP = 2A TO 4A AT 2A/µs
C_{OUT_POSCAP} = 1×150µF/4V/7mΩ
$C_{OUT\_CERAMIC}$ = 1×22µF/10V/X7R/1206
C_{FF} = 220pF

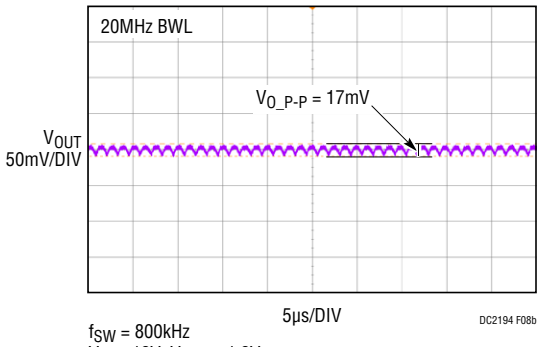
Figure 7b. Load Transient Response (CH2) Dual Phase Dual Outputs

QUICK START PROCEDURE



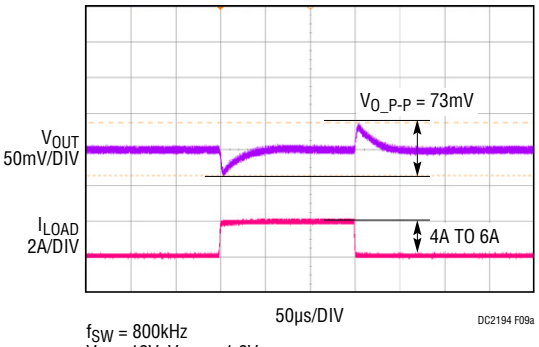
f_{SW} = 800kHz
V_{IN} = 12V, V_{OUT} = 1.8V
I_{LOAD} = 4A
C_{OUT_POSCAP} = 1×150µF/4V/7mΩ
$C_{OUT\_CERAMIC}$ = 1×22µF/10V/X7R/1206
C_{FF} = 220pF

Figure 8a. Output Ripple Voltage (CH1), Dual Phase Dual Outputs



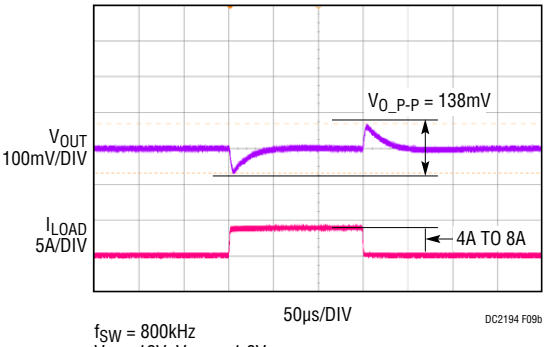
f_{SW} = 800kHz
V_{IN} = 12V, V_{OUT} = 1.2V
I_{LOAD} = 4A
C_{OUT_POSCAP} = 1×150µF/4V/7mΩ
$C_{OUT\_CERAMIC}$ = 1×22µF/10V/X7R/1206
C_{FF} = 220pF

Figure 8b. Output Ripple Voltage (CH2) Dual Phase Dual Outputs



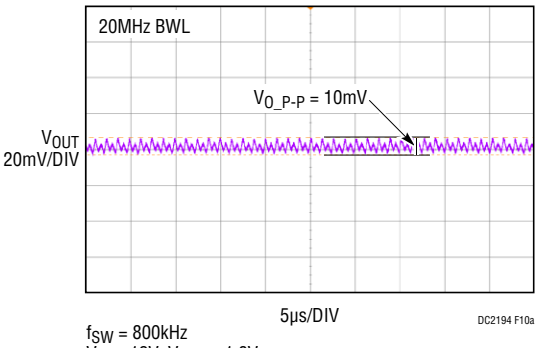
f_{SW} = 800kHz
V_{IN} = 12V, V_{OUT} = 1.8V
I_{LOAD} STEP = 4A TO 6A AT 2A/µs
$C_{OUT\_CERAMIC}$ = 1×100µF/6.3V/X5R/1206
+ 1×47µF/6.3V/X5R/1206
C_{FF} = 220pF

Figure 9a. Load Transient Response, Dual Phase Single Output



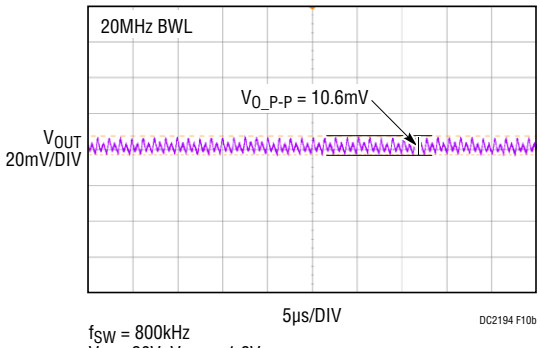
f_{SW} = 800kHz
V_{IN} = 12V, V_{OUT} = 1.8V
I_{LOAD} STEP = 4A TO 8A AT 4A/µs
$C_{OUT\_CERAMIC}$ = 1×100µF/6.3V/X5R/1206
+ 1×47µF/6.3V/X5R/1206
C_{FF} = 220pF

Figure 9b. Load Transient Response, Dual Phase Single Output



f_{SW} = 800kHz
V_{IN} = 12V, V_{OUT} = 1.8V
I_{LOAD} = 8A
$C_{OUT\_CERAMIC}$ = 1×100µF/6.3V/X5R/1206
+ 1×47µF/6.3V/X5R/1206
C_{FF} = 220pF

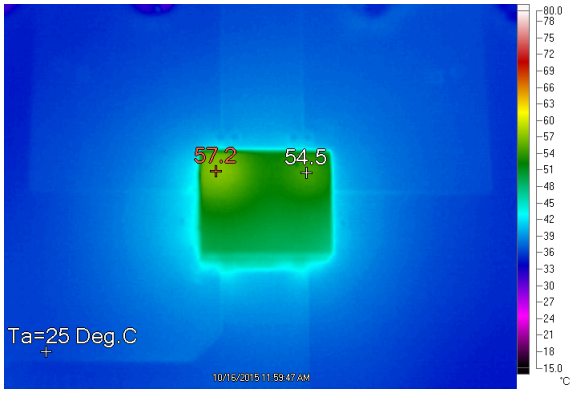
Figure 10a. Output Ripple Voltage, Dual Phase Single Output



f_{SW} = 800kHz
V_{IN} = 20V, V_{OUT} = 1.8V
I_{LOAD} = 8A
$C_{OUT\_CERAMIC}$ = 1×100µF/6.3V/X5R/1206
+ 1×47µF/6.3V/X5R/1206
C_{FF} = 220pF

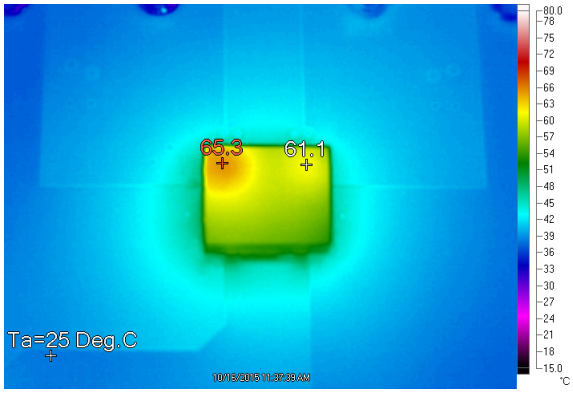
Figure 10b. Output Ripple Voltage, Dual Phase Single Output

QUICK START PROCEDURE



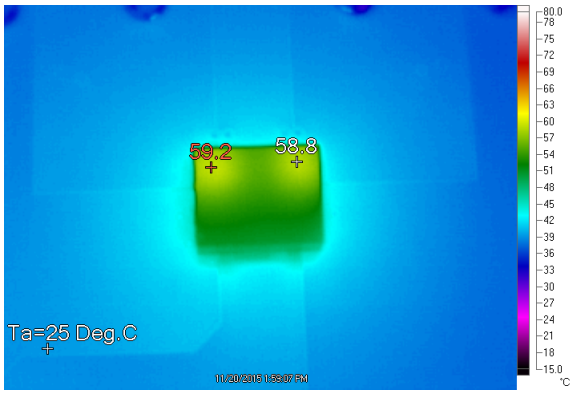
f_{SW} = 800kHz
V_{OUT1} = 1.8V, V_{OUT2} = 1.2V
V_{IN} = 12V, I_{LOAD} = 4A PER PHASE
TA = 25°C, NO FORCED AIRFLOW, NO HEAT SINK

Figure 11a. Thermal Performance at $12V_{IN}$, Dual Phase Dual Outputs



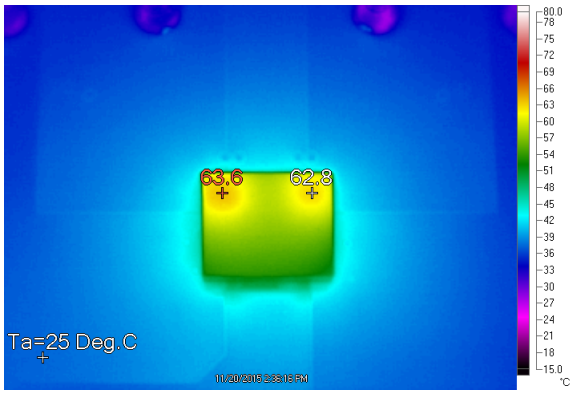
f_{SW} = 800kHz
V_{OUT1} = 1.8V, V_{OUT2} = 1.2V
V_{IN} = 20V, I_{LOAD} = 4A PER PHASE
TA = 25°C, NO FORCED AIRFLOW, NO HEAT SINK

Figure 11b. Thermal Performance at $20V_{IN}$, Dual Phase Dual Outputs



f_{SW} = 800kHz
V_{OUT} = 1.8V
V_{IN} = 12V, I_{LOAD} = 8A
TA = 25°C, NO FORCED AIRFLOW, NO HEAT SINK

Figure 12a. Thermal Performance at $12V_{IN}$, Dual Phase Single Output



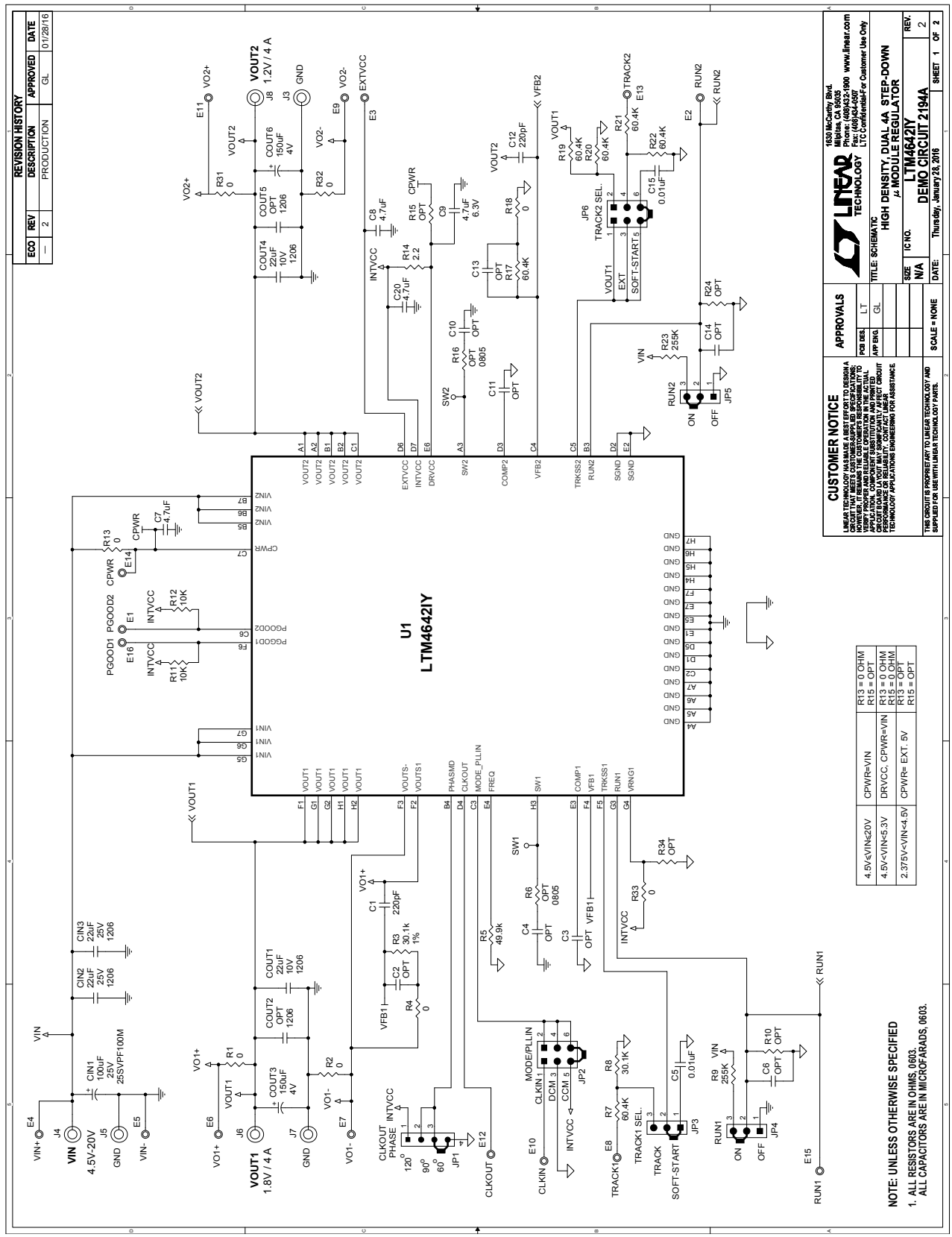
f_{SW} = 800kHz
V_{OUT} = 1.8V
V_{IN} = 20V, I_{LOAD} = 8A
TA = 25°C, NO FORCED AIRFLOW, NO HEAT SINK

Figure 12b. Thermal Performance at $20V_{IN}$, Dual Phase Single Output

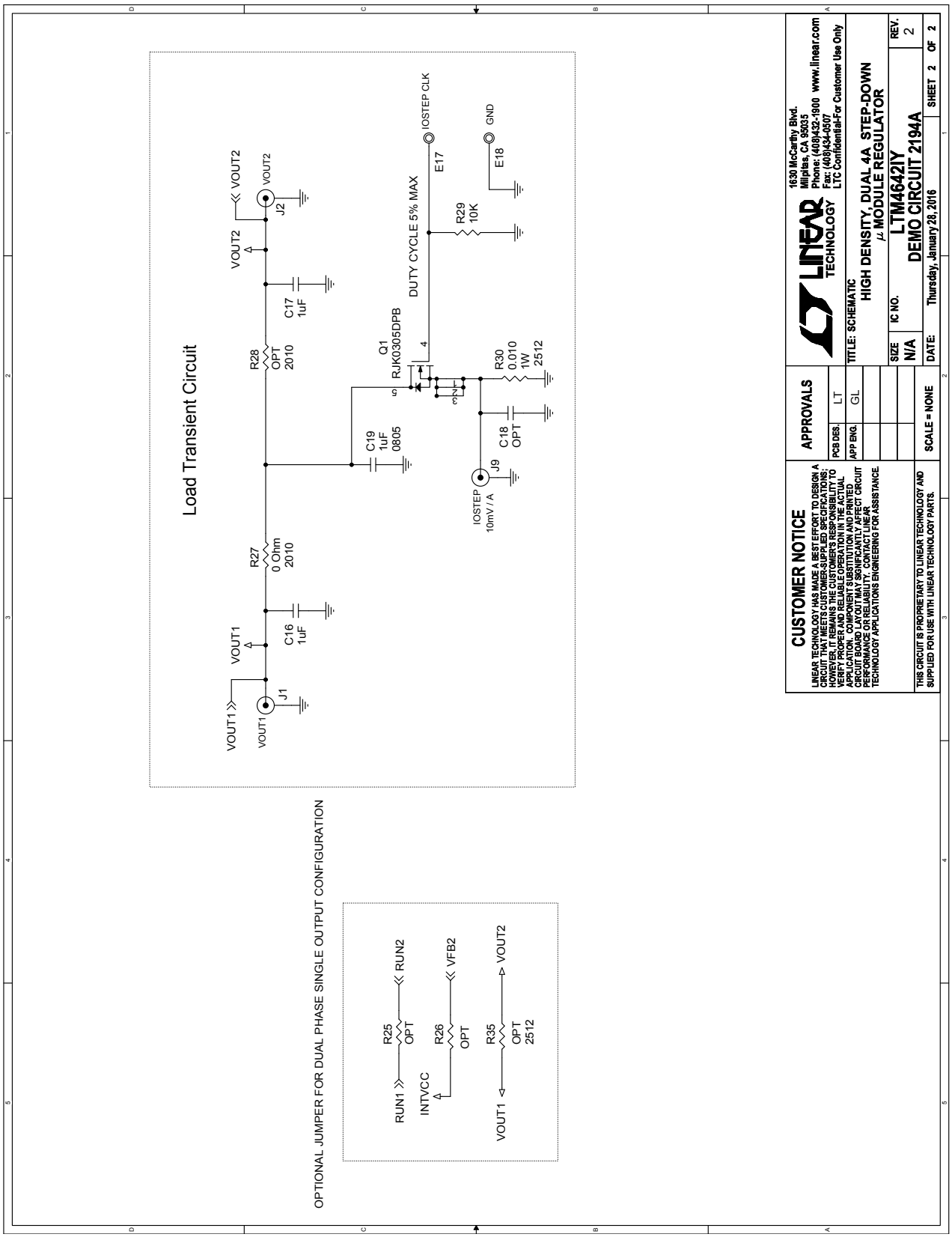
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CIN1	CAP., ALUM. ELECT., 100µF, 25V, 7343	PANASONIC, 25SVPF100M
2	2	CIN2, CIN3	CAP., 22µF, X5R, 25V, 10%, 1206	MURATA, GRM31CR61E226KE15L
3	2	COUT1, COUT4	CAP., 22µF, X7R, 10V, 20%, 1206	MURATA, GRM31CR71A226K
4	2	COUT3, COUT6	CAP., ALUM. ELECT., 150µF, 4V, 7343	PANASONIC, EEFSX0G151E7
5	2	C1, C12	CAP., 220pF, C0G, 50V, 5%, 0603	AVX, 06035A221JAT2A
6	2	C5, C15	CAP., 0.01µF, X7R, 25V, 10%, 0603	TDK, C1608X7R1E103K080AA
7	4	C7, C8, C9, C20	CAP., 4.7µF, X5R, 25V, 10%, 0603	MURATA, GRM188R61E475KE11D
8	2	C16, C17	CAP., 1µF, X5R, 6.3V, 10%, 0603	MURATA, GRM188R60J105KA01D
9	1	C19	CAP., 1µF, X7R, 10V, 10%, 0805	AVX, 0805ZC105KAT2A
10	1	Q1	MOSFET SPEED SRS 30V 30A LFPAK	RENESAS, RJK0305DPB-02#J0
11	8	R1, R2, R4, R13, R18, R31, R32, R33	RES., 0 OHM, 1/10W, 0603	VISHAY, CRCW06030000Z0EA
12	2	R3, R8	RES., 30.1k, 1/10W, 1%, 0603	VISHAY, CRCW060330K1FKEA
13	1	R5	RES., 49.9k, 1/10W, 1%, 0603	VISHAY, CRCW060349K9FKEA
14	6	R7, R17, R19, R20, R21, R22	RES., 60.4k, 1/10W, 1%, 0603	VISHAY, CRCW060360K4FKEA
15	2	R9, R23	RES., 255k, 1/10W, 1%, 0603	VISHAY, CRCW0603255KFKEA
16	3	R11, R12, R29	RES., 10k, 1/10W, 1%, 0603	VISHAY, CRCW060310K0FKEA
17	1	R14	RES., 2.2Ω, 1/10W, 1%, 0603	VISHAY, CRCW06032R20FKEA
18	1	R27	RES., 0Ω, 2010	TEPRO (NAKOMA), RNH6083
19	1	R30	RES., 0.010Ω, 1W, 1%, 2512	VISHAY, WSL2512R0100FEA
20	1	U1	I.C., LTM4642IY#PBF, BGA56-11.25X9X4.92	LINEAR TECH., LTM4642IY#PBF
Additional Demo Board Circuit Components				
1	0	COUT2, COUT5	CAP., OPT, 1206	OPT
2	0	C2, C3, C4, C6, C10, C11, C13, C14, C18	CAP., OPTION 0603	OPT
3	0	R6, R16	RES., OPTION, 0805	OPT
4	0	R10, R15, R24, R25, R26, R34	RES., OPTION, 0603	OPT
5	0	R28	RES., OPT, 2010	OPT
6	0	R35	RES., OPTION, 2512	NIC, NRC100ZOTRF
Hardware: For Demo Board Only				
1	18	E1-E18	TEST POINT, TURRET, 0.094" MTG. HOLE	MILL-MAX, 2501-2-00-80-00-00-07-0
2	1	JP1	CONN., HEADER, 1X4, 2mm	WURTH ELEKTRONIK, 62000411121
3	2	JP2, JP6	CONN., HEADER, 2X3, 2mm	WURTH ELEKTRONIK, 62000621121
4	3	JP3, JP4, JP5	CONN., HEADER, 1X3, 2mm	WURTH ELEKTRONIK, 62000311121
5	6	XJP1-XJP6	SHUNT, 2mm	WURTH ELEKTRONIK, 60800213421
6	3	J1, J2, J9	CONN, BNC, 5 PINS	CONNEX, 112404
7	6	J3-J8	CONN., JACK, BANANA, NON-INSULATED, 0.218"	KEYSTONE, 575-4
8	4	(STAND-OFF)	STAND-OFF, NYLON, SNAP-ON, 0.500"	KEYSTONE, 8833(SNAP ON)

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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