LTC6951
Multichannel JESD204B ADC with Clocking

DESCRIPTION

Demonstration Circuit 2226A-A is a reference design for a four-channel, 250Msps ADC system consisting of two LTC®2123, dual 14-bit 250Msps ADCs and a JESD204B Subclass 1 clocking solution based on the LTC6951 Clock Synthesizer with Integrated VCO. Other dash options reserved for future use. No external clock source is required to operate the board; however, the onboard 100MHz reference oscillator may be bypassed, allowing synchronization to other equipment.

Figure 1 is a block diagram of the DC2226A clock configuration, consisting of two LTC6951s in a JESD204B subclass 1, ParallelSync™ configuration. More detailed information is available on the LTC6951 product page.

Design files for this circuit board are available at http://www.linear.com/demo/DC2226A

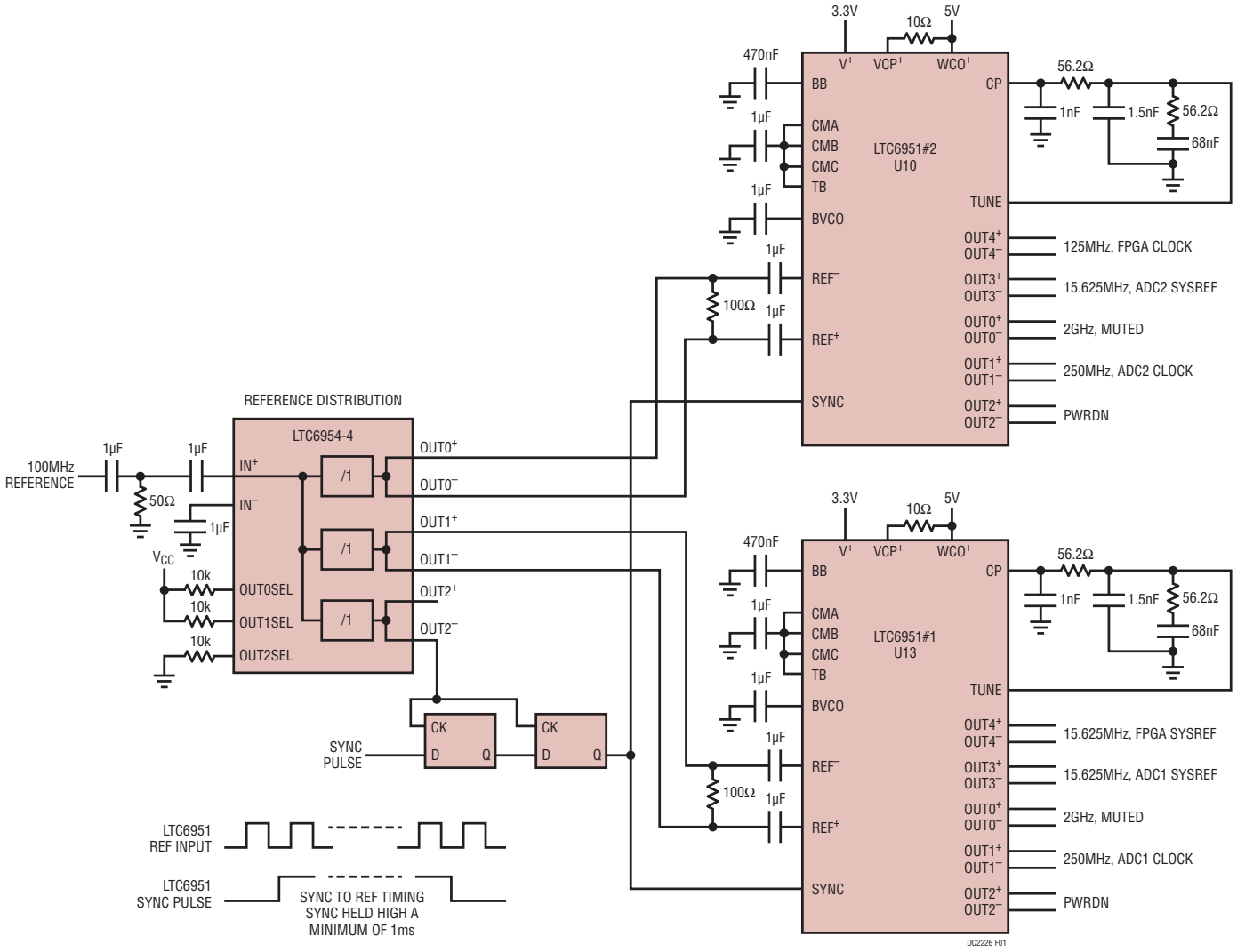

Figure 1. Subclass 1 ParallelSync Design Example

QUICK START PROCEDURE

1) Install PScope™ from http://www.linear.com/solutions/PScope. This step will also install the USB drivers required to communicate with the DC2226A demo system. Quit PScope after the installation is finished. Note that PScope does not directly support the DC2226A demo system, however the Matlab and Python scripts can export data files that may be opened in PScope for analysis.

2) Install LinearLabTools from http://www.linear.com/solutions/linearlabtools, following the procedure for either Matlab or Python. Both Matlab and Python code for DC2226A are included in the \matlab\DemoBoardExamples\LTC2123 and \python\demo_board_examples\ltc2123 directories, respectively. The main scripts run through a series of tests, concluding with capturing data from all four channels and displaying time and frequency domain plots.

3) Do NOT plug the USB cable into the DC2159 FMC Communication Interface board before powering up the KC705 board.

4) Refer to Figure 2. Power up the KC705 board using the adapter supplied with the KC705. If the board was obtained from Linear Technology as part of a kit, the correct bitfile was installed into the onboard configuration PROM.

5) If necessary, load the .bit file (included in the design files PDF subdirectory) into the KC705 board using the appropriate Xilinx tool (Impact, Vivado, or Vivado lab). Alternatively, create a .mcs file from the bitfile and load into the onboard configuration PROM. (See KC705 documentation for details.)

6) Connect the DC2159 FMC board to the host PC with a USB-A/Mini-B cable.

7) Apply 6V and 3V to the turret posts as shown in Figure 2. Both supplies should be low-noise benchtop supplies, with current limit set to 2A.

8) Apply analog input signals to J2, J3, J4, J5. The DC2226A is populated with an input network that has 50Ω characteristic impedance over a wide frequency range, refer to LTC2123 data sheet for details. A 70MHz, 1.5V_{P-P} sine wave is a good starting point for testing DC2226A. If an RF generator is used, it should be followed by a bandpass filter to limit noise and harmonics. Alternatively, DC1164 High Speed ADC Signal Source may be used.

9) Run the appropriate test script (Ltc2123Dc2226DualClockingSolution.m for Matlab, ltc2123_dc2226_dual_clocking_solution.py for Python). Plots similar to Figures 3 and 4 should appear. At this point, data is stored in program variables for further manipulation and testing.

10) The default test scripts set the ADC sample rate to 250MSPS, with a SYSREF frequency of 15.625MHz (JESD204B K=16). Design examples on the LTC6951 product page detail the process for changing clock frequencies.

QUICK START PROCEDURE

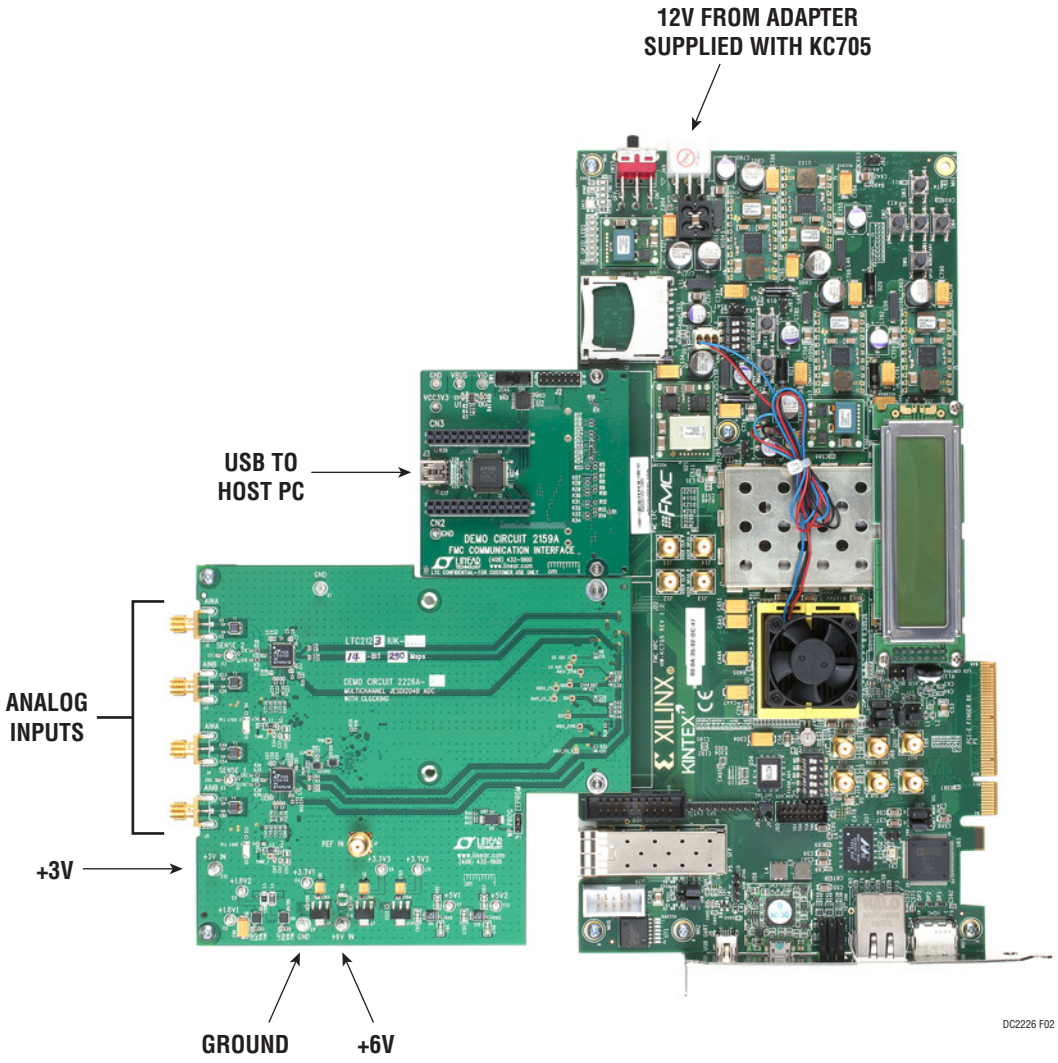

Figure 2. Basic Connections

QUICK START PROCEDURE

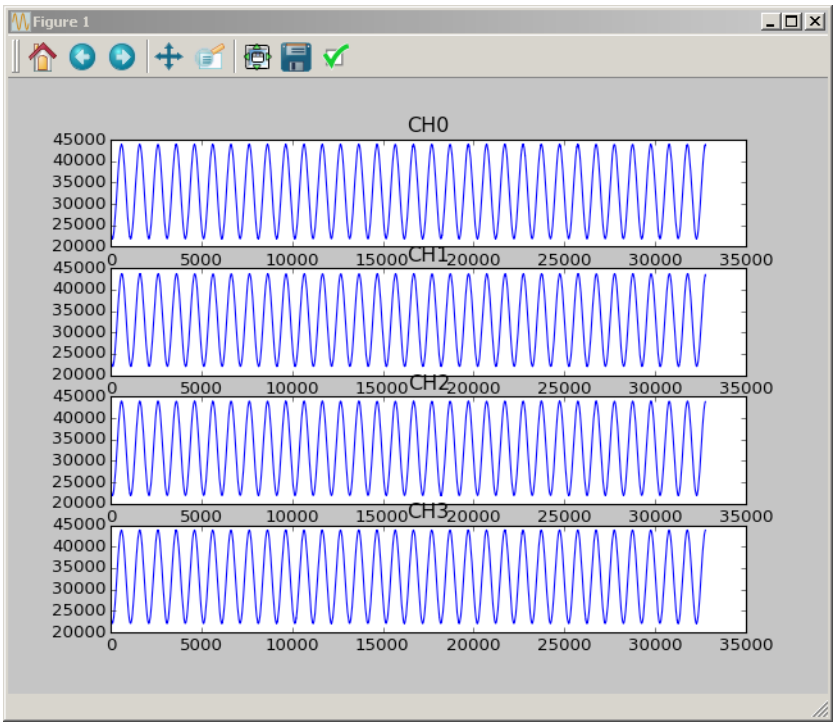

Figure 3. Example Time Domain Plot

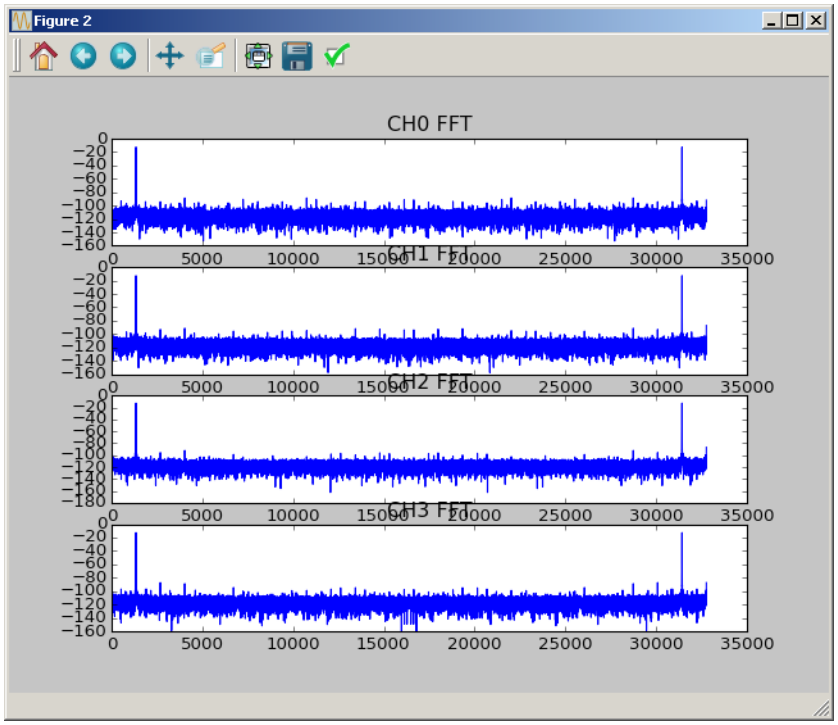

Figure 4. Example Frequency Domain Plot

HARDWARE SETUP

DC2226A Power Connections

E14: +6V Power Input. Connect to a low-noise supply set to a current limit of 2A.

E12: +3V Power Input. Connect to a low-noise supply set to a current limit of 2A.

E1, E9: GND - Ground connections for power supplies.

E5, E8: 1.8V test points. Measure 1.8V supply voltages at these points. (Measurement only, do not apply power.)

E4, E6, E11: 3V3_1, 3V3_2, 3V3_3 test points. Measure 3.3V supply voltages at these points. (Measurement only, do not apply power.)

E7, E13: 5V_1, 5V_2 test points. Measure 5V supply voltages at these points. (Measurement only, do not apply power.)

DC2226A Signal Connections

J2, J3: Analog inputs for U1, 50Ω impedance. Maximum signal level is $1.5V_{P-P}$.

J4, J5: Analog inputs for U3, 50Ω impedance. Maximum signal level is $1.5V_{P-P}$.

J1: External Reference Clock Input. Not connected, requires component changes, refer to schematic.

J6: FMC HPC interface to FPGA carrier board.

APPENDIX A

Xilinx KC705 Based Evaluation System

The DC2226A system consists of the DC2226A itself, a Xilinx KC705 FPGA evaluation board, a DC2159 USB communication board, and a host PC running the various test programs. Complete systems that ship from Linear Technology will have the KC705 board configured to automatically load the default FPGA image for DC2226A from the onboard configuration EEPROM. The procedure for bringing up the system is as follows:

1) If the boards were obtained separately, assemble them as shown in Figure 1 (FMC connectors are fragile, make sure they are properly aligned before seating.)
2) Connect power supply to the KC705 board and turn on the power switch. If the assembled system was obtained from Linear Technology, the FPGA bitstream will load automatically from the onboard configuration memory.
3) Boards not obtained from Linear Technology will need to be configured as described in the Alternate FPGA Configuration section.
4) Apply power and analog input signals to the DC2226A board.
5) Verify that PScope software is installed. Connect DC2159 to the host PC with a USB-mini cable. Driver installation will start automatically and PScope will recognize the system when installation finishes. Quit PScope and run Matlab/Python test scripts.

Note: Power must be applied to the KC705 board when the USB cable is connected or the driver installation will not complete properly.

Alternate FPGA Configuration

KC705 boards not obtained from Linear Technology will need to be configured via JTAG. FPGA images are located in the PScope installation directory in the FPGA_images folder. Connect a USB micro cable to the JTAG USB connector on the KC705 board and use a Xilinx tool such as Impact or Vivado Lab Edition to load the bitfile. Once the FPGA is configured, remove the USB cable and exit the software. (The onboard JTAG adapter and the DC2159 USB communication board use the same USB controller and they may interfere with one another.)

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