LTC4236-1/LTC4236-2
Dual Ideal Diode-OR and Single Hot Swap Controller with Current Monitor

DESCRIPTION

Demonstration circuit 2314A is intended to demonstrate the performance of the LTC4236-1/LTC4236-2 Dual Ideal Diode-OR and Single Hot Swap Controller with Current Monitor. The controller operates in redundant supply circuits, where each rail has an individual ideal diode, and the outputs are connected to the load through a single Hot Swap circuit. The controller enables monitoring of the load current by providing a signal that is 100× the sense resistor voltage.

The DC2314A allows verification of the LTC4236 Hot Swap and ideal diode functionality during individual rail ramp-up and ramp-down events, during power supply switchover, in steady state, and in overcurrent fault conditions.

The DC2314A is configured for 12V operation with a 10A current load.

The main board components are the LTC4236 controller, two power MOSFETs functioning as ideal diodes and one power MOSFET controlled as a Hot Swap switch, two jumpers for enabling the second ideal diode and Hot Swap, four LEDs to indicate the power good state, fault condition, and the state of the MOSFETs operating as ideal diodes, seven banana jacks for connecting power supplies and loads, and many turrets and pads for observing circuit signals.

Table 1. DC2314A Assembly Options

Version	Part	Overcurrent Fault
DC2314A-A	LTC4236-1	LATCHOFF
DC2314A-B	LTC4236-2	RETRY

Design files for this circuit board are available at http://www.linear.com/demo/DC2314A

BOARD AND CONTROLLER PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supplies						
V_{IN}	Input Supply Range		2.9		18.0	V
I_{LIM}	Board Current Limit	OUT = 11V	8.91	10	11.11	A
V_{INTVCC}	Internal Regulator Voltage		4.5	5	5.5	V
$V_{INTVCC(UVL)}$	Internal V_{CC} Undervoltage Lockout	$INTV_{CC}$ Rising	2.1	2.2	2.3	V
Ideal Diode Control						
$\Delta V_{FWD(REG)}$	Forward Regulation Voltage ($V_{INN} - V_{SENSE}$)		2	15	28	mV
ΔV_{DGATE}	External N-Channel Gate Drive ($V_{DGATE1} - V_{IN1}$) and ($V_{DGATE2} - V_{D2SRC}$)	IN < 7V, ΔV_{FWD} = 0.15V; I = 0, –1µA IN = 7V to 18V, ΔV_{FWD} = 0.15V; I = 0, –1µA	5 10	7 12	14 14	V V
$I_{CPO(UP)}$	CPO_n Pull-Up Current	CPO = IN = D2SRC = 2.9V CPO = IN = D2SRC = 18V	–60 –50	–100 –90	–130 –120	µA µA
$I_{DGATE(FPU)}$	$DGATE_n$ Fast Pull-Up Current	ΔV_{FWD} = 0.2V, ΔV_{DGATE} = 0V, CPO = 17V		–1.5		A
$I_{DGATE(FPD)}$	$DGATE_n$ Fast Pull-Down Current	ΔV_{FWD} = –0.2V, ΔV_{DGATE} = 5V		1.5		A
$I_{DGATE2(DN)}$	DGATE2 Off Pull-Down Current	D2OFF = 2V, ΔV_{DGATE2} = 2.5V	50	100	200	µA
$t_{ON(DGATE)}$	$DGATE_n$ Turn-On Delay	ΔV_{FWD} = 0.2V, C_{DGATE} = 10nF		0.25	0.5	µs
$t_{OFF(DGATE)}$	$DGATE_n$ Turn-Off Delay	ΔV_{FWD} = –0.2V, C_{DGATE} = 10nF		0.2	0.5	µs
$t_{PLH(DGATE2)}$	D2OFF Low to DGATE2 High			50	100	µs

BOARD AND CONTROLLER PERFORMANCE SUMMARY Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Hot Swap Diode Control						
$\Delta V_{SENSE(TH)}$	Current Limit Sense Voltage Threshold ($V_{SENSE^+} - V_{SENSE^-}$)	FB = 1.3V FB = 0V	22.5 5.8	25 8.3	27.5 10.8	mV mV
$V_{SENSE+(UVL)}$	SENSE+ Undervoltage Lockout	SENSE+ Rising	1.8	1.9	2	V
$\Delta V_{SENSE+(HYS)}$	SENSE+ Undervoltage Lockout Hysteresis		10	50	90	mV
ΔV_{HGATE}	External N-Channel Gate Drive ($V_{HGATE} - V_{OUT}$)	IN < 7V, I = 0, –1µA IN = 7V to 18V, I = 0, –1µA	5 10	7 12	14 14	V V
$\Delta V_{HGATE(H)}$	Gate High Threshold ($V_{HGATE} - V_{OUT}$)		3.6	4.2	4.8	V
$I_{HGATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate Drive On, HGATE = 0V	–7	–10	–13	µA
$I_{HGATE(DN)}$	External N-Channel Gate Pull-Down Current	Gate Drive Off, OUT = 12V, HGATE = OUT +5V	1	2	4	mA
$I_{HGATE(FPD)}$	External N-Channel Gate Fast Pull-Down Current	Fast Turn-Off, OUT = 12V, HGATE = OUT +5V	100	200	350	mA
Input/Output Pin						
$V_{IN(TH)}$	ON, FB Pin Threshold Voltage	Voltage Rising	1.21	1.235	1.26	V
$V_{ON(RESET)}$	ON Pin Fault Reset Threshold Voltage	ON Falling	0.57	0.6	0.63	V
$V_{D2OFF(H,TH)}$	D2OFF Pin High Threshold	D2OFF Rising	1.21	1.235	1.26	V
$V_{TMR(H)}$	FTMR, DTMR Pin High Threshold		1.198	1.235	1.272	V
$I_{FTMR(UP)}$	FTMR Pull-Up Current	FTMR = 1V, in Fault Mode	–80	–100	–120	µA
$I_{FTMR(DN)}$	FTMR Pull-Down Current	FTMR = 2V, No Faults	1.3	2	2.7	µA
Current Monitor						
G_{IMON}	IMON Voltage Gain	ΔV_{SENSE} = 20mV and 5mV	99	100	101	V/V
$V_{IMON(MAX)}$	IMON Maximum Output Voltage	ΔV_{SENSE} = 70mV, 5V ≤ SENSE+ ≤ 18V ΔV_{SENSE} = 35mV, SENSE+ = 2.9V	3.5 2.7		5.5 2.9	V V
$R_{IMON(OUT)}$	IMON Output Resistance	ΔV_{SENSE} = 200µV	15	20	27	kΩ

OPERATING PRINCIPLES

The LTC4236 is intended to build a combination of a diode-OR circuit for two rails and a common single Hot Swap path for inrush current limiting and overcurrent protection.

The LTC4236 regulates the forward voltage drop across the ideal diode MOSFET to ensure smooth current transfer from one supply to the other without oscillation. A fast ideal diode MOSFET turn-on reduces the load voltage droop during supply switchover. If the input supply fails or is shorted, a fast turn-off minimizes reverse current transients.

The Hot Swap fast acting current limit and internal timed circuit breaker protect circuit components when a short-circuit fault occurs.

The Hot Swap section of the LTC4236 has independent on/off control (ON pin).

Each ideal diode MOSFET is activated from an individual charge pump source, and the second one has an additional on/off control (D2OFF pin).

The LTC4236 features an adjustable debounce time — the delay time between events when the controller is enabled and when it starts up.

The DC2314A-A (LTC4236-1) circuit features a latchoff circuit breaker, and DC2314A-B (LTC4236-2) provides automatic retry after a fault.

BANANA JACKS WITH ASSOCIATED TURRETS

IN1 (E1, E2): First rail input.
IN2 (E5, E6): Second rail input.
GND (E3, E4, E7, E8, E14, E15, E21, E22): Power and control ground.
SENSE$^+$ (E16, E26): SENSE$^+$ power node.
OUT (E12, E13): Circuit output for load connection.

TURRETS

ON (E18): Hot Swap ON control input.
$\overline{EN}$ (E19): Enable input.
D2OFF (E20): Enable ideal diode 2.
$\overline{PWRGD}$ (E9): Power status output.
$\overline{FAULT}$ (E10): Fault status output.
CMON (E11): Current sense monitoring output.

JUMPERS

JP1 (ON_SEL): Hot Swap ON control signal selection.
JP2 (EN_SEL): ENABLE signal selection.
JP3 (DIODE2_OFF): Diode 2 OFF-ON control.
JP4 (PPRI_SEL): Prioritizer function selection.
JP5 (FB_SEL): Foldback circuit selection.
JP6 (DEBOUNCE): Debounce time selection.
JP8 (DSTAT2_SEL): $\overline{DSTAT2}$ pin functionality selection.
JP9 (D2OFF_SEL): D2OFF control in the prioritizer mode.

LEDS

D3: Indicates $\overline{PWRGD}$ pin signal.
D4: Indicates $\overline{FAULT}$ pin signal.
D5: Indicates $\overline{DSTAT1}$ pin signal.
D6: Indicates $\overline{DSTAT2}$ pin signal.

QUICK START PROCEDURE

Demonstration circuit 2314A is easy to set up to evaluate LTC4236. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

The DC2314A test includes independent test of the LTC4236 Hot Swap functionality and ideal diode functionality.

HOT SWAP FUNCTIONALITY TEST

This test is performed with singe rail operation when the output is provided through two series connected MOSFETs. One MOSFET functions as an ideal diode and the other one as a Hot Swap circuit switch.

The parameters of four different transients completely characterize the Hot Swap circuit performance. These transients are:

A Power-Up Without Any Additional Load

A Current Limit Operation After Successful Power-Up

A Power-Up With Shorted Output

A Power-Up With Pure Capacitive Load For Confirming Foldback Current Limiting

1. Initially, install the jumpers in the following positions, if the first ideal diode is used in the test:

   JP1 ON_SEL in the position OFF

   JP2 EN_SEL in the position EN

   JP3 DIODE2_OFF in the position OFF_EXT

   If the second ideal diode is used:

   JP1 ON_SEL in the position OFF

   JP2 EN_SEL in the position EN

   JP3 DIODE2_OFF in the position ON

   Connect a +12V power supply to turrets IN1 (or IN2) and GND. Do not load the output. Place the current probe on the +12V wire, voltage probes on the OUT turret and a voltmeter on the CMON and GND turrets. Provide an ON signal at the ON pin by changing the JP1 header position from the OFF position to 12V. Observe the transient. The output voltage rise time should be in the range of 8.3ms – 19.7ms. The $\overline{\text{PWRGD}}$ green LED D3 must light up. The voltmeter at the CMON turret should display an absolute value not larger than 15mV. Turn off the rail using the ON_SEL jumper.

2. Connect a disabled electronic load to the OUT turret and GND. Turn on the rail and slowly increase the load current up to the circuit breaker threshold level. The current limit range should be from 8.91A to 11.11A. The voltage at the CMON turret should be in the range from 2.18V to 2.83V. Turn off the rail with the ON_SEL jumper.

3. Initially short the output with an external wire. Place the current probe on this wire. Turn on the rail and record the current shape. The maximum current should be in the 2.30A to 4.36A range, and the voltage at the CMON turret should be in the range from 0.57V to 1.09V.

4. With no rail voltages and JP1 in the OFF position, connect a 1000µF capacitor to the board output. Place a scope current probe on any wire between the board and the 1000µF capacitor, and a voltage probe at the output. Provide +12V to any input (IN1 or IN2) and enable the ON signal. Confirm that current limit is characterized by a foldback functionality.

IDEAL DIODE FUNCTIONALITY TEST

In this test, both ideal diodes are active and small variations in the input voltage forces one ideal diode to be off and the other ideal diode to be on.

Connect input turrets (IN1 and IN2) of each ideal diode with individual independent lab supplies. Adjust each input voltage to +12V with maximum possible accuracy. Place one voltmeter between IN1 and IN2 turrets to measure the difference between the two input voltages. Connect an electronic load to the output turret. Activate both rails and keep the load around 1A to 3A. Play with the input voltage levels and be sure that when the difference between input voltages exceeds 28mV, only one rail feeds the load.

QUICK START PROCEDURE

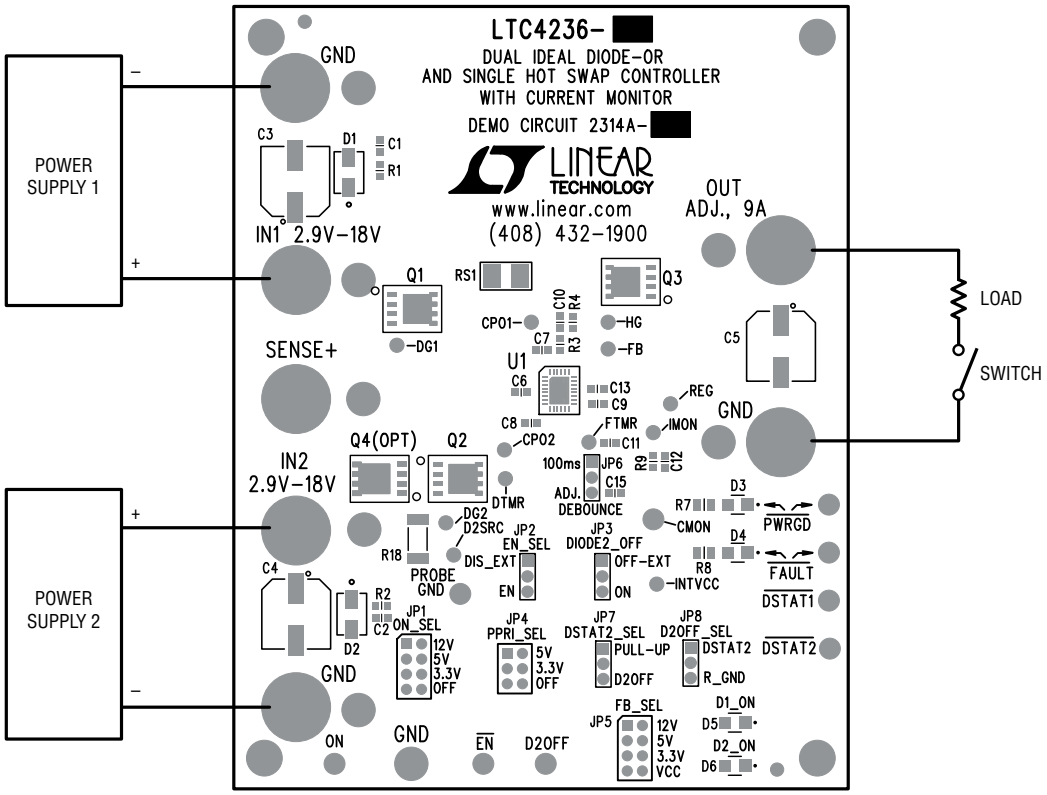
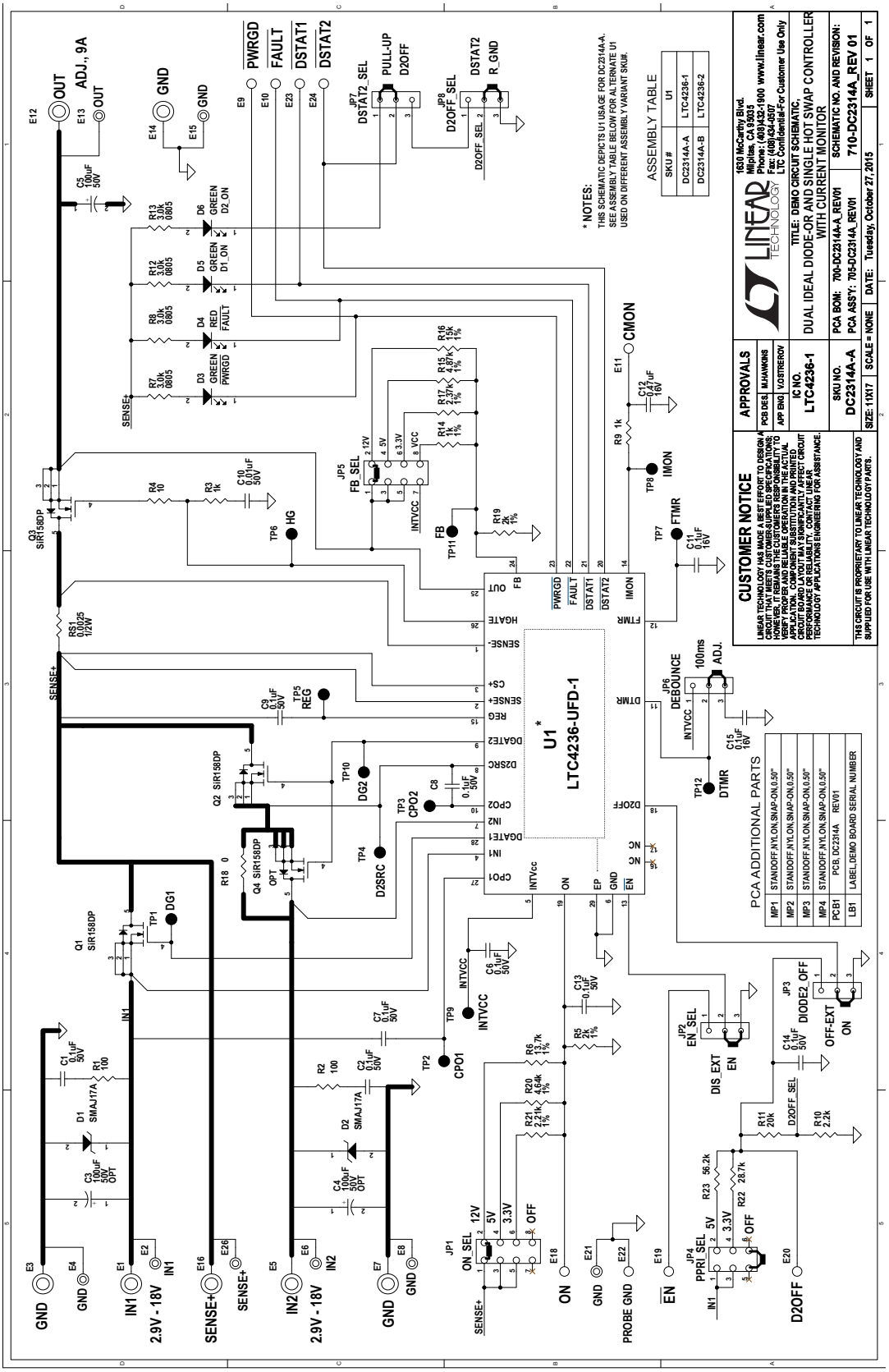


Figure 1. Measurement Equipment Setup

SCHEMATIC DIAGRAM



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