

LTC4235-1/LTC4235-2

Dual 12V Ideal Diode-OR and Single Hot Swap Controller with Current Monitor

DESCRIPTION

Demonstration circuit 2315A is intended to demonstrate the performance of the [LTC®4235-1/LTC4235-2](#) Dual 12V Ideal Diode-OR and Single Hot Swap™ Controller with Current Monitor. The controller operates in redundant 12V supply circuits, where each rail has an individual ideal diode, and the outputs are connected to the load through a single Hot Swap circuit. The controller enables monitoring of the load current by providing a signal that is 100× the sense resistor voltage.

The DC2315A allows verification of the LTC4235 Hot Swap and ideal diode functionality during individual rail ramp-up and ramp-down events, during power supply switchover, in steady state, and in overcurrent fault conditions.

The DC2315A is configured for 12V operation with a 9.0A maximum current load.

The main board components are the LTC4235 controller, two power MOSFETs functioning as ideal diodes and one power MOSFET controlled as a Hot Swap switch, two jumpers for enabling the second ideal diode (DIODE2_OFF) and Hot Swap (ON_SEL), two LEDs to indicate power good (PWRGD) and fault (FAULT) conditions, seven banana jacks for connecting power supplies and load, and many turrets and pads for observing circuit signals.

Table 1. DC2315A Assembly Options

VERSION	PART	OVERCURRENT FAULT
DC2315A-A	LTC4235-1	LATCHOFF
DC2315A-B	LTC4235-2	RETRY

Design files for this circuit board are available at <http://www.linear.com/demo/DC2315A>

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PERFORMANCE SUMMARY Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supplies						
V _{IN}	Input Supply Range		9		14.0	V
I _{LIM}	Board Current Limit	OUT = 11V OUT = 0V	8 2.3	9 3.3	11.1 4.3	A A
V _{INTVCC}	Internal Regulator Voltage		4.5	5	5.5	V
V _{INTVCC(UVL)}	Internal V _{CC} Undervoltage Lockout	INTV _{CC} Rising	2.1	2.2	2.3	V
Ideal Diode Control						
ΔV _{FWD(REG)}	Forward Regulation Voltage (V _{INn} - V _{SENSE+})		2	15	28	mV
ΔV _{DGATE}	External N-Channel Gate Drive (V _{DGATEn} - V _{INn})	ΔV _{FWD} = 0.15V, I = 0, -1μA	10	12	14	V
I _{CPO(UP)}	CPOn Pull-Up Current	CPO = IN = 12V	-50	-90	-120	μA
I _{DGATE(FPU)}	DGATEn Fast Pull-Up Current	ΔV _{FWD} = 0.2V, ΔV _{DGATE} = 0V, CPO = 17V		-1.5		A
I _{DGATE(FPD)}	DGATEn Fast Pull-Down Current	ΔV _{FWD} = -0.2V, ΔV _{DGATE} = 5V		1.5		A
I _{DGATE2(DN)}	DGATE2 Off Pull-Down Current	D2OFF = 2V, ΔV _{DGATE2} = 2.5V	50	100	200	μA
t _{ON(DGATE)}	DGATEn Turn-On Delay	ΔV _{FWD} = 0.2V, C _{DGATE} = 10nF		0.25	0.5	μs
t _{OFF(DGATE)}	DGATEn Turn-Off Delay	ΔV _{FWD} = -0.2V, C _{DGATE} = 10nF		0.2	0.5	μs
t _{PLH(DGATE2)}	D2OFF Low to DGATE2 High			50	100	μs

PERFORMANCE SUMMARY

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Hot Swap Diode Control						
$\Delta V_{SENSE(TH)}$	Current Limit Sense Voltage Threshold ($V_{SENSE+} - V_{SENSE-}$)	OUT = 11V OUT = 0V	22.5 5.8	25 8.3	27.5 10.8	mV mV
$V_{SENSE+(UVL)}$	SENSE+ Undervoltage Lockout	SENSE+ Rising	1.8	1.9	2	V
$\Delta V_{SENSE+(HYS)}$	SENSE+ Undervoltage Lockout Hysteresis		10	50	90	mV
ΔV_{HGATE}	External N-Channel Gate Drive ($V_{HGATE} - V_{OUT}$)	$I = 0, -1\mu A$	10	12	14	V
$\Delta V_{HGATE(H)}$	External N-Channel Gate High Threshold ($V_{HGATE} - V_{OUT}$)		3.6	4.2	4.8	V
$I_{HGATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate Drive On, $H_{GATE} = 0V$	-7	-10	-13	μA
$I_{HGATE(DN)}$	External N-Channel Gate Pull-Down Current	Gate Drive Off, OUT = 12V, $H_{GATE} = OUT + 5V$	1	2	4	mA
$I_{HGATE(FPD)}$	External N-Channel Gate Fast Pull-Down Current	Fast Turn-Off, OUT = 12V, $H_{GATE} = OUT + 5V$	100	200	350	mA
$V_{OUT(PGTH)}$	OUT Power Good Threshold	OUT Rising	10.2	10.5	10.8	V
Input/Output Pin						
$V_{ON(TH)}$	ON Pin Threshold Voltage	ON Rising	1.21	1.235	1.26	V
$V_{ON(RESET)}$	ON Pin Fault Reset Threshold Voltage	ON Falling	0.57	0.6	0.63	V
$V_{D2OFF(H,TH)}$	D2OFF Pin High Threshold Voltage	D2OFF Rising	1.21	1.235	1.26	V
$V_{D2OFF(L,TH)}$	D2OFF Pin Low Threshold Voltage	D2OFF Pin Failing	1.19	1.215	1.24	
$V_{FTMR(H)}$	FTMR Pin High Threshold Voltage		1.198	1.235	1.272	V
$I_{FTMR(UP)}$	FTMR Pull-Up Current	FTMR = 1V, In Fault Mode	-80	-100	-120	μA
$I_{FTMR(DN)}$	FTMR Pull-Down Current	FTMR = 2V, No Faults	1.3	2	2.7	μA
D_{RETRY}	Auto-Retry Duty Cycle		0.07	0.15	0.23	%
Current Monitor						
ΔV_{REG}	Floating Regulator Voltage ($V_{SENSE+} - V_{SENSE-}$)	$I_{REG} = \pm 1\mu A$	3.6	4.1	4.6	V
$V_{IMON(OS)}$	IMON Input Offset Voltage	$\Delta V_{SENSE} = 0V$			± 150	μV
G_{IMON}	IMON Voltage Gain	$\Delta V_{SENSE} = 20mV$ and $5mV$	99	100	101	V/V
$V_{IMON(MIN)}$	IMON Minimum Output Voltage	$\Delta V_{SENSE} = 200\mu V$			40	mV
$R_{IMON(OUT)}$	IMON Output Resistance	$\Delta V_{SENSE} = 200\mu V$	15	20	27	k Ω

OPERATING PRINCIPLES

The LTC4235 is intended to build a combination of two diode-OR circuits (for two rails) and a common single Hot Swap path for inrush current limiting and overcurrent protection.

The LTC4235 regulates the forward voltage drop across the ideal diode MOSFET to ensure smooth current transfer from one supply to the other without oscillation. A fast ideal diode MOSFET turn-on reduces the load voltage droop during supply switchover. If the input supply fails or is shorted, a fast turn-off minimizes reverse current transients.

The Hot Swap fast acting current limit and internal timed circuit breaker protect circuit components when a short-circuit fault occurs.

The Hot Swap section of the LTC4235 has independent on/off control (ON pin).

Each ideal diode MOSFET is activated from an individual charge pump source and the second ideal diode has an additional on/off control (D2OFF pin).

The DC2315A-A (LTC4235-1) features a latching circuit breaker, while the DC2315A-B (LTC4235-2) provides automatic retry after a fault.

Banana Jacks with Associated Turrets

IN1 (E1, E2): First rail input.

IN2 (E5, E6): Second rail input.

GND (E3, E4, E7, E8, E14, E15, E21, E22): Power and control ground.

SENSE+ (E16, E17): SENSE+ power node.

OUT (E12, E13): Circuit output for load connection.

Turrets

ON (E18): On control input.

$\overline{\text{EN}}$ (E19): Enable input.

D2OFF (E20): Enable ideal diode 2.

$\overline{\text{PWRGD}}$ (E9): Power status output.

$\overline{\text{FAULT}}$ (E10): Fault status output.

CMON (E11): Current sense monitoring output.

Jumpers

JP1 (ON_SEL): ON control signal selection.

JP2 (EN_SEL): Enable signal selection.

JP3 (DIODE2_OFF): Diode 2 Off-On control.

JP4 (PPRI_SEL): Prioritizer function selection.

LEDs

D3: Indicates power good signal.

D4: Indicates fault signal.

QUICK START PROCEDURE

Demonstration circuit 2315A is easy to set up to evaluate the performance of the LTC4235. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below.

The DC2315A test includes independent test of the LTC4235 Hot Swap functionality and ideal diode functionality.

HOT SWAP FUNCTIONALITY TEST

This test is performed with a single rail operation when the output is provided through two series connected MOSFETs. One MOSFET functions as an ideal diode and the other as a Hot Swap circuit switch.

The parameters of the three different transients completely characterize the Hot Swap circuit performance. These transients are:

- A Power-Up Without Any Additional Load
- A Current Limit Operation After Successful Power-Up
- A Power-Up With Shorted Output

1. Initially, install the jumpers in the following positions, if the first ideal diode is used in the test:

JP1: ON_SEL in the position OFF

JP2: EN_SEL in the position EN

JP3: DIODE2_OFF in the position OFF_EXT

If the second ideal diode is used:

JP1: ON_SEL in the position OFF

JP2: EN_SEL in the position EN

JP3: DIODE2_OFF in the position ON

Connect a +12V power supply to turrets IN1 and GND. Do not load the output. Place the current probe on the +12V wire, voltage probes on the OUT turret and a voltmeter on the CMON and GND turrets.

Provide an ON signal at the ON pin by changing the JP1 header position from the OFF position to 12V. Observe the transient. The output voltage rise time should be in the range of 8.9ms – 19.7ms. The PWRGD green LED D3 must light. The voltmeter at the CMON turret should display an absolute value not larger than 15mV. Turn off the rail using the ON_SEL jumper.

2. Connect a disabled electronic load to the OUT turret and GND. Turn on the rail and slowly increase the load current up to the circuit breaker threshold level. The current limit range should be from 8.0A to 11.1A. The voltage at the CMON turret should be in the range from 2.22V to 2.77V. Turn off the rail with the ON_SEL jumper.
3. Initially short the output with an external wire. Place the current probe on this wire. Turn on the rail and record the current shape. The maximum current should be in the 2.3A to 4.3A range, and the voltage at the CMON turret should be in the range from 0.57V to 1.09V.

IDEAL DIODE FUNCTIONALITY TEST

In this test, both ideal diodes are active and small variations in the input voltage forces one ideal diode to be off and the other ideal diode to be on.

Connect input turrets (IN1 and IN2) of each ideal diode with independent lab supplies. Adjust each input voltage to +12V with maximum possible accuracy. Place one voltmeter between IN1 and IN2 turrets to measure the difference between the two input voltages. Connect an electronic load to the output turret. Activate both rail and keep a load around 9A. Play with the input voltage levels and check that when the difference between input voltages exceeds 28mV, only one rail feeds the load.

QUICK START PROCEDURE

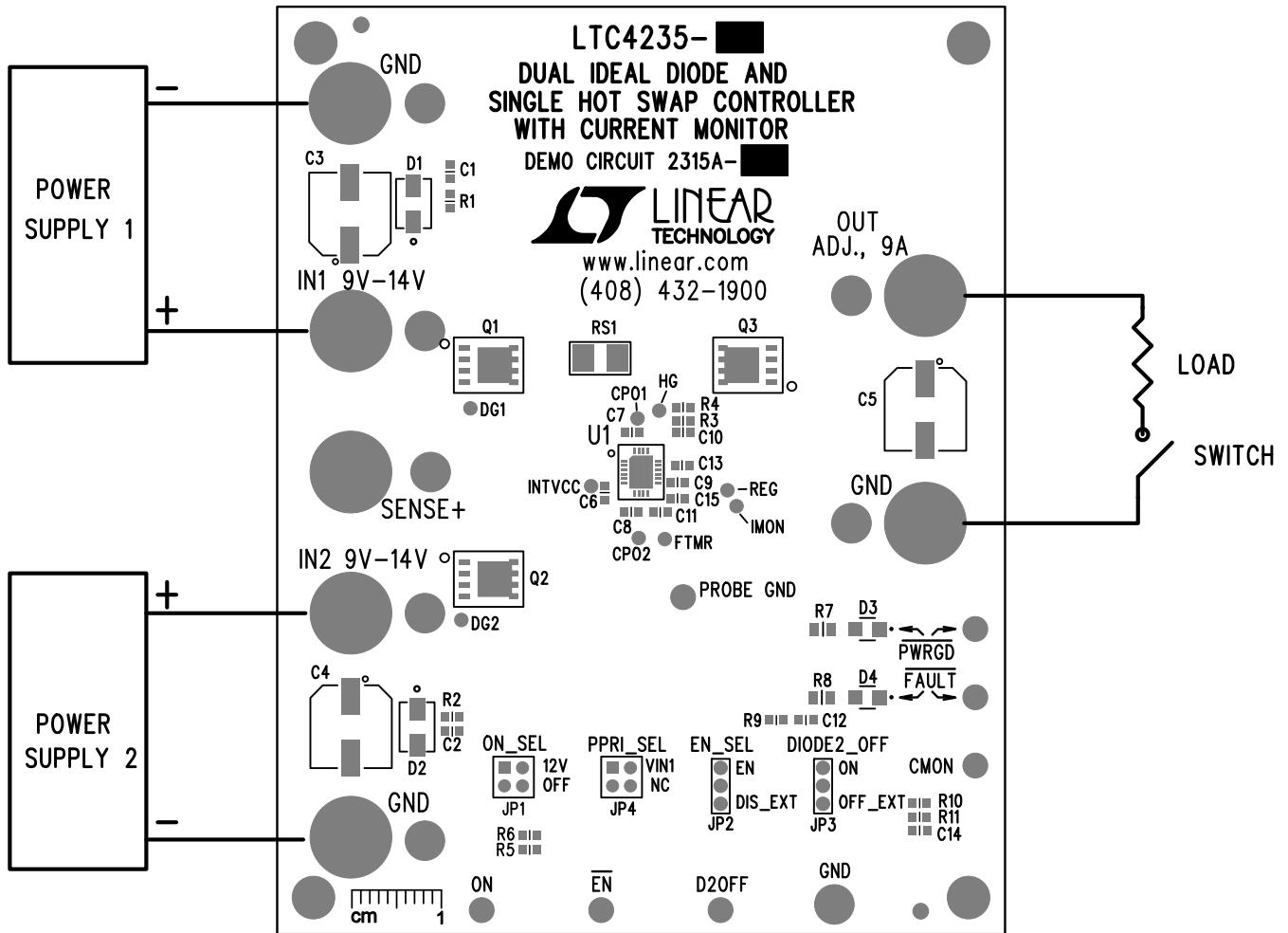


Figure 1. Proper Measurement Equipment Setup

DEMO MANUAL DC2315A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	8	C1, C2, C6, C7, C8, C9, C13, C14	CAP., 0.1 μ F, X7R, 50V, 10%, 0603	TDK, C1608X7R1H104K
2	0	C3, C4	CAP., 100 μ F, ALUM. ELECT., 50V, 20%, SMT (OPTIONAL)	SUNCON, 50CE100BS
3	1	C5	CAP., 100 μ F, ALUM. ELECT., 50V, 20%, SMT	SUNCON, 50CE100BS
4	1	C10	CAP., 0.01 μ F, X7R, 50V, 10%, 0603	AVX, 06035C103KAT2A
5	2	C11, C15	CAP., 0.1 μ F, X7R, 16V, 10%, 0603	AVX, 0603YC104KAT2A
6	1	C12	CAP., 0.47 μ F, X7R, 16V, 10%, 0603	TDK, C1608X7R1C474K
7	2	D1,D2	DIODE, TVS, 17V, SMA	DIODES INC., SMAJ17A-13-F
8	1	D3	LED, GREEN, WATERCLEAR, 3 \times 2mm	ROHM, SML-010FTT86
9	1	D4	LED, RED, WATERCLEAR, 3 \times 2mm	ROHM, SML-010VTT86
10	7	E1, E3, E5, E7, E12, E14, E16	BANANA JACK, NON-INSULATED	KEYSTONE, 575-4
11	8	E2, E4, E6, E8, E13, E15, E17, E21	TEST POINT, TURRET, 0.094" MTG. HOLE	MILL-MAX, 2501-2-00-80-00-00-07-0
12	7	E9, E10, E11, E18, E19, E20, E22	TEST POINT, TURRET, 0.064" MTG. HOLE	MILL-MAX, 2308-2-00-80-00-00-07-0
13	2	JP1, JP4	CONN., HEADER, 2 \times 2, 2mm, THRU-HOLE, VERTICAL	SAMTEC, TMM-102-02-L-D
14	2	JP2, JP3	CONN., HEADER, 1 \times 3, 2mm, THRU-HOLE, VERTICAL	SAMTEC, TMM-103-02-L-S
15	4	MP1, MP2, MP3, MP4	STANDOFF, NYLON 0.5"	KEYSTONE, 8833 (SNAP ON)
16	3	Q1, Q2, Q3	MOSFET, N-CH 30V 60A METAL OXIDE, PPAK	VISHAY, SIR158DP-T1-GE3
17	1	RS1	RES., 0.0025 Ω , METAL ELEMENT, 1%, 1/2W 2010	VISHAY, WSL20102L500FEA
18	2	R1, R2	RES., 100 Ω , 1/10W, 1%, 0603	YAGEO, RC0603FR-07100RL
19	2	R3, R9	RES., 1k, 1/10W, 1%, 0603	YAGEO, RC0603JR-071KL
20	1	R4	RES., 10 Ω , 1/10W, 1%, 0603	YAGEO, RC0603FR-0710RL
21	1	R5	RES., 2k, 1/10W, 1%, 0603	YAGEO, RC0603FR-072KL
22	1	R6	RES., 13.7k, 1/10W, 1%, 0603	YAGEO, RC0603FR-0713K7L
23	2	R7, R8	RES., 3.0k, 1/8W, 1%, 0805	VISHAY, CRCW08053K00FKEA
24	1	R10	RES., 2.49k, 1/10W, 1%, 0603	YAGEO, RC0603FR-072K49L
25	1	R11	RES., 21k, 1/10W, 1%, 0603	VISHAY, CRCW060321K0FKEA
26	4	XJP1, XJP2, XJP3, XJP4	SHUNT, 2mm	SAMTEC, 2SN-BK-G

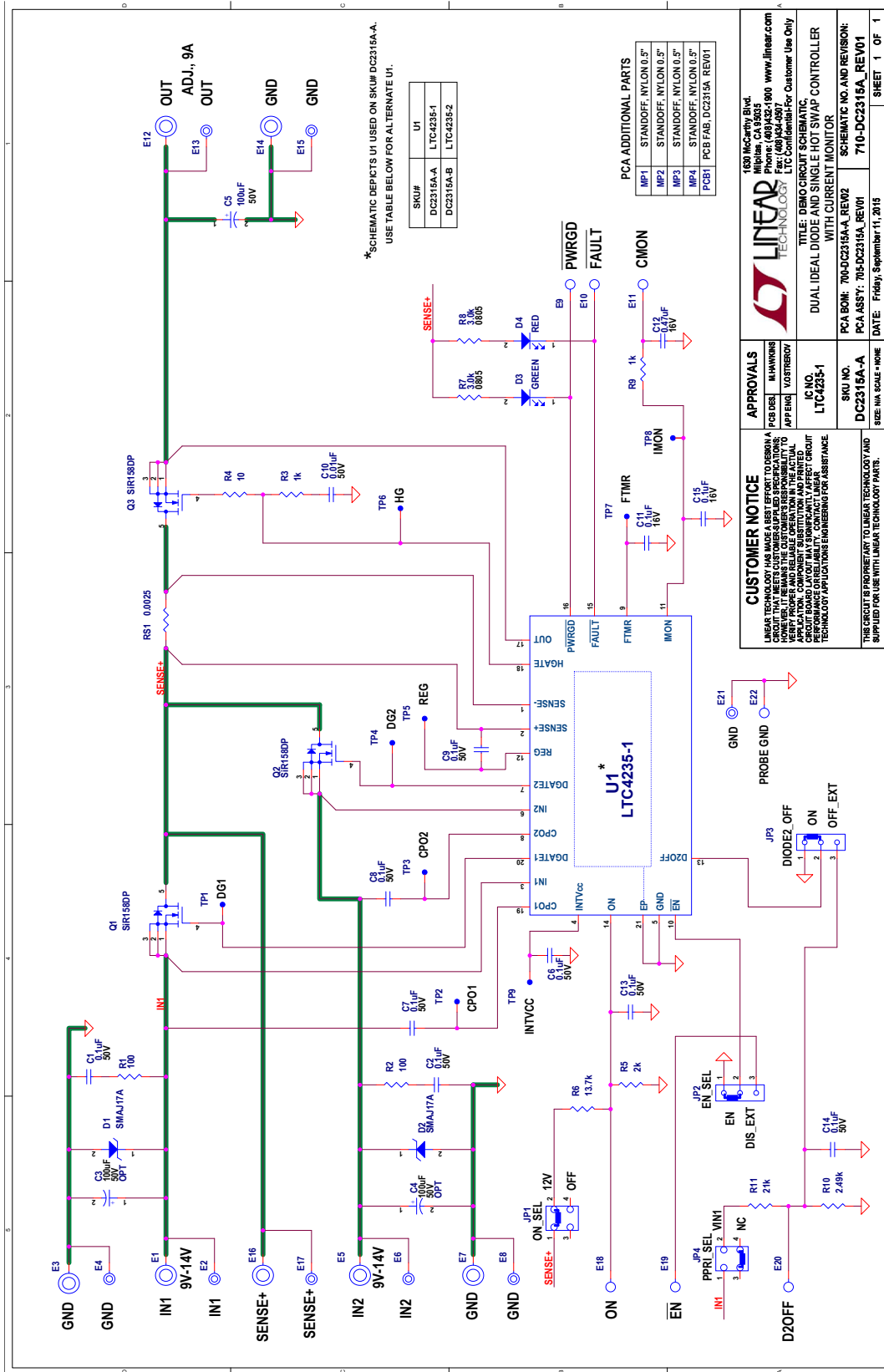
DC2315A-A

1	1	U1	IC, IDEAL DIODE & Hot Swap CONTROLLER, QFN	LINEAR TECH., LTC4235IUFD-1
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DC2315A-B

1	1	U1	IC, IDEAL DIODE & Hot Swap CONTROLLER, QFN	LINEAR TECH., LTC4235IUFD-2
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SCHEMATIC DIAGRAM



Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

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