

# LTC5589

## 700MHz to 6000MHz LOW POWER I/Q MODULATOR

### DESCRIPTION

Demonstration circuit 2391A is optimized for evaluation of the [LTC<sup>®</sup>5589](#) low power I/Q modulator up to 4.5GHz. For frequencies above 4.5GHz, LO matching circuit on the DC2391A demo board can be easily modified for improved image rejection performance. Refer to data sheet for additional information. The four balanced I- and Q-baseband input ports can be either AC-coupled with internal bias supplied, or DC-coupled from a source with a common-mode voltage level of about +1.4V. The SPI interface is used to set internal registers which control the gain, optimum center frequency, I-offset, Q-offset and sideband suppression. In addition to the digital gain control with 1dB steps, there is an analog gain control,  $V_{CTRL}$ . An on-chip thermometer can be used to compensate for the gain vs temperature variations using a digital gain control change. The update can either be automatically triggered, or entirely switched off.

### ABSOLUTE MAX INPUT RATINGS

Supply Voltage: .....	+3.8V
Common Mode Level of BBPI, BBMI, BBPQ, and BBMQ: .....	+2V
LOL, LOC DC Voltage: .....	±50mV
LOL, LOC Input Power: .....	+20dBm
TEMP, SDO Current Sink .....	10mA
Voltage on Any Pin Not to Exceed .....	-0.3V to ( $V_{CC} + 0.3V$ )
$T_{JMAX}$ .....	150°C
Operating Temperature Range .....	-40°C to 105°C
Storage Temperature Range .....	-65°C to 150°C

**CAUTION:** This part is sensitive to electrostatic discharge (ESD). Observe proper ESD precautions when handling the LTC5589.

Design files for this circuit board are available at <http://www.linear.com/demo/DC2391A>

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### TEST SETUP

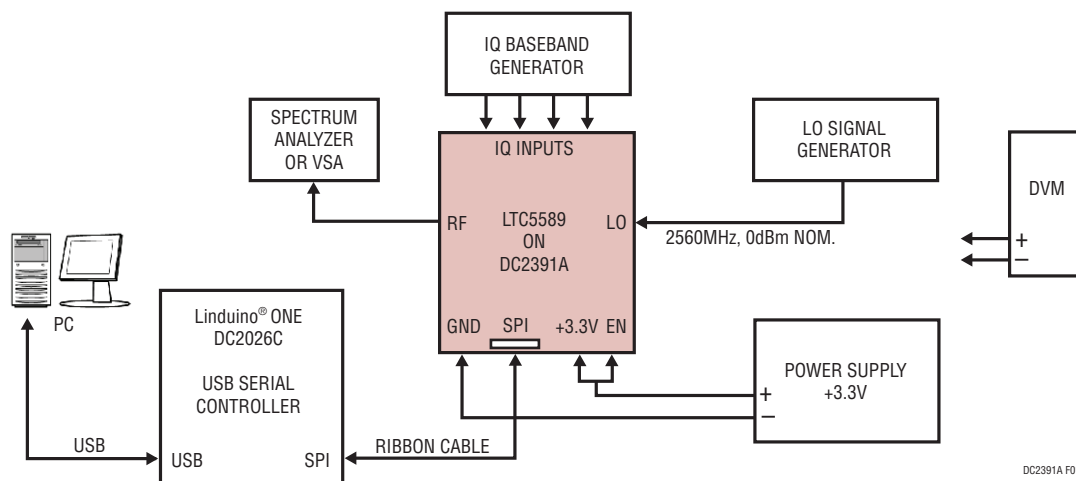


Figure 1: Test Setup for RF Performance Measurements

## NOTES ON TEST EQUIPMENT AND SETUP

- Use a high performance baseband signal generator with differential outputs, such as the Rohde & Schwarz SMJ100A vector signal generator or equivalent.
- The LO harmonics can degrade image rejection severely. Third harmonic should be kept at least 6dB lower than the desired image rejection, or it should be compensated by adjusting the quadrature phase balance, register 0x05. In the extreme case of nearly square wave LO drive, large offset values may be required for registers 0x04 and 0x05.
- Use narrow resolution bandwidth (RBW) and engage video averaging on the spectrum analyzer to lower the displayed average noise level (DANL). The trade-off is increased sweep time.
- Spectrum analyzers can produce significant internal distortion products if overdriven. Generally, spectrum analyzers are designed to operate their best with about  $-30$  to  $-40$ dBm at their 1st mixer. Sufficient spectrum analyzer input attenuation should be used to avoid overdrive, but too much attenuation reduces sensitivity and dynamic range.
- Before taking measurements, the system performance should be evaluated to ensure that: 1) clean baseband signals can be produced, 2) the LO harmonics and phase noise are minimized for CW LO drive, 3) the spectrum analyzer's internal distortion is minimized, and noise floor is satisfactory.

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## QUICK START PROCEDURE

1. Remove the DC2391A from its protective packaging in an ESD-safe working area (see Figure 1). Make sure jumper JP1 is installed ( $V_{CTRL} = V_{CC}$ ).
2. Set the baseband signal generator output DC common-mode voltage to +1.4VDC, set the amplitude ( $V_{emf}$ ) = 1V diff, but do not yet connect the 4 cables to the DC2391A.
3. Connect the DC power supply and increase voltage to +3.3V. Using a voltmeter, verify the voltage at the LTC5589  $V_{CC}$  pin or JP1 is +3.3V. Adjust if necessary.
4. Apply 3.3V to DC2391A's enable input (EN). The enable voltage must never exceed the LTC5589's  $V_{CC}$  supply voltage by 0.3V or drop below  $-0.3$ V.
5. Verify the total  $V_{CC}$  supply current is approximately 29mA.
6. Connect the RF output to the spectrum analyzer.
7. Connect the LO source to the LO input and apply a 2560MHz, 0dBm CW LO signal.
8. Configure the baseband signal source to provide a single CW carrier with 100kHz offset. I- and Q-channels should be in phase-quadrature and set for lower sideband selection.
9. Observe the modulator's RF output on the spectrum analyzer at 2559.9MHz. Also observe the sideband suppression (aka Image Rejection) at 2560.1MHz, and the LO Leakage at 2560MHz.
10. Up to this point, the I/Q Modulator has been at default center frequency and gain, with no trims. To change modulator center frequency, gain, etc., connect the Linduino to the DC2391A with the ribbon cable provided. Make sure jumper JP3 on the DC2026C is set to 3.3V.
11. Run QuikEval™ to start the GUI associated with the I/Q modulator.
12. Be sure to update the QuikEval to get latest software version that supports the LTC5589. LTC5589 GUI will automatically be installed on the computer for the first time when DC2391A is connected to Linduino DC2026C.
13. The turn off procedure is the reverse of the turn on procedure: Make sure  $V_{EN}$  is removed before  $V_{CC}$ .

**QuikEval SOFTWARE**

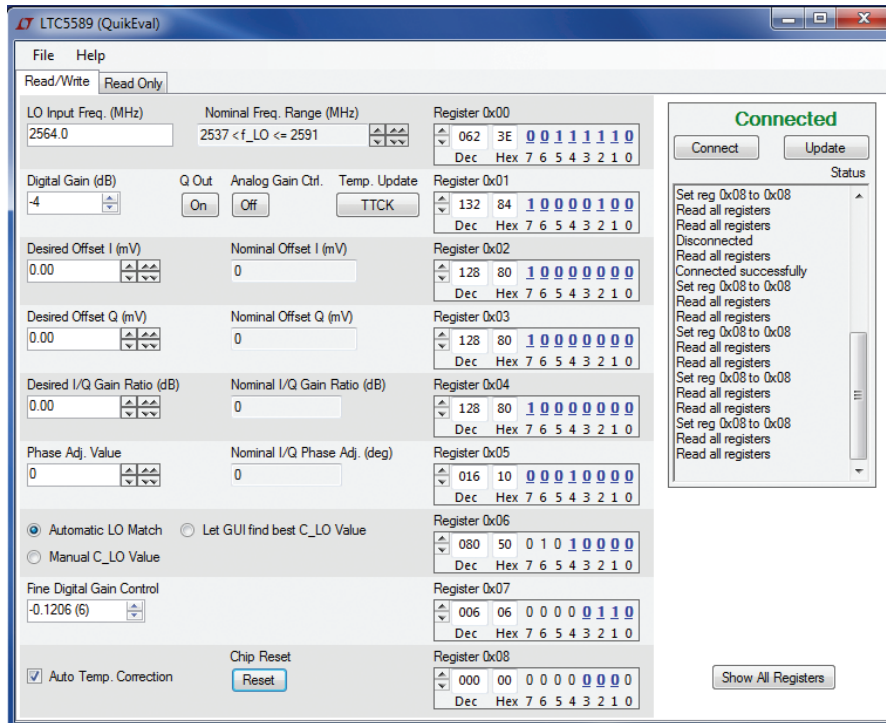


Figure 2: QuikEval Screen

**QuikEval Usage Notes**

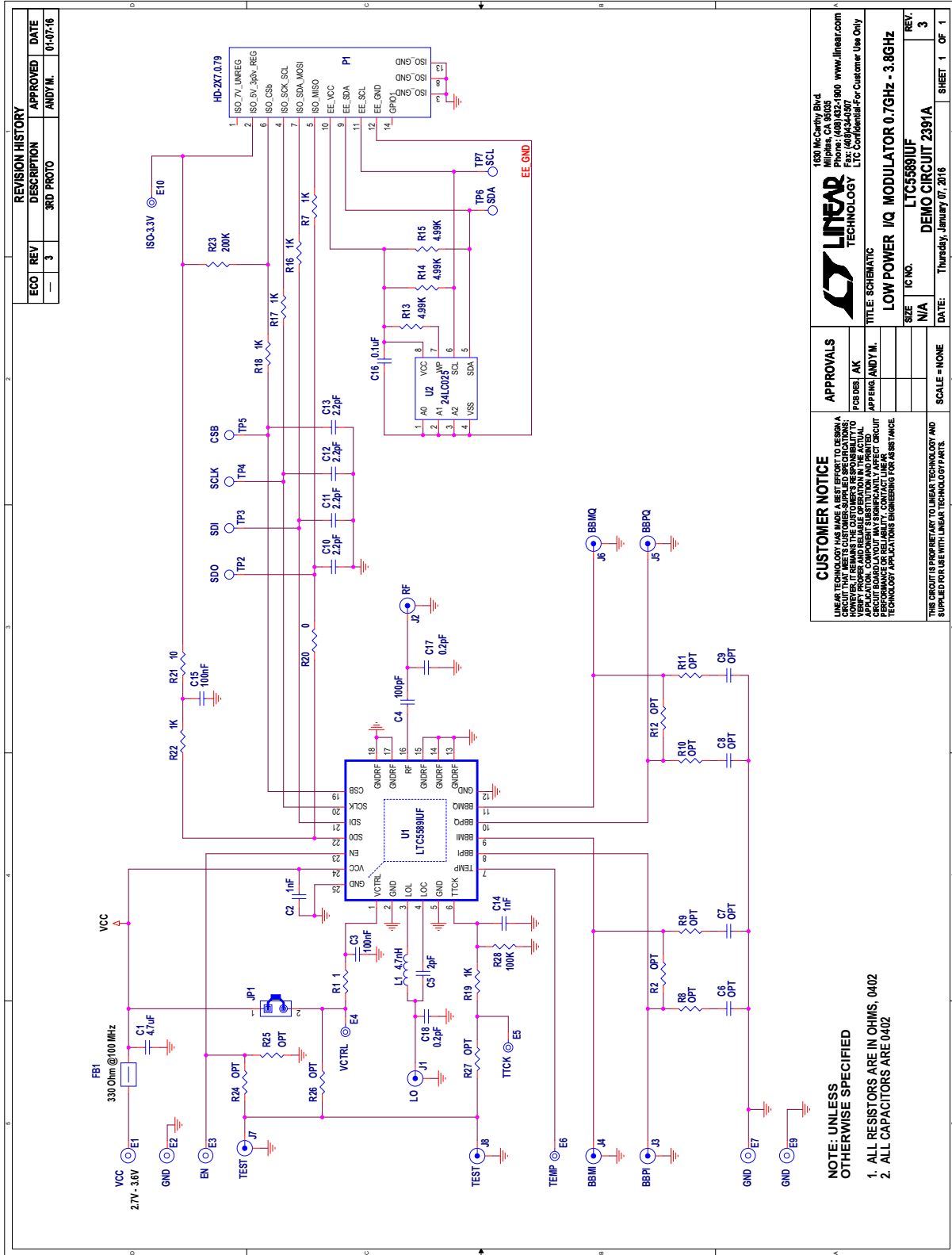
1. The LTC5589 QuikEval is a modified version of the LTC5599 QuikEval program. The Windows Start Menu for LTC5589 will say LTC5599 LTC5589. That's OK. The correct form will be automatically loaded.
2. The status box at the right shows activity, and should show Connected. Begin by clicking "Reset". Red font notification occurs if anything wrong. If SPI connection is lost, simply click "Connect" near top right corner.
3. When a new LO frequency is entered in the top left corner of the form, followed by Enter key, the software calculates a new register 0x00 value, shows it, loads it, and reads back to verify.
4. Gain is easily modified here. DC current consumption automatically scales with gain changes (lower RF output power permits lower DC current).
5. If desired, I and Q DC offsets can be trimmed out, as can SSB suppression, via the controls on left side of form.
6. In end applications, Linduino C code is available to help user get from engineering units (MHz, dB gain, mV, dB and degrees imbalance) to register values, and vice versa.
7. The LTC5589 registers reset to default while starting QuikEval GUI, which defaults CLOEN bit (bit 4, register 0x06) to 1. This allows for the automatic adjustment of the LO match. For large phase adjustments, the I/Q phase extension bits are changed from default, and it is recommended to let GUI find the best C\_LO values (checkbox in GUI) in order to avoid phase discontinuities during I/Q phase extension bits changes. In that case, the CLOEN bit is cleared and CLOO override bits in register 0x06 are used to keep the LO match the same while the polyphase filter center frequency is adjusted in order to maintain a smooth phase adjustment during the I/Q phase extension bits changes. For more information, refer to the LTC5589 data sheet.

# DEMO MANUAL DC2391A

## PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	1	C1	CAP, X5R, 4.7µF, 10%, 16V, 0603	MURATA, GRM188R61C475KAAJD
2	2	C2, C14	CAP, COG, 1000pF, 5%, 50V, 0402	MURATA, GRM1555C1H102JA01D
3	3	C3, C15, C16	CAP, X7R, 0.1µF, 10%, 16V, 0402	MURATA, GRM155R71C104KA88D
4	1	C4	CAP, COG, 100pF, 5%, 25V, 0402	MURATA, GRM1555C1E101JA01D
5	1	C5	CAP, COG, 2pF, ±0.05pF, 50V, 0402	MURATA, GJM1555C1H2R0WB01D
6	0	R2, C6, C7, R8, C8, R9, C9, R10, R11, R12, R24, R25, R26, R27	OPT, OPT	
7	4	C10, C11, C12, C13	CAP, COG, 2.2pF, ±0.1pF, 25V, 0402	MURATA, GRM1555C1E2R2BZ01D
8	2	C17, C18	CAP, COG, 0.2pF, ±0.05pF, 50V, 0402	MURATA, GRM1555C1HR20WA01D
9	5	E1, E2, E3, E7, E9	TESTPOINT, TURRET, 0.094"	MILL-MAX, 2501-2-00-80-00-00-07-0
10	4	E4, E5, E6, E10	TESTPOINT, TURRET, 0.063"	MILL-MAX, 2308-2-00-80-00-00-07-0
11	1	FB1	FERRITE BEAD, 330Ω @100MHz	TDK, MPZ1608S331AT00
12	1	JP1	HEADER, 2-PIN 0.079 SINGLE ROW	SULLINS, NRPN021PAEN-RC
13	1	XJP5	SHUNT, 2mm CTRS.	SAMTEC, 2SN-BK-G
14	6	J1-J6	CONN., SMA, 50Ω, EDGE-LANCH	E. F. JOHNSON, 142-0701-851
15	0	J7, J8	CON., OPT	
16	1	L1	IND., 4.7nH, 0402HP	COILCRAFT, 0402HP-4N7XJLU
17	1	P1	HEADER, 2X7PIN, 0.079CC	MOLEX, 87831-1420
18	1	R1	RES., CHIP, 1, 1%, 0402	VISHAY, CRCW04021R00FKED
19	6	R7, R16, R17, R18, R19, R22	RES., CHIP, 1k, 1%, 0402	VISHAY, CRCW04021K00FKED
20	3	R13, R14, R15	RES., CHIP, 4.99k, 1%, 0402	VISHAY, CRCW04024K99FKED
21	1	R20	RES., CHIP, 0Ω, 0402	VISHAY, CRCW04020000Z0ED
22	1	R21	RES., CHIP, 10Ω, 1%, 0402	VISHAY, CRCW040210R0FKED
23	1	R23	RES., CHIP, 200k, 1%, 0402	VISHAY, CRCW0402200KFKED
24	1	R28	RES., CHIP, 100k, 1%, 0402	VISHAY, CRCW0402100KFKED
25	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 2391A
26	1	U1	IC., LOW POWER DIRECT QUADRATURE MODULATOR, QFN-24-4X4	LINEAR TECH., LTC5589IUF#PBF
27	1	U2	IC, EEPROM 2-KBIT 400kHz 8TSSOP	MICROCHIP TECH., 24LC025-I/ST
28	2		STENCIL (TOP AND BOTTOM)	STENCIL DC2391A
29	1		CABLE ASSY., 8 STRIP	LINEAR RIBBON CABLE ;

SCHEMATIC DIAGRAM



REVISION HISTORY			
ECO	REV	DESCRIPTION	APPROVED DATE
—	3	3RD PROTO	ANDY M. 01/07/16

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**APPROVALS**  
PCB DES: AK  
APP'NG: ANDY M.

**TITLE: SCHEMATIC**

**LOW POWER I/Q MODULATOR 0.7GHz - 3.8GHz**

IC NO. **LTC5589JUF**

REV. **3**

DATE: Thursday, January 07, 2016

SHEET 1 OF 1

SCALE = NONE

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- NOTE: UNLESS OTHERWISE SPECIFIED**
1. ALL RESISTORS ARE IN OHMS, 0402
  2. ALL CAPACITORS ARE 0402

# DEMO MANUAL DC2391A

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