## LTC3246EMSE <br> Wide $\mathrm{V}_{\mathrm{IN}}$ Range Buck-Boos $\dagger$ Charge Pump with Watchdog Timer

## DESCRIPTION

Demonstration circuit 2466A is a buck-boost 500 mA charge pump with pin selectable output voltages and includes a watchdog timer featuring the LTC ${ }^{\circledR} 3246 E M S E$. The LTC3246 operates with a wide input voltage range from 2.7 V to 38 V and is engineered for diagnostic coverage for ISO 262262 compliant systems. The wide VIN operating range will allow the LTC3246 to provide up to 500 mA sufficiently during an automotive cold crank.

The LTC3246 data sheet gives a complete description of the device, operation and application information. The data sheet must be read in conjunction with this demo manual.

Design files for this circuit board are available at http://www.linear.com/demo/DC2466A
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## PGRFORMANCE SUMMARY

Specifications are at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| $V_{\text {IN }}$ | $V_{\text {IN }}$ Input VoItage Range |  | 2.7 | 38 | V |  |
| $V_{\text {ADJ }}$ | SEL2 $=$ LOW, SEL1 $=$ HIGH | $2.7 \mathrm{~V}<\mathrm{V}_{\text {IN }}<38 \mathrm{~V}$ | 1.07 | 1.1 | 1.13 | V |
| $V_{\text {OUTS_5 }}$ | SEL2 $=$ HIGH, SEL1 $=$ LOW | $2.7 \mathrm{~V}<\mathrm{V}_{\text {IN }}<38 \mathrm{~V}$ | 4.8 | 5.0 | 5.2 | V |
| $V_{\text {OUTS_3 }}$ | SEL2 $=$ HIGH, SEL1 $=$ HIGH | $2.7 \mathrm{~V}<\mathrm{V}_{\text {IN }}<38 \mathrm{~V}$ | 3.17 | 3.3 | 3.43 | V |

## BOARD PHOTO



## DEMO MANUAL DC2466A

## TYPICAL APPLICATIONS

Regulated 5V Output with Pushbutton Reset


Output Voltage vs Input Voltage


## PUICK START PROCEDURE

Refer to Figure 1 for the proper measurement equipment setup and jumper settings and follow the procedure below.
NOTE: When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the $\mathrm{V}_{\text {IN }}$ or $V_{\text {OUT }}$ and GND terminals. See Figure 2 for proper scope probe technique.

1. Make sure the jumper settings are as follows:

JP1: SEL1 is on the HI position
JP2: SEL2 is on the HI position
JP3: CRT is on the INT position
JP4: CWT is on the DIS position
JP5: RSTI is on the HI position
2. Set PS1 to 14 V and then turn on.
3. Slowly increase LD1 to 500 mA and observe VOUT is regulating at 3.3 V and that the input current is about $1 / 2$ of the output current. The LTC3246 is in 2:1 mode.
4. Decrease PS1 to 5 V and observe that VOUT is 3.3 V and the input current is about equal to the output current. The LTC3246 is in $1: 1$ mode.
5. Decrease PS1 to 3 V and observe that VOUT is 3.3 V and the input current is about $2 x$ the output current. The LTC3246 is in 1:2 mode.
6. Turn off PS1 and set LD1 to OA.
7. Set the SEL1 jumper, JP1, to the L0 position.
8. Set PS1 to 14 V and then turn on.
9. Slowly increase LD1 to 500 mA and observe VOUT is regulating at 5 V and that the input current is about $1 / 2$ of the output current. The LTC3246 is in 2:1 mode.
10. Decrease PS1 to 9 V and observe that VOUT is 5 V and the input current is about equal to the output current. The LTC3246 is in $1: 1$ mode.
11. Decrease PS1 to 3.3 V and observe that VOUT is 5 V and the input current is about $2 x$ the output current. The LTC3246 is in 1:2 mode.
12. Set PS1 to 14 V and then turn off LD1.
13. Short the RSTI turret to GND and observe that the voltage on the $\overline{\mathrm{RST}}$ turret is near OV .
14. Remove the short on the RSTI turret and observe with an oscilloscope that the voltage on the RST turret returns to about VOUT.
Note: The reset time can be adjusted by setting the CRT jumper, JP3, to the EXT position and using external capacitors if desired. The external CRT capacitor, C9, is populated with a 2.2 nF to match the times referenced in the data sheet. The reset time can be increased by placing a parallel capacitor on the

## DUICK START PROCEDURE

optional C8 capacitor pads on the bottom side of the board.
15. Set the CWT jumper, JP4, to the EXT positions and observe that the voltage on the RST turret is pulsing between OV and VOUT.
16. Set a pulse generator with a 0 to 5 V , 1 ms pulse width and a 20 ms period on the WDI turret. Observe the voltage on the RST turret is high.
17. Decrease the pulse period below 4.5 ms and observe the voltage on the RST is pulsing again.
18. Slowly increase the pulse period to above 220 ms and observed the voltage on the $\overline{\text { RST }}$ turret returns and stays at VOUT when the period is between about 10 ms and about 160 ms . The voltage on the RST tur-
ret starts to pulse again when the pulse period on the WDI turret increases above 220 ms .

Note: The watchdog time can be adjusted using external capacitors if desired. The external WDT capacitor, C 6 , is populated with a 2.2 nF to match the times referenced in the data sheet. The watchdog time can be increased by placing a parallel capacitor on the optional C7 capacitor pads on the bottom side of the board.
19. To observe the internal watchdog time, set the CWT jumper, JP4, to the INT position. The watchdog upper boundary will now be about 1.6 s and the lower boundary is about 50 ms .
20. Turn off the loads, pulse generator and supply when done evaluation.
21. Return the jumpers to their default settings as shown in Figure 1 if desired.


Figure 1. Proper Measurement Equipment Setup for DC2466A

## DEMO MANUAL DC2466A

## PUICK START PROCEDURE



Figure 2. Measuring Input or Output Ripple

## APPLICATIONS INFORMATION

Figures 3 and 4 illustrate how the efficiency and power loss changes as the input voltage increases for the 5 V and 3.3V output settings.

A $47 \mu \mathrm{~F}$ output capacitor was used on the demo board to provide better output ripple with voltages below 3.3V. Refer to the VOUT ripple and capacitor selection of the data sheet for more information on output capacitor selection.


Figure 4. 3.3V Efficiency and Power Loss vs Input Voltage

## DEMO MANUAL DC2466A

## APPLICATIONS INFORMATION

Figures 5, 6, and 7 show the CISPR 25 class 5 peak conducted and radiated emissions. The data was collected using the ALSE antenna method and a CISPR25 LISN for conducted emissions. The EMI tests were conducted using a 14V input on the VIN EMI input terminal, a $10 \Omega$ resistor on VOUT with VOUT set to 5 V .

Linear Technology has made every effort to provide useful and accurate EMI data, but it remains the responsibility of the customer to ensure product compliance.

CISPR 25
Conducted Emissions -Voltage Method
Supply


Figure 5. CISPR25 Conducted Emissions

## DEMO MANUAL DC2466A

## APPLICATIONS InFORMATION

CISPR 25


Figure 6. CISPR25 Radiated Emissions with Vertical Polarization

## APPLICATIONS INFORMATION

CISPR 25
Radiated Emissions


Figure 7. CISPR25 Radiated Emissions with Horizontal Polarization

## DEMO MANUAL DC2466A

## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| Required Circuit Components |  |  |  |  |
| 1 | 1 | C1 | CAP, 2.2 $\mu \mathrm{F}, \mathrm{X} 5 \mathrm{R}, 10 \mathrm{~V}, 10 \%$, 0603 | MURATA GRM188R61A225KE34D |
| 2 | 1 | C3 | CAP, 1 $\mu \mathrm{F}, \mathrm{X7R}, 50 \mathrm{~V}, 10 \%$, 0805 | MURATA GRM21BR71H105KA12L |
| 3 | 1 | C4 | CAP, 47山F, X5R, 6.3V, 20\%, 0603 | MURATA GRM188R60J476ME15D |
| 4 | 1 | C5 | CAP, 10山F, 6.3V, 10\%, X5R, 0603 | TDK CORPORATION C1608X5ROJ106K080AB |
| 5 | 1 | U1 | IC, WIDE VIN RANGE BB CHARGE PUMP WITH WD TIMER | LINEAR TECHNOLOGY LTC3246EMSE\#PBF |

Additional Demo Board Circuit Components

| 6 | 2 | C2, C12 | CAP, $10 \mu \mathrm{~F}, \mathrm{X} 5 \mathrm{R}, 50 \mathrm{~V}, 10 \%, 1206$ | TDK C3216X5R1H106K |
| :---: | :--- | :--- | :--- | :--- |
| 7 | 2 | C6, C9 | CAP, 2200pF, C0G, $25 \mathrm{~V}, 5 \%, 0402$ | KEMET C0402C222J3GACTU |
| 8 | 0 | C7, C8 | CAP, OPTION, 0402 |  |
| 9 | 0 | C10 | CAP, OPTION, 0805 |  |
| 10 | 1 | C11 | CAP, $0.1 \mu \mathrm{~F}, \mathrm{X} 7 \mathrm{R}, 50 \mathrm{~V}, 10 \%, 0402$ | MURATA GRM155R71H104KE14D |
| 11 | 1 | L1 | IND, $4.7 \mu \mathrm{H}, \mathrm{FERRITE,20} \mathrm{\%,1.95A,90m} \mathrm{\Omega,3mm} \mathrm{\times 2.5mm} \mathrm{\times 1.5mm}$ | TDK VLF302515MT-4R7M |
| 12 | 2 | R1, R2 | RES, $100 \mathrm{k} \Omega, 5 \%, 1 / 16 \mathrm{~W}, 0402$ | YAGEO RC0402JR-07100KL |
| 13 | 1 | R3 | RES, $0 \Omega, 1 / 16 \mathrm{~W}, 0402$ | ROHM MCR01MZPJ000 |
| 14 | 0 | R4 | RES, 0 PTION, 0402 |  |
| 15 | 2 | R5, R7 | RES, $510 \mathrm{k} \Omega, 5 \%, 1 / 16 \mathrm{~W}, 0402$ | VISHAY CRCW0402510KJNED |
| 16 | 1 | R6 | RES, $10 \mathrm{M} \Omega, 5 \%, 1 / 16 \mathrm{~W}, 0402$ | VISHAY CRCW040210MOJNED |

Hardware: For Demo Board Only

| 17 | 5 | E1 TO E4, E11 | TEST POINT, TURRET, 0.094", MTG HOLE | MILL-MAX 2501-2-00-80-00-00-07-0 |
| :---: | :---: | :--- | :--- | :--- |
| 18 | 6 | E5 T0 E10 | TEST POINT, TURRET, 0.064", MTG HOLE | MILL-MAX 2308-2-00-80-00-00-07-0 |
| 19 | 4 | JP1, JP2, JP3,JP5 | CONN, HDR, MALE, $1 \times 3,2 \mathrm{~mm}$, THT, STR | WURTH ELEKTRONIK 62000311121 |
| 20 | 1 | JP4 | CONN, HDR, MALE, $1 \times 4,2 \mathrm{~mm}$, THT, STR | WURTH ELEKTRONIK 62000411121 |
| 21 | 4 | MP1 TO MP4 | STANDOFF, NYLON, SNAP-ON, 0.250" | KEYSTONE 8831 |
| 22 | 5 | XJP1 TO XJP5 | CONN, SHUNT, FEMALE, 2 POS, 2mm | WURTH ELEKTRONIK 60800213421 |

## SCHEMATIC DIAGRAM



## DEMO MANUAL DC2466A

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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