LTC4279
Single Port PoE/PoE+/LTPoE++ PSE Controller

DESCRIPTION

Demonstration circuit 2541A features the LTC®4279, an autonomous single port Power Sourcing Equipment (PSE) controller for use in IEEE 802.3at Type 1, Type 2 and LTPoE++® compliant Power over Ethernet (PoE) systems. The LTC4279 simplifies IEEE and LTPoE++ PSE implementation, requiring only a 45-57V supply and a small number of passive support components.

The DC2541A provides jumper selections for setting the LTC4279 power mode, LEGACY pin, DUALPD pin, and MID pin, as well as the PSE output 2-pair or 4-pair mode. A pushbutton switch resets the LTC4279. LEDs indicate main supply power and output power are up. The Data-In RJ45 connects to a PHY data source and the Data-and-Power-Out RJ45 connects to a PD. The DC2541A is Ethernet Alliance™ certified.

Design files for this circuit board are available.

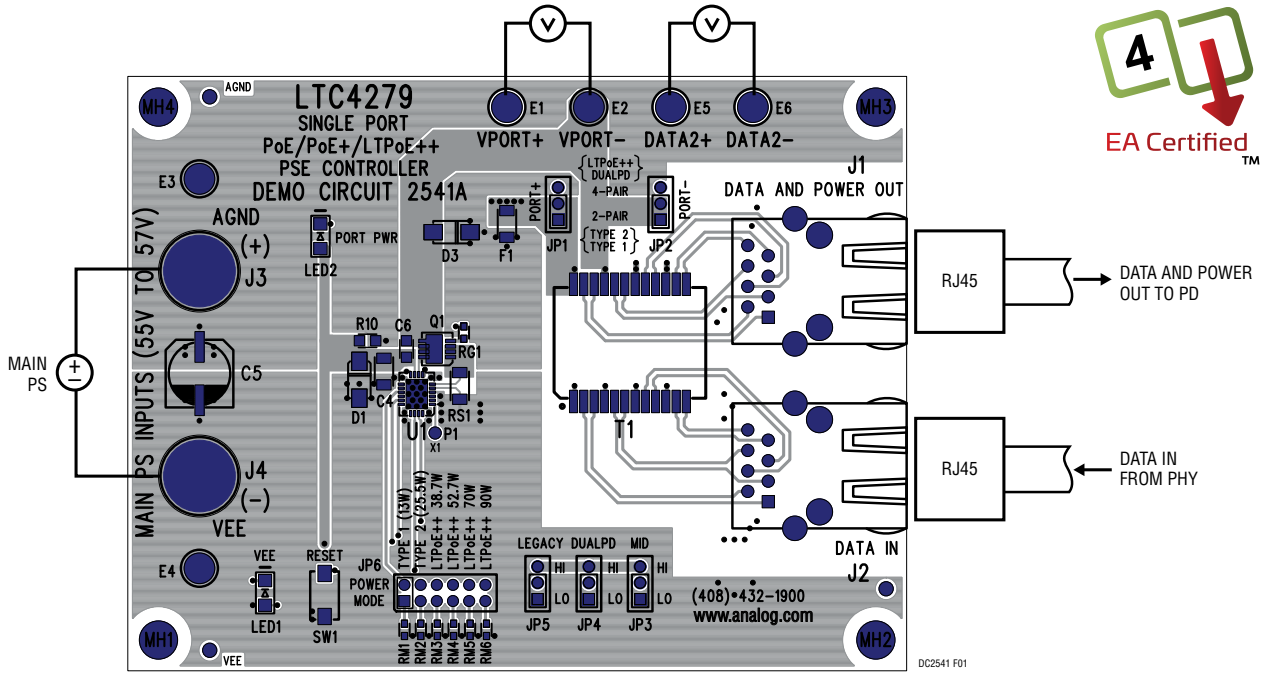

Figure 1. DC2541A Connection Diagram

QUICK START PROCEDURE

Demonstration circuit 2541A is easy to set up for evaluating the performance of the LTC4279. Refer to Figure 1 for proper measurement equipment setup, Table 1 for jumper and supply settings, and follow the procedure below.

1) Select the evaluation PSE Type as shown in Table 1 and set the jumpers accordingly.
2) Connect a power supply with the positive to AGND (J3) and negative to VEE (J4).
3) Ramp up the supply to the recommended values specified in Table 1 for the configured mode. VEE LED1 will turn on when the board is powered.
4) Connect test measurement probes across VPORT+ and VPORT– for 2-pair measurements, and optionally additional test measurement probes across DATA2+ and DATA2– for 4-pair measurements.
5) Connect a PD with a Cat5e Ethernet cable to RJ45 connector J1. PORT PWR LED2 will turn on if the port power is on.
6) Connect a 10BASE-T, 100BASE-T or 1000BASE-T PHY data source with an Ethernet cable to J2 for data testing (optional).

Table 1. Example Jumper Settings and VEE Supply Range for the Various PSE Types (Note 1)

PSE TYPE	POWER MODE (JP6)	PORT+ (JP1)/ PORT– (JP2)	MID (JP3)	DUALPD (JP4)	LEGACY (JP5)	MAIN PS
IEEE 802.3at Type 1 (13W)	TYPE 1 (13W)	2-PAIR	LO/HI	LO	LO	45V to 57V
Legacy	TYPE 1 (13W)	2-PAIR	LO/HI	LO	HI	48V (Typical)
IEEE 802.3at Type 2 (25.5W)	TYPE 2 (25.5W)	2-PAIR	LO/HI	LO	LO	51V to 57V
LTPoE++ (38.7W)	LTPoE++ (38.7W)	4-PAIR	LO/HI	LO	LO	51V to 57V
LTPoE++ (52.7W)	LTPoE++ (52.7W)	4-PAIR	LO/HI	LO	LO	51V to 57V
Dual PD	LTPoE++ (52.7W)	4-PAIR	LO/HI	HI	LO	51V to 57V
LTPoE++ (70W)	LTPoE++ (70W)	4-PAIR	LO/HI	LO	LO	54.75V to 57V
LTPoE++ (90W)	LTPoE++ (90W)	4-PAIR	LO/HI	LO	LO	54.75V to 57V

Note 1: The application is not limited to these settings. See the LTC4279 data sheet pin descriptions.

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Power Control

The primary function of the LTC4279 is to control the delivery of power to the PSE port. It does this by controlling the gate drive voltage of an external power MOSFET (Q1) while monitoring the current via an external sense resistor (RS1) and the output voltage at the OUT pin. This circuitry serves to couple the raw VEE input supply to the port in a controlled manner that satisfies the PD's power needs while minimizing both power dissipation in the MOSFET and disturbances on the VEE backplane.

Power Mode

The LTC4279 is a fully autonomous PSE controller and provides a complete PSE solution for detection, classification and powering of PD devices in an IEEE 802.3 or LTPoE++ compliant system. The LTC4279 will power all valid PDs with I_{CUT} and I_{LIM} values based on the PWRMODE pin and the PD classification result. The LTC4279 will remove power automatically if the port generates a current cutoff or limit fault. The LTC4279 senses removal of a PD and turns off power when the PD is disconnected. Internal control circuits comply with IEEE timing and electrical parameters.

The resistance value at the LTC4279 PWRMODE pin to VEE sets the LTC4279 maximum delivered power. On the DC2541A, the PWRMODE pin is connected with a 10k resistor (RM6) to VEE. The POWER MODE jumper (JP6) selects various resistances in parallel with RM6 to match the recommended R_{PM} value specified in the LTC4279 data sheet. The DC2541A can be set to 13W (IEEE 802.3af), 25.5W (IEEE 802.3at), LTPoE++ 38.7W, 52.7W, 70W, or 90W maximum power levels and defaults to the LTPoE++ 90W power level if the shunt at JP6 is removed.

The PWRMODE pin configures the PSE's maximum available power. Based on the PD Class result, the PD is allocated power if sufficient power is available. The DC2541A does not support the LTC4279 UltraPWR mode. Refer to the DC2579A for LTC4279 UltraPWR evaluation.

Power Supply Range

The power supply voltage to the DC2541A must be set to meet the requirements of the PSE Type as listed in Table 1. The IEEE standard and LTPoE++ specification have defined voltage ranges for the PSE output. The power supply voltage to a legacy-configured PSE is dependent on the legacy PD and system requirements.

Data In/Data and Power Out

The DC2541A can be set up in a midspan PSE configuration for data and power evaluation. A PD is connected with a Cat5e cable to DATA AND POWER OUT RJ45 connector (J1). Power is injected on to the Ethernet lines through the center taps of the 1000BASE-T Ethernet transformer (T1). A 10BASE-T, 100BASE-T or 1000BASE-T PHY data source is connected with an Ethernet cable to DATA IN RJ45 connector J2 for optional data testing. Data is passed from J2 through to J1 with power.

LED Indicators

The VEE LED1 across the main power supply input indicates the DC2541A is powered. The PORT PWR LED2 is connected from the AGND_P node to the LTC4279 LED open-drain output pin. The LED pin pulls low and turns on LED2 when the port is powered. Each LED has a current limiting resistor in series.

2-Pair vs. 4-Pair

The DC2541A jumpers PORT+ (JP1) and PORT– (JP2) select whether power is applied on only 2, or all 4, of the Ethernet cable pairs. The shunt settings at JP1 and JP2 must match. Table 1 lists the JP1 and JP2 settings as a function of PSE Type. If JP1 and JP2 are configured for 2-PAIR, power is applied with the voltage high side connected to Ethernet pair 1/2 and low side connected to Ethernet pair 3/6. If JP1 and JP2 are configured for 4-PAIR, power is applied in parallel with the 2-PAIR configuration, and with the voltage high side connected to Ethernet pair 4/5 and the low side connected to Ethernet pair 7/8.

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Test Turrets

Test turrets on the DC2541A are provided to connect test measurement equipment across the main supply (AGND and VEE), 2-pair configured output (VPORT+ and VPORT–), and 4-pair configured output (VPORT+, VPORT–, DATA2+ and DATA2–). If using an oscilloscope, connect the scope probe ground leads to a common point or use isolated differential probes for multiple channels with different ground references.

$\overline{\text{RESET}}$

The DC2541A pushbutton switch (SW1) momentarily connects the LTC4279 $\overline{\text{RESET}}$ pin to VEE when pushed and released. When the $\overline{\text{RESET}}$ pin is logic low, the LTC4279 is held inactive with the port off. When the $\overline{\text{RESET}}$ pin is released logic high, the LTC4279 restarts normal operation. An external RC network at the LTC4279 $\overline{\text{RESET}}$ pin on the DC2541A provides a power turn-on delay.

MID

The DC2541A MID jumper (JP3) ties the LTC4279 MID pin high to the AGND_P node or low to VEE. When MID is high, the LTC4279 acts as a midspan device with the Midspan Mode Detection Backoff timer enabled. When MID is low, the LTC4279 acts as an endpoint device with the Midspan Mode Detection Backoff timer disabled. The LTC4279 MID pin is internally pulled down to VEE if the shunt at JP3 is removed.

DUALPD

The DC2541A DUALPD jumper (JP4) ties the LTC4279 DUALPD pin high to the AGND_P node or low to VEE. When DUALPD is high, the LTC4279 detects, classifies and powers dual-signature PDs. Valid dual-signature PDs are present when two Type 2 PD signatures are detected and classified in parallel. PWRMODE must be set to 52.7W or greater. When the LTC4279 DUALPD pin is low, dual-signature PD support is disabled. The LTC4279 DUALPD pin is internally pulled down to VEE if the shunt at JP4 is removed. Warning: Dual-signature detect, class and power on is not IEEE 802.3at compliant.

LEGACY

The DC2541A LEGACY jumper (JP5) ties the LTC4279 LEGACY pin high to the AGND_P node for enabling LEGACY mode, or low to VEE for disabling LEGACY mode. See the LTC4279 data sheet for further details on LEGACY mode. The LTC4279 LEGACY pin is internally pulled down to VEE if the shunt at JP5 is removed. Warning: Legacy detect is, by definition, not IEEE compliant.

Logic Pin Protection

The DC2541A has a 100Ω resistor (R6, R7 and R8) in series from each of the LTC4279 logic pins (MID, DUALPD and LEGACY) and to their respective jumpers (JP3, JP4 and JP5). These resistors provide current limit protection against high voltage transients when moving the shunt position at the jumper. In the end application, if the logic pin is hard tied high to the LTC4279 AGND pin or hard tied low to VEE, this resistor is not required.

Fuse

A fuse is not a requirement of the LTC4279, however, some end applications may require one to meet safety requirements. The DC2541A fuse (F1) provides a suggested fuse location and component value.

Surge Protection

Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components are required at the main supply, at the LTC4279 supply pins, and at the output port. On the DC2541A, a bulk transient voltage suppression diode (D2) and a bulk capacitance (C5) are across the main PoE supply and absorb a majority of the surge energy coming in to the LTC4279. In the end

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application, these should be sized to accommodate system surge level requirements. Across the LTC4279 AGND pin and VEE pin are a local SMAJ58A, 58V TVS (D1) and a 1µF, 100V bypass capacitor (C4) component, both placed close to the LTC4279 pins. An S1B standard rectifier diode (100V, 1A) provides reverse polarity protection at the port output as shown at D3 on the DC2541A.

Kelvin Sense

Proper connection of the port current sense lines is important for current threshold accuracy and IEEE compliance. On the DC2541A, the LTC4279 VSSK pin is connected to a Kelvin sense trace that leads to the sense resistor pad as shown in Figure 2 and is not connected directly to VEE copper areas. Similarly, the LTC4279 SENSE pin is connected to a Kelvin sense trace that leads to the sense resistor pad and is not connected in the power path between the sense resistor and the MOSFET. The LTC4279 VEE pins and the sense resistor VEE pad connect to the VEE copper areas.

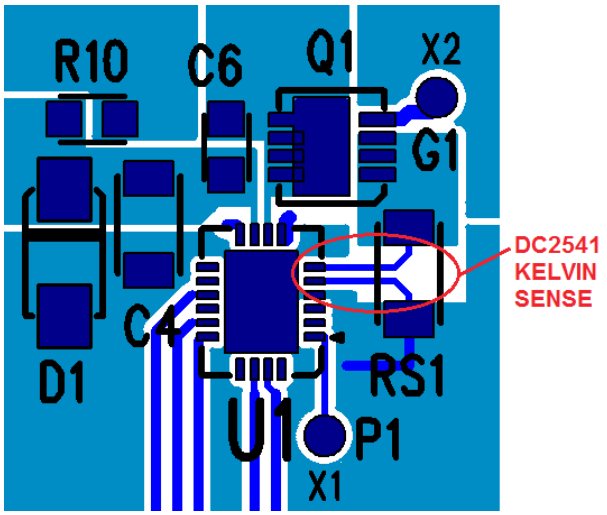


Figure 2. DC2541A Kelvin Sense

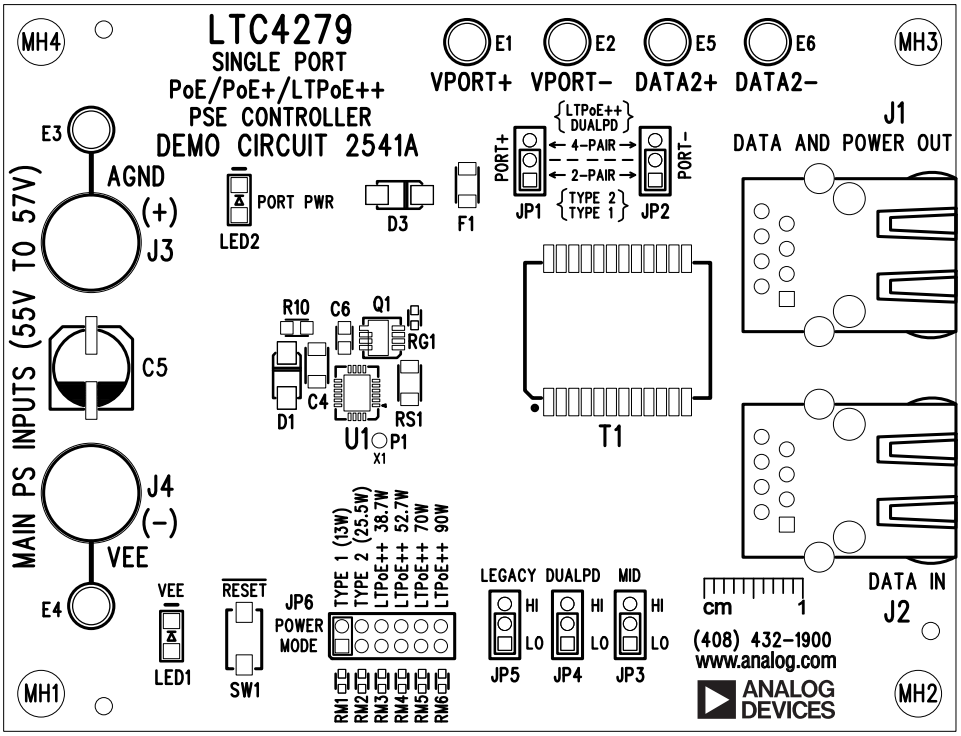
Recommended Component Selection

The DC2541A power path components (RS1, Q1, and T1) are chosen to accommodate all power levels up to LTPoE++ 90W. In the end application, these components can be optimized for the respective power level as listed in Table 2.

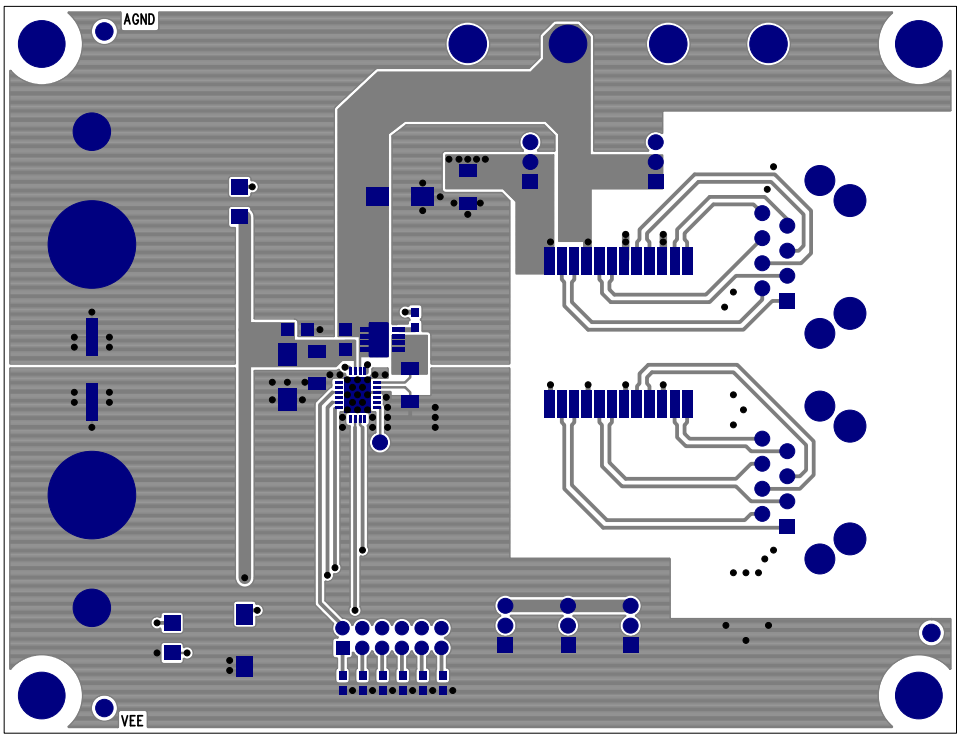
Table 2. Recommended Power Path and Setting Components for the Various Power Levels

Power Level	Type 1 (13W)	Type 2 (25.5W)	LTPoE++ (38.7W)	LTPoE++ (52.7W)	LTPoE++ (70W)	LTPoE++ (90W)
Power Mode Resistor (R_{PM})	2.37k, 1%	3.32k, 1%	4.64k, 1%	5.90k, 1%	7.87k, 1%	10.0k, 1%
Sense Resistor (RS1)	0.1Ω, 1%, 1/10W, ±200ppm/°C	0.1Ω, 1%, 1/10W, ±200ppm/°C	0.1Ω, 1%, 1/4W, ±200ppm/°C	0.1Ω, 1%, 1/2W, ±200ppm/°C	0.1Ω, 1%, 1/2W, ±200ppm/°C	0.1Ω, 1%, 1W, ±200ppm/°C
Ethernet Transformer (T1)	Würth 749023015	Würth 749022017	Würth 749022016, Coilcraft ETH1-460L	Würth 749022016, Coilcraft ETH1-460L	Würth 749022016, Coilcraft ETH1-460L	Würth 749022016, Coilcraft ETH1-460L
MOSFET (Q1)	NXP PSMN075-100MSE	NXP PSMN075-100MSE	NXP PSMN040-100MSE	NXP PSMN040-100MSE	NXP PSMN040-100MSE	NXP PSMN040-100MSE

PCB LAYOUT



Top Assembly



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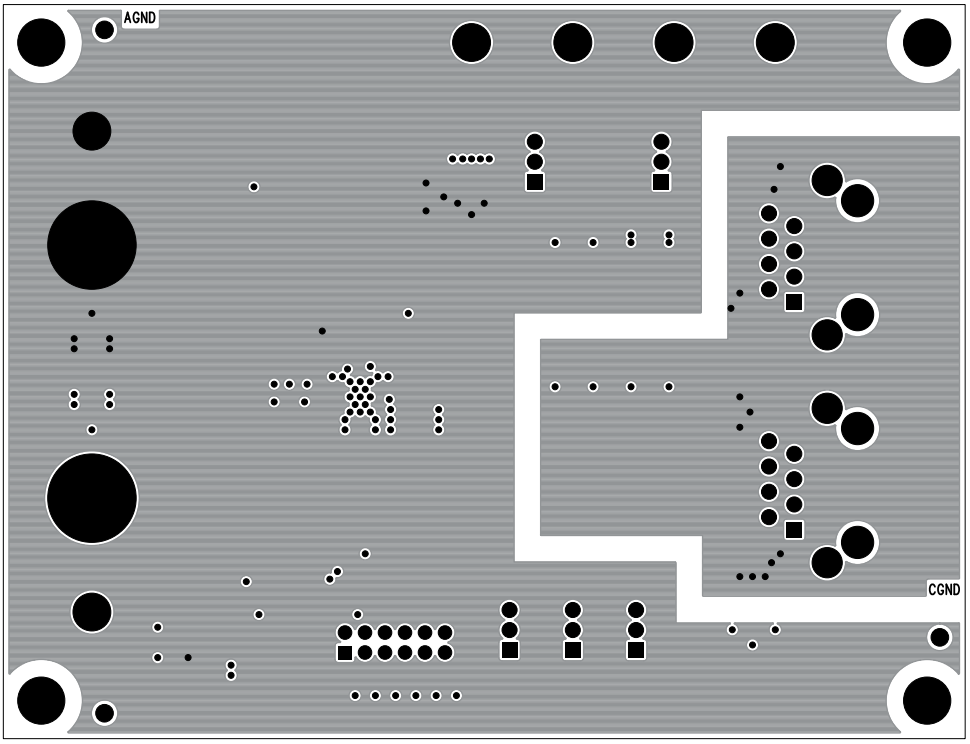

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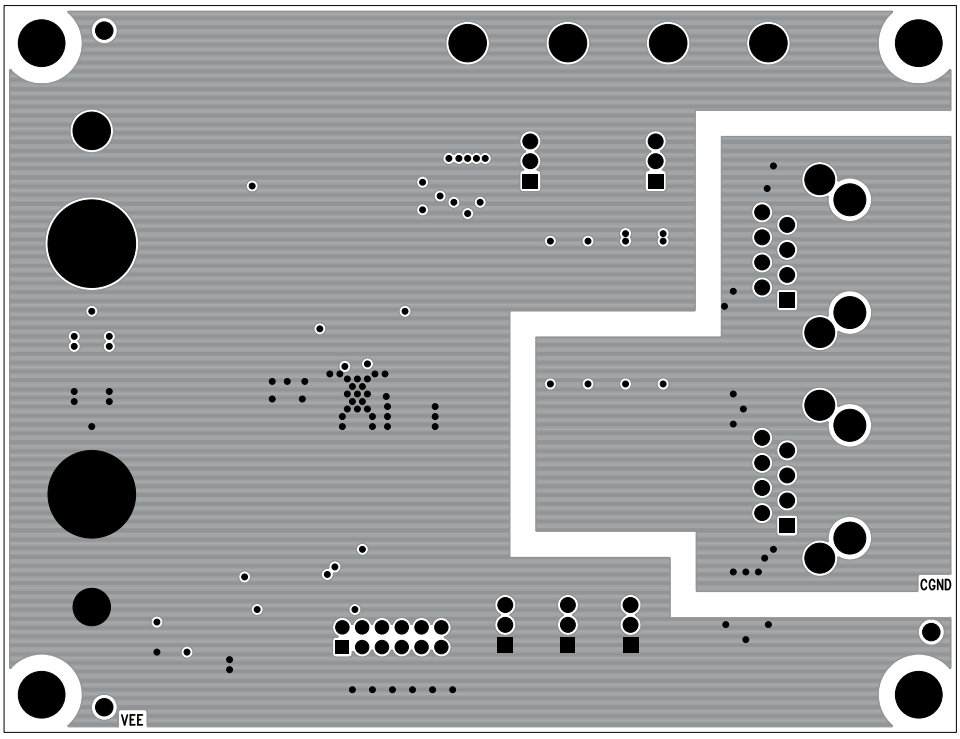

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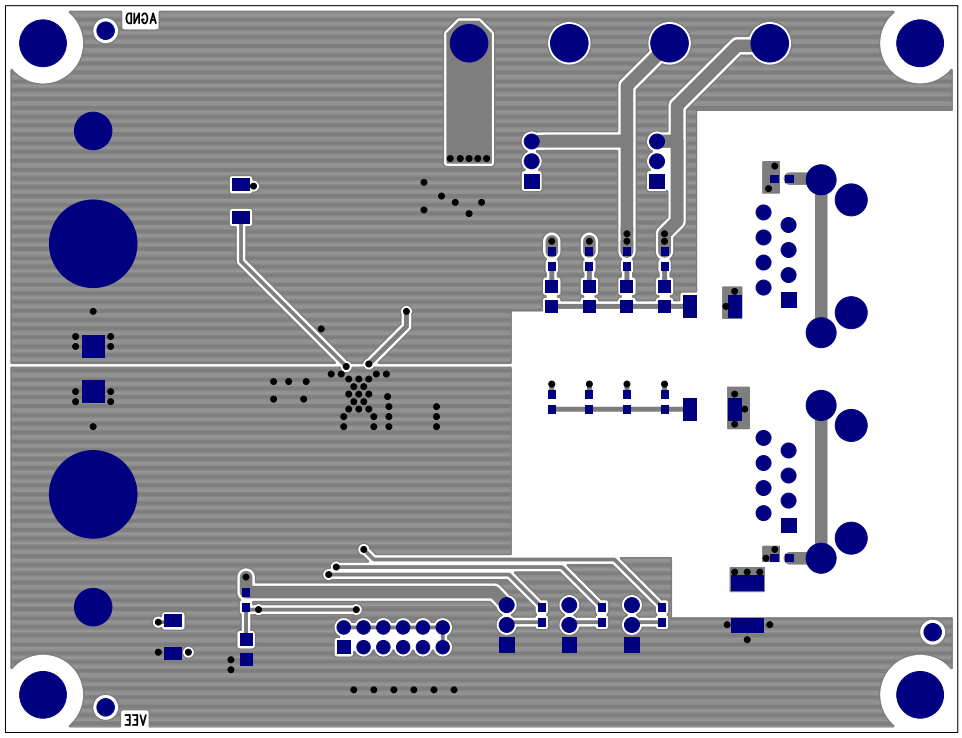

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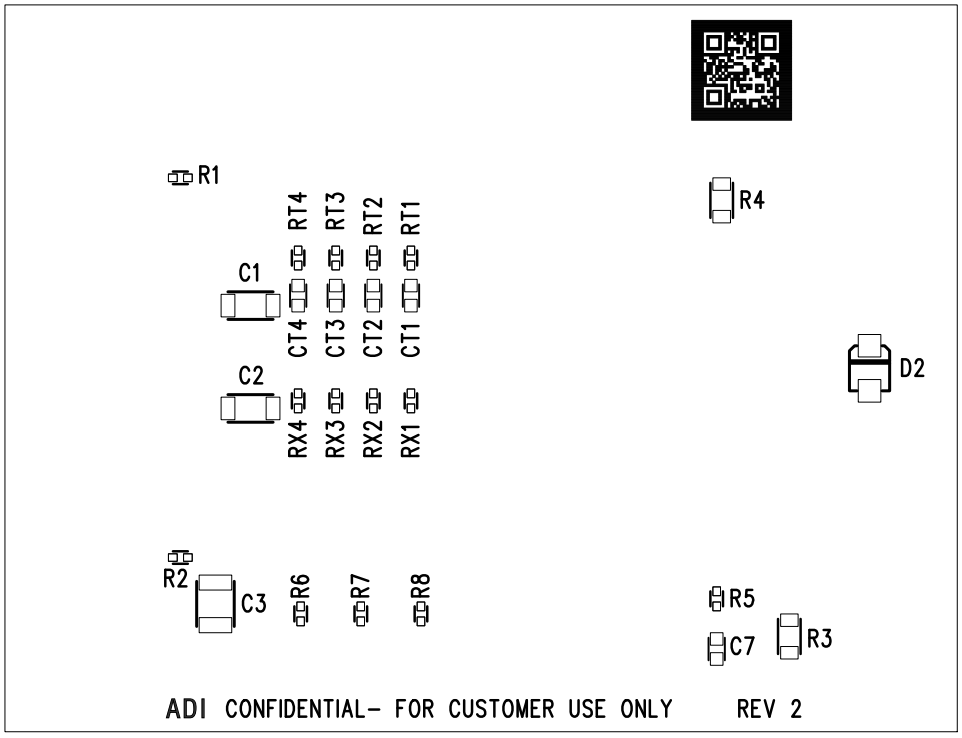
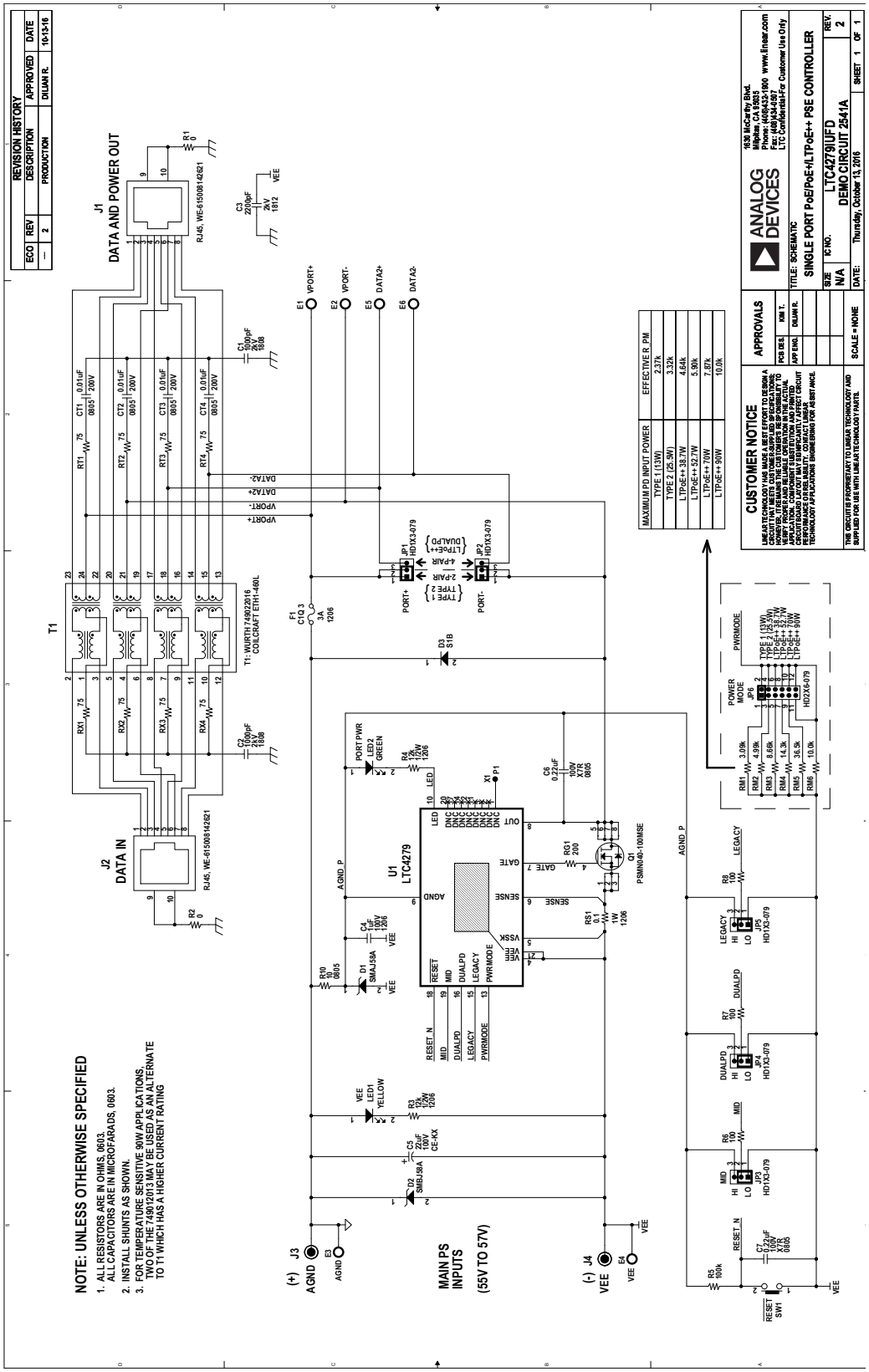


Bottom Assembly

SCHEMATIC DIAGRAM



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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