LTC4279
Single Port UltraPWR PSE Controller

DESCRIPTION

Demonstration Circuit 2579A features the LTC®4279, an autonomous single port power sourcing equipment (PSE) controller, configured in its UltraPWR mode. UltraPWR mode aggressively turns on and powers custom high power PDs requiring high inrush and/or operational currents.

The DC2579A requires a single power supply and provides power on all four Ethernet pairs to valid detected PDs. Jumper selections are provided on the DC2579A for setting the LTC4279 LEGACY pin, DUALPD pin and MID pin. A pushbutton switch resets the LTC4279. LEDs indicate main supply power and output power are up. Data-In RJ45 connects to a PHY data source and Data-and-Power-Out RJ45 connects to a custom high power PD.

Design files for this circuit board are available at http://www.linear.com/demo/DC2579A

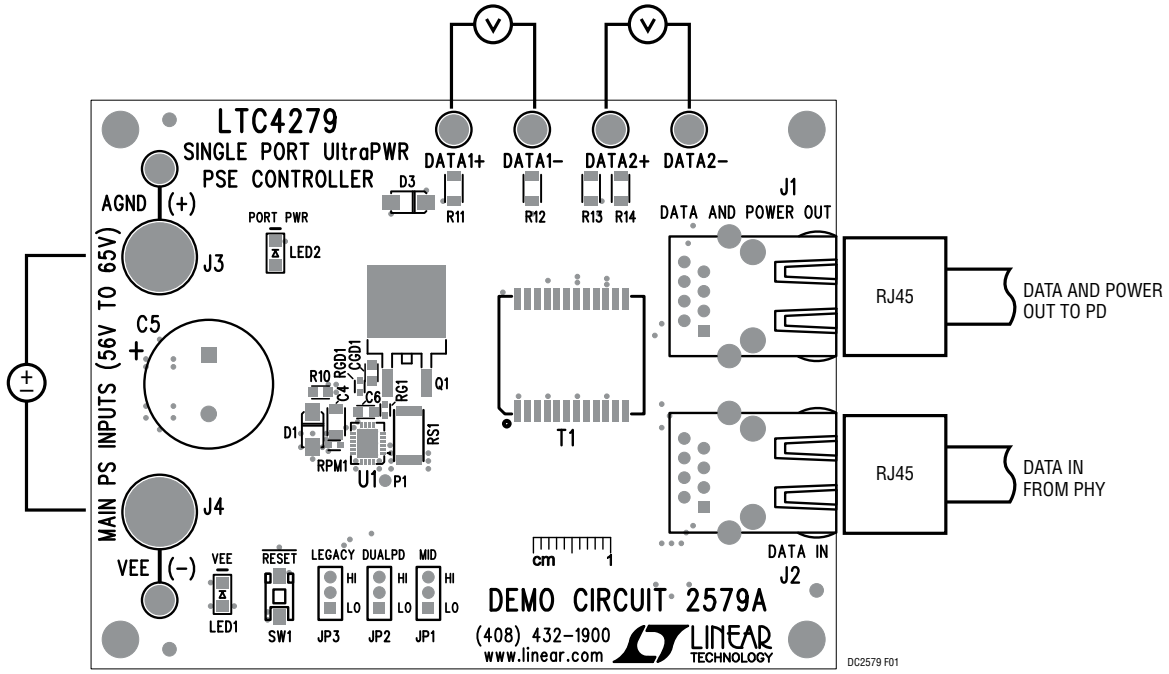


Figure 1. DC2579A Connections

QUICK START PROCEDURE

Demonstration circuit 2579A is easy to setup for evaluating the performance of the LTC4279. Refer to Figure 1 for proper measurement equipment setup, Table 1 for supply settings, and follow the procedure below.

1. Select HI at LEGACY jumper JP3 to enable LEGACY mode or select LO to disable LEGACY mode.
2. Select HI at DUALPD jumper JP2 to enable DUALPD mode or select LO to disable DUALPD mode.
3. Select HI at MID jumper JP1 to enable midspan mode or select LO to disable midspan mode.
4. Connect a power supply with the positive to AGND (J3) and negative to VEE (J4).
5. Ramp up the supply to within the range specified in Table 1 for the configured mode. VEE LED1 will turn on when the board is powered.

Table 1. Power Supply Range

SELV Required	MAIN PS Range
Yes	55V – 60V
No	55V – 65V

6. Connect test measurement probes across DATA1+ to DATA1–, and DATA2+ to DATA2– for port output measurements.
7. Connect a custom high power PD with a Cat5E Ethernet cable to RJ45 connector J1. PORT PWR LED2 will turn on if the port power is on.
8. Connect a 10BASE-T, 100BASE-T or 1000BASE-T PHY data source with an Ethernet cable to J2 for data testing (optional).

Note: Any change in the jumper selections while power is on will require a power cycle or pushbutton reset for the change to take effect.

OPERATION

Power Control

The primary function of the LTC4279 is to control the delivery of power to the PSE port. It does this by controlling the gate drive voltage of an external power MOSFET (Q1) while monitoring the current via an external sense resistor (RS1) and the output voltage at the OUT pin. This circuitry serves to couple the raw VEE input supply to the port in a controlled manner that satisfies the PD's power needs while minimizing both power dissipation in the MOSFET and disturbances on the VEE backplane.

UltraPWR Mode

The LTC4279 is configured for UltraPWR mode by a 13.0k resistor (RPM1) from the PWRMODE pin to VEE. Unlike LTPoE++ and the IEEE 802.3at standard, UltraPWR is not a system defined standard. A PSE in UltraPWR mode issues up to three class events and powers valid detected PDs with maximum deliverable power, as determined by the PSE output voltage, V_{PSE}. Warning: UltraPWR mode is not IEEE compliant.

Certain existing very high power PDs proprietary to the PD manufactures benefit from the UltraPWR mode of the LT4279. The LTC4279 in UltraPWR mode simply provides very high power to these proprietary PDs.

Figure 12 (UltraPWR Power vs V_{PSE}) in the LTC4279 data sheet shows PSE source power (at the PSE RJ45 jack) and PD delivered power (at the PD RJ45 jack) vs V_{PSE}. The gray shaded area above 60V shows voltages exceeding SELV maximum; systems exceeding SELV maximum voltage may incur additional regulatory hurdles.

Data In/Data And Power Out

The DC2579A can be set up in a midspan PSE configuration for data and power evaluation. A PD is connected with a Cat5e cable to DATA AND POWER OUT RJ45 connector (J1). Power is injected on to the Ethernet lines through the center taps of the 1000BASE-T Ethernet transformer (T1). A 10BASE-T, 100BASE-T or 1000BASE-T PHY data source is connected with an Ethernet cable to DATA IN RJ45 connector J2 for optional data testing. Data is passed from J2 to J1 along with the injected power.

OPERATION

LED Indicators

The VEE LED1 across the main power supply input indicates the DC2579A is powered. The PORT PWR LED2 is connected from the AGND_P node to the LTC4279 LED open-drain output pin. The LED pin pulls low and turns on LED2 when the port is powered. Each LED has a current limiting resistor in series.

Test Points

Test turrets on the DC2579A are provided to connect test measurement equipment across the main supply (AGND and VEE), and 4-pair configured output (DATA1+ and DATA1–, DATA2+ and DATA2–). If using an oscilloscope, connect the scope probe ground leads to a common point or use isolated differential probes for multiple channels with different ground references.

RESET

The DC2579A pushbutton switch (SW1) momentarily connects the LTC4279 RESET pin to VEE when pushed and released. When the RESET pin is logic low, the LTC4279 is held inactive with the port off. When the RESET pin is released logic high, the LTC4279 restarts normal operation. An external RC network at the LTC4279 RESET pin on the DC2579A provides a power turn-on delay.

MID

The DC2579A MID jumper (JP1) ties the LTC4279 MID pin high to the AGND_P node or low to VEE. When MID is high, the LTC4279 acts as a midspan device with the Midspan Mode Detection Backoff timer enabled. When MID is low, the LTC4279 acts as an endpoint device with the Midspan Mode Detection Backoff timer disabled. The LTC4279 MID pin is internally pulled down to VEE if the shunt at JP1 is removed.

DUALPD

The DC2579A DUALPD jumper (JP2) ties the LTC4279 DUALPD pin high to the AGND_P node or low to VEE. When DUALPD is high, the LTC4279 detects, classifies and powers dual-signature PDs. Valid dual-signature PDs are present when two Type 2 PD signatures are detected and classified in parallel. When the LTC4279 DUALPD pin is low, dual-signature PD support is disabled. The LTC4279 DUALPD pin is internally pulled down to VEE if the shunt at JP2 is removed. Warning: Dual-signature detect, class and power on is not IEEE compliant.

LEGACY

The DC2579A LEGACY jumper (JP3) ties the LTC4279 LEGACY pin high to the AGND_P node for enabling LEGACY mode, or low to VEE for disabling LEGACY mode. See the LTC4279 data sheet for further details on LEGACY mode. The LTC4279 LEGACY pin is internally pulled down to VEE if the shunt at JP3 is removed. Warning: Legacy detect is, by definition, not IEEE compliant.

Logic Pin Protection

The DC2579A has a 100Ω resistor (R6, R7 and R8) in series from each of the LTC4279 logic pins (MID, DUALPD and LEGACY) and to their respective jumpers (JP1, JP2 and JP3). These resistors provide current limit protection against high voltage transients when moving the shunt position at the jumper. In the end application, if the logic pin is hard tied high to the LTC4279 AGND pin or hard tied low to VEE, this resistor is not required.

Surge Protection

Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components are required at the main supply, at the LTC4279 supply pins, and at the output port. On the DC2579A, a bulk transient voltage suppression diode (D2) and a bulk capacitance (C5) are across the main PoE supply and absorb a majority of the surge energy coming in to the LTC4279. In the end application, these should be sized to accommodate system surge energy requirements. The LTC4279 requires a 10Ω, 0805 resistor (R10) in series from supply AGND to the LTC4279 AGND pin for added surge protection. Across the LTC4279 AGND pin and VEE pin are a local SMAJ58A, 58V TVS (D1) and a 1µF, 100V bypass capacitor (C4) component, both placed close to the LTC4279 pins. An S1B standard rectifier diode (100V, 1A) provides reverse polarity protection at the port output as shown at D3 on the DC2579A.

OPERATION

MOSFET and Gate RC Network

The DC279A external Hot Swap MOSFET and gate RC network have been selected to meet loop stability and harsh current foldback conditions. Using different component values is not recommended.

KELVIN Sense

Proper connection of the port current sense lines is important for current threshold accuracy and IEEE compliance. On the DC2579A, the LTC4279 VSSK pin is connected to a Kelvin sense trace that leads to the sense resistor pad and is not connected directly to VEE copper areas. Similarly, the LTC4279 SENSE pin is connected to a Kelvin sense trace that leads to the sense resistor pad and is not connected in the power path between the sense resistor and the MOSFET. Figure 2 highlights in red these two Kelvin traces from the LTC4279 (U1) to the sense resistor (RS1). The LTC4279 VEE pins and the sense resistor VEE pad connect to the VEE copper areas.

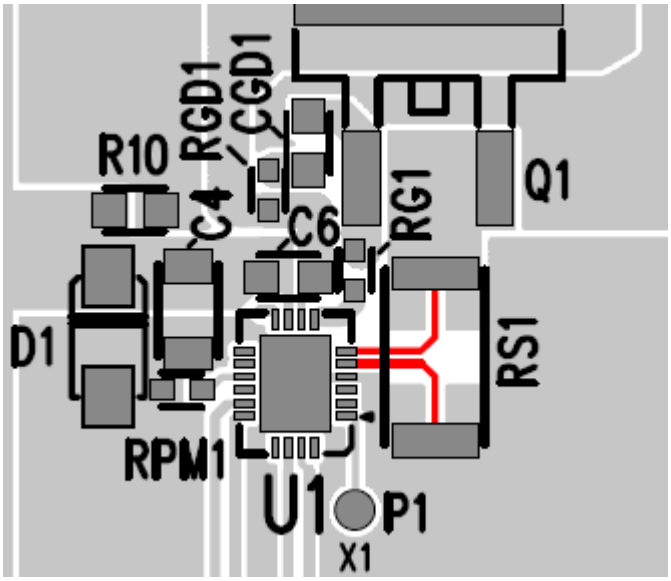
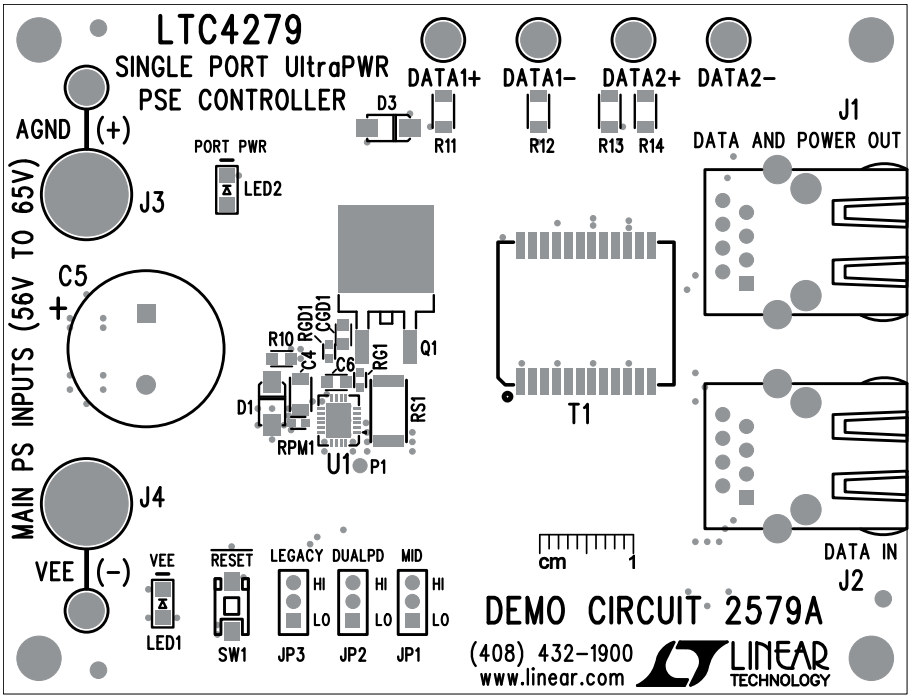
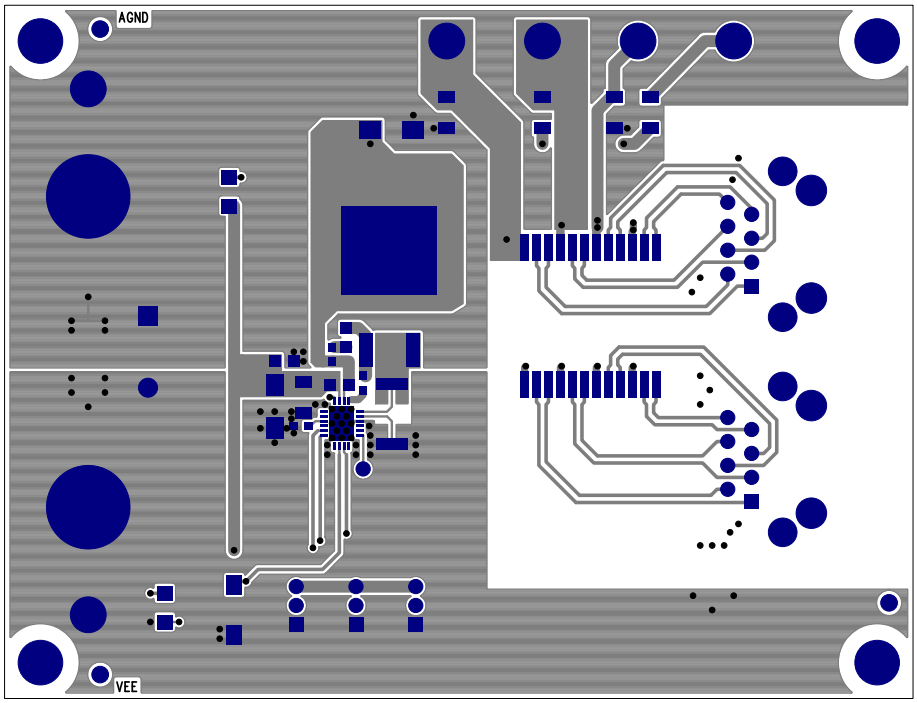


Figure 2. DC2579 Kelvin Sense

PCB LAYOUT

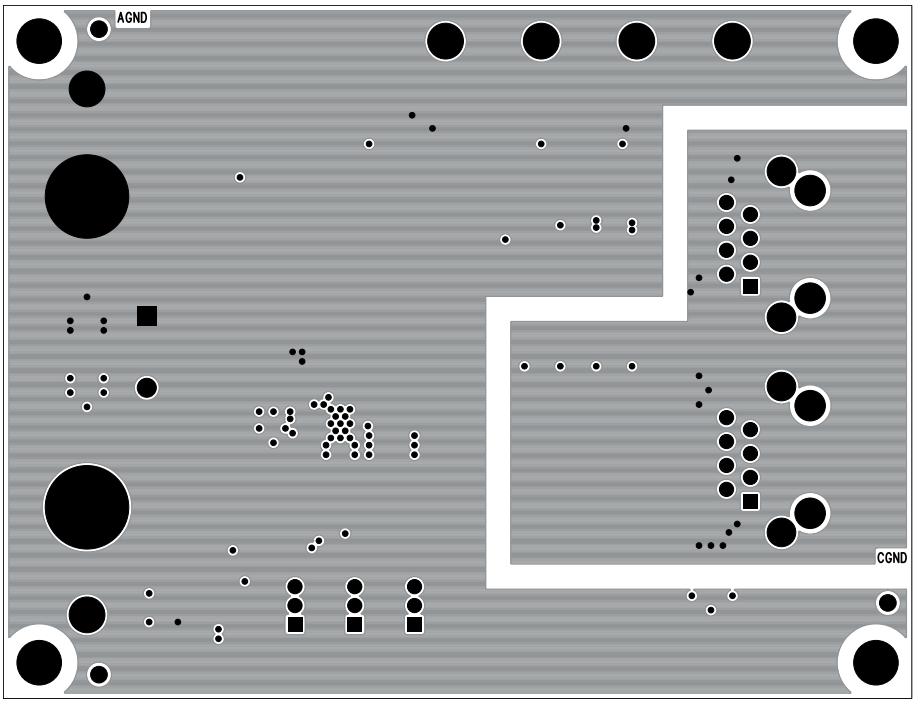


Top Silkscreen

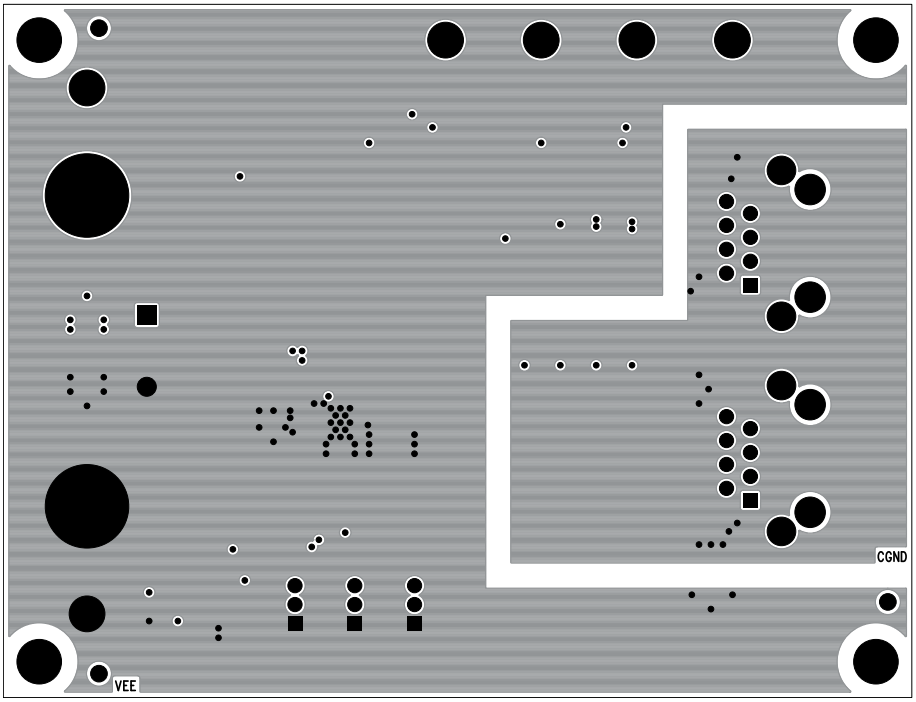


Layer 1—Top Layer

PCB LAYOUT

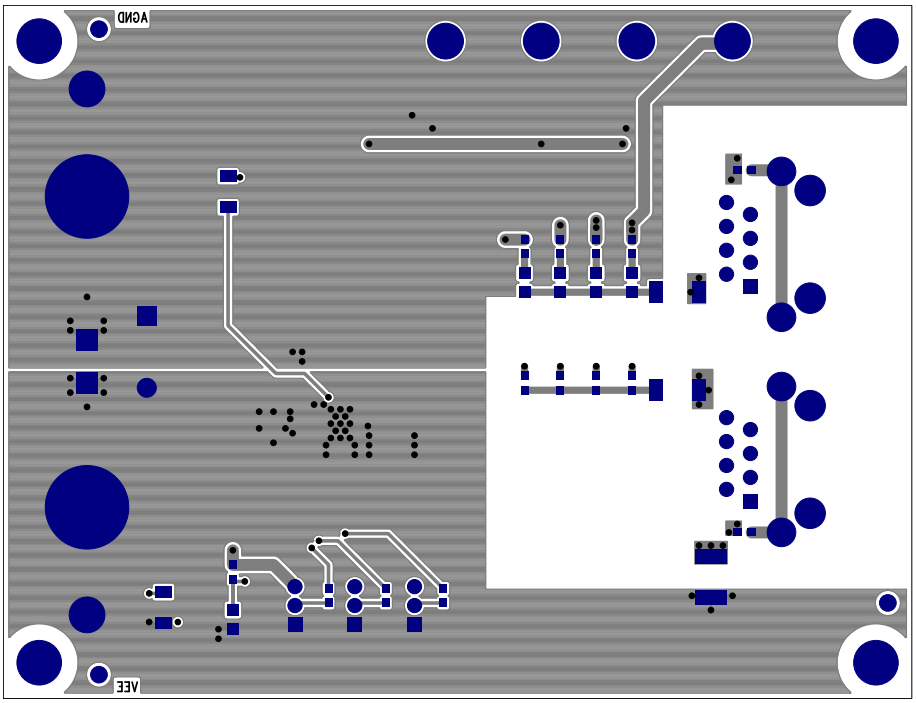


Layer 2—AGND + CGND Plane

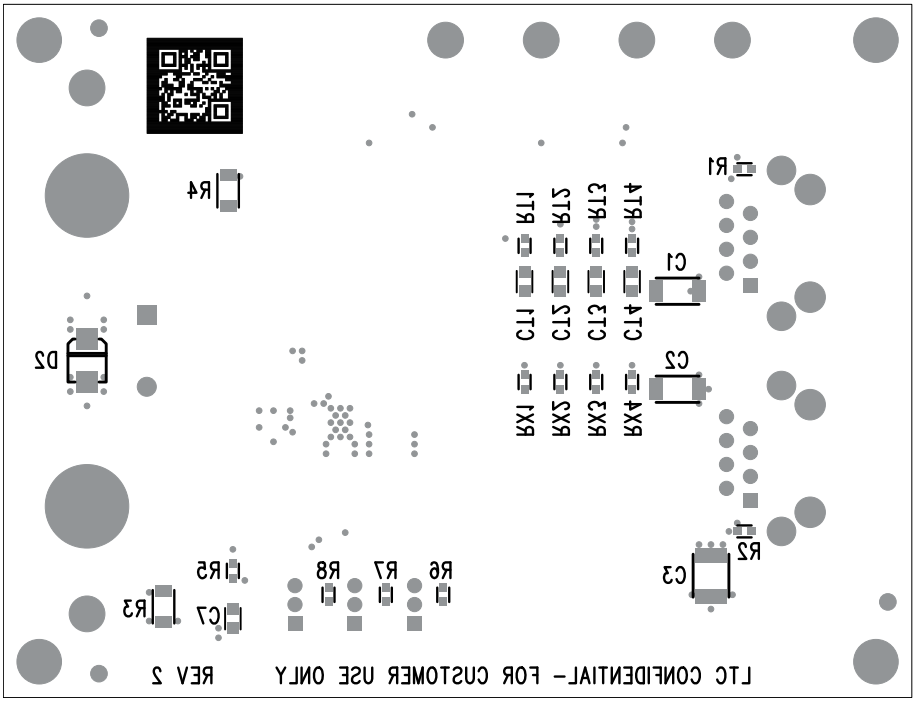


Layer 3—VEE + CGND Plane

PCB LAYOUT



Layer 4—Bottom Layer

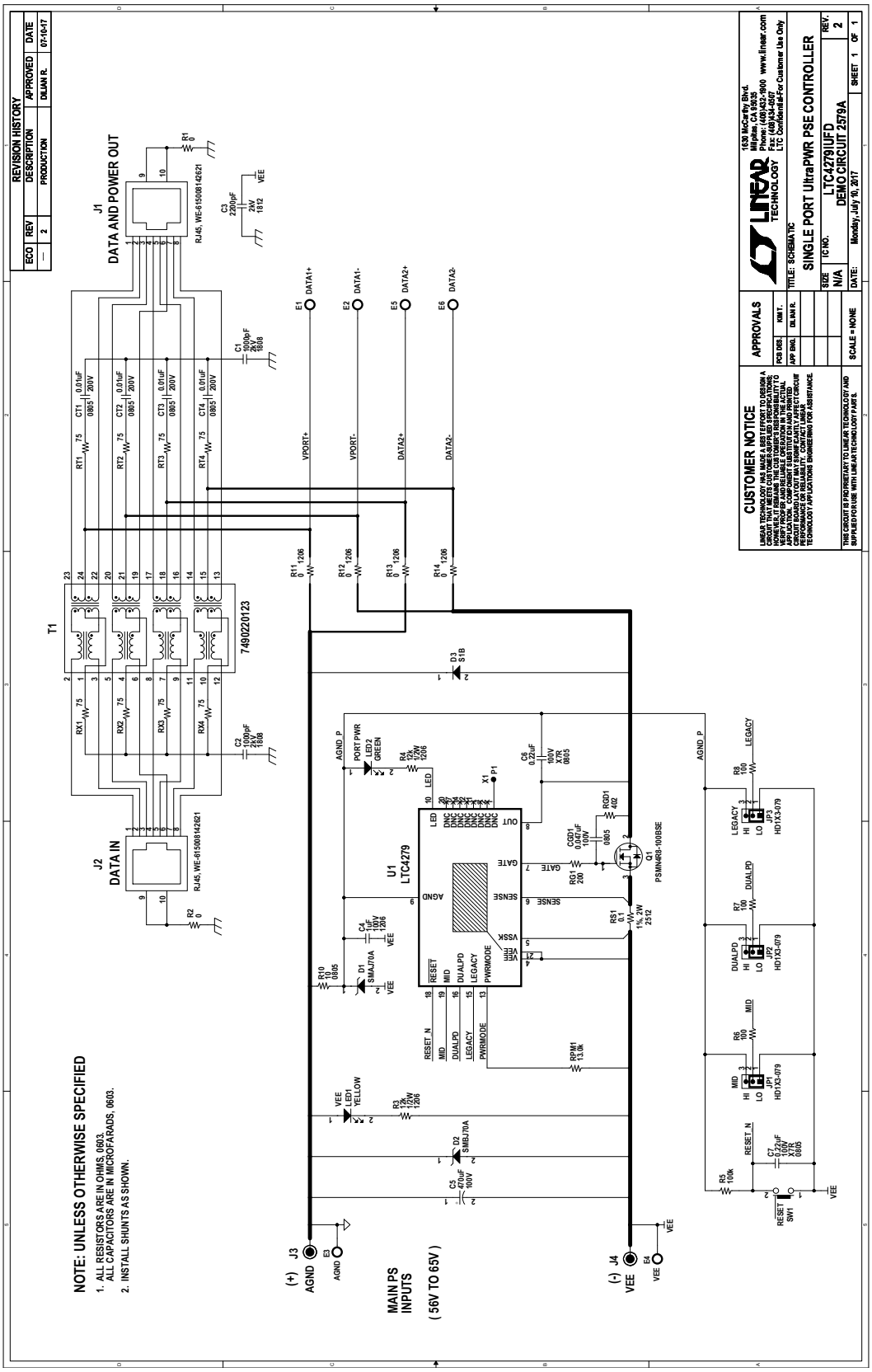


Bottom Silkscreen

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CGD1	CAP., 0.047µF, X7R, 100V, 20%, 0805	TDK, C2012X7R2A473M125AA
2	4	CT1, CT2, CT3, CT4	CAP, 0.01µF, X7R, 200V, 10%, 0805	MURATA, GRM21BR72D103KW03L
3	2	C1, C2	CAP, 1000pF, X7R, 2kV, 10%, 1808	MURATA, GR442QR73D102KW01L
4	1	C3	CAP, 2200pF, X7R, 2kV, 10%, 1812	MURATA, GR443QR73D222KW01L
5	1	C4	CAP, 1µF, X7R, 100V, 10%, 1206	MURATA, GRM31CR72A105KA01L
6	1	C5	CAP., ELECT., 470µF 100V, CAP-PANA-NHG-16X25	PANASONIC, ECA2AHG471
7	2	C6, C7	CAP., 0.22µF, X7R, 100V, 10%, 0805	MURATA, GRM21AR72A224KAC5L
8	1	D1	DIODE, TVS, 400W, 70V, SMA-DIODE	DIODES INC., SMAJ70A-13-F
9	1	D2	DIODE, TVS, 600W, 70V, SMB-DIODE	DIODES INC., SMBJ70A-13-F
10	1	D3	DIODE, RECTIFIER, LOW LEAKAGE, SMA-DIODE	FAIRCHILD SEMI., S1B
11	6	E1-E6	TEST POINT, TURRET, 0.094", MTG. HOLE	MILL-MAX, 2501-2-00-80-00-00-07-0
12	3	JP1, JP2, JP3	CONN., HEADER, MALE, 1X3, 2mm, THT	WURTH ELEKTRONIK 62000311121
13	2	J1, J2	CONN, RJ45, RJ45-WE-615008142621	WURTH ELEKTRONIK, 615008142621
14	2	J3, J4	CONN, JACK, BANANA	KEYSTONE, 575-4
15	1	LED1	LED, YELLOW, LED-ROHM-SML-01	ROHM, SML-012Y8TT86
16	1	LED2	LED, GREEN, LED-ROHM-SML-01	ROHM, SML-012P8TT86
17	1	Q1	MOSFET, N-CH, 100V 4.8mΩ, D2PAK	NXP, PSMN4R8-100BSEJ
18	1	RGD1	RES., 402Ω, 1%, 1/10W, 0603	VISHAY, CRCW0603402RFKEA
19	1	RG1	RES., 200Ω, 1%, 1/10W, 0603	VISHAY, CRCW0603200RFKEA
20	1	RPM1	RES., 13.0kΩ, 1%, 1/10W, 0603	VISHAY, CRCW060313K0FKEA
21	1	RS1	RES., SENSE, 0.1Ω, 1%, 2W, 2512	STACKPOLE, CSRN2512FTR100
22	8	RX1-RX4, RT1-RT4	RES., 75Ω, 5%, 1/10W, 0603	VISHAY, CRCW060375R0JNEA
23	2	R1, R2	RES., 0Ω, 1/10W, 0603	VISHAY, CRCW06030000Z0EA
24	2	R3, R4	RES., 12kΩ, 5%, 1/2W, 1206	VISHAY, CRCW120612K0JNEAHP
25	1	R5	RES., 100kΩ, 5%, 1/10W, 0603	VISHAY, CRCW0603100KJNEA
26	3	R6, R7, R8	RES., 100Ω, 5%, 1/10W, 0603	VISHAY, CRCW0603100RJNEA
27	1	R10	RES., 10Ω, 5%, 1/10W, 0805	VISHAY, CRCW080510R0JNEA
28	4	R11-R14	RES., 0Ω, 1/4W, 1206	VISHAY, CRCW12060000Z0EA
29	1	SW1	SWITCH, LIGHT TOUCH, SW-WE-434123050816	WURTH ELEKTRONIK, 434123050816
30	1	T1	XFMR, PoE PLUS ETHERNET MAGNETICS, TRANS-WE-7490220123	WURTH ELEKTRONIK, 7490220123
31	1	U1	IC, QFN20UFD-4X5	LINEAR TECH., LTC4279IUFD#PBF
32	3	SHUNTS FOR JP1-JP3 PINS 1 AND 2	SHUNT, 2mm	WURTH ELEKTRONIK, 60800213421
33	4	MH1-MH4	STAND-OFF, NYLON, 0.5"	WURTH ELEKTRONIK, 702935000
34	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT #2579A
35	2		STENCILS FOR BOTH SIDES	STENCIL DC2579A-2

SCHEMATIC DIAGRAM



dc2579af

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