5V 3A Output, 42V Input USB Charger with Cable Drop Compensation and Dataline Protection

FEATURES

- **Wide V_{IN} Range Up to 42V**
- **Programmable Cable Drop Compensation Provides Accurate 5V Regulation to Remote USB Sockets**
- **High Speed USB 2.0 Compliant Dataline Switches**
- **Selectable Charger Profiles Including Major Vendors' and USB BC 1.2 Profiles**
- **Silent Switcher®2 Technology and Selectable Spread-Spectrum Modulation Provide Ultralow EMI**
- Robust Dataline Protection
  - Tolerant of Short Condition Up to 20V
  - ESD Protected Up to IEC61000-4-2 8kV Contact Discharge and 15kV Air Discharge
- Available Status and Fault Output Pins
- Programmable and Synchronizable Switching Frequency 300kHz to 3MHz
- Selectable Forced Continuous or Pulse-Skipping Modes
- Small 4mm × 6mm × 0.94mm LQFN Package with 0.75mm Spacing from V_{IN} to GND Pins
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive USB
- Industrial USB

DESCRIPTION

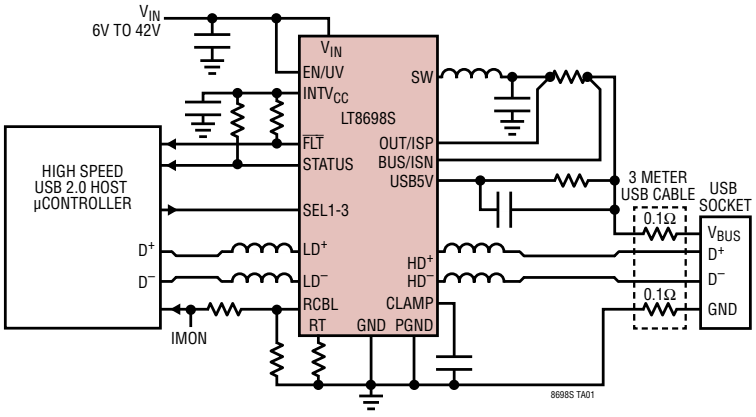
The LT®8698S is a compact, high efficiency, synchronous monolithic step-down switching regulator designed to power the 5V USB V_{BUS} rail with up to 3A from an input voltage as high as 42V. Programmable cable drop compensation maintains accurate 5V V_{BUS} regulation even for USB sockets separated from the LT8698S by a long cable such as an automobile wiring harness. Silent Switcher Technology and selectable spread-spectrum modulation provide ultralow EMI/EMC.

The LT8698S supports a wide variety of portable device charger profiles including USB BC 1.2 CDP, DCP, and SDP as well as common proprietary profiles. Integrated V_{BUS} reset and V_{BUS} regulator disable functions support USB OTG functionality.

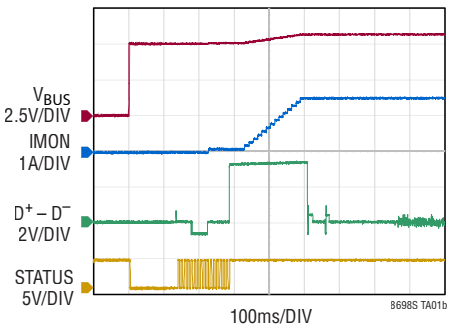
The LT8698S's robust high speed USB 2.0 data line switches protect the upstream USB host µController from short-circuit conditions up to 20V and ESD events up to IEC61000-4-2 8kV contact discharge and 15kV air discharge levels. Further V_{BUS} monitor and fault protection features eliminate the need for a USB power switch. The LT8698S includes two parallel 10nF capacitors from V_{IN} to PGND for improved EMI/EMC performance. The LT8698S-1 does not include these capacitors.

TYPICAL APPLICATION

Automotive Charger with High Speed Dataline Protection and Cable Drop Compensation



USB BC1.2 CDP Session



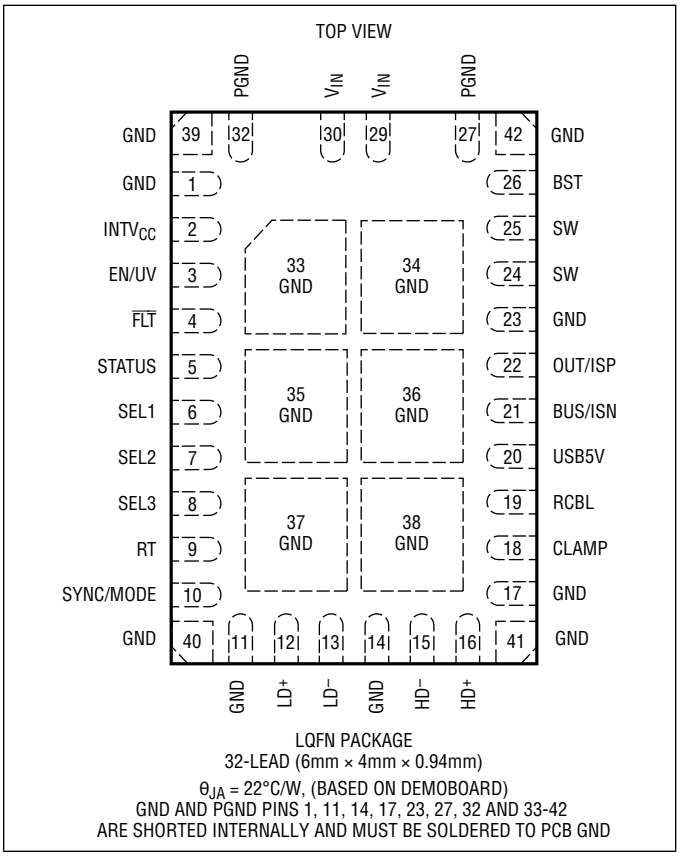
Rev. B

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UV, OUT/ISP, BUS/ISN, USB5V 42V
HD^+, HD^-, CLAMP.....20V
SYNC/MODE, $\overline{FLT}$, STATUS,
SEL1, SEL2, SEL3, LD^+, LD^- 6V
RCBL, RT 2V
Operating Junction Temperature Range (Note 2)
LT8698SE ..... –40°C to 125°C
LT8698SJ ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Peak Package Body Reflow Temperature ..... 260°C

PIN CONFIGURATION



LQFN PACKAGE
32-LEAD (6mm × 4mm × 0.94mm)
θ_{JA} = 22°C/W, (BASED ON DEMOBOARD)
GND AND PGND PINS 1, 11, 14, 17, 23, 27, 32 AND 33-42
ARE SHORTED INTERNALLY AND MUST BE SOLDERED TO PCB GND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
			DEVICE	FINISH CODE			
LT8698SEV#PBF	LT8698SEV#TRPBF	Au (RoHS)	8698V	e4	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C
LT8698SJV#PBF	LT8698SJV#TRPBF						–40°C to 150°C
LT8698SEV-1#PBF	LT8698SEV-1#TRPBF		8698S1				–40°C to 125°C
LT8698SJV-1#PBF	LT8698SJV-1#TRPBF						–40°C to 150°C
AUTOMOTIVE PRODUCTS**							
LT8698SEV#WPBF	LT8698SEV#WTRPBF	Au (RoHS)	8698V	e4	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C
LT8698SJV#WPBF	LT8698SJV#WTRPBF						–40°C to 150°C
LT8698SEV-1#WPBF	LT8698SEV-1#WTRPBF		8698S1				–40°C to 125°C
LT8698SJV-1#WPBF	LT8698SJV-1#WTRPBF						–40°C to 150°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended PCB Assembly and Manufacturing Procedures.
- Package and Tray Drawings

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	V_{IN} Shutdown Current	$V_{EN/UV}$ = 0.25V, V_{IN} = 12V			0.1	1	µA
	V_{IN} Current in Regulation	I_{LOAD} = 0A, $V_{SYNC/MODE}$ = 0V, V_{IN} = 12V (Note 4) I_{LOAD} = 0A, $V_{SYNC/MODE}$ = Open, V_{IN} = 12V (Note 4)	● ●		2.5 23	4 36	mA mA
V_{CHG}	Regulator Output Voltage at BUS/ISN	I_{LOAD} = 0A, R_{CBL} = 3.57k (Note 4) I_{LOAD} = 2.4A, R_{CBL} = 3.57k (Note 4) I_{LOAD} = 0A, V_{USB5V} = 0V (Note 4)	● ● ●	4.925 5.52 5.93	5.00 5.61 6.05	5.063 5.680 6.13	V V V
	USB5V Voltage	V_{IN} = 5V to 42V	●	4.915	4.99	5.053	V
	Upper $\overline{FLT}$ Threshold Offset	Percentage of V_{USB5V}, V_{USB5V} Falling	●	4	7	10	%
	Lower $\overline{FLT}$ Threshold Offset	Percentage of V_{USB5V}, V_{USB5V} Rising	●	4	7	10	%
	$\overline{FLT}$ Threshold Hysteresis	Percentage of V_{USB5V}			3		%
I_{CDP}	Regulator Output Current Limit	$V_{BUS/ISN}$ = 4.5V, R_{SEN} = 10mΩ		2.55	2.65	2.75	A
	Latch-On Time in Current Limit	$V_{BUS/ISN}$ = 0.2V		3.4	4.2	5	ms
T_{SHTDWN_REC}	Latch-Off Time in Current Limit	$V_{BUS/ISN}$ = 0.2V		48	59	70	ms
	Regulator Output Current STATUS Threshold	$I_{BUS/ISN}$ Falling, R_{SEN} = 10mΩ		20	100	180	mA
	Regulator Output Current STATUS Threshold Hysteresis	R_{SEN} = 10mΩ			20		mA
	Regulator Output Sink Current	$V_{BUS/ISN}$ = 6.3V (Note 4)		–2.9	–2.3	–1.7	A
	R_{CBL} Monitor Voltage	I_{LOAD} = 0A, R_{SEN} = 10mΩ I_{LOAD} = 2.4A, R_{SEN} = 10mΩ	● ●	0 1.05	2 1.10	50 1.15	mV V
	Oscillator Frequency	R_T = 9.09k R_T = 66.5k R_T = 5.76k	● ● ●	1.8 255 2.7	2 300 3	2.2 345 3.3	MHz kHz MHz
	SYNC/MODE Low Threshold for Pulse-Skip Operation	$V_{SYNC/MODE}$ Rising	●	0.3	0.7	1.1	V
	SYNC/MODE Input High for Synced Operation		●	1.5			V
	SYNC/MODE Input Low for Synced Operation		●			0.4	V
	SYNC/MODE High Threshold for Spread Spectrum Operation	$V_{SYNC/MODE}$ Rising	●	2.7	3.2	3.7	V
	SYNC/MODE Pull Up Current for Forced Continuous Operation	$V_{SYNC/MODE}$ = 2V	●	2	4.25	6.5	µA
	Top Switch Max Current Limit			5	6	7	A
	Top Switch On Resistance	I_{SW} = 1A			75		mΩ
	Bottom Switch On Resistance	I_{SW} = 1A			75		mΩ
	SW Leakage Current			–1	0	1	µA
	EN/UV Threshold	$V_{EN/UV}$ Falling	●	1.17	1.31	1.45	V
	EN/UV Threshold Hysteresis				150		mV
	EN/UV Current	$V_{EN/UV}$ = 2V		–100		100	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	$\overline{FLT}$ Pull Down Resistance	$V_{\overline{FLT}}$ = 0.1V	●		150	300	Ω
	$\overline{FLT}$ Leakage	$V_{\overline{FLT}}$ = 4V				1	µA
	STATUS Pull Down Resistance	V_{STATUS} = 0.1V	●		150	300	Ω
	STATUS Leakage	V_{STATUS} = 4V				1	µA
	SEL1-3 Low Threshold	V_{SEL} Rising	●	0.48	0.58	0.68	V
	SEL1-3 Low Threshold Hysteresis				35		mV
	SEL1-3 High Threshold	V_{SEL} Falling	●	1.31	1.41	1.51	V
	SEL1-3 High Threshold Hysteresis				35		mV
	SEL1-3 Float Voltage		●	0.9	1.0	1.1	V
	SEL1-3 Input Current	V_{SEL} = 4V V_{SEL} = 0V			45 –15		µA µA
	SEL1-3 De-bounce Time			1.25	1.5	1.75	ms
	Soft Start Time			0.7	1.1	1.6	ms
DATALINE SWITCHES							
V_{OL}, V_{OH}	Signal Range		●	0		3.6	V
	Off HD^+, HD^- Current	V_{HD}^+, V_{HD}^- = 3.6V, V_{LD}^+, V_{LD}^- = 0V V_{HD}^+, V_{HD}^- = 20V, V_{LD}^+, V_{LD}^- = 0V		–1	0 0.75	1 1	µA mA
	Off LD^+, LD^- Current	V_{HD}^+, V_{HD}^- = 0V, V_{LD}^+, V_{LD}^- = 3.6V V_{HD}^+, V_{HD}^- = 20V, V_{LD}^+, V_{LD}^- = 0V		–1 –1	0 0	1 1	µA µA
	On Leakage Current	V_{HD}^+, V_{HD}^- = 3.6V, 0V		–100	0	100	nA
	On Resistance	V_{HD}^+, V_{HD}^- = 0V, 3.6V, I_{LD}^+, I_{LD}^- = 20mA			3		Ω
	On Capacitance to Ground	V_{HD}^+, V_{HD}^- = 200mV_{DC}, 400mV_{P-P}, 480MHz (Note 5)			6.1		pF
V_{BUS} DISCHARGE							
	BUS/ISN Discharge Current Sink	$V_{BUS/ISN}$ = 5V		6	9	12	mA
V_{BUS_LKG}	BUS/ISN Discharge Status Threshold	$V_{BUS/ISN}$ Falling			0.5	0.7	V
	BUS/ISN Discharge Status Threshold Hysteresis				0.35		V
T_{VLD_VLKG}	Maximum BUS/ISN Discharge Time	$V_{BUS/ISN}$ = 1V			400	500	ms
T_{VBUS_REAPP}	Minimum BUS/ISN Low Time	$V_{BUS/ISN}$ = 1V		100	120		ms
	STATUS Oscillation Period			7.5	9	10.5	ms
V_{BUS} OFF							
$I_{VBUS\_LKG\_SRC}$	Regulator Output Leakage Current	$V_{BUS/ISN}$ = 0V $V_{BUS/ISN}$ = 5V		–70	–0.1 15	 80	µA µA
R_{OTG_VBUS}	Regulator Output Resistance	$V_{BUS/ISN}$ = 0.75V		10	350		kΩ

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
USB BCS 1.2 CHARGING DOWNSTREAM PORT PROFILE							
V_{DAT_REF}	HD^+ Data Detect Voltage	V_{HD}^+ Rising		0.25	0.32	0.40	V
	HD^+ Data Detect Hysteresis				45		mV
V_{IH}	HD^+, HD^- Logic High			2.0			V
V_{IL}	HD^+, HD^- Logic Low					0.8	V
V_{LGC}	HD^+, HD^- Logic Threshold			0.8	1.4	2.0	V
V_{DM_SRC}	HD^- Voltage Source	I_{HD}^- = –100µA, V_{HD}^+ = 0.6V		0.5	0.6	0.7	V
I_{DP_SINK}	HD^+ Current Source	V_{HD}^+ = 0.6V		25	100	175	µA
V_{DAT_SINK}	HD^+ Data Sink Voltage	I_{HD}^+ = 25µA			0.06	0.15	V
T_{VDMSRC_EN}	HD^- Voltage Source Enable Time	V_{HD}^+ = 0.6V			0.5	20	ms
$T_{CON\_IDPSNK\_DIS}$	HD^+ Current Source Connect Disable Time	V_{HD}^+ = 2V			0.75	10	ms
T_{VDPSRC_ON}	Minimum Accepted HD^+ Voltage Source On Time	V_{HD}^+ = 0.6V			32	40	ms
T_{VDMSRC_DIS}	HD^- Voltage Source Disable Time	V_{HD}^+ = 0V			0.5	20	ms
	Minimum Accepted HD^+ Source Voltage Off Time	V_{HD}^+ = 0V			32	40	ms
$T_{SVLD\_CON\_PWD}$	Maximum Accepted USB Connect Time	V_{HD}^+, $_{HD}^-$ = 0V		1	1.15		s
USB BCS 1.2 DEDICATED CHARGING PORT PROFILE							
R_{DCP_DAT}	Dataline Short Resistance	V_{HD}^+ = 0.6V, I_{HD}^- = –2.5mA			85	200	Ω
R_{DAT_LKG}	Dataline Short Pull Down Resistance			300	500		kΩ
USB BCS 1.2 STANDARD DOWNSTREAM PORT PROFILE							
R_{DP_DWN}, R_{DM_DWN}	Dataline Termination Resistor			14.25	20	24.8	kΩ
2.4A CHARGER PROFILE							
	HD^+ Voltage	$V_{BUS/ISN}$ = 5V		2.60	2.68	2.76	V
	HD^+ Output Resistance				23		kΩ
	HD^- Voltage	$V_{BUS/ISN}$ = 5V		2.60	2.68	2.76	V
	HD^- Output Resistance				23		kΩ
2.1A CHARGER PROFILE							
	HD^+ Voltage	$V_{BUS/ISN}$ = 5V		2.60	2.68	2.76	V
	HD^+ Output Resistance				23		kΩ
	HD^- Voltage	$V_{BUS/ISN}$ = 5V		1.94	2.00	2.06	V
	HD^- Output Resistance				30		kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
1A CHARGER PROFILE							
	HD^+ Voltage	$V_{BUS/ISN}$ = 5V		1.94	2.00	2.06	V
	HD^+ Output Resistance				30		kΩ
	HD^- Voltage	$V_{BUS/ISN}$ = 5V		2.60	2.68	2.76	V
	HD^- Output Resistance				23		kΩ
2A CHARGER PROFILE							
	HD^+, HD^- Voltage	$V_{BUS/ISN}$ = 5V		1.2	1.25	1.35	V
	HD^+, HD^- Output Resistance				7.5		kΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8698SE and LT8698SE-1 are guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8698SJ and LT8698SJ-1 are guaranteed over the full –40°C to 150°C operating temperature range. High junction temperatures degrade operating lifetime. Operating lifetime is de-rated at junction temperatures greater than 125°C. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (PD in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

Note 4: DUT configured in closed loop test circuit similar to page 36 CDP charger application circuit.

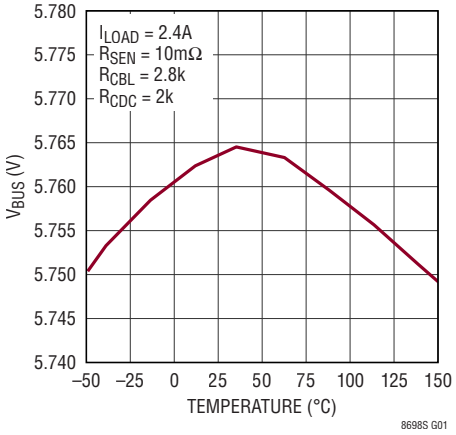
Note 5: Parameter not tested in production.

Note 6: θ values are determined by simulation per JESD51 conditions, except θ_{JA} value is determined by simulation with demo board. See Applications Information section for more information on PCB layout considerations and example thermal data.

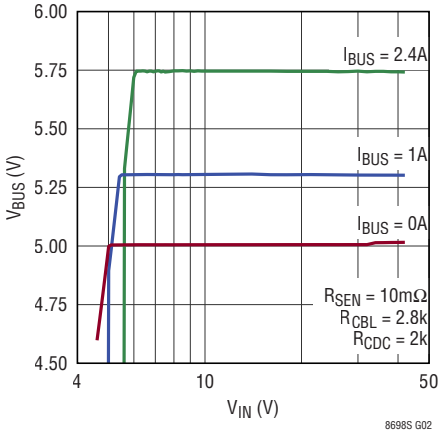
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V unless otherwise noted.

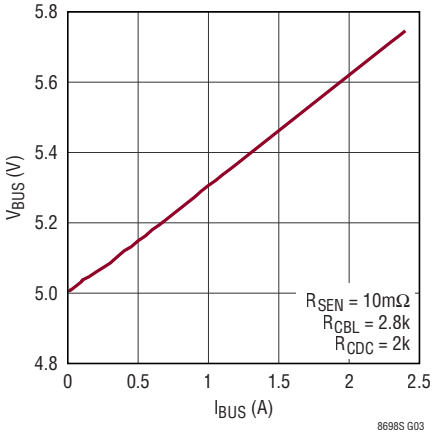
V_{BUS} vs Temperature



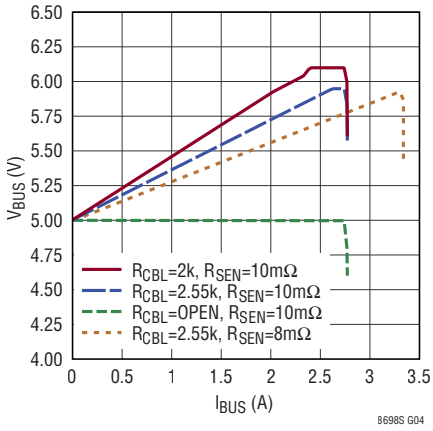
V_{BUS} vs V_{IN}



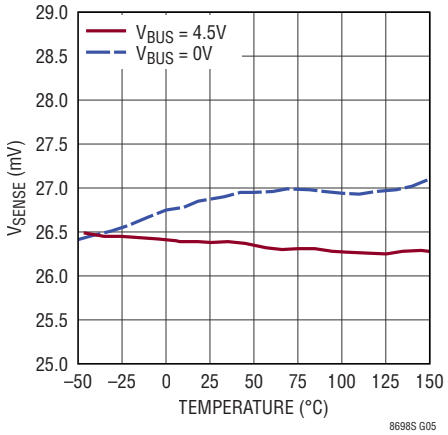
V_{BUS} vs I_{BUS}



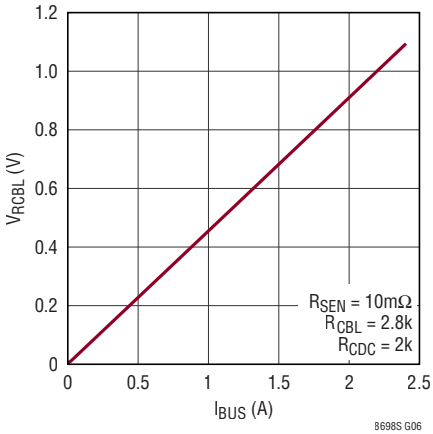
Output Current Load Line



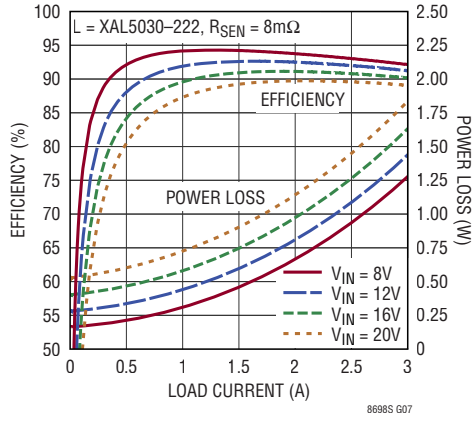
Sense Voltage (V_{ISP} – V_{ISN}) vs Temperature



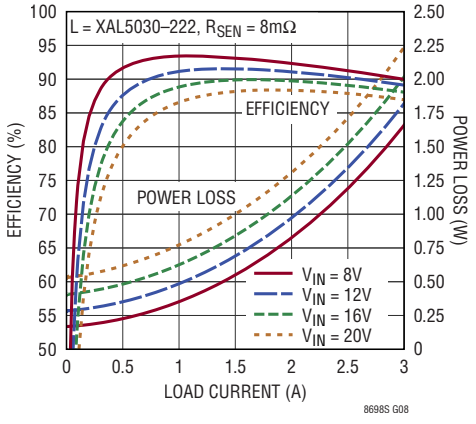
RCBL Voltage vs Load



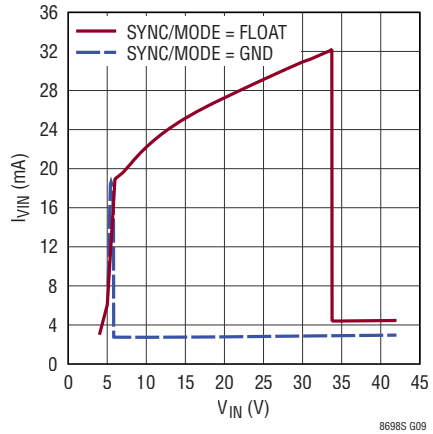
Efficiency at T_A = 25°C



Efficiency at T_A = 90°C



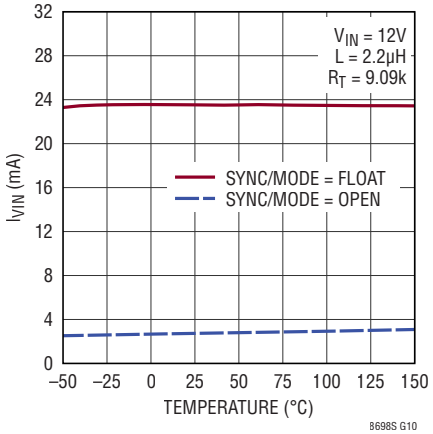
No Load Input Current vs V_{IN}



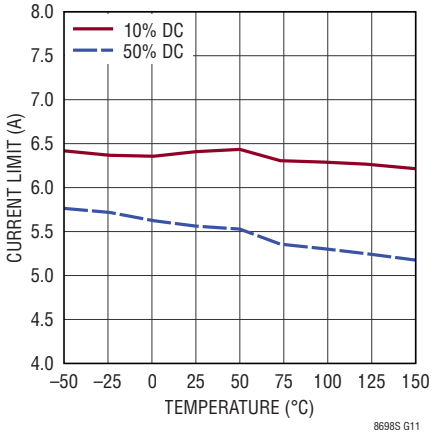
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V unless otherwise noted.

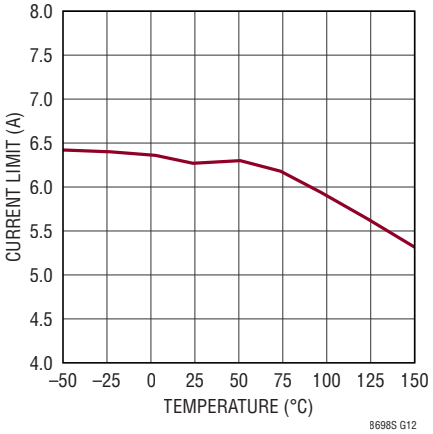
No Load Input Current vs Temperature



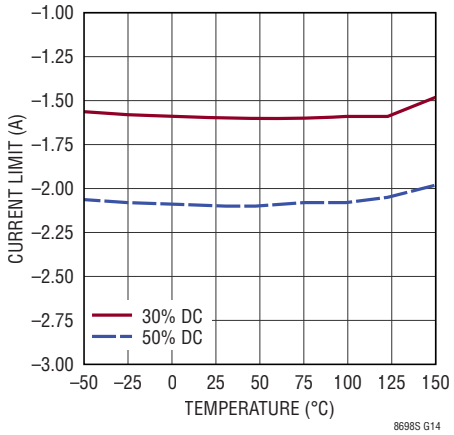
Top FET Current Limit



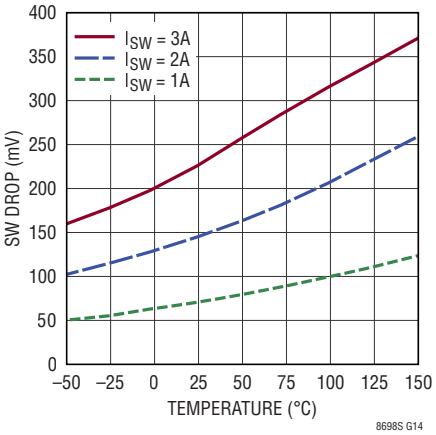
Bottom FET Positive Current Limit vs Temperature



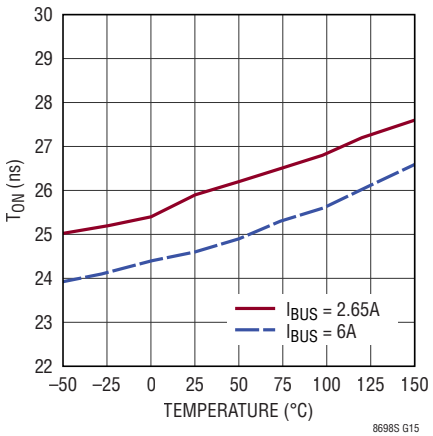
Top FET Negative Current Limit



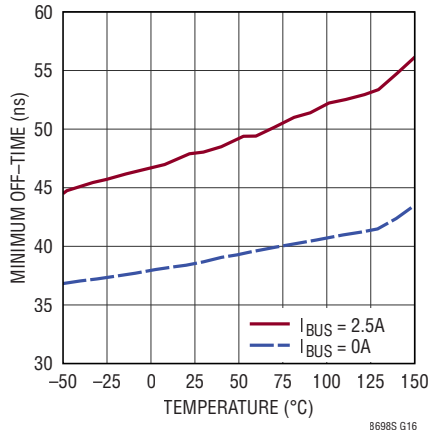
Top FET/ Bottom FET Drop



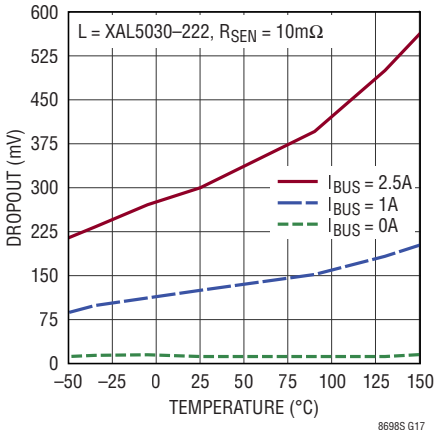
Top FET Minimum On-Time



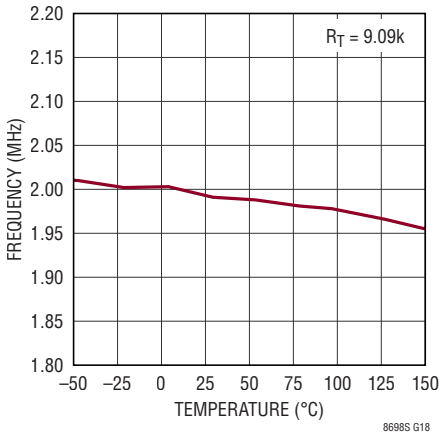
Minimum Off-Time vs Temperature



V_{IN} - V_{BUS} Dropout



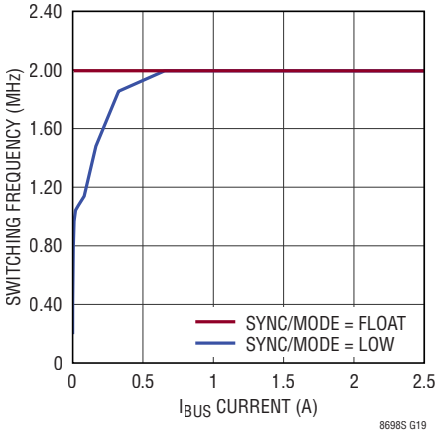
Switching Frequency vs Temperature



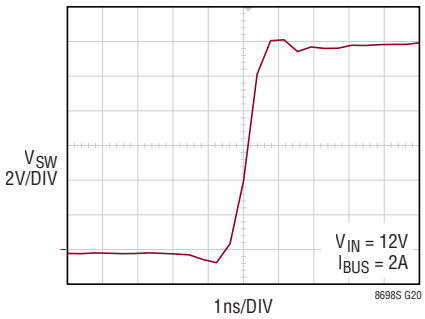
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V unless otherwise noted.

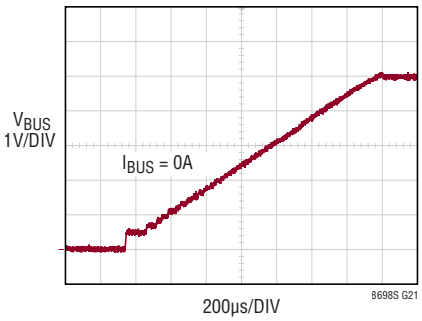
Switching Frequency vs Load Current



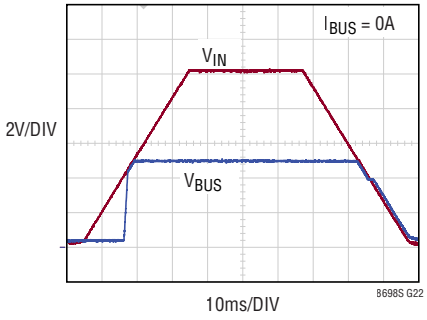
Switch Rising Edge



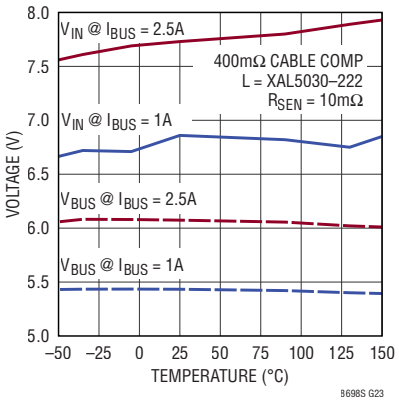
Soft-Start vs Time



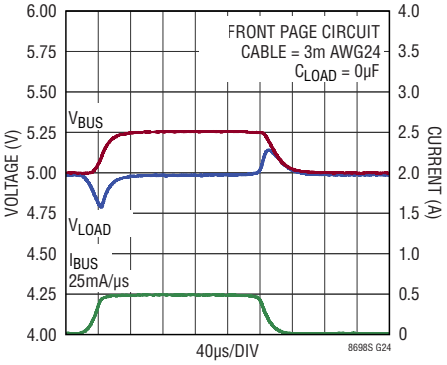
Start-Up/Dropout



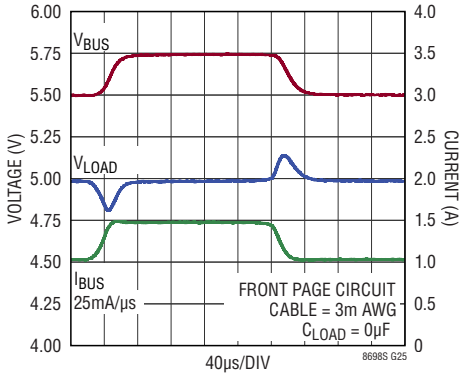
Minimum V_{IN} for Full Frequency Regulation @ 2MHz with 400mΩ Cable Drop Compensation



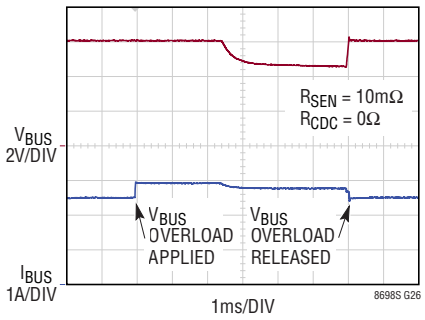
Load Transient Response Through Cable



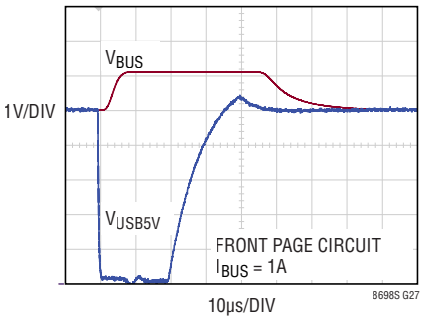
Load Transient Response Through Cable



Output Current Limit Transient



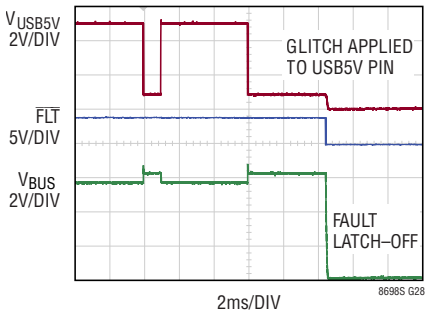
USB5V (Feedback) Shorted to Ground Transient



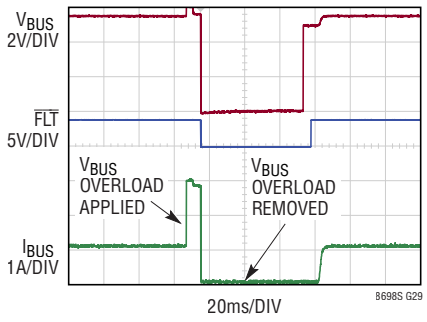
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V unless otherwise noted.

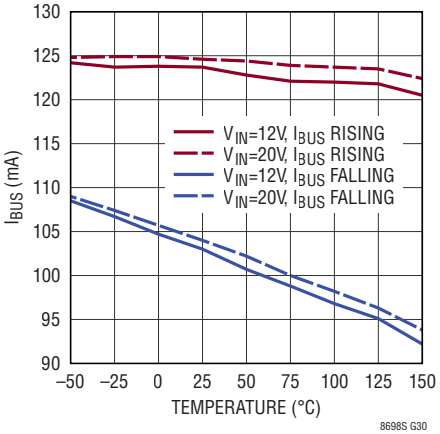
$\overline{FLT}$ Deglitching



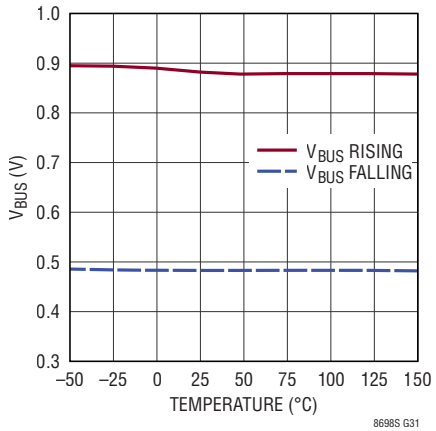
Latch-Off and Auto-Retry



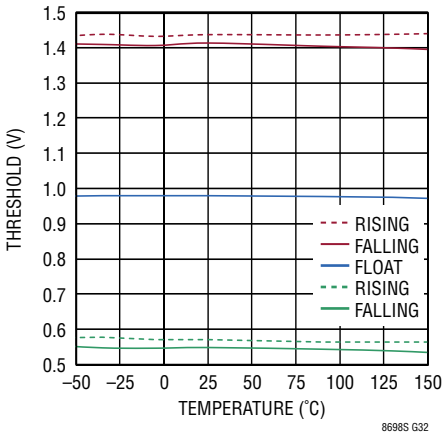
STATUS I_{BUS} Threshold



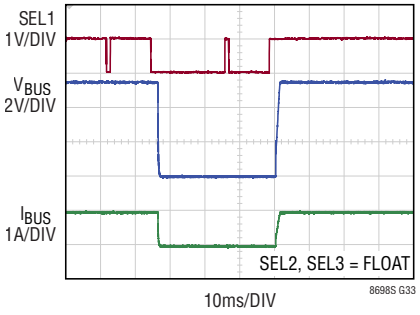
STATUS V_{BUS} Threshold



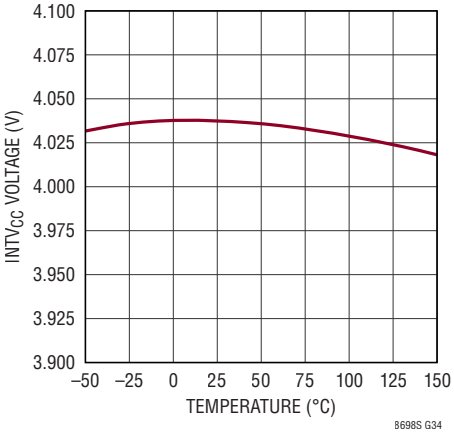
SEL1-3 High and Low Threshold



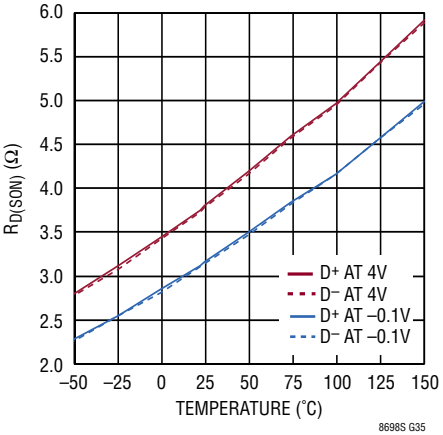
SEL1-3 Deglitching



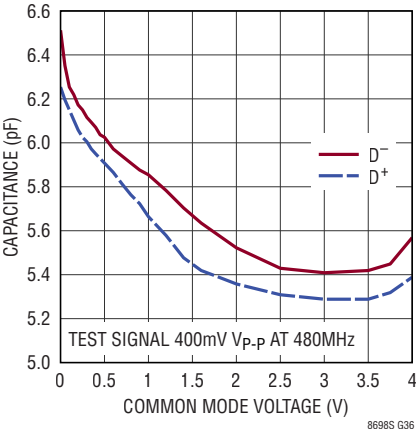
$INTV_{CC}$ Voltage vs Temperature



Dataline Switch $R_{DS(ON)}$



Dataline Switch Capacitance to Ground, Switch On

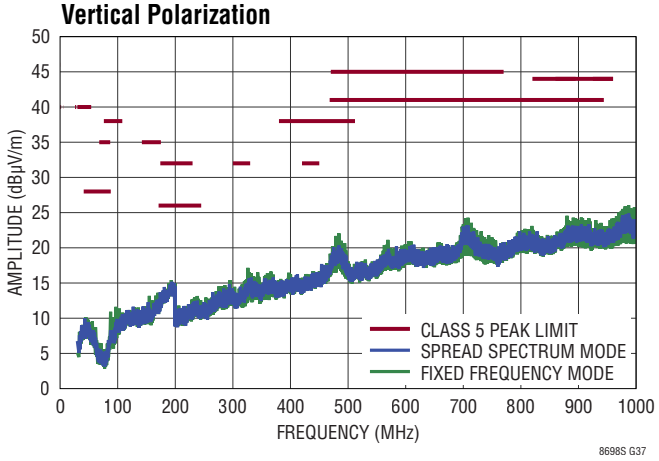


TYPICAL PERFORMANCE CHARACTERISTICS

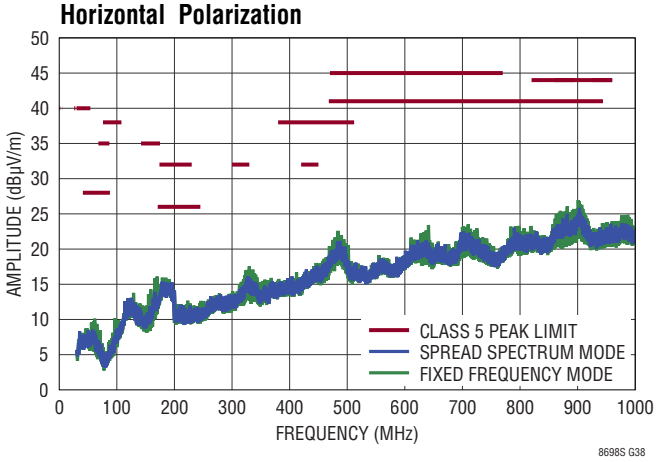
T_A = 25°C, V_{IN} = 12V unless otherwise noted.

Radiated EMI Performance, (CISPR25 Radiated Emission with Peak Detector and Class 5 Peak Limit)
DC2688A Demo Board with EMI Filter Installed, V_{IN} = 14V, I_{VBUS} = 2.5A, f_{SW} = 2MHz,
L = XFL4020-222, C_{VIN2} and C_{VIN3} Populated, LT8698S Only

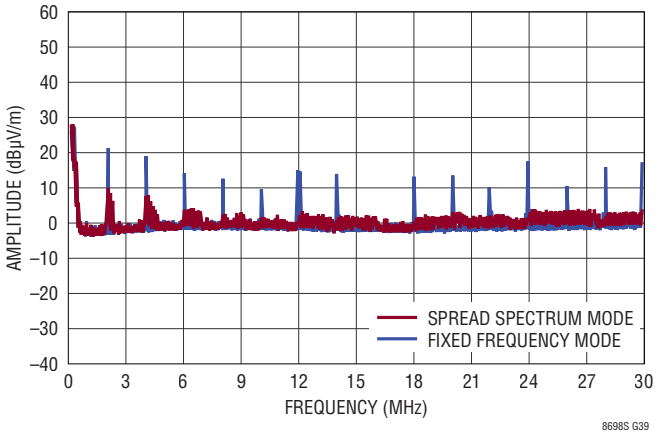
Vertical Polarization



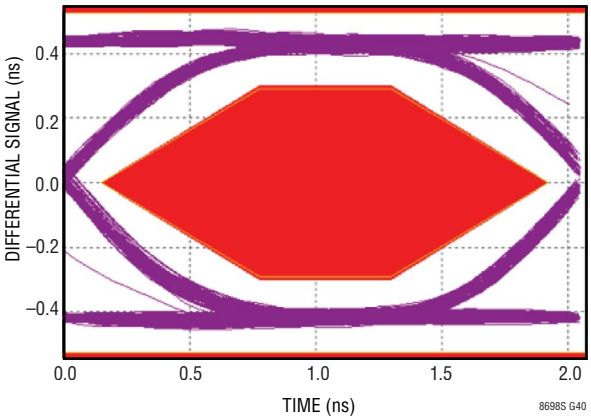
Horizontal Polarization



Conducted EMI Performance
DC2688A Demo Board with EM Filter Installed, V_{IN} = 14V, I_{VBUS} = 2.5A, f_{SW} = 2MHz,
L = XFL4020-222, C_{VIN2} and C_{VIN3} Populated, LT8698S Only



High Speed USB 2.0 Eye Diagram
DC2688A Demo Board, Measured at Test Plane 2 with Template 1 Waveform Requirements



PIN FUNCTIONS

GND (Pins 1, 11, 14, 17, 23): The GND pins are the return side of the internal control circuits and must be tied to ground. All GND and PGND pins are internally shorted together.

$INTV_{CC}$ (Pin 2): $INTV_{CC}$ is the bypass pin of the internal 4V linear regulator. This pin powers the internal power switch gate drivers and control circuits. $INTV_{CC}$ may be loaded by external termination resistors up to 1mA. For reliable operation, do not overload $INTV_{CC}$. Bypass this pin to ground with a 1µF low ESR ceramic capacitor placed close to the LT8698S.

EN/UV (Pin 3): EN/UV is the enable and programmable undervoltage lockout pin. The LT8698S is shut down when the EN/UV pin is below its threshold and enabled when above. The threshold voltage is 1.46V with EN/UV rising and 1.31V with EN/UV falling. EN/UV below 0.25V reduces the V_{IN} current to <1µA. An external resistor divider from V_{IN} can be used to program an undervoltage lockout threshold below which the LT8698S will shut down. See the Applications Information section for additional information. Tie EN/UV to V_{IN} if not used.

$\overline{FLT}$ (Pin 4): $\overline{FLT}$ is the open drain output of the internal fault logic. $\overline{FLT}$ pulls low after 4.2ms of a sustained fault condition in which the output voltage is not is regulation. $\overline{FLT}$ pulls low immediately if $INTV_{CC}$ < 3.6V or if the internal thermal shutdown feature activates. $\overline{FLT}$ transitions to high impedance after 4.2ms in the sustained absence of a fault condition. $\overline{FLT}$ is valid when V_{IN} > 4.5V and EN/UV > 1.46V. Float $\overline{FLT}$ if not used.

STATUS (Pin 5): STATUS is an open drain output indicator. The STATUS pin function depends on the state selected by the SEL1-3 pins. Refer to Table 6 for more information. STATUS is de-bounced for 4.2ms and is valid when V_{IN} > 4.5V and EN/UV > 1.46V. Float STATUS if not used.

SEL1, SEL2, SEL3 (Pins 6-8): SEL1-3 are tristate input pins used to select the desired USB functionality of the LT8698S. Refer to Table 6 in the Applications Information section for detailed information. Tie below 0.58V for logic low, above 1.41V for logic high and float for tristate. Keep leakage currents under 1µA for robust tristate detection. The SEL1-3 pins are de-bounced for 1.5ms for robust transitions between USB states.

RT (Pin 9): RT is the switching frequency programming pin. Tie a resistor from RT to ground to select the switching frequency. See the Applications Information section for additional information.

SYNC/MODE (Pin 10): SYNC/MODE is the clock synchronization and mode selection input pin. Ground SYNC/MODE for pulse-skipping mode. Tie to a clock source for synchronization to an external frequency and forced continuous mode. Float for forced continuous mode with RT programing the switching frequency. Tie to $INTV_{CC}$ for forced continuous mode with spread-spectrum modulation of the switching frequency for improved EMI/EMC performance.

LD^+ (Pin 12): LD^+ is the low voltage host side of the internal USB D^+ dataline switch. Float this pin if not used.

LD^- (Pin 13): LD^- is the low voltage host side of the internal USB D^- dataline switch. Float this pin if not used.

HD^- (Pin 15): HD^- is the high voltage USB cable and device side of the internal USB D^- dataline switch. Both dataline switches are disconnected if HD^- > 4.5V. Float this pin if not used.

HD^+ (Pin 16): HD^+ is the high voltage USB cable and device side of the internal USB D^+ dataline switch. Both dataline switches are disconnected if HD^+ > 4.5V. Float this pin if not used.

CLAMP (Pin 18): Bypass CLAMP with a 0.1µF 20V or greater low ESR capacitor to ground.

RCBL (Pin 19): RCBL is the cable drop compensation programming pin. A resistor R_{CBL} tied from RCBL to ground programs the cable drop compensation by setting the USB5V input current. RCBL can source 2mA. Excessive capacitive loading on RCBL can degrade load transient response. Isolate load capacitance on this pin by tying a 100k resistor between RCBL and the capacitive load. The RCBL load monitor output is valid when the LT8698S is enabled; otherwise the output is low. See the Applications Information section for additional information.

PIN FUNCTIONS

USB5V (Pin 20): USB5V is the 5V regulator feedback pin. For cable drop compensation, the USB5V pin input current is proportional to the sensed output current. Tie R_{CDC} from USB5V to the BUS/ISN output for 5V regulation plus cable drop compensation. Tie C_{CDC} from USB5V to BUS/ISN to limit the cable drop compensation loop bandwidth. Short USB5V to VBUS if no cable drop compensation is desired.

BUS/ISN (Pin 21): BUS/ISN is the USB VBUS output and negative current sense input pin. BUS/ISN provides an additional input to the error amplifier to ensure the maximum output regulation voltage does not exceed 6.05V. In addition, BUS/ISN provides the negative input to the internal current sense amplifier. BUS/ISN must be tied to the R_{SEN} sense resistor for cable drop compensation and output current limit. Kelvin connect the BUS/ISN pin to the sense resistor to separate regulator output current from the BUS/ISN PCB trace. See the Applications Information section for additional operation and PCB layout information.

OUT/ISP (Pin 22): OUT/ISP is the switching regulator output. OUT/ISP must be tied to the inductor terminal opposite the SW and must be bypassed by the output capacitor. Also, the OUT/ISP pin is the noninverting input to the current sense amplifier and must be tied to the R_{SEN} sense resistor for cable drop compensation and output current limit. Kelvin connect the OUT/ISP pin to the sense resistor to separate regulator output current from the OUT/ISP trace. See the Applications Information section for additional information.

SW (Pins 24, 25): SW is the output node of the internal top and bottom side power switches. Connect to the switching regulator inductor. This node should be kept small on the PCB for good performance.

BST (Pin 26): BST provides a drive voltage, higher than the input voltage, to the top side power switch. Leave BST floating.

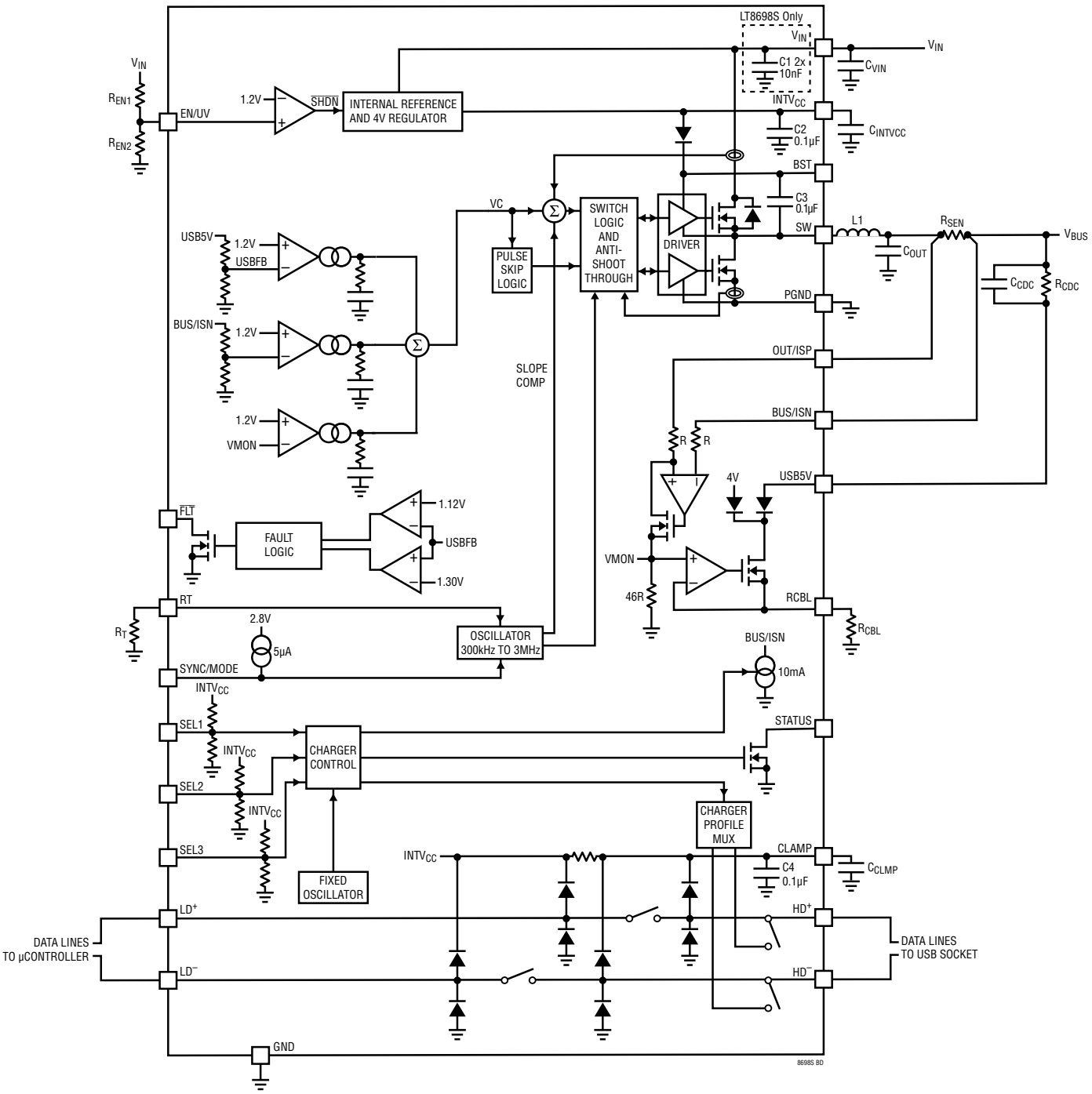
PGND (Pins 27, 32): The PGND pins are the return path of the internal bottom side power switch and must be tied together. Place negative terminal of the input capacitors as close as possible to the PGND pins. See Applications Information section for a sample layout. All GND and PGND pins are internally shorted together.

V_{IN} (Pins 29, 30): The V_{IN} pins are the input path of the internal top side power switch and must be tied together. The LT8698S requires a minimum of 2µF local input bypass capacitance to PGND. A single 2.2µF capacitor may be placed between V_{IN} and PGND. Best practice for low EMI/EMC is to tie two additional 0.1µF input bypass capacitors to V_{IN}. One 0.1µF capacitor should be placed between V_{IN} and pin 27 PGND. A second 0.1µF capacitor of equal value should be placed between V_{IN} and pin 32 PGND. These capacitors should be placed as close as possible to the LT8698S. See Application Information section for a sample layout.

Exposed Pads (Pins 33–38): The exposed pads must be connected to ground. Keep the top layer PCB connection to these pins large to lower the thermal resistance from the LT8698S package to ambient. See the Applications Information section for detailed recommendations.

Corner Support Pads (Pins 39–42): The four pads at each corner of the package are support pads intended to improve board level mechanical reliability. These pads are tied to ground internally to the LT8698S. The pads must be tied to PCB ground.

BLOCK DIAGRAM



OPERATION

The LT8698S is a highly efficient synchronous, monolithic USB charger with cable drop compensation and robust USB dataline protection. As such, the LT8698S includes a switching regulator optimized for powering the 5V USB V_{BUS} rail and two analog switches that tie to the high speed USB 2.0 datalines to provide fault and ESD protection to the upstream USB host IC. Finally, the LT8698S includes many USB charger profiles to allow high current charging of portable devices.

The LT8698S regulator is a monolithic, constant frequency, peak current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the V_C node. The error amplifier compares the output voltage on the USB5V pin through an internal resistor divider to an internal reference and servos the V_C node to regulate the USB5V pin to 5V. When the load current increases it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the V_C voltage until average inductor current matches the new load current. When the top power switch turns off, the synchronous bottom power switch turns on until the next clock cycle begins or inductor current falls to zero when not in forced continuous mode. If overload conditions result in a current higher than the bottom switch current limit flowing in the bottom switch, the next clock cycle will be delayed until switcher current returns to a safe level. In addition, during a fault condition in which USB5V is shorted to ground, the BUS/ISN voltage is regulated to 6.05V to limit the output voltage to a safe level for connected devices. Finally, during an output fault condition, the LT8698S provides an accurate, average output current limit using an external sense resistor connected across the OUT/ISP and BUS/ISN pins.

The LT8698S includes cable drop compensation to provide 5V regulation of the V_{BUS} rail at the end of a long, resistive cable even with high load current. To implement cable drop compensation, the LT8698S drives the RCBL pin to $46 \bullet (V_{OUT/ISP} - V_{BUS/ISN})$. Current sourced from the RCBL pin through the R_{CBL} resistor is derived from the USB5V pin, creating an output offset across the R_{CDC} resistor above the 5V USB5V pin voltage that is proportional to the R_{CDC}/R_{CBL} resistor ratio.

The "S" in the LT8698S part name refers to the second generation Silent Switcher Technology. This technology allows fast switching edges for high switching regulator efficiency at high switching frequency, while simultaneously achieving good EMI performance. This technology includes the integration of ceramic capacitors into the package for the V_{IN}, $INTV_{CC}$ and BST (C1 to C4 in the Block Diagram). These capacitors keep all of the AC current loops small which improves EMI performance. The LT8698S-1 does not include integrated ceramic capacitors tied to V_{IN}.

An EN/UV pin voltage above 1.46V enables the switching regulator, dataline switches and associated circuitry. An EN/UV pin voltage below 1.31V stops switching and opens the dataline switches. EN/UV pin voltage below 0.25V reduces V_{IN} current to <1µA.

The LT8698S operates primarily in forced continuous mode (FCM) for fast transient response and full frequency operation over a wide load range. To improve regulator efficiency at light load, the LT8698S can operate in pulse-skip mode (PSK). PSK reduces the switching frequency at light load current and reduces V_{IN} quiescent current between pulses. Ground the SYNC/MODE pin for PSK operation, float it for FCM operation or apply a DC voltage higher than 3.2V to use FCM with spread spectrum modulation (SSM). If a clock is applied to the SYNC/MODE pin, the internal oscillator will synchronize to the external clock frequency and operate in FCM. While in FCM the oscillator operates continuously and rising SW transitions are aligned to the clock. During light loads, the inductor current is allowed to go negative to maintain the programmed switching frequency. The LT8698S can sink current from the output, improving the load step response. Minimum current limits for both power switches are enforced to prevent large negative inductor current from flowing back into the input. SSM dithers the switching frequency from the programmed value set by the RT pin up to 20% higher than the programmed value to spread out the switching energy in the frequency domain.

Comparators monitoring the USB5V pin voltage will pull the $\overline{FLT}$ pin low if the output voltage varies more than ±7% (typical) from the set point, or if a power supply fault condition is present.

OPERATION

Dataline analog switches allow connection and disconnection between the HD^+ pin and the LD^+ pin and between the HD^- pin and the LD^- pin. When connected, the switches provide low resistance over the full 0V to 3.6V common mode range and can block 0V to 20V on the $HD^{+/-}$ side and 6V on the $LD^{+/-}$ side. High speed circuitry disconnects the switches in the event of a fault or ESD on the $HD^{+/-}$ side.

The LT8698S includes many charger profiles including USB BC 1.2 CDP, DCP, and SDP as well as common proprietary profiles. Each profile ties various components to the datalines. This could be resistive dividers, a short between the datalines, or voltage sources and current sources. These profiles might be passive or could react to the device plugged into the USB socket in some active manner. The profile allows the device plugged into the USB socket to identify a high current charger and draw more current from V_{BUS} than the 0.5A that would usually be allowed from a standard USB 2.0 socket.

SEL1-3 pins are tristate inputs that allow the host µController to control the behavior of the LT8698S. Internal resistive dividers bias these pins to 1V when a high Z input is applied. The SEL1-3 pins are de-bounced for 1.5ms prior to allowing a state change to the LT8698S.

The STATUS pin is an open drain output whose function is determined by the state selected by the SEL1-3 pins. This pin can output high or low or oscillate with a 9ms period.

APPLICATIONS INFORMATION

Cable Drop Compensation

The LT8698S includes the necessary circuitry to implement cable drop compensation. Cable drop compensation allows the regulator to maintain 5V regulation on the USB V_{BUS} rail despite high cable resistance. The LT8698S increases its local output voltage ($V_{BUS/ISN}$) above 5V as the load increases to keep V_{BUS} regulated to 5V. This compensation does not require running an additional pair of Kelvin sense wires from the regulator to the load, but does require the system designer to know the cable resistance R_{CABLE} as the LT8698S does not sense this value.

Program the cable drop compensation using the ratio of Equation 1.

$$R_{CBL} = 46 \bullet \left(\frac{R_{SEN} \bullet R_{CDC}}{R_{CABLE}} \right) \quad (1)$$

where R_{CDC} is a resistor tied between the regulator output and the USB5V pin, R_{CBL} is a resistor tied between the RCBL pin and GND, R_{SEN} is the sense resistor tied between the OUT/ISP and BUS/ISN pins in series between the regulator output and the load, and R_{CABLE} is the cable resistance. R_{SEN} must be 10mΩ for 2.4A applications and 8mΩ for 3A applications for the LT8698S to function properly.

The current flowing into the USB5V pin through R_{CDC} is identical to the current flowing through R_{CBL}. While the ratio of these two resistors should be chosen per the equation above, choose the absolute values of these resistors to keep this current between 30µA and 1200µA at full load current. This restriction results in R_{CBL} and R_{CDC} values between 1k and 40.2k. If I_{USB5V} is too low, capacitive loading on the R_{CBL} pin will degrade the load step transient performance of the regulator. If I_{USB5V} is too high, the R_{CBL} pin will go into current limit and the cable drop compensation feature will not work.

Capacitance across the remote load to ground downstream of R_{SEN} forms a left half plane zero in the LT8698S device's feedback loop due to cable drop compensation. C_{BUS} and the input capacitance of a portable device tied to the USB socket typically form this zero. C_{CDC} reduces the cable drop compensation gain at high frequency. The 4.7nF C_{CDC} capacitor tied across the 2k R_{CDC} is required for stability of the LT8698S's output. If R_{CDC} is changed, C_{CDC} should also be changed to maintain roughly the same 10µs RC time constant. If the capacitance across the remote load is large compared to the LT8698S output capacitors C_{OUT} and C_{BUS}, a longer $R_{CDC} \bullet C_{CDC}$ time constant may be necessary for stability depending on the amount of cable drop compensation used. Output stability should always be verified in the end application circuit.

APPLICATIONS INFORMATION

Short USB5V to the VBUS output if no cable drop compensation is desired.

The LT8698S limits the maximum voltage of V_{BUS} by limiting the voltage on the BUS/ISN pin to 6.05V. If the cable drop compensation is programmed to compensate for more than 1.05V of cable drop at the maximum I_{BUS}, this limit will prevent $V_{BUS/ISN}$ from rising higher and the voltage at the point of load V_{BUS} will drop below 5V. Equation 2 shows how to derive the LT8698S output voltage.

$$V_{OUT} = 5V + \frac{46 \bullet I_{BUS} \bullet R_{SEN} \bullet R_{CDC}}{R_{CBL}} \quad (2)$$

Refer to Figure 1 for load lines of $V_{BUS/ISN}$ and V_{BUS} to see how cable drop compensation works.

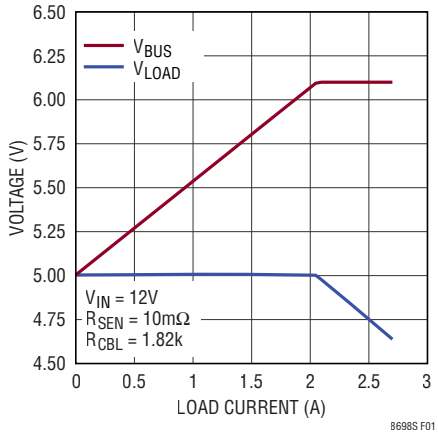
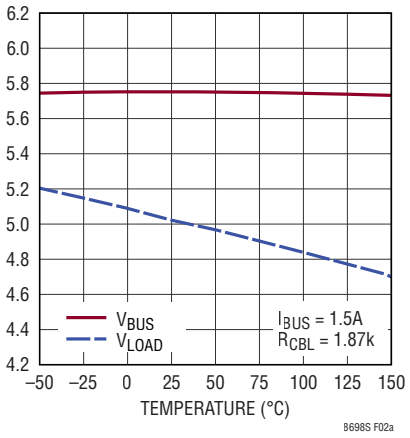


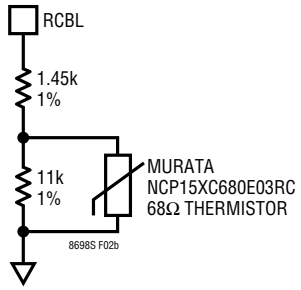
Figure 1. Example Cable Drop Compensation Load Line

Cable Drop Compensation Over a Wide Temperature Range

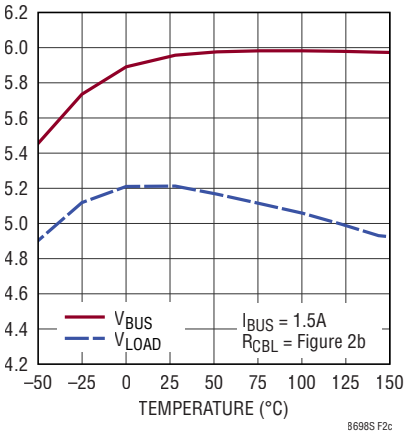
Cable drop compensation with zero temperature variation may be used in many applications (see Figure 2a,b,c). However, matching the cable drop compensation temperature variation to the cable resistance temperature variation may result in better overall output voltage accuracy over a wide operating temperature range. For example, in an application with 0.49Ω of wire resistance and a maximum output current of 1.5A, cable drop compensation adds 0.735V at 25°C to the output at max load for a fully compensated wire resistance. If the wire in this example is copper, the copper resistance temperature coefficient



(a) Cable Drop Compensation Through 3m of AWG 24 Twisted-Pair Cable (490mΩ) without Temperature Compensation



(b) R_{CBL} Resistor Network for Matching Copper Wire Temperature Coefficient



(c) Cable Drop Compensation Through 3m of AWG 24 Twisted-Pair Cable (490Ω) with Temperature Compensation Using NTC R_{CBL}

Figure 2. Cable Drop Compensation Applications

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of about 4000ppm/°C results in an output voltage error of 294mV at 125°C and 191mV at –40°C. Figure 2a shows this behavior.

See Table 1 for a list of copper wire resistances vs gauge.

Table 1. Copper Wire Resistance vs Wire Gauge

AWG	RESISTANCE OF CU WIRE AT 20°C (mΩ/m)
15	10.4
16	13.2
17	16.6
18	21.0
19	26.4
20	33.3
21	42.0
22	53.0
23	66.8
24	84.2
25	106
26	134
27	169
28	213
29	268
30	339
31	427
32	538
33	679
34	856
35	1080
36	1360
37	1720
38	2160
39	2730
40	3440

Cable drop compensation can be made to vary positively versus temperature with the addition of a negative temperature coefficient (NTC) resistor as a part of the R_{CBL} resistance. This circuit idea assumes the NTC resistor is at the same temperature as the cable. Figure 2b shows an example resistor network for R_{CBL} that matches copper resistance variation over a wide –40°C to 150°C temperature range. Figure 2c shows the resultant cable drop compensation output at several temperatures using R_{CBL} with negative temperature variation.

The NTC resistor does not give a perfectly linear transfer function versus temperature. Here, for typical component values, the worst case error is <20% of the cable compensation output, or <4% of the total output voltage accuracy. Better output voltage accuracy versus temperature can be achieved if R_{CBL} resistor values are optimized for a narrower temperature range.

Effect of Cable Inductance on Load Step Transient Response

The inductance of long cabling limits the peak-to-peak transient performance of a 2-wire sense regulator to fast load steps (see Figure 3). Since a 2-wire sense regulator like the LT8698S detects the output voltage at its local output and not at the point of load, the load step response degradation due to cable inductance is present even with cable resistance compensation. The local regulator output capacitor and the input capacitor of the remote load form a LC tank circuit through the inductive cabling between them. Fast load steps through long cabling show a large peak-to-peak transient response and ringing at the resonant frequency of the circuit. This ringing is a property of the LC tank circuit and does not indicate regulator instability.

Figure 3a shows the LT8698S load step transient response to a 125mA/µs, 0.5A load step. Two cable impedances are compared: resistive only and then resistive plus inductive. First, a surface mount 0.5Ω resistor is tied between the LT8698S output and the load step generator. This resistor stands in for a purely resistive “cable”. Second, AWG 24 twisted-pair cabling 3 meters long with 0.5Ω of total resistance and about 0.8µH of inductance is connected between the LT8698S output and the load step generator. Even though the resistance in these two circuits is the same, the transient load step response in the cable is worse due to the inductance. The degree that cable inductance degrades LT8698S load transient response performance depends on the inductance of the cable and on the load step rate. Long cables have higher inductance than short cables. Cables with less separation between supply and return conductor pairs show lower inductance per unit length than those with separated conductors. A faster load step rate exacerbates the effect of inductance on load step response.

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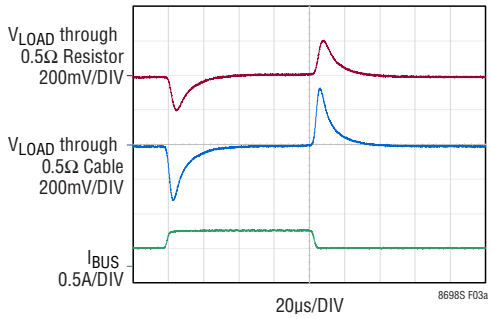
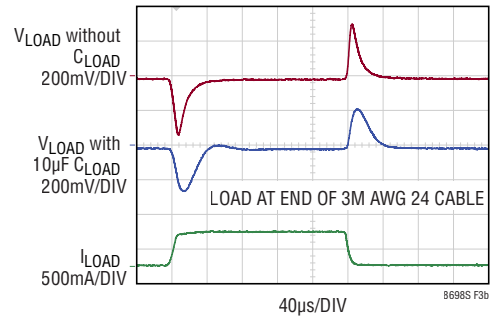


(a)



(b)

Figure 3. Effect of Cable Inductance on Load Step Transient Response

Figure 3b shows the effect of remote capacitance at the load side of the cable on the LT8698S transient response. The load step is a 60mA/µs, 0.5A load step through a 0.5Ω, 3 meter long cable. Without remote capacitance C_{LOAD} at the load step location, there is no LC tank and therefore no observed ringing. In this case, given 100% of the dI/dt of the load step occurs across the cable resistance R and inductance L, the peak to peak V_{LOAD} deviation is ±300mV. When 10µF of remote C_{LOAD} is added at the load step location, the cable L and load capacitance form a tank circuit leading to modest ringing. In this case, given the effective dI/dt across the cable R and L is reduced, the peak to peak V_{LOAD} deviation is reduced to less than ±250mV.

Probing a Remote Output Correctly

Take care when probing the LT8698S's remote output to obtain correct results. With cable drop compensation the local regulator output has a different voltage than the remote output at the end of a cable due to the cable resistance and high load current. The same is true for the ground return line which also has resistance and carries the same current as the output. Since the local ground at the LT8698S is separated by a current carrying cable from the remote ground at the point of load, the ground reference points for these two locations are different.

Use a differential probe across the remote output at the end of the cable to measure output voltage at that point, as shown in Figure 4b. Do not simultaneously tie an oscilloscope's probe ground leads to both the local LT8698S ground and the remote point of load ground, as shown in Figure 4a. Doing so will result in high current flow in the probe ground lines and a strange and incorrect measurement. Figure 4c shows this strange behavior. A 1.3A load step is applied to the LT8698S output through 3 meters of AWG 24 twisted-pair cable. On one curve, the resultant output voltage is measured correctly using a differential probe tied across the point of load. On the other curve, the oscilloscope ground lead is tied to the remote ground. This poor probing causes both a DC error due to the lower ground return resistance and an AC error showing increased overshoot. Do not add your oscilloscope, lab bench, and input power supply ground lines into your measurement of the LT8698S remote output.

Reducing Output Overshoot

A consequence of the use of cable drop compensation is that the local output voltage at the LT8698S BUS/ISN pin is regulated to a voltage that is higher than the remote output voltage at the point of load. Several hundred mΩ of line resistance can separate these two outputs, so at 2A of load current, $V_{BUS/ISN}$ may be up to 1.05V higher than the nominal 5V output at the point of load. Ensure that any components tied to the LT8698S output can withstand this increased voltage.

The LT8698S has several features designed to mitigate any effects of higher output voltage due to cable drop compensation. First, the LT8698S error amplifier, in addition to regulating the voltage on the USB5V pin to 5V for the primary output, also regulates the BUS/ISN pin voltage to less than 6.05V. This 6.05V upper limit on the maximum BUS/ISB voltage protects components tied to the LT8698S output such as a portable device from an overvoltage condition, but reduces the possible amount of cable drop compensation to 1.05V.

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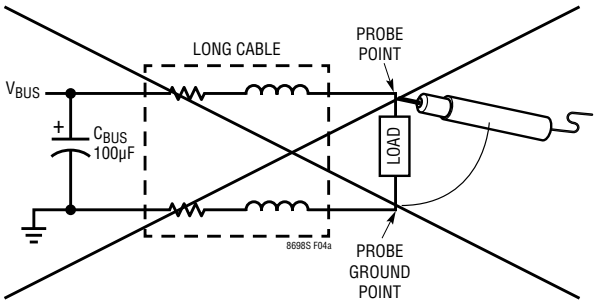
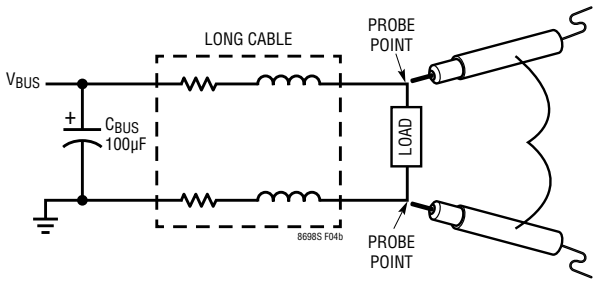
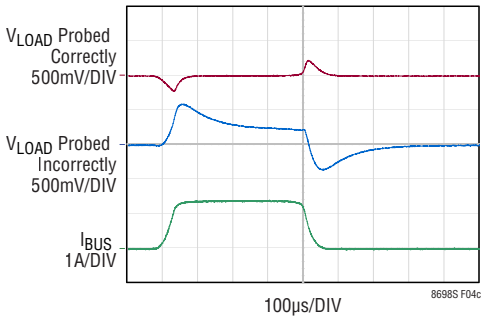


(a) Incorrect Remote Output Probing



(b) Correct Remote Output Probing



(c) Effect of Probing Remote Output Incorrectly

Figure 4. Probing a Remote Output Correctly

Additionally, the LT8698S can sink current from the output when in forced continuous mode (FCM). This feature improves the step response for a load step from high to low. Cable drop compensation adds voltage to the output to compensate for voltage drop across the cable resistance at high load. Since most DC/DC convertors can only source current, a load step from high to near zero current leaves the output voltage high and out of regulation. The LT8698S fixes this problem by allowing the regulator to sink current from the output when USB5V is too high using FCM. Figure 5 shows the output voltage of the front page application circuit with both FCM and PSK modes in response to a fast, 1.3A load step through a 3m cable. The load step response from high current to zero in PSK mode is extremely slow and is limited by the OUT/ISP, BUS/ISN and USB5V pin bias currents. However, with FCM enabled, the output slews quickly back into regulation.

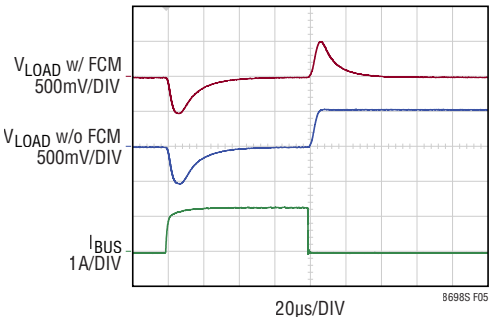


Figure 5. Load Step Response with and without Forced Continuous Mode

Lastly, the LT8698S positive switch peak current and negative valley current limits exceed the positive output current limit of 2.65A. This large current range allows the LT8698S to slew the output capacitor quickly for cable drop compensation during a transient load step.

Output Current Limit

In addition to regulating the output voltage, the LT8698S limits the average output current with a current regulation loop. Output current regulation limits power dissipation in the case of a fault on the USB cable or of the device plugged into the socket. The LT8698S measures the voltage drop across the external sense resistor R_{SEN} using the OUT/ISP and BUS/ISN pins. This resistor should be connected on the load side of the output capacitor C_{OUT}, in series with the load. The LT8698S control loop modulates the cycle-by-cycle switch current limit such that the average voltage across the OUT/ISP to BUS/ISN pins does not exceed its regulation point. When load current exceeds the output current limit and current regulation is active, the output voltage will drop below its regulation point.

The LT8698S also includes latch-off and auto-retry functionality in the output current regulation loop. If the output

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voltage is 7% below is regulation point for at least 4.2ms, the LT8698S will stop switching for 59ms. After 59ms, the LT8698S will start switching. If the output can return to its nominal regulation point within 4.2ms after starting to switch, then normal operation will resume. Otherwise, if the output still remains more than 7% below its regulation point, the LT8698S will again stop switching for 59ms and this sequence will repeat. This latch-off and auto-retry feature reduces the power dissipation in a fault condition to about an 7% duty cycle of what it otherwise would have been.

Using RCBL as an Output Current Monitor

The primary function of the RCBL pin is to set the cable drop compensation as discussed in the Cable Drop Compensation section. The secondary function of the RCBL pin is to produce an output voltage that is proportional to the output load current. The RCBL pin can therefore be used as an output load monitor. The voltage on the RCBL pin obeys Equation 3 relation to USB load current.

$$V_{RCBL} = I_{LOAD} \bullet R_{SEN} \bullet 46 \quad (3)$$

This formula is valid when the LT8698S is enabled.

Since the RCBL pin current is part of the cable drop compensation control loop, excessive capacitive loading on the RCBL pin can cause USB output voltage overshoot during load steps. Keep the capacitive loading on the RCBL pin below 100pF or isolate the load capacitance with 100kΩ in series between the RCBL pin and the input it is driving as shown in Figure 6.

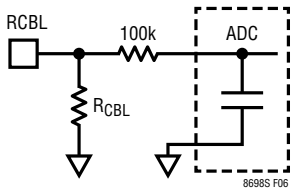

Figure 6. Using the RCBL Pin as Output Current Monitor

Setting the Switching Frequency

The LT8698S uses a constant frequency PWM architecture that can be programmed to switch from 300kHz to 3MHz by using a resistor tied from the RT pin to ground.

Table 2 shows the ideal R_T value for a desired switching frequency.

Table 2. Switching Frequency vs R_T Value

Switching Frequency (MHz)	R_T (kΩ)
3	5.76
2.8	6.19
2.6	6.81
2.4	7.5
2.2	8.25
2	9.09
1.8	10.2
1.6	11.5
1.5	12.4
1.4	13.3
1.3	14.7
1.2	15.8
1.1	17.4
1	19.1
0.9	21.5
0.8	24.3
0.7	28
0.6	32.4
0.5	39.2
0.4	49.9
0.3	66.5

R_T can also be found for the desired switching frequency using Equation 4 where f is in MHz.

$$R_T = \frac{20.25}{f} - 1.013k \quad (4)$$

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range.

The highest switching frequency ($f_{SW(MAX)}$) for a given application before min on-time limited can be calculated using Equation 5.

$$f_{SW(MAX)} = \frac{V_{OUT/ISP}}{t_{ON(MIN)} \bullet V_{IN(MAX)}} \bullet 1000 \quad (5)$$

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where $V_{IN(MAX)}$ is the maximum input voltage without skipped cycles, $V_{OUT/ISP}$ is the output voltage at OUT/ISP, and $t_{ON(MIN)}$ is the minimum top switch on-time of about 30ns. This equation shows that a slower switching frequency is necessary to accommodate a high $V_{IN}/V_{OUT/ISP}$ ratio.

For transient operation, V_{IN} may go as high as the absolute maximum rating of 42V regardless of the R_T value; however the LT8698S will reduce switching frequency as necessary to maintain control of inductor current to assure safe operation.

The LT8698S is capable of a maximum duty cycle of greater than 99%, and the V_{IN} to $V_{BUS/ISN}$ dropout is limited by the $R_{DS(ON)}$ of the top switch. Operating in this region results in lower switching frequency.

The highest switching frequency ($f_{SW(MAX)}$) for a given application before min off-time limited can be calculated using Equation 6.

$$f_{SW(MAX)} = \left(\frac{1}{t_{OFF(MIN)}} - \frac{V_{OUT/ISP}}{t_{OFF(MIN)} \bullet V_{IN(MIN)}} \right) \bullet 1000 \qquad (6)$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, $V_{OUT/ISP}$ is the output voltage at OUT/ISP, and $t_{OFF(MIN)}$ is the minimum switch off-time of 40ns. Note that higher switching frequency will increase the minimum input voltage for full frequency operation.

Inductor Selection and Maximum Output Current

The LT8698S is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions the LT8698S safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

Based on the desired switching frequency, pick an inductor for the LT8698S according to Table 3.

Table 3 lists nominal values for inductors. Inductors are typically de-rated versus current, versus temperature and have a tolerance spec. This table assumes the inductance in the application will not be 40% less than the nominal value at worst case operating conditions and tolerance.

For robust operation, use an inductor with value equal to or greater than the value on Table 3.

Table 3. Inductor Value by Switching Frequency

SWITCHING FREQUENCY (MHz)	MINIMUM NOMINAL INDUCTOR VALUE (µH)
2.4 – 3.0	1.5
1.9 – 2.4	2.2
1.3 – 1.9	3.3
0.89 – 1.3	4.7
0.61 – 0.89	6.8
0.51 – 0.61	8.2
0.30 – 0.51	10

Table 4 lists inductor vendors and associated inductor product series names that are recommended for use with the LT8698S.

Table 4. Inductor Manufacturers

VENDOR	SERIES	WEBSITE
TDK	SLF, VLC, VLF	www.tdk.com
Sumida	CRH, CDR, CDMC	www.sumida.com
Coilcraft	XAL, XFL, MSS	www.coilcraft.com
NIC	NPIM, NPIS	www.niccomp.com
Würth	TPC, SPC, PD, PDF, PD3	www.we-online.com

Input Capacitor

Bypass the input of the LT8698S circuit with a ceramic capacitor with the appropriate temperature and voltage rating, placed as close as possible to the V_{IN} and PGND pins. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 2.2µF to 4.7µF ceramic capacitor is adequate to bypass the LT8698S and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT8698S and to force this very high frequency switching

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current into a tight local loop, minimizing EMI. A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT8698S. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8698S circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8698S's voltage rating. This situation is easily avoided (see ADI Application Note 88).

Output Capacitor and Output Ripple

The output capacitor C_{OUT} tied from the OUT/ISP pin to ground has two essential functions. Along with the inductor, it filters the square wave generated by the LT8698S to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8698S's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Applications section.

On a switching regulator with fixed output voltage, transient performance can generally be improved with a higher value output capacitor. However, the LT8698S's cable drop compensation feature changes the local output voltage in response to a load step. Since transient load steps require the LT8698S to slew C_{OUT}, larger C_{OUT} in this case can degrade transient response. Only remote capacitance tied at the end of the cable near the USB socket can improve transient response. The minimum local output capacitance required for LT8698S loop stability and for output voltage ripple requirements is the best choice for C_{OUT}. See the Typical Applications section in this data sheet for suggested capacitor values.

The USB 2.0 specification document requires a minimum of 120µF low-ESR capacitor be tied from V_{BUS} to ground on a hub. Since the downstream device fixed V_{BUS} capacitance is limited to a maximum of 10µF, this minimum 120µF V_{BUS} capacitance prevents hot plugging of one downstream device from glitching the V_{BUS} and disrupting another connected device. If the LT8698S is powering V_{BUS} on a hub, then this requirement can be satisfied with extra C_{OUT} tied from either OUT/ISP to ground. There must always be a minimum of 22µF capacitance tied from OUT/ISP to ground.

Keep the capacitance tied to the BUS/ISN node lower in magnitude than the capacitance tied to the OUT/ISP node. Large BUS/ISN node capacitance to ground degrades the regulator loop phase margin and gives poor cable drop compensation transient response. If an output capacitance much larger than 22µF is desired, tie this capacitor to the OUT/ISP node, not to the BUS/ISN node.

When choosing a capacitor, special attention should be given to the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8698S due to their piezoelectric nature. In pulse-skipping mode operation, the LT8698S's switching frequency depends on the load current, and at very light loads the LT8698S can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8698S operates at a lower current limit during pulse-skipping operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

Table 5. Ceramic Capacitor Manufacturers

VENDOR	WEBSITE
Taiyo Yuden	www.ty-top.com
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.tdk.com

EN/UV Pin

The LT8698S is in shutdown when the EN/UV pin is < 0.25V and active when the pin is high. The falling threshold of the EN/UV comparator is 1.31V, with 150mV of hysteresis. The EN/UV pin can be tied to V_{IN} if the shutdown feature is not used, or driven to the desired logic

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level if shutdown control is required. The LT8698S EN/UV pin has an internal 5.5V clamp in a series with an approximately 1Meg resistor.

Adding a resistor divider from V_{IN} to EN/UV programs the LT8698S to operate only when V_{IN} is above a desired voltage. Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. This threshold can be adjusted by setting the values R_{EN1} and R_{EN2} such that they satisfy Equation 7.

$$V_{IN(EN)} = \left(\frac{R_{EN1}}{R_{EN2}} - 1\right) \bullet 1.46V \quad (7)$$

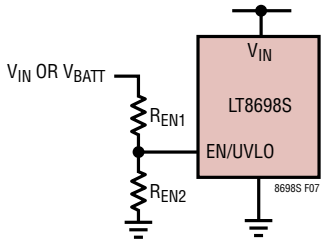

Figure 7. UVLO Divider

where the LT8698S will remain off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN)}$.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 4V supply from V_{IN} that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ LDO can supply enough current for the LT8698S's circuitry and must be bypassed to ground with a 1.0µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers.

Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. $INTV_{CC}$ can be loaded up to 1mA for such purposes as providing a resistor pull-up to the STATUS and $\overline{FLT}$ open drain output pins.

For reliable operation do not overload the $INTV_{CC}$ LDO with >1mA.

Soft-Start

The LT8698S includes an internal soft-start function. The output voltage ramp-up takes 1.1ms. The purpose of this soft start feature is to limit inrush current into the regulator as it charges the output capacitors during startup. V_{IN} undervoltage lockout, $INTV_{CC}$ under and overvoltage lockout, EN/UV low, thermal shutdown, output current limit latch off, and the SEL1-3 pins selecting a state with the switcher off all reset the soft start ramp.

$\overline{FLT}$ Pin

When the LT8689S's output voltage is within a ±7% window of the regulation point, which is a USB5V pin voltage in the range of 4.64V to 5.34V (typical), the output voltage is considered not to be in fault and the open-drain $\overline{FLT}$ pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the $\overline{FLT}$ pin low. To prevent glitching, both the upper and lower thresholds include 3% of hysteresis and the output is de-bounced over 4.2ms.

The $\overline{FLT}$ pin is also actively pulled low during several fault conditions: V_{IN} under voltage lockout, $INTV_{CC}$ under and over voltage lockout, EN/UV low, and thermal shutdown. Lastly, the $\overline{FLT}$ pin can pull low for 4.2ms at the end of the bus reset state machine sequence if V_{BUS} is held above 0.5V.

Synchronization

To select pulse-skipping mode operation, tie the SYNC/MODE pin below 0.3V. To select forced continuous mode (FCM), float the SYNC/MODE pin. To select FCM with spread spectrum modulation (SSM), tie the SYNC/MODE pin above 3.7V (SYNC/MODE can be tied to $INTV_{CC}$). To synchronize the LT8698S oscillator to an external frequency connect a 20% to 80% duty cycle square wave to the SYNC/MODE pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V. When synchronized to an external clock the LT8698S will use FCM.

The LT8698S may be synchronized over a 300kHz to 3MHz range. The R_T resistor should be chosen to set the LT8698S switching frequency equal to or below the

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lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for nominal 500kHz.

A synchronizing signal that incorporates spread spectrum may reduce EMI.

Forced Continuous Mode

Forced continuous mode (FCM) is activated by either floating the SYNC/MODE pin, applying a DC voltage above 1.1V to the SYNC/MODE pin or applying an external clock to the SYNC/MODE pin.

While in FCM, discontinuous mode operation is disabled and the inductor current is allowed to go negative so that the regulator can switch at the programmed frequency all the way down to 2.3A of negative output current. This has the advantage of maintaining the programmed switching frequency across the entire load range so that the switch harmonics and EMI are consistent and predictable. Also, the ability to sink current from the output improves load release transient response when cable drop compensation is used. The disadvantage of FCM is that the light load efficiency will be low compared to pulse-skip mode operation.

There are several operating conditions in which the LT8698S does not maintain the full switching frequency with FCM selected. For instance, FCM is disable in dropout which occurs at very low input voltages. When operating in dropout, the LT8698S skips off times, reducing the switching frequency to improve regulation performance.

Spread Spectrum Modulation

Spread spectrum modulation (SSM) is activated by applying a DC voltage above 3.7V to the SYNC pin. This can be accomplished by shorting the SYNC/MODE pin to the $INTV_{CC}$ pin. SSM reduces the EMI emissions by modulating the switching frequency between the value programmed by RT to approximately 20% higher than that value. For example, when the LT8698S is programmed to 2MHz and the SSM feature is enabled, the switching frequency will vary from 2MHz to 2.4MHz.

Output Short Circuit and Reverse Input Protection

The LT8698S is robust to output short circuit conditions. When operating with the output short circuited to ground, the bottom switch current is monitored such that if inductor current is beyond safe levels, switching of the top switch will be delayed until such time as the inductor current falls to safe levels.

When operating with the output short circuited to a high voltage, such as an automobile battery, the current flow within the system will depend on the state of the LT8698S input supply V_{IN}. If V_{IN} is disconnected, such as may occur with the ignition switch in the off position, the LT8698S will draw approximately 2.5mA of quiescent current from the output if EN/UV is driven high and 0µA if the EN/UV is low. If V_{IN} is grounded or reverse connected, the body diode of the internal TOP power FET allows uncontrolled current flow from the output (SW) to the input (V_{IN}), potentially damaging the LT8698S. To prevent possible uncontrolled reverse current, see Figure 8.

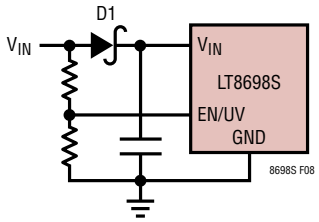

Figure 8. Reverse V_{IN} Protection

Output Cable Fault

The LT8698S is robust to cable faults on the V_{BUS} output to either GND or up to 20V. Input reverse protection described above must prevent excessive top switch body diode current from SW to V_{IN} if the output is held high. 20V on V_{BUS} is a fault condition that could damage a portable device plugged into the USB socket powered by the LT8698S. While the LT8698S can survive this condition, it will not prevent damage to the portable device.

An output cable fault with a fast step to 20V can result in ringing on V_{IN} up to 40V due to energy built up in the cable inductance and the switching regulator inductor. The 42V V_{IN} abs max withstands this ringing, but a cable

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fault above 20V could violate the V_{IN} abs max spec and damage the IC due to inductive ringing. This damage to V_{IN} can occur despite the 42V abs max rating of the V_{BUS} output pins OUT/ISP, BUS/ISN and USB5V. Figure 9 shows a fast output hot plug to 20V.

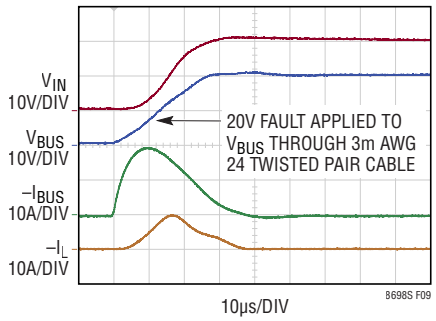

Figure 9. 20V Fault on V_{BUS}

Select Pins SEL1, SEL2, SEL3

The select pins SEL1-3 are tristate input pins intended to interface with a USB host µController. These pins select the operational state of the LT8698S's HD^+ and HD^- pins tied to the USB datalines D^+ and D^-. If dynamic state changes are not desired, the select pins may individually be tied low, high or left open to select a single LT8698S state. The select pins also can disable the switching regulator for USB On-The-Go (OTG) functionality and can initiate a 9mA active discharge of the USB V_{BUS} rail.

Each select pin has a resistive divider tied from $INTV_{CC}$ to GND that biases the pin to 1V when left floating. Tie below 0.48V for input low. Tie above 1.51V or to $INTV_{CC}$ for input high. Float with less than 1µA of leakage current for the tristate, high Z input. The select pin inputs are debounced for 1.5ms prior to passing the pin input state to the internal state machine.

The function of the STATUS output pin depends on the state selected by the SEL1-3 pins. The function of the $\overline{FLT}$ pin also can depend on the state selected by the SEL1-3 pins. For the bus reset functions accessed by select state 5, 11, 14 and 20 with V_{BUS} not powered, $\overline{FLT}$ can pull low due to V_{BUS} too high, in addition to the normal $\overline{FLT}$ pin function.

Please refer to Table 6 for a lookup table linking the SEL1-3 pin states to the selected LT8698S states.

Dataline Switches

The LT8698S includes two High Speed USB 2.0 compliant analog switches. These switches are placed in series with the USB D^+ and D^- datalines between the USB socket and the host µController. The switches connect the HD^+ pin to the LD^+ pin and the HD^- pin to the LD^- pin of the LT8698S. The switches disconnect to protect the host from an up to 20V fault or an ESD strike on the dataline. The switches also disconnect when commanded to do so by the SEL1-3 pin inputs, such as when muxing in one of the various charger emulation profiles.

The USB 2.0 specification document requires that the D^+ and D^- datalines maintain a characteristic impedance in the PCB traces and be terminated for high speed 480Mb/s communication. Specifically, the dataline single ended impedance for D^+ and D^- to PCB ground is 45Ω and the differential impedance across D^+ to D^- is 90Ω. The LT8698S datalines switches and package have 3Ω typical series resistance and present about 6pF parallel capacitance at high frequency from each dataline to ground. The 3Ω of real resistance from the $R_{DS(ON)}$ of the switches is small enough relative to the 45Ω termination to not cause a signal integrity problem on the eye diagram. To eliminate signal reflections on the dataline from the 6pF capacitive discontinuity created by the dataline switches, add four small inductors between HD^+, HD^-, LD^- and LD^- and the corresponding dataline PCB trace. Place these inductors as close as possible to the LT8698S. The total series inductance on each dataline should be about 20nH for good impedance matching, so 10nH on each dataline pin HD^+, HD^-, LD^+ and LD^- is recommended. Minimum 10nH inductor tied in series to HD^+, HD^-, LD^+ and LD^- are required for robustness to IEC61000-4-2 ESD strikes to the HD^+ and HD^- pins.

To further ensure good high speed USB 2.0 signal integrity, the dataline bandwidth is production-tested on all parts.

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Table 6. Select Pin Lookup Table

SELECT PIN INPUT			SELECT STATE	STATE NAME	V_{BUS} STATE	HD+ STATE	HD– STATE	STATUS FUNCTION
SEL1	SEL2	SEL3						
LOW	LOW	LOW	0	USB CDP 1	5V	CDP Sequence, Short to LD+	CDP Sequence, Short to LD–	Indicates CDP State
TRI	LOW	LOW	1	USB CDP 2	5V	CDP Sequence with 20k to GND, Then Short to LD+	CDP Sequence with 20k to GND, Then Short to LD–	Indicates CDP State
HIGH	LOW	LOW	2	USB CDP 3	5V	Short to LD+	Short to LD–	Indicates Successful CDP Negotiation
LOW	TRI	LOW	3	USB SDP 1	0V	Short to LD+, 20k to GND	Short to LD–, 20k to GND	Indicates V_{BUS} Voltage
TRI	TRI	LOW	4	USB SDP 2	5V	Short to LD+, 20k to GND	Short to LD–, 20k to GND	Indicates I_{BUS} Current
HIGH	TRI	LOW	5	USB SDP 3	Discharge	Short to LD+, 20k to GND	Short to LD–, 20k to GND	Indicates V_{BUS} Discharge State
LOW	HIGH	LOW	6	Null	5V	Open	Open	Oscillates
TRI	HIGH	LOW	7	Null	5V	Open	Open	Oscillates
HIGH	HIGH	LOW	8	Null	5V	Open	Open	Oscillates
LOW	LOW	TRI	9	V_{BUS} Off with Data Pass Through	0V	Short to LD+	Short to LD–	Indicates V_{BUS} Voltage
TRI	LOW	TRI	10	V_{BUS} On with Data Pass Through	5V	Short to LD+	Short to LD–	Indicates I_{BUS} Current
HIGH	LOW	TRI	11	V_{BUS} Off and Discharged with Data Pass Through	Discharge	Short to LD+	Short to LD–	Indicates V_{BUS} Discharge State
LOW	TRI	TRI	12	V_{BUS} Off	0V	Open	Open	Indicates V_{BUS} Voltage
TRI	TRI	TRI	13	V_{BUS} On without Data Pass Through	5V	Open	Open	Reset State, STATUS Pin Indicates I_{BUS}
HIGH	TRI	TRI	14	V_{BUS} Off and Discharged without Data Pass Through	Discharge	Open	Open	Indicates V_{BUS} Discharge State
LOW	HIGH	TRI	15	Null	5V	Open	Open	Oscillates
TRI	HIGH	TRI	16	Null	5V	Open	Open	Oscillates
HIGH	HIGH	TRI	17	Null	5V	Open	Open	Oscillates
LOW	LOW	HIGH	18	USB SDP 4	0V	20k to GND	20k to GND	Indicates V_{BUS} Voltage
TRI	LOW	HIGH	19	USB SDP 5	5V	20k to GND	20k to GND	Indicates I_{BUS} Current
HIGH	LOW	HIGH	20	USB SDP 6	Discharge	20k to GND	20k to GND	Indicates V_{BUS} Discharge State
LOW	TRI	HIGH	21	USB DCP	5V	Short to HD–, 500k to GND	Short to HD+	Indicates I_{BUS} Current
TRI	TRI	HIGH	22	2.0A Charger	5V	Short to HD–, 1.25V V_{BUS} Divider	Short to HD+	Indicates I_{BUS} Current
HIGH	TRI	HIGH	23	Null	5V	Open	Open	Oscillates
LOW	HIGH	HIGH	24	2.4A Charger	5V	2.7V V_{BUS} Divider	2.7V V_{BUS} Divider	Indicates I_{BUS} Current
TRI	HIGH	HIGH	25	2.1A Charger	5V	2.7V V_{BUS} Divider	2.0V V_{BUS} Divider	Indicates I_{BUS} Current
HIGH	HIGH	HIGH	26	1.0 Charger	5V	2.0V V_{BUS} Divider	2.7V V_{BUS} Divider	Indicates I_{BUS} Current

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Internal diodes are connected between each pin, HD+ and HD–, to both CLAMP and ground as shown in Figure 10. In a similar way, internal diodes also connect each pin, LD+ and LD– to both $INTV_{CC}$ and ground. These diodes protect the host side dataline pins during ESD events. High speed comparators on the HD+ and HD– pins disconnect the dataline switches if the voltage on the datalines is too high. This disconnect threshold is a diode above 4.3V.

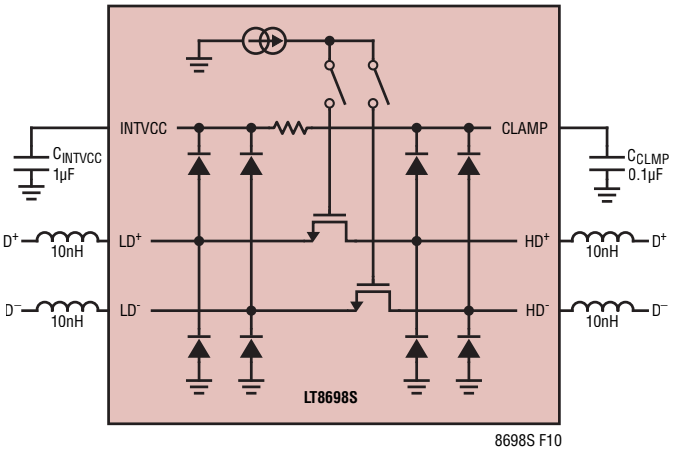

Figure 10. Dataline Switches

An integrated charge pump provides the voltage required to bias the NMOS gates of the dataline switches. This charge pump takes about 1ms to fully turn on the dataline switches after commanded to do so by the SEL1-3 pins state.

Clamp Pin

The CLAMP pin connects to the cathodes of two large diodes connected to HD+ and HD–. For positive ESD strikes on the datalines, high ESD current is shunted from the dataline through the diodes to the CLAMP pin. The capacitor on the clamp pin absorbs this energy, and a resistive divider on the CLAMP pin dissipates this energy over about 10ms. For an 8kV Contact Discharge IEC61000-4-2 ESD strike to HD+ or HD–, the CLAMP pin will increase in voltage momentarily from 4V to about 18V and then decay back down to 4V. See Figure 11 for a oscilloscope capture of this ESD event. Window comparators on the CLAMP pin disconnect the dataline switches if the CLAMP voltage is > 4.3V.

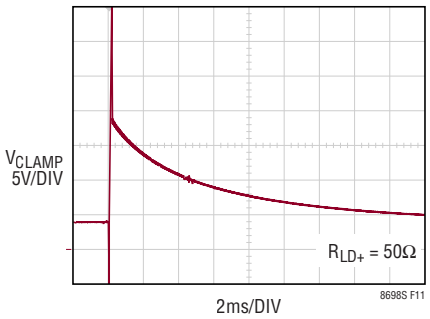

Figure 11. IEC61000-4-2 15kV Air Discharge ESD Strike

Tie a 0.1µF ceramic cap with at least a 25V rating from the CLAMP pin to GND for robust ESD and DC fault performance.

Fast cable faults can result in overshoot over the fault voltage on the HD+, HD– and CLAMP pins due to the cable inductance. A zener clamp diode can also be added from CLAMP to ground in parallel with the 0.1µF cap to limit excessive voltage overshoot from a DC fault with a fast step. Ensure that the zener breakdown voltage exceeds the maximum desired DC fault voltage on the HD+ and HD– pins under all operating conditions for robust operation. Diodes Inc DFLT22A or equivalent is a good choice. Figure 12a shows an example CLAMP circuit for robust tolerance to fast 20V cable faults to HD+ and HD–. See Figure 12b for a oscilloscope capture showing a fast 20V fault applied to HD+ through 3m of AWG 24 twisted pair cable with the Figure 12a CLAMP circuit.

CDP Modes of Operation

The LT8698S integrates the necessary hardware to implement the USB BC 1.2 Charging Downstream Port (CDP) charger profile. This mode of operation allows compliant devices to draw high current of up to 1.5A from V_{BUS} while simultaneously communicating with the host at high speed. CDP operates by inserting a simple handshake sequence into the normal USB connection sequence between a host and a portable device.

Per Table 6, select states 0, 1 and 2 operate CDP. Select state 0 performs the CDP sequence with the dataline switches closed and without termination. Select state 0 assumes the host µController will properly terminate the datalines for a USB connection and will otherwise not

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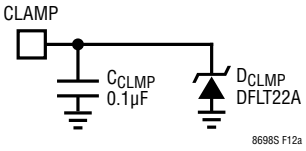
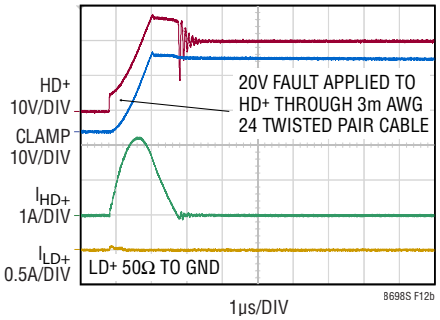


(a) CLAMP Circuit to Reduce Overshoot



(b) 20V Fault on HD+

Figure 12. Cable Faults

interfere with the LT8698S CDP sequence. Select state 0 keeps the dataline switches closed. Select state 1 performs the CDP sequence with the dataline switches open and 20k termination resistors tied from HD+ and HD– to GND. Select state 1 allows the LT8698S to handle the CDP sequence independently of the host µController and only connects the dataline switches after the CDP sequence is complete or the portable device attempts a connection without CDP. In select state 1, after the CDP sequence is complete, the internal 20k termination resistors are removed from the datalines and the dataline switches are closed.

When CDP is selected with either select 0 or select 1 states, the LT8698S connects a 100µA current source to D+, asserts STATUS low and waits for a device to attach to the USB socket. Once a device is attached, a CDP compliant device will place a 0.6V voltage source on D+ and a 100µA current source on D– for 40ms. The LT8698S will recognize 0.6V on D+ and will apply a 0.6V voltage source to D– within 20ms. This is CDP primary detection, and it indicates that the host port is either CDP or dedicated charger Port (DCP) capable. The LT8698S will also start to oscillate the STATUS pin with a 9ms period to indicate a CDP connection in progress. While the STATUS pin oscillates, the select pins are locked out from changing the LT8698S state.

The device will then remove the voltage source from D+ and the current source from D– and place a 100µA current source on D+ and a 0.6V voltage source on D– for 40ms. The LT8698S will respond by removing the 0.6V voltage source from D–. The LT8698S will monitor D– to see if the 0.6V voltage source is present for 40ms. This is secondary detection, and it indicates that the host port is CDP capable. The STATUS pin will continue to oscillate and the select pins will continue to be locked out.

The device can now charge from V_{BUS} at up to 1.5A and proceed to enumerate, pulling either D+ or D– above logic high to initiate a USB connection and to indicate the speed of the connection. When either D+ or D– is pulled above logic high, the LT8698S will remove the 100µA current source from D+ and the STATUS pin will stop oscillating and stay high, indicating that the CDP sequence is done. When STATUS is not oscillating, the select pins are no longer locked out.

This enumeration must occur within 1s of the initial attach when D+ is pulled to 0.6V or the LT8698S will stop the CDP handshake and return to the initial CDP state, waiting for a connection. If the device pulls D+ or D– above logic high during the CDP sequence before the sequence is completed, the LT8698S will interpret that the device is not CDP capable, will stop the CDP sequence, and indicate that the CDP handshake failed.

D+ or D– pulled above logic high will end the CDP handshake sequence. To restart CDP, the select pins must input any state other than select state 0, 1, or 2 and then be returned to the desired CDP input state.

Select state 2 allows the user to query if the CDP handshake sequence was successful or not. It is intended to be used after a portable device connects during select state 0 or 1. It does not affect the datalines, but after a connection, the STATUS pin will indicate if a successful CDP sequence was completed. While select state 2 is selected, STATUS high indicates a successful CDP connection, and STATUS low indicates an unsuccessful CDP connection. If select 2 is selected with neither select 0 nor 1 states

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having been selected nor a USB connection made, select 2 cannot return a valid response. In this case, select state 2 indicates an invalid response with a 9ms oscillation on the STATUS pin. Selecting any state other than select state 0, 1, or 2 clears the CDP connection information from the internal register.

Refer to Figure 13 and Figure 14 for a timing diagram of a successful CDP handshake sequence. Note, the LT8698S will report an unsuccessful CDP session if a portable device takes longer than 1 second to enumerate and connect. Select 2 accuracy can depend on a portable device's compliance to the USB specification, state, and configuration.

SDP Modes of Operation

The LT8698S implements the USB BC 1.2 Specification Standard Downstream Port (SDP). This is the most common USB host configuration and allows a device to draw up to 500mA of charge current. Select state 3, 4, 5, 18, 19 and 20 activate various versions of the LT8698S SDP modes. What is common to these states is the termination pull-down resistors that LT8698S places from D^+ and D^- to ground. The SDP modes differ by allowing the user to open or close the dataline switches, to power V_{BUS}, not power V_{BUS} or discharge V_{BUS}. See Table 6.

For SDP modes of operation with V_{BUS} in regulation (select states 4 and 19), STATUS high indicates I_{BUS} load >120mA and STATUS low indicates I_{BUS} load <100mA. For SDP modes of operation with V_{BUS} disabled (select states 3 and 18), STATUS high indicates V_{BUS} < 0.85V and STATUS low indicates V_{BUS} > 0.85V. For SDP modes of operation with V_{BUS} being discharged (select states 5 and 20), the STATUS pin indicates the discharge state. Refer to the Bus Reset Modes of Operation section for more details.

Data Pass Through Modes of Operation

The LT8698S implements several modes of operation that close the dataline switches to allow data to pass through the LT8698S but otherwise do not tie any resistor termination to the datalines. Select states 9, 10 and 11 activate various versions of the data pass through modes. What is common to these states is that the dataline switches are closed. These data pass through modes differ by allowing the user to power V_{BUS}, not power V_{BUS} or discharge V_{BUS}. See Table 6.

For data pass through mode of operation with V_{BUS} in regulation (select state 10), STATUS high indicates I_{BUS} load > 120mA and STATUS low indicates I_{BUS} load <100mA. For data pass through mode of operation with V_{BUS} disabled (select state 9), STATUS high indicates V_{BUS} < 0.5V and STATUS low indicates V_{BUS} > 0.85V. For data pass through mode of operation with V_{BUS} being discharged (select state 11), the STATUS pin indicates the discharge state. Refer to the Bus Reset Modes of Operation section for more details.

Charger Modes of Operation

The LT8698S implements several common USB charger profiles. These charger profiles have the datalines switches open and do not allow data communication. These charger profiles allow compatible devices to draw I_{BUS} current in excess of the 0.5A that a standard USB socket allows. The LT8698S includes the USB BC 1.2 Dedicated Charger Port (DCP) profile and vendor proprietary 2.0A, 2.4A, 2.1A and 1.0A profiles. These profiles tie various combinations of resistor dividers from V_{BUS} to the datalines or short the datalines together. See Table 6.

Select state 21 accesses the USB BC 1.2 DCP profile. This mode of operation connects a 100Ω short from D^+ to D^- and a 500kΩ resistor from D^+ and D^- to ground. This state allows compatible devices to draw 1.5A of charge current.

Select state 22 accesses the 2.0A vendor charger profile. This mode of operation connects a 100Ω short from D^+ to D^- and a 1.25V resistive divider from V_{BUS} to D^+ and D^-. This state allows compatible devices to draw 2.0A of charge current.

Select State 24 accesses the 2.4A vendor charger profile. This mode of operation connects two separate 2.7V resistive dividers from V_{BUS} to D^+ and D^-. This state allows compatible devices to draw 2.4A of charge current.

Select State 25 accesses the 2.1A vendor charger profile. This mode of operation connects a 2.7V resistive divider from V_{BUS} to D^+ and a 2.0V resistive divider from V_{BUS}

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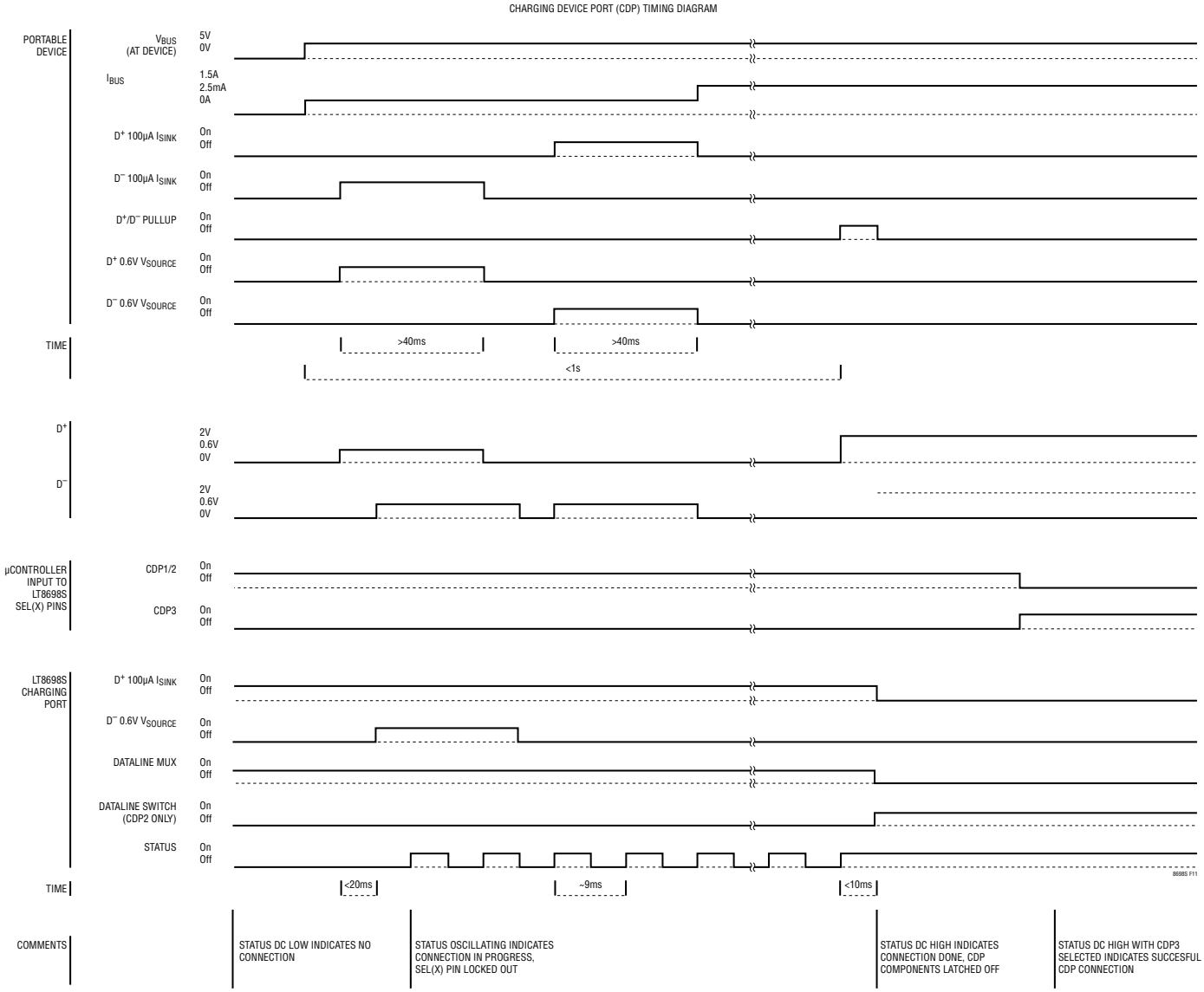

Figure 13. CDP Timing Diagram

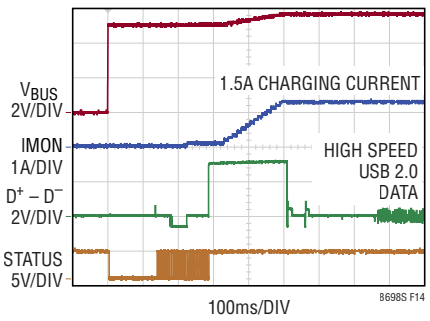

Figure 14. CDP Sequence

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to D^-. This state allows compatible devices to draw 2.1A of charge current.

Select State 26 accesses the 1.0A vendor charger profile. This mode of operation connects a 2.0V resistive divider from V_{BUS} to D^+ and a 2.7V resistive divider from V_{BUS} D^-. This state allows compatible devices to draw 1.0A of charge current.

For charger modes of operation (select states 21, 22, 24, 25 and 26), STATUS high indicates I_{BUS} load >120mA and STATUS low indicates I_{BUS} load <100mA.

V_{BUS} Only Modes of Operation

The LT8698S implements several modes of operation that manipulate V_{BUS} but leave the datalines switches open and do not tie any resistor termination to the datalines. Select states 12, 13 and 14 activate various versions of the V_{BUS} only modes. What is common to these states is that the dataline switches are open. These V_{BUS} only modes differ by allowing the user to power V_{BUS}, not power V_{BUS} or discharge V_{BUS}. See Table 6.

For the V_{BUS} only modes of operation with V_{BUS} in regulation (select state 13), STATUS high indicates I_{BUS} load >120mA and STATUS low indicates I_{BUS} load <100mA. For V_{BUS} only mode of operation with V_{BUS} disabled (select state 12), STATUS high indicates V_{BUS} < 0.5V and STATUS low indicates V_{BUS} > 0.85V. For V_{BUS} only mode of operation with V_{BUS} being discharged (select state 14), the STATUS pin indicates the discharge state. Refer to the Bus Reset Modes of Operation section for more details.

Bus Reset Modes of Operation

The LT8698S implements several modes of operation that discharge V_{BUS}. Select states 5, 11, 14 and 20 activate various versions of this V_{BUS} reset mode. What is common to these states is that the switcher stops delivering power to the V_{BUS} output, a 9mA current sink is tied from BUS/ISN to GND for 400ms, and the $\overline{FLT}$ pin can indicate an unsuccessful discharge for 4.2ms at the end of the discharge cycle. These V_{BUS} reset modes differ by tying various resistor terminations to the datalines or by opening or closing the dataline switches. See Table 6.

To initiate a bus reset sequence, normally the LT8698S is in a state with V_{BUS} powered up. The select pin's input state is then changed to the desired BUS reset mode. Within 1.5ms, switching stops and the LT8698S stops delivering power to the V_{BUS} output. Also, a 9mA current sink is connected from BUS/ISN to GND. The LT8698S will also start to oscillate the STATUS pin with a 9ms period to indicate a bus reset sequence in progress. While the STATUS pin oscillates, the select pins are locked out from changing the LT8698S state.

The LT8698S discharges V_{BUS} with the 9mA current sink for 400ms. After 400ms, the LT8698S turns off the current sink and measures the resultant V_{BUS} voltage for 120ms. If V_{BUS} is < 0.5V for 120ms, the discharge sequence is completed successfully. If V_{BUS} is > 0.85V at any point during this 120ms time, the discharge sequence is completed unsuccessfully.

When the discharge sequence is complete, the STATUS pin stops oscillating and pulls high, indicating that the bus reset is done and that the select pins are no longer locked out. If the bus reset was completed successfully, the $\overline{FLT}$ pin does not change state. If the bus reset was not completed successfully, the $\overline{FLT}$ pin pulls low for 4.2ms.

Refer to Figure 15 and Figure 16 for a timing diagram of unsuccessful and successful BUS reset sequences.

V_{BUS} Off Modes of Operations

The LT8698S is compatible with the USB On-The-Go (OTG) and Embedded Host 2.0 Specification. This specification allows hosts and peripheral devices to exchange roles. This role exchange means that V_{BUS} may be driven by the peripheral device on the B side of the USB connection. The LT8698S offers V_{BUS} off modes of operation with a high input resistance on V_{BUS} that allow a portable device to drive V_{BUS}. The LT8698S does not support the Attach Detect Protocol (ADP) on the A side, but as a piece of the A side device the LT8698S is compatible with ADP on the B side.

Select state 3, 9, 12 and 18 activate various versions of the LT8698S V_{BUS} off modes. What is common to these states is that switching is disabled and that the V_{BUS} input resistance is > 10kΩ. The V_{BUS} off modes differ by

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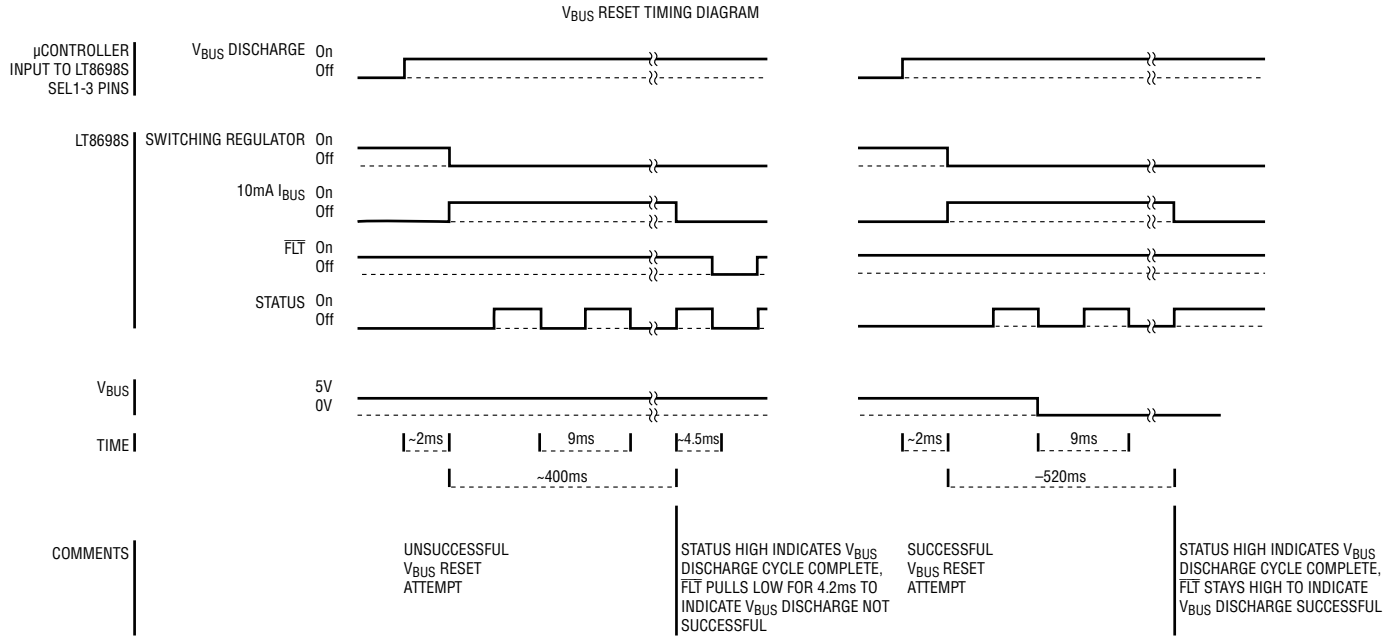
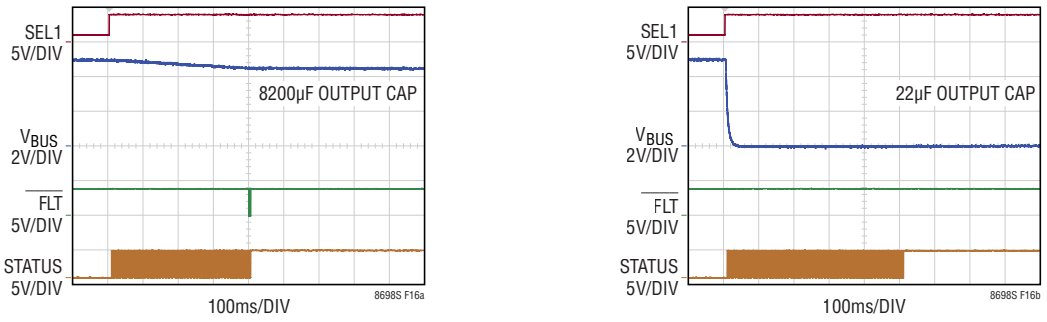


Figure 15. V_{BUS} RESET Diagram



(a) Unsuccessful Bus Reset

(b) Successful Bus Reset

Figure 16. V_{BUS} RESET Sequence

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allowing the user terminate the datalines with 20k and open or close the dataline switches in any combination. See Table 6.

For V_{BUS} off modes of operation, STATUS high indicates V_{BUS} < 0.5V and STATUS low indicates V_{BUS} > 0.85V.

Null Modes of Operation

The LT8698S does not use all of the 27 possible select pin tristate input combinations. The unused select states are states 6, 7, 8, 15, 16, 17 and 23. These unused states are called Null states in Table 6. These null states all behave the same. The switching regulator is active and powering V_{BUS}, the dataline switches are open with no resistor termination tied to the datalines, and the STATUS pin oscillates at 9ms indicating an invalid select state.

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 17 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT8698S's V_{IN} pins, PGND pins, and the input capacitors. The loop formed by the input capacitor should be made as small as possible by placing the capacitor adjacent to the V_{IN} and PGND pins. When using a physically large input capacitor the resulting loop may become too large in which case using a small case/value capacitor placed close to the V_{IN} and PGND pins plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BST nodes should be as small as possible. Finally, keep the USB5V and RT nodes short and use ground traces to shield them from the SW and BST nodes as needed.

Care should be taken in the layout of the PCB to ensure good heat sinking of the LT8698S. The exposed pads on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat

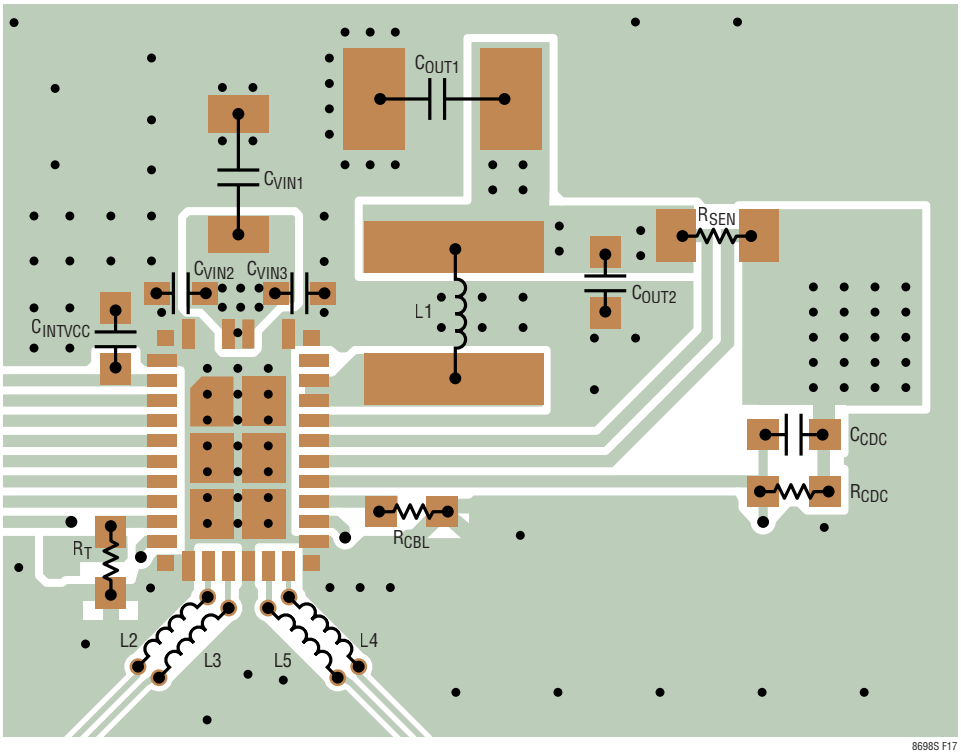


Figure 17. Recommended PCB Layout

APPLICATIONS INFORMATION

dissipated by the LT8698S. Placing additional vias can reduce thermal resistance further.

Use good 4-point Kelvin PCB layout for the R_{SEN} resistor and the associated connections to OUT/ISP and BUS/ISN pins. This resistor is only 8 to 10mΩ, so stray PCB resistance can easily add a temperature dependent error to the resistance seen by the OUT/ISP and BUS/ISN, producing inaccurate cable drop compensation and output current limit. Route the high current path from the inductor to the R_{SEN} resistor and from the R_{SEN} resistor to the V_{BUS} power output separately from the OUT/ISP and BUS/ISN pin connections. Keep high current off of the traces to the OUT/ISP and BUS/ISN pins.

The exposed pads act as a heat sink and are connected electrically to ground. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT8698S to additional ground planes within the circuit board and on the bottom side. See Figure 17 for example PCB layout.

High Temperature Considerations

The maximum load current the LT8698S delivers must be de-rated as the ambient temperature approaches the maximum junction temperature rating. Power dissipation within the LT8698S can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8698S power dissipation by the thermal resistance from junction to ambient.

The LT8698S will stop switching and indicate a fault condition if the internal thermal shutdown temperature is exceeded. The thermal shutdown temperature is above the maximum operating temperature and is only intended to help protect the LT8698S during an overload condition.

Temperature rise of the LT8698S is highest when operating at high load, high V_{IN}, and high switching frequency. If the case temperature is too high for a given application, then either V_{IN}, switching frequency or load current can be decreased to reduce the temperature to an acceptable level. Figure 18 shows the LT8698S junction temperature under common operating conditions measured for a typical part using demo board DC2688A.

Since the LT8698S temperature rise depends on these operating conditions and also on the PCB layout, airflow over the IC, and possibly on other nearby heat sources on the PCB, careful evaluation of a given application is required to ensure that the LT8698S does not exceed its maximum junction temperature rating.

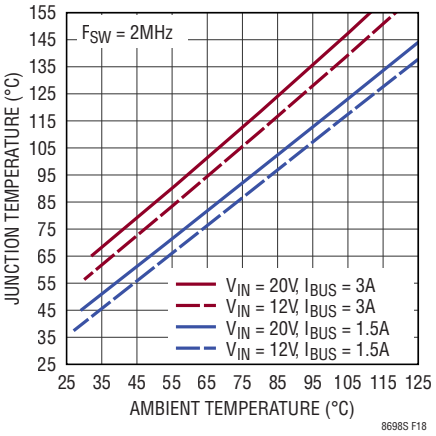
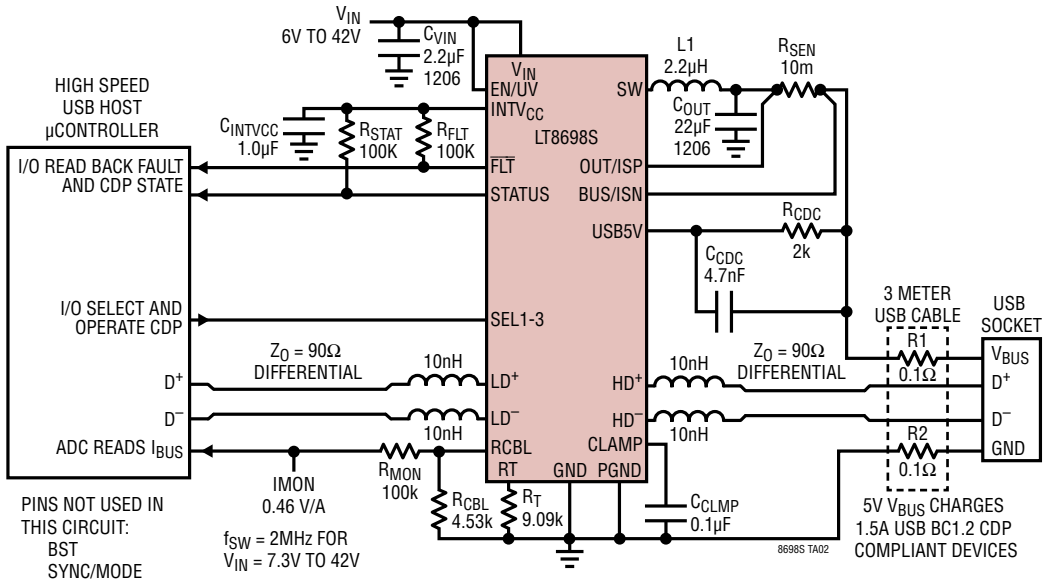


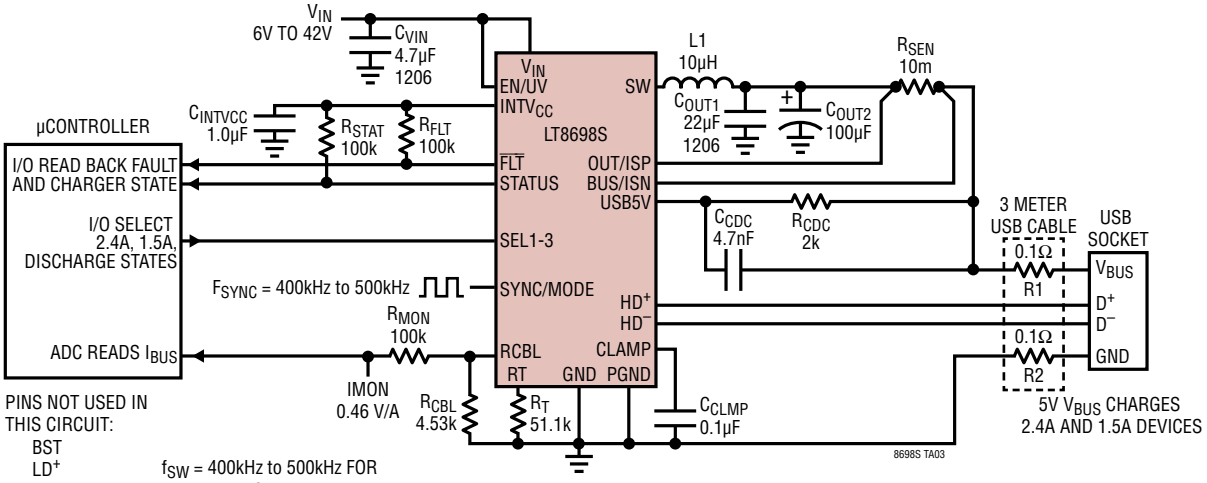
Figure 18. Junction Temperature Rise (DC2688A Demo Board with R_{SEN} = 8mΩ)

TYPICAL APPLICATIONS

Automotive USB BC1.2 CDP Charger with High Speed Dataline Protection and Cable Drop Compensation

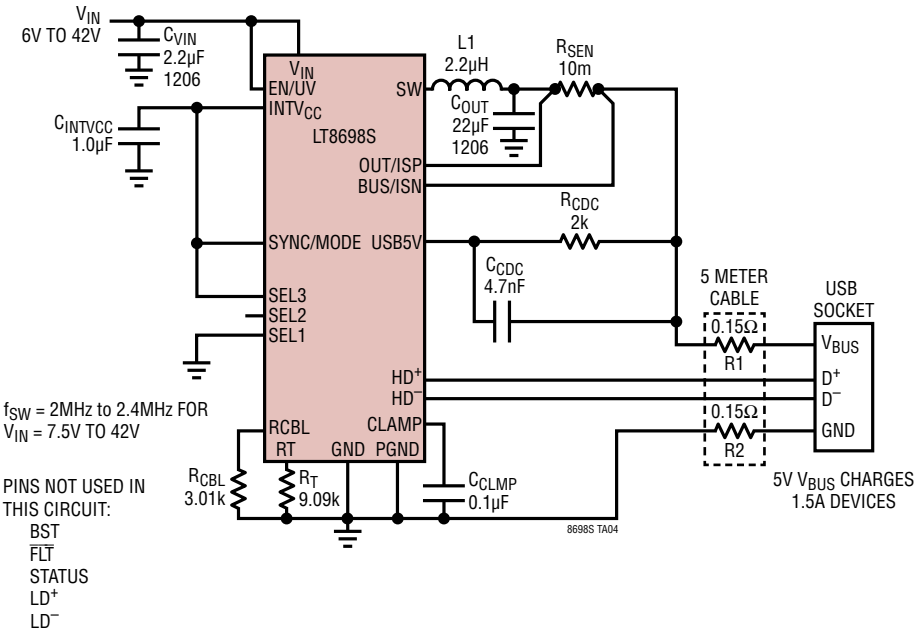


2.4A/1.5A Automatic Profile Detection Charger with Current Monitor

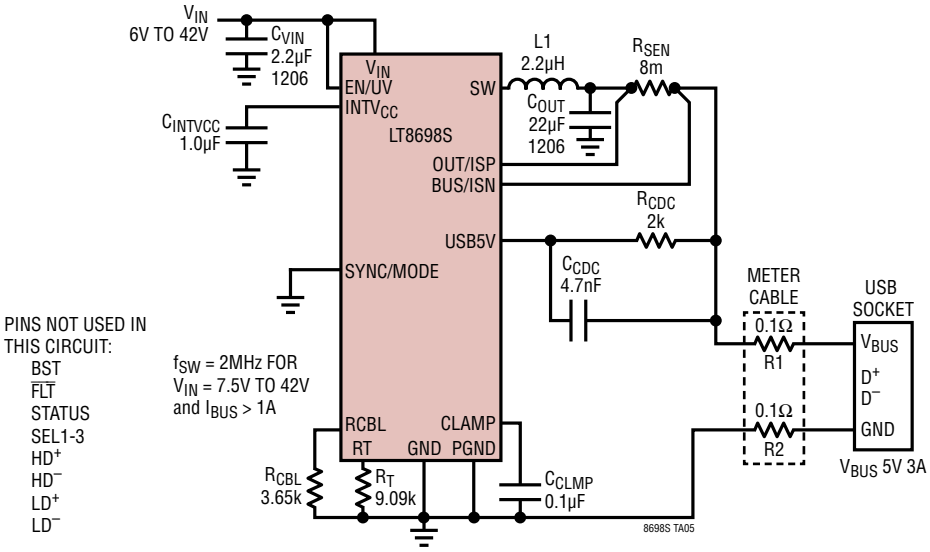


TYPICAL APPLICATIONS

USB Dedicated Charge Port (DCP) V_{BUS} Regulator with Spread Spectrum Modulation for Low EMI/EMC

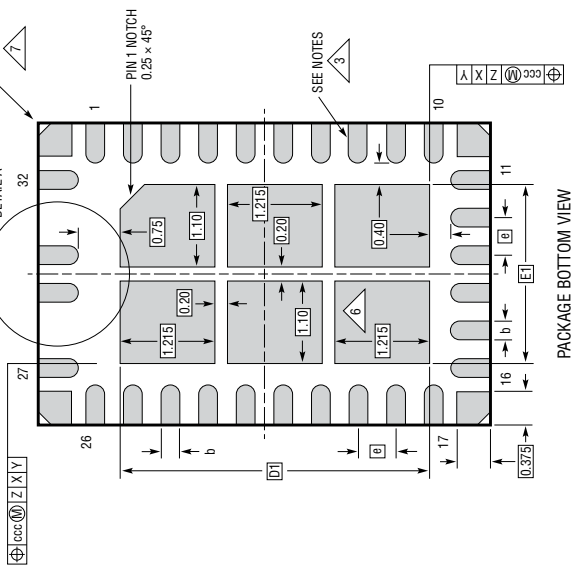


USB 5V, 3A V_{BUS} Regulator with Cable Drop Compensation and Low Quiescent Current

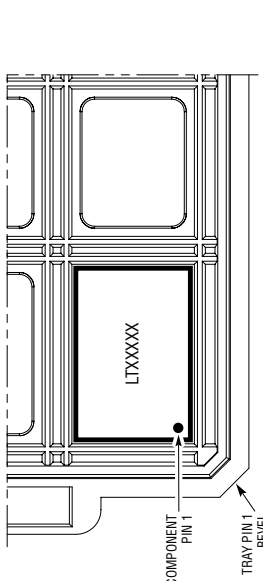


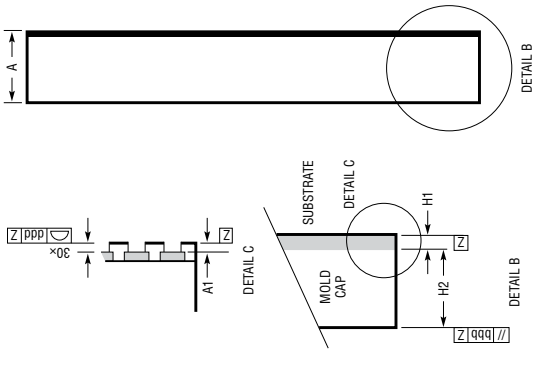
PACKAGE DESCRIPTION

LQFN Package
32(30)-Lead (6mm × 4mm × 0.94mm)
(Reference LTC DWG # 05-08-1558 Rev A)

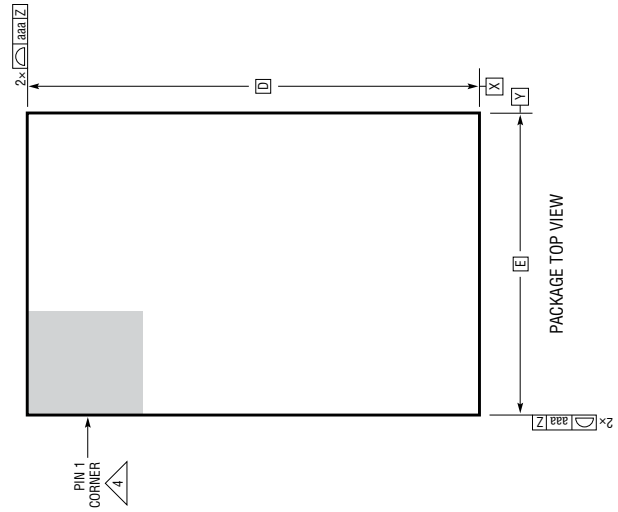


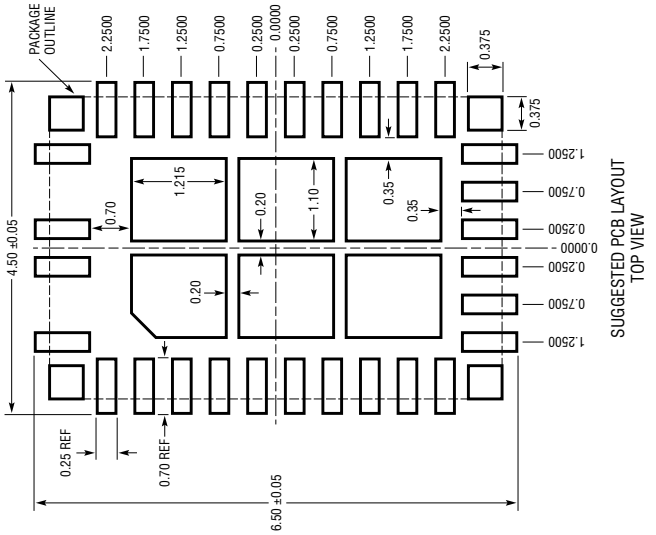
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL





DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.94	1.03	
A1			0.03	
b	0.22	0.25	0.28	
D		6.00		
E		4.00		
e		0.50		
D1		4.045		
E1		2.40		
H1		0.24 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.08	
ddd			0.10	
eee			0.15	
fff			0.08	





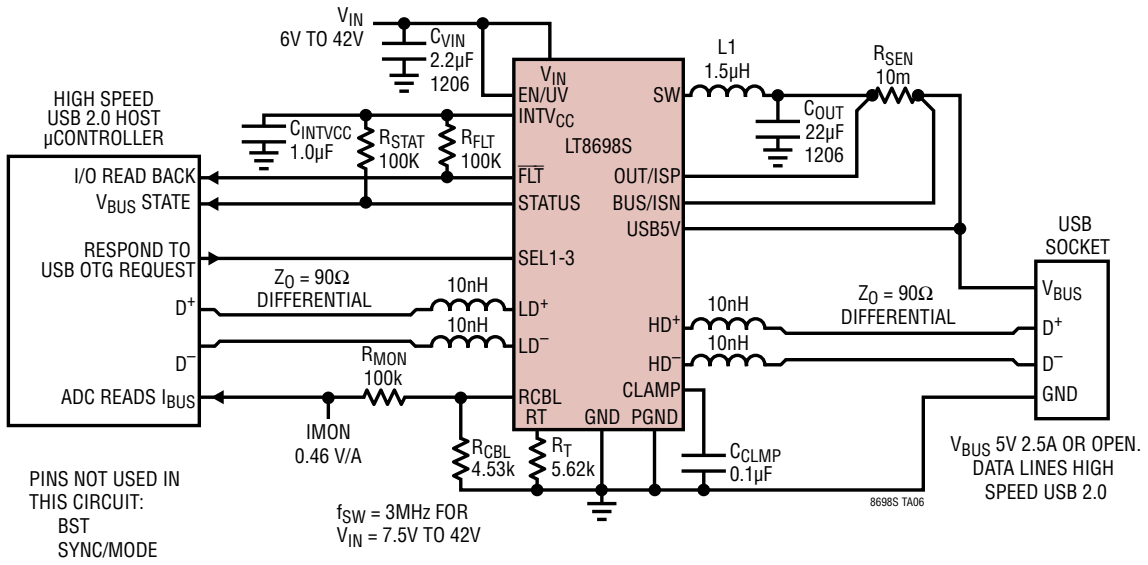
Rev. B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/21	AEC-Q100 statement updated.	1
B	08/21	Addition of Tape and Reel option.	2

TYPICAL APPLICATION

V_{BUS} Regulator with USB On-The-Go Functionality and High Speed USB 2.0 Dataline Protection



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8697	5V USB, 42V Input, 2.5A, 95% Efficiency, 2.2MHz Synchronous Step-Down DC/DC Converter with Cable Drop Compensation	$V_{IN(MIN)}$ = 5V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 5.0V to 5.25V, I_{SD} <1µA, 3mm × 5mm QFN-24 Package
LT3697	5V USB, 35V Input, 60V Transient, 2.5A, 2.2MHz Step-Down DC/DC Converter with Cable Drop Compensation	$V_{IN(MIN)}$ = 5V, $V_{IN(MAX)}$ = 35V (Transient to 60V), $V_{OUT(MIN)}$ = 5.0V to 5.25V, ISD <1µA, MSOP-16E Package
LT8650S	42V Dual 4A, 95% Efficiency, 2.2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 6.2µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 6.2µA, I_{SD} <2µA, 4mm × 6mm LQFN-32 Package
LT8652S	18V Dual 8.5A, 94% Efficiency, 2.2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 16µA	V_{IN} = 3V to 18V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 16µA, I_{SD} <6µA, 4mm × 7mm LQFN-36 Package
LT8653S	42V Dual 2A, 94% Efficiency, 2.2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 6.2µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 6.2µA, I_{SD} <2µA, 4mm × 3mm LQFN-20 Package
LT8636	42V 5A, 95% Efficiency, 2MHz Synchronous Silent Switcher Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} <1µA, 4mm × 3mm LQFN-20 Package
LT8648S	42V 15A, 95% Efficiency, 2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 6.2µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 100µA in Burst Mode Operation 7mm × 4mm LQFN-36 Package
LT8611	42V, 2.5A, 946% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA and Input/Output Current Limit/Monitor	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 5mm QFN-24 Package
LT6110	Cable/Wire Drop Compensator	$V_{IN(MIN)}$ = 2V, $V_{IN(MAX)}$ = 50V, $V_{OUT(MIN)}$ = 0.4V, I_Q = 16µA, SOT-8, 2mm × 2mm DFN-8 Packages
LT4180	Virtual Remote Sense Controller	$V_{IN(MIN)}$ = 3.1V, $V_{IN(MAX)}$ = 50V, Transient to 80V, I_Q = 1mA, SSOP-24 Package

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