

DICE/DWF SPECIFICATION

LTC2662-16 5-Channel, 300mA Current-Source-Output 16-Bit SoftSpan™ DACs

PAD FUNCTION

DIE CROSS REFERENCE



10. REF 26 11. REFCOMP 27 12. FSADJ 28	8. GND 24. OU 9. REFLO 25. V _{DD}	7. LDAC 23. OUT1	6. $\overline{\text{CS}}/\text{LD}$ 22. V_{DD1}	5. SCK 21. V _{DD2}	4. SD0 20. OUT2	3 SDI 19 OUT3	1. GND 17. V _{DD4}
13. V _{CC} 29 14. GND 30	10. REF 26. V 11. REFCOMP 27. V ⁺ 12. FSADJ 28. MU 13. V _{CC} 29. IOV 14. GND 30. FAL	8. GND 24. OUTC 9. REFLO 25. V_{DD0} 10. REF 26. V^- 11. REFCOMP 27. V^+ 12. FSADJ 28. MUX 13. V_{CC} 29. IOV_{CC} 14. GND 30. FAUL	7. LDAC 23. OUT1 8. GND 24. OUT0 9. REFLO 25. V_{DD0} 10. REF 26. V^- 11. REFCOMP 27. V^+ 12. FSADJ 28. MUX 13. V_{CC} 29. IOV_{CC} 14. GND 30. FAUL	$\begin{array}{cccc} 6. \ \overline{\text{CS}/\text{LD}} & 22. \ \text{V}_{\text{DD1}} \\ 7. \ \overline{\text{LDAC}} & 23. \ \text{OUT1} \\ 8. \ \text{GND} & 24. \ \text{OUT0} \\ 9. \ \text{REFLO} & 25. \ \text{V}_{\text{DD0}} \\ 10. \ \text{REF} & 26. \ \text{V}^- \\ 11. \ \text{REFCOMP} & 27. \ \text{V}^+ \\ 12. \ \text{FSADJ} & 28. \ \text{MUX} \\ 13. \ \text{V}_{\text{CC}} & 29. \ \ 10\text{V}_{\text{CC}} \\ 14. \ \text{GND} & 30. \ \overline{\text{FAULI}} \end{array}$	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	2. IGP 16. V_{DD3} 3. SDI 19. $OUT3$ 4. SDO 20. $OUT2$ 5. \underline{SCK} 21. V_{DD2} 6. $\underline{CS/LD}$ 22. V_{DD1} 7. $LDAC$ 23. $OUT1$ 8. GND 24. $OUT0$ 9. $REFLO$ 25. V_{DD0} 10. REF 26. V^- 11. $REFCOMP$ 27. V^+ 12. $FSADJ$ 28. MUX 13. V_{CC} 29. IOV_{CC} 14. GND 30. $FAULT$
13. V _{CC} 29 14. GND 30 15. V [−] 31	10. REF 26. V^- 11. REFCOMP 27. V^+ 12. FSADJ 28. MU 13. V_{CC} 29. IOV 14. GND 30. FAL 15. V^- 31. CLF	8. GND 24. OUTC 9. REFLO 25. V_{DD0} 10. REF 26. V^- 11. REFCOMP 27. V^+ 12. FSADJ 28. MUX 13. V_{CC} 29. IOV_{CC} 14. GND 30. FAUL 15. V^- 31. CLR	7. LDAC 23. OUT1 8. GND 24. OUT0 9. REFLO 25. V_{DD0} 10. REF 26. V^- 11. REFCOMP 27. V^+ 12. FSADJ 28. MUX 13. V_{CC} 29. IOV_{CC} 14. GND 30. FAUL 15. V^- 31. CLR	6. \overline{CS}/LD 22. V_{DD1} 7. $LDAC$ 23. $OUT1$ 8. GND 24. $OUT0$ 9. $REFLO$ 25. V_{DD0} 10. REF 26. V^- 11. $REFCOMP$ 27. V^+ 12. $FSADJ$ 28. MUX 13. V_{CC} 29. IOV_{CC} 14. GND 30. $FAULT$ 15. V^- 31. CLR	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	4. SD0 20. OUT2 5. SCK 21. V_{DD2} 6. $\overline{CS/LD}$ 22. V_{DD1} 7. LDAC 23. OUT1 8. GND 24. OUT0 9. REFL0 25. V_{DD0} 10. REF 26. V^- 11. REFCOMP 27. V^+ 12. FSADJ 28. MUX 13. V_{CC} 29. IOV_{CC} 14. GND 30. FAULT 15. V^- 31. CLR	2. IGP 10. V_{DD3} 3. SDI 19. $OUT3$ 4. SDO 20. $OUT2$ 5. SCK 21. V_{DD2} 6. \overline{CS}/LD 22. V_{DD1} 7. LDAC 23. $OUT1$ 8. GND 24. $OUT0$ 9. REFLO 25. V_{DD0} 10. REF 26. V^- 11. REFCOMP 27. V^+ 12. FSADJ 28. MUX 13. V_{CC} 29. IOV_{CC} 14. GND 30. FAULT 15. V^- 31. CLR
13. V _{CC} 29 14. GND 30 15. V ⁻ 31	10. REF 26. V 11. REFCOMP 27. V ⁺ 12. FSADJ 28. MU 13. V _{CC} 29. IOV 14. GND 30. FAL 15. V 31. CLF 16. OUT4 32. GNI	8. GND 24. OUTC 9. REFLO 25. V_{DD0} 10. REF 26. V^- 11. REFCOMP 27. V^+ 12. FSADJ 28. MUX 13. V_{CC} 29. IOV_{CC} 14. GND 30. FAUL 15. V^- 31. CLR 16. OUT4 32. GND	7. $\overline{\text{LDAC}}$ 23. $\overline{\text{OUT1}}$ 8. $\overline{\text{GND}}$ 24. $\overline{\text{OUT0}}$ 9. $\overline{\text{REFLO}}$ 25. V_{DD0} 10. $\overline{\text{REF}}$ 26. V^- 11. $\overline{\text{REFCOMP}}$ 27. V^+ 12. $\overline{\text{FSADJ}}$ 28. $\overline{\text{MUX}}$ 13. V_{CC} 29. $\overline{\text{IOV}_{CC}}$ 14. $\overline{\text{GND}}$ 30. $\overline{\text{FAUL}}$ 15. V^- 31. $\overline{\text{CLR}}$ 16. $\overline{\text{OUT4}}$ 32. $\overline{\text{GND}}$	6. \overline{CS}/LD 22. V_{DD1} 7. \overline{LDAC} 23. $OUT1$ 8. GND 24. $OUT0$ 9. $REFLO$ 25. V_{DD0} 10. REF 26. V^- 11. $REFCOMP$ 27. V^+ 12. $FSADJ$ 28. MUX 13. V_{CC} 29. IOV_{CC} 14. GND 30. $FAULT$ 15. V^- 31. \overline{CLR} 16. $OUT4$ 32. GND	5. SCK 21. V_{DD2} 6. \overline{CS}/LD 22. V_{DD1} 7. \overline{LDAC} 23. $OUT1$ 8. GND 24. $OUT0$ 9. $REFLO$ 25. V_{DD0} 10. REF 26. V^- 11. $REFCOMP$ 27. V^+ 12. $FSADJ$ 28. MUX 13. V_{CC} 29. IOV_{CC} 14. GND 30. $FAULT$ 15. V^- 31. CLR 16. $OUT4$ 32. GND	4. SD0 20. OUT2 5. SCK 21. V_{DD2} 6. $\overline{CS/LD}$ 22. V_{DD1} 7. LDAC 23. OUT1 8. GND 24. OUT0 9. REFLO 25. V_{DD0} 10. REF 26. V ⁻ 11. REFCOMP 27. V ⁺ 12. FSADJ 28. MUX 13. V _{CC} 29. IOV _{CC} 14. GND 30. FAULT 15. V ⁻ 31. CLR 16. OUT4 32. GND	2. IGP 10. $VDD3$ 3. SDI 19. $OUT3$ 4. SDO 20. $OUT2$ 5. SCK 21. V_{DD2} 6. \overline{CS}/LD 22. V_{DD1} 7. $LDAC$ 23. $OUT1$ 8. GND 24. $OUTO$ 9. $REFLO$ 25. V_{DD0} 10. REF 26. V^- 11. $REFCOMP$ 27. V^+ 12. $FSADJ$ 28. MUX 13. V_{CC} 29. IOV_{CC} 14. GND 30. $FAULT$ 15. V^- 31. CLR 16. $OUT4$ 32. GND
	10. REF 26. V ⁻ 11. REFCOMP 27. V ⁺ 12 FSAD.I 28 MII	8. GND 24. OUTC 9. REFLO 25. V _{DD0} 10. REF 26. V ⁻ 11. REFCOMP 27. V ⁺ 12 FSADJ 28 MUX	7. LDAC 23. OUT1 8. GND 24. OUT0 9. REFLO 25. V _{DD0} 10. REF 26. V ⁻ 11. REFCOMP 27. V ⁺ 12 ESAD.I 28. MUX	6. CS/LD 22. V _{DD1} 7. LDAC 23. OUT1 8. GND 24. OUT0 9. REFLO 25. V _{DD0} 10. REF 26. V [−] 11. REFCOMP 27. V ⁺ 12. FSAD.I 28. MUX	5. SCK 21. V _{DD2} 6. <u>CS/LD</u> 22. V _{DD1} 7. LDAC 23. OUT1 8. GND 24. OUT0 9. REFLO 25. V _{DD0} 10. REF 26. V ⁻ 11. REFCOMP 27. V ⁺ 12. SAD.I 28. MUX	4. SD0 20. OUT2 5. SCK 21. V _{DD2} 6. <u>CS/LD</u> 22. V _{DD1} 7. LDAC 23. OUT1 8. GND 24. OUT0 9. REFLO 25. V _{DD0} 10. REF 26. V ⁻ 11. REFCOMP 27. V ⁺ 12 ESAD.I 28. MUX	2. IGP 16. V_{DD3} 3. SDI 19. $OUT3$ 4. SDO 20. $OUT2$ 5. \underline{SCK} 21. V_{DD2} 6. $\overline{CS/LD}$ 22. V_{DD1} 7. $LDAC$ 23. $OUT1$ 8. GND 24. $OUT0$ 9. $REFLO$ 25. V_{DD0} 10. REF 26. V^- 11. $REFCOMP$ 27. V^+ 12. $FSAD.I$ 28. $MIIX$

LTC Finished Order Part Number Part Number LTC2662-16 LTC2662-16DWF#6AJ LTC2662-16DICE#6AJ

Please refer to LTC2662-16 standard product data sheet for other applicable product information.

*DWF = DICE in wafer form.

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DICE/DWF ELECTRICAL TEST LIMITS

$T_1 = 2$	25°C.	Vcc =	IOVcc =	5V: V-	= -5V:	Vnnn_4 =	= 5V: V	+ = 5\	1:
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FSADJ = V_{CC} , V_{REF} = 1.25V External, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	ТҮР	MAX	UNITS
DC Performa	nce All Ranges (Note 2)		i			
	Resolution		16			Bits
	Monotonicity	(Note 1)	16			Bits
DNL	Differential Nonlinearity	(Note 1)		±0.2	±1	LSB
INL	Integral Nonlinearity	(Note 1)		±12	±64	LSB
IOS	Offset Error Current	(Note 1)		±0.1	±0.4	%FSR
GE	Gain Error (Note 2)	300mA, 200mA, 100mA Ranges		0.3	0.9	%FSR
		50mA, 25mA Ranges		0.4	1.2	%FSR
		12.5mA, 6.25mA, 3.125mA Ranges		0.7	1.5	%FSR
TUE	Total Unadjusted Error (Note 2)	300mA, 200mA, 100mA Ranges		0.4	1.4	%FSR
		50mA, 25mA Ranges		0.5	1.7	%FSR
		12.5mA, 6.25mA, 3.125mA Ranges		0.8	2	%FSR
DC Performa	ice					
V _{DROPOUT}	Dropout Voltage (V _{DDX} – V _{OUTX}) (Notes 2, 3)	$I_{OUTX} \le 200$ mA, $(V_{DDX} - V^{-}) = 4.75$ V		0.7	1	V
	Hi-Z Output Leakage Current	$I_{OUTX} = Hi-Z, (V_{DDX} - V^{-}) = 4.75V$		0.1	1	μA
R _{PULL-DOWN}	OUTX Pull-Down Switch Resistance to V ⁻ Supply	Span Code = 1000b, Sinking 50mA		8	12	Ω
Reference					•	
V _{REF}	Reference Output Voltage	Internal Reference	1.248	1.25	1.252	V
	•					Bev A

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LTC2662-16

DICE/DWF ELECTRICAL TEST LIMITS

 $T_J = 25^{\circ}C. V_{CC} = IOV_{CC} = 5V; V^- = -5V; V_{DD0-4} = 5V; V^+ = 5V;$

FSADJ = V_{CC} , V_{REF} = 1.25V External, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	ТҮР	MAX	UNITS
Power Supply						
V _{CC}	Analog Supply Voltage	V _{CC} Must Not Exceed V ⁺	2.85		5.5	V
IO _{VCC}	Digital I/O Supply Voltage		1.71		V _{CC}	V
V-	Negative Supply Voltage		-15.75		0	V
V ⁺	Positive Supply Voltage		2.85		V ⁻ + 33	V
V_{DD0} to V_{DD4}	Output Supply Voltages		2.85		V+	V
	Supply Current V _{CC}	All Ranges (Code = 0, All Channels)		2.6	3.8	mA
	Supply Current IOV _{CC}	All Ranges (Code = 0, All Channels)		0.01	2	μA
	Supply Current V ⁺	All Ranges (Code = 0, All Channels)		385	500	μA
	Supply Current V ⁻	All Ranges (Code = 0, All Channels)		2.3	3.2	mA
	Supply Current V _{DD0-4}	All Ranges (Code = 0, per Channel)		0.7	1.2	mA
I _{SLEEP}	Shutdown Current V _{CC}	(Note 4)		1	10	μA
	Shutdown Current IO _{VCC}	(Note 4)		0.01	2	μA
	Shutdown Current V ⁺	(Note 4)		20	45	μA
	Shutdown Current V ⁻	(Note 4)		30	65	μA
	Shutdown Current V _{DD0-4}	(Note 4) per Channel		4.2	8.1	μA

Note 1: Linearity is defined from code 384 to code 65,535. Offset current is measured at code 384.

Note 3: Test conditions: 200mA range; $I_{OUTx} = 100$ mA.

Note 4: Digital Inputs at 0V or IOV_{CC} .

Note 2: Wafer probe testing is performed at output currents of up to 100mA. Output currents over 100mA are guaranteed by design and characterization.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

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Rev. A



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