

**2-Channel ±60V Power System Manager**

**FEATURES**

- **Sequence, Trim, Margin, Supervise, Manage and Log Faults, and Monitor Telemetry of Two Power Supplies**
- **Monitor Input Voltage from 0V to 60V, Input Current to Within 1%, and Accumulate Energy**
- **Manage Outputs from -60V to 60V and Margin or Trim to within 0.25%**
- **1.8V to 3.3V PMBus/SMBus/I<sup>2</sup>C Compliant Serial Interface**
- **Supported by LTpowerPlay® GUI**
- **Coordinate Sequencing and Fault Management Across Multiple ADI PSM Devices**
- **Operate Autonomously Without Additional Software**
- **Connect Directly to Regulator IMON Pins**
- **Can Be Powered from 3.3V, or 4.5V to 60V**
- **Available in a 49-Pin 7mm × 7mm BGA Package**

**APPLICATIONS**

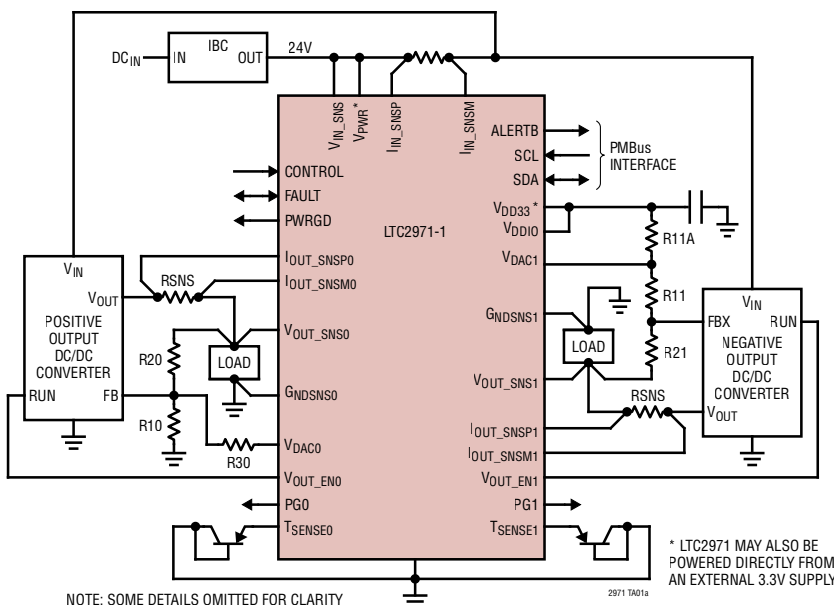
- **Computers and Network Servers**
- **Industrial Test and Measurement**
- **High Reliability Systems**
- **Video and Medical Imaging**

**DESCRIPTION**

The **LTC®2971**, LTC2971-1, LTC2971-2, and LTC2971-3 are 2-channel high voltage Power System Managers used to sequence, trim (servo), margin, supervise, manage faults, provide telemetry and log faults. DACs use a proprietary soft-connect algorithm to minimize supply disturbances. Supervisory functions include over and under voltage and temperature threshold limits for two power supply output channels and one input channel. Programmable fault responses can disable the power supplies, configure retry, and trigger black box EEPROM storage of fault status and associated telemetry. An internal 16-bit ADC monitors two output voltages, two output currents, two external temperatures, input voltage and current, and die temperature. Input power, energy, and output power are also calculated. A programmable watchdog timer monitors microprocessor activity and resets if necessary. A single wire bus synchronizes power supplies across multiple ADI Power System Management (PSM) devices. Configuration EEPROM with ECC supports autonomous operation without additional software.

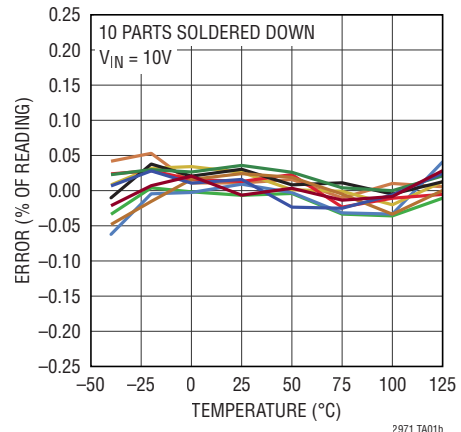
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**TYPICAL APPLICATION**



OPTION	CHANNEL 0	CHANNEL 1
LTC2971	0V TO 60V	0V TO 60V
LTC2971-1	0V TO 60V	-60V TO 0V
LTC2971-2	-60V TO 0V	-60V TO 0V
LTC2971-3	0V TO 60V	0V TO 1.8V

**Closed-Loop Servo Error vs Temperature**



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## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

### Supply Voltages:

$V_{PWR}$ .....	-0.3V to 63V
$V_{PWR}$ Current.....	-20mA
$V_{DD33}$ .....	-0.3V to 3.6V
$V_{DD25}$ .....	-0.3V to 2.75V

### Digital Input/Output Voltages:

ALERTB, SDA, SCL, CONTROL0, CONTROL1, PG[1:0], $V_{DDIO}$ .....	-0.3V to 3.6V
PWRGD, SHARE_CLK, WDI/RESETB, WP, FAULTB0, FAULTB1.....	-0.3V to 3.6V
ASELO, ASEL1.....	-0.3V to 3.6V

### Analog Voltages:

REFP.....	-0.3V to 1.35V
REFM.....	-0.3V to 0.3V
$V_{IN\_SNS}$ , $I_{IN\_SNSP}$ , $I_{IN\_SNSM}$ .....	-0.3V to 63V
$I_{IN\_SNSP}$ to $I_{IN\_SNSM}$ .....	-0.3V to 0.3V
$V_{OUT\_SNS0}$ , $I_{OUT\_SNSP0}$ , $I_{OUT\_SNSM0}$ LTC2971, LTC2971-1, LTC2971-3.....	-0.3V to 63V
LTC2971-2.....	-63V to 0.3V
$V_{OUT\_SNS1}$ , $I_{OUT\_SNSP1}$ , $I_{OUT\_SNSM1}$ LTC2971.....	-0.3V to 63V
LTC2971-1, LTC2971-2.....	-63V to 0.3V
LTC2971-3.....	-0.3V to 3V
$I_{OUT\_SNSP0}$ to $I_{OUT\_SNSM0}$ LTC2971, LTC2971-1, LTC2971-3.....	-0.3V to 3V
LTC2971-2.....	-0.3V to 0.3V
$I_{OUT\_SNSP1}$ to $I_{OUT\_SNSM1}$ LTC2971, LTC2971-3.....	-0.3V to 3V
LTC2971-1, LTC2971-2.....	-0.3V to 0.3V
$GND_{SNS[1:0]}$ .....	-0.3V to 0.3V
$V_{OUT\_EN[1:0]}$ , AUXFAULTB.....	-0.3V to 63V
$V_{DAC[1:0]}$ .....	-0.3V to 5.5V
$T_{SENSE[1:0]}$ .....	-0.3V to 3.6V

### Operating Junction Temperature Range:

LTC2971C, LTC2971C-1, LTC2971C-2, LTC2971C-3.....	0°C to 70°C
LTC2971I, LTC2971I-1, LTC2971I-2, LTC2971I-3.....	-40°C to 105°C
LTC2971H, LTC2971H-1, LTC2971H-2, LTC2971H-3.....	-40°C to 125°C

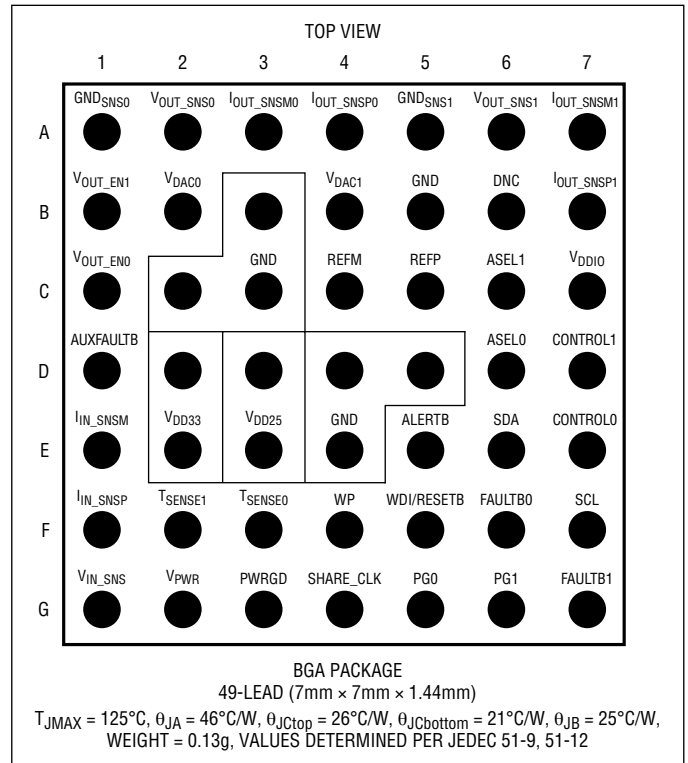
Storage Temperature Range ..... -65°C to 150°C\*

Maximum Junction Temperature ..... 125°C\*

Peak Solder Reflow Package Body Temperature... 260°C

\*See OPERATION section for detailed EEPROM derating information for junction temperatures in excess of 125°C.

## PIN CONFIGURATION



## ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	OPERATING JUNCTION TEMPERATURE RANGE
		DEVICE	FINISH CODE			
LTC2971CY#PBF	SAC305 (RoHS)	LTC2971Y	e1	BGA	3	0°C to 70°C
LTC2971IY#PBF						-40°C to 105°C
LTC2971HY#PBF						-40°C to 125°C
LTC2971CY-1#PBF	SAC305 (RoHS)	LTC2971Y-1	e1	BGA	3	0°C to 70°C
LTC2971IY-1#PBF						-40°C to 105°C
LTC2971HY-1#PBF						-40°C to 125°C
LTC2971CY-2#PBF	SAC305 (RoHS)	LTC2971Y-2	e1	BGA	3	0°C to 70°C
LTC2971IY-2#PBF						-40°C to 105°C
LTC2971HY-2#PBF						-40°C to 125°C
LTC2971CY-3#PBF	SAC305 (RoHS)	LTC2971Y-3	e1	BGA	3	0°C to 70°C
LTC2971IY-3#PBF						-40°C to 105°C
LTC2971HY-3#PBF						-40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. \*Pad or ball finish code is per IPC/JEDEC J-STD-609.
- [Recommended LGA and BGA PCB Assembly and Manufacturing Procedures](#)
- [LGA and BGA Package and Tray Drawings](#)

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_J = 25^\circ\text{C}$ .  $V_{PWR} = 12\text{V}$ ,  $V_{DDIO} = V_{DD33}, V_{DD33}, V_{DD25}$ , REFP, and REFV pins floating, unless otherwise indicated.  $C_{VDD33} = 100\text{nF}$ ,  $C_{VDD25} = 100\text{nF}$ , and  $C_{REF} = 100\text{nF}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Power Supply Characteristics</b>							
$V_{PWR}$	$V_{PWR}$ Supply Input Operating Range	$V_{DD33}$ Floating (Note 2)	●	4.5	60	V	
$I_{PWR}$	$V_{PWR}$ Supply Current	$4.5\text{V} \leq V_{PWR} \leq 60\text{V}$ , $V_{DD33}$ Floating (Note 2)	●	6	8.5	mA	
$I_{VDD33}$	$V_{DD33}$ Supply Current	$3.13\text{V} \leq V_{VDD33} \leq 3.47\text{V}$ , $V_{PWR} = V_{VDD33}$	●	6	8.5	mA	
$V_{UVLO\_VDD33}$	$V_{DD33}$ Undervoltage Lockout	$V_{DD33}$ Ramping Up, $V_{PWR} = V_{VDD33}$	●	2.25	2.55	2.8	V
	$V_{DD33}$ Undervoltage Lockout Hysteresis			120		mV	
$V_{DD33}$	Supply Input Operating Range	$V_{PWR} = V_{VDD33}$	●	3.13	3.47	V	
	Regulator Output Voltage	$4.5\text{V} \leq V_{PWR} \leq 60\text{V}$	●	3.13	3.26	3.47	V
	Regulator Output Short-Circuit Current	$V_{PWR} = 4.5\text{V}$ , $V_{VDD33} = 0\text{V}$ Includes Internal Current	●	20	30	40	mA
$V_{DD25}$	Regulator Output Voltage	$3.13\text{V} \leq V_{VDD33} \leq 3.47\text{V}$	●	2.35	2.5	2.6	V
	Regulator Output Short-Circuit Current	$V_{PWR} = V_{VDD33} = 3.47\text{V}$ , $V_{VDD25} = 0\text{V}$	●	30	55	80	mA
$t_{INIT}$	Initialization Time	Time from $V_{IN}$ applied until the TON_DELAY Timer Starts		30		ms	
$V_{DDIO}$	$V_{DDIO}$ Input Operating Range		●	1.62	3.6	V	
$R_{IN}$	$V_{DDIO}$ Input Resistance	$0 \leq V_{VDDIO} \leq 3.6\text{V}$	●	53	68.8	86	k $\Omega$

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_J = 25^\circ\text{C}$ .  $V_{VPWR} = 12\text{V}$ ,  $V_{VDD10} = V_{VDD33}, V_{VDD33}, V_{DD25}, \text{REFP}, \text{and REFm}$  pins floating, unless otherwise indicated.  $C_{VDD33} = 100\text{nF}$ ,  $C_{VDD25} = 100\text{nF}$ , and  $C_{REF} = 100\text{nF}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS		
<b>Voltage Reference Characteristics</b>								
$V_{REF}$	Output Voltage (Note 3)	$V_{REF} = V_{REFP} - V_{REFM}, 0 < I_{REFP} < 100\mu\text{A}$	●	1.215	1.230	1.245	V	
	Temperature Coefficient			3			ppm/ $^\circ\text{C}$	
	Hysteresis	(Note 4)		100			ppm	
<b>ADC Characteristics</b>								
$V_{IN\_ADC}$	Voltage Sense Input Range (Note 5)	Differential Voltage	LTC2971	●	0	60	V	
			$V_{VOUT\_SNS0} - V_{GNDNSNS0}$		0	60	V	
			$V_{VOUT\_SNS1} - V_{GNDNSNS1}$					
			LTC2971-1	●	0	60	V	
			$V_{VOUT\_SNS0} - V_{GNDNSNS0}$		-60	0	V	
$V_{VOUT\_SNS1} - V_{GNDNSNS1}$								
LTC2971-2	●	-60	0	V				
$V_{VOUT\_SNS0} - V_{GNDNSNS0}$		-60	0	V				
$V_{VOUT\_SNS1} - V_{GNDNSNS1}$								
LTC2971-3	●	0	60	V				
$V_{VOUT\_SNS0} - V_{GNDNSNS0}$		0	1.8	V				
$V_{VOUT\_SNS1} - V_{GNDNSNS1}$								
		Single-Ended Voltage: $V_{GNDNSNSn}$		-0.1	0.1	V		
	Current Sense Input Range $Mfr\_config\_imon\_sel = 0$	Single-Ended Voltage	LTC2971	●	3	60	V	
			$V_{IOUT\_SNSP/M0}$		3	60	V	
			$V_{IOUT\_SNSP/M1}$	●				
			LTC2971-1	●	3	60	V	
			$V_{IOUT\_SNSP/M0}$		-60	-0.5	V	
			$V_{IOUT\_SNSP/M1}$	●				
			LTC2971-2	●	-60	-0.5	V	
			$V_{IOUT\_SNSP/M0}$		-60	-0.5	V	
			$V_{IOUT\_SNSP/M1}$	●				
			LTC2971-3	●	3	60	V	
$V_{IOUT\_SNSP/M0}$		0	1.65	V				
$V_{IOUT\_SNSP/M1}$	●							
		Differential Current Sense Voltage: $V_{IOUT\_SNSPn} - V_{IOUT\_SNSMn}$	●	-80	80	mV		
	Current Sense Input Range $Mfr\_config\_imon\_sel = 1$ (Note 6)	Differential Current Sense Voltage	LTC2971, $V_{IOUT\_SNSPn} - V_{IOUT\_SNSMn}$	●	-0.1	1.8	V	
			LTC2971-1, $V_{IOUT\_SNSP0} - V_{IOUT\_SNSM0}$	●	-0.1	1.8	V	
			LTC2971-3, $V_{IOUT\_SNSPn} - V_{IOUT\_SNSMn}$	●	-0.1	1.8	V	
			Single-Ended Voltage: $V_{IOUT\_SNSMn}$	●	-0.1	0.1	V	
$N\_ADC$	Voltage Sense Resolution	$0\text{V} \leq  V_{IN\_ADC}  \leq 60\text{V}, \text{READ\_VOUT}$		4.5		mV/LSB		
		LTC2971-3, $0\text{V} \leq V_{VOUT\_SNS1} - V_{GNDNSNS1} \leq 1.8\text{V}, \text{READ\_VOUT}$		122		$\mu\text{V}/\text{LSB}$		
	Current Sense Resolution with $I_{OUT\_CAL\_GAIN} = 1\Omega$	$Mfr\_config\_imon\_sel = 0$			15.625		$\mu\text{A}/\text{LSB}$	
		$0\text{mV} \leq  V_{IN\_ADC}  \leq 16\text{mV}$ (Note 7)			31.25		$\mu\text{A}/\text{LSB}$	
		$16\text{mV} \leq  V_{IN\_ADC}  \leq 32\text{mV}$			62.5		$\mu\text{A}/\text{LSB}$	
$32\text{mV} \leq  V_{IN\_ADC}  \leq 63.9\text{mV}$			125		$\mu\text{A}/\text{LSB}$			
$63.9\text{mV} \leq  V_{IN\_ADC}  \leq 80\text{mV}$								
$Mfr\_config\_imon\_sel = 1$				62.5		$\mu\text{A}/\text{LSB}$		
Temperature Sense Resolution				0.0476		$^\circ\text{C}/\text{LSB}$		

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_J = 25^\circ\text{C}$ .  $V_{VPWR} = 12\text{V}$ ,  $V_{VDDIO} = V_{VDD33}, V_{VDD33}, V_{DD25}, \text{REFP}, \text{and REFEM}$  pins floating, unless otherwise indicated.  $C_{VDD33} = 100\text{nF}$ ,  $C_{VDD25} = 100\text{nF}$ , and  $C_{REF} = 100\text{nF}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TUE_ADC_VOUT	Total Unadjusted Error Voltage Sense Inputs (Note 3)	$10\text{V} \leq  V_{IN\_ADC}  \leq 60\text{V}$	●		$\pm 0.25$	% of Reading
		$0\text{V} \leq  V_{IN\_ADC}  \leq 10\text{V}$	●		$\pm 25$	mV
		LTC2971-3, $1\text{V} \leq V_{VOUT\_SNS1} - V_{GND\_SNS1} \leq 1.8\text{V}$	●		$\pm 0.25$	% of Reading
		LTC2971-3, $0\text{V} \leq V_{VOUT\_SNS1} - V_{GND\_SNS1} \leq 1\text{V}$			$\pm 2.5$	mV
TUE_ADC_IOUT	Total Unadjusted Error Current Sense Inputs (Note 3)	Mfr_config_imon_sel = 0 $20\text{mV} \leq  V_{IN\_ADC}  \leq 80\text{mV}$	●		$\pm 0.6$	% of Reading
		Mfr_config_imon_sel = 0 $ V_{IN\_ADC}  \leq 20\text{mV}$	●		$\pm 120$	$\mu\text{V}$
		Mfr_config_imon_sel = 1 $V_{IN\_ADC} \geq 1\text{V}$	●		$\pm 0.25$	% of Reading
		Mfr_config_imon_sel = 1 $0 \leq V_{IN\_ADC} \leq 1\text{V}$	●		$\pm 2.5$	mV
V <sub>OS_ADC</sub>	Offset Error	$V_{IOUT\_SNSPn} = V_{IOUT\_SNSMn}$ , $V_{OS} \cdot I_{OUT\_CAL\_GAIN}$ , $I_{OUT\_CAL\_GAIN} = 1000\text{m}\Omega$ Mfr_config_imon_sel = 0	●		$\pm 70$	$\mu\text{V}$
CMRR_IOUT	DC CMRR	$ V_{IOUT\_SNSPn} - V_{IOUT\_SNSMn}  = 80\text{mV}$ , over Single-Ended Voltage Range		135		dB
		LC2971-3, $ V_{IOUT\_SNSP1} - V_{IOUT\_SNSM1}  = 80\text{mV}$ , over Single-Ended Voltage Range		100		dB
t <sub>CONV_ADC</sub>	Conversion Time (Note 8)	$V_{OUT\_SNSn}, GND_{SNSn}, V_{IN\_SNS}$ Inputs		6.15		ms
		$I_{OUT\_SNSPn}, I_{OUT\_SNSMn}, I_{IN\_SNSPn}, I_{IN\_SNSMn}$ Inputs Mfr_config_imon_sel = 0		24.6		ms
		$I_{OUT\_SNSPn}, I_{OUT\_SNSMn}$ Inputs Mfr_config_imon_sel = 1		6.15		ms
		Internal Temperature (READ_TEMPERATURE_2)		24.6		ms
t <sub>UPDATE_ADC</sub>	Update Time (Note 8)	Mfr_ein_config_hd = 0		135		ms
		Mfr_ein_config_hd = 1		305		ms
f <sub>IN_ADC</sub>	Input Sampling Frequency			62.5		kHz

#### Sense Input Characteristics (Note 9)

R <sub>IN_VSENSE</sub>	Input Resistance	$V_{OUT\_SNSn}$ and $GND_{SNSn}$ Inputs	●	400	500	625	k $\Omega$
		LTC2971-3 $V_{OUT\_SNS1}$ and $GND_{SNS1}$ Inputs	●	500			k $\Omega$
I <sub>IN_IOUT_SNS</sub>	Input Current	$I_{OUT\_SNSPn}$ and $I_{OUT\_SNSMn}$ Inputs Mfr_config_imon_sel = 0	●			$\pm 10$	$\mu\text{A}$
		$I_{OUT\_SNSPn}$ and $I_{OUT\_SNSMn}$ Inputs Mfr_config_imon_sel = 1	●			$\pm 1$	$\mu\text{A}$
	Differential Input Current	$I_{OUT\_SNSPn}$ and $I_{OUT\_SNSMn}$ Inputs, $ V_{IN\_DIFF}  = 80\text{mV}$ , Mfr_config_imon_sel = 0	●		$\pm 0.1$		$\mu\text{A}$
		$I_{OUT\_SNSPn}$ and $I_{OUT\_SNSMn}$ Inputs, $ V_{IN\_DIFF}  = 80\text{mV}$ , Mfr_config_imon_sel = 1	●		$\pm 1$		$\mu\text{A}$

#### DAC Output Characteristics

N_VDAC	Resolution			10		Bits
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## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_J = 25^\circ\text{C}$ .  $V_{VPWR} = 12\text{V}$ ,  $V_{VDD10} = V_{VDD33}, V_{DD33}, V_{DD25}, \text{REFP}, \text{and REFm}$  pins floating, unless otherwise indicated.  $C_{VDD33} = 100\text{nF}$ ,  $C_{VDD25} = 100\text{nF}$ , and  $C_{REF} = 100\text{nF}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{FS\_VDAC}$	Full-Scale Output Voltage (Programmable)	DAC Code=0x3FF	●	1.3	1.38	1.44	V
		DAC Polarity=1	●	2.5	2.65	2.77	V
$INL\_VDAC$	Integral Nonlinearity	(Note 10)	●		±2	LSB	
$DNL\_VDAC$	Differential Nonlinearity	(Note 10)	●		±2.4	LSB	
$V_{OS\_VDAC}$	Offset Voltage	(Note 10)	●		±12	mV	
$V_{DAC}$	Load Regulation	$V_{DACn}$ programmed to 2.65V, $I_{VDACn} = 2\text{mA}$		0.5		Ω	
		$V_{DACn}$ programmed to 0.1V, $I_{VDACn} = -2\text{mA}$		0.5		Ω	
	PSRR	DC: $3.13\text{V} \leq V_{VDD33} \leq 3.47\text{V}$ , $V_{VPWR} = V_{VDD33}$		60		dB	
	Leakage Current	$V_{DACn}$ Hi-Z, $0\text{V} \leq V_{VDACn} \leq 5\text{V}$	●		±100	nA	
	Short-Circuit Current Low	$V_{DACn}$ Shorted to GND	●	-12	-2.5	mA	
	Short-Circuit Current High	$V_{DACn}$ Shorted to $V_{DD33}$	●	2.5	12	mA	
$C_{OUT}$	Output Capacitance	$V_{DACn}$ Hi-Z		10		pF	
$t_{S\_VDAC}$	DAC Output Update Rate	Fast Servo Mode		250		μs	

### Voltage Supervisor Characteristics

$V_{IN\_VS}$	Input Voltage Range (Programmable) (Note 5)	Differential Voltage, Low Resolution Mode	LTC2971	●	0	60	V
			$V_{VOUT\_SNS0} - V_{GNDSNS0}$	●	0	60	V
			$V_{VOUT\_SNS1} - V_{GNDSNS1}$	●	0	60	V
			LTC2971-1	●	0	60	V
			$V_{VOUT\_SNS0} - V_{GNDSNS0}$	●	-60	0	V
			$V_{VOUT\_SNS1} - V_{GNDSNS1}$	●	-60	0	V
		Differential Voltage, High Resolution Mode	LTC2971-2	●	-60	0	V
			$V_{VOUT\_SNS0} - V_{GNDSNS0}$	●	-60	0	V
			LTC2971-3	●	0	60	V
			$V_{VOUT\_SNS0} - V_{GNDSNS0}$	●	0	1.8	V
			$V_{VOUT\_SNS1} - V_{GNDSNS1}$	●	0	34	V
			$V_{VOUT\_SNS1} - V_{GNDSNS1}$	●	0	34	V
		Single-Ended Voltage: $V_{GNDSNSn}$	LTC2971-1	●	0	34	V
			$V_{VOUT\_SNS0} - V_{GNDSNS0}$	●	-34	0	V
$V_{VOUT\_SNS1} - V_{GNDSNS1}$	●		-34	0	V		
LTC2971-2	●		-34	0	V		
$V_{VOUT\_SNS0} - V_{GNDSNS0}$	●		-34	0	V		
$V_{VOUT\_SNS1} - V_{GNDSNS1}$	●		-34	0	V		
$N\_VS$	Voltage Sensing Resolution	Low Resolution Mode	LTC2971-3	●	0	34	V
			$V_{VOUT\_SNS0} - V_{GNDSNS0}$	●	0	1.5	V
		High Resolution Mode	$0\text{V} \leq  V_{IN\_VS}  \leq 60\text{V}$		70.4		mV/LSB
			$0\text{V} \leq  V_{IN\_VS}  \leq 34\text{V}$		35.2		mV/LSB
		LTC2971-3, $0\text{V} \leq V_{VOUT\_SNS1} - V_{GNDSNS1} \leq 1.8\text{V}$		3.2		mV/LSB	
		LTC2971-3, $0\text{V} \leq V_{VOUT\_SNS1} - V_{GNDSNS1} \leq 1.5\text{V}$		1.6		mV/LSB	



**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_J = 25^\circ\text{C}$ .  $V_{VPWR} = 12\text{V}$ ,  $V_{VDD10} = V_{VDD33}, V_{VDD33}, V_{DD25}, \text{REFP}, \text{and REFm}$  pins floating, unless otherwise indicated.  $C_{VDD33} = 100\text{nF}$ ,  $C_{VDD25} = 100\text{nF}$ , and  $C_{REF} = 100\text{nF}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
TUE_VS_VOUT	Total Unadjusted Error	Low Resolution Mode	$9\text{V} \leq  V_{IN\_VS}  \leq 60\text{V}$	●		$\pm 1.5$	% of Reading
			$0\text{V} \leq  V_{IN\_VS}  \leq 9\text{V}$	●		$\pm 135$	mV
			LTC2971-3, $0.5\text{V} \leq V_{VOUT\_SNS1} - V_{GND\SNS1} \leq 1.8\text{V}$	●		$\pm 1.25$	% of Reading
			LTC2971-3, $0\text{V} \leq V_{VOUT\_SNS1} - V_{GND\SNS1} \leq 0.5\text{V}$	●		$\pm 6$	mV
		High Resolution Mode	$4.5\text{V} \leq  V_{IN\_VS}  \leq 34\text{V}$	●		$\pm 1.25$	% of Reading
			$0\text{V} \leq  V_{IN\_VS}  \leq 4.5\text{V}$	●		$\pm 56$	mV
			LTC2971-3, $0.5\text{V} \leq V_{VOUT\_SNS1} - V_{GND\SNS1} \leq 1.5\text{V}$	●		$\pm 1.25$	% of Reading
			LTC2971-3, $0\text{V} \leq V_{VOUT\_SNS1} - V_{GND\SNS1} \leq 0.5\text{V}$	●		$\pm 6$	mV
tS_VS	Update Rate			12.21		$\mu\text{s}$	

#### V<sub>IN\_SNS</sub> Input Characteristics

V <sub>IN_SNS</sub>	V <sub>IN_SNS</sub> Input Voltage Range	(Note 11)	●	0	60	V	
R <sub>VIN_SNS</sub>	V <sub>IN_SNS</sub> Input Resistance		●	400	500	625	k $\Omega$
TUE_VS_VIN	VIN_ON, VIN_OFF Threshold Total Unadjusted Error	Low Resolution Mode	$9\text{V} \leq V_{IN\_SNS} \leq 60\text{V}$	●		$\pm 1.5$	% of Reading
			$0\text{V} \leq V_{IN\_SNS} \leq 9\text{V}$	●		$\pm 135$	mV
		High Resolution Mode	$4.5\text{V} \leq V_{IN\_SNS} \leq 34\text{V}$	●		$\pm 1.25$	% of Reading
			$0\text{V} \leq V_{IN\_SNS} \leq 4.5\text{V}$	●		$\pm 56$	mV
TUE_ADC_VIN	READ_VIN Total Unadjusted Error	$10\text{V} \leq V_{IN\_SNS} \leq 60\text{V}$	●		$\pm 0.5$	% of Reading	
		$0\text{V} \leq V_{IN\_SNS} \leq 10\text{V}$ (Note 11)	●		$\pm 50$	mV	

#### DAC Soft-Connect Comparator Characteristics

V <sub>OS_CMP</sub>	Offset Voltage	V <sub>DACn</sub> programmed to 0.2V	●	$\pm 1$	$\pm 18$	mV
		V <sub>DACn</sub> programmed to 1.38V	●	$\pm 2$	$\pm 26$	mV
		V <sub>DACn</sub> programmed to 2.65V	●	$\pm 3$	$\pm 52$	mV

#### Input Current Sense Characteristics

V <sub>IIN</sub>	Input Range	Single-Ended Voltage: V <sub>IIN_SNSP</sub> , V <sub>IIN_SNSM</sub> (Note 11)	●	3	60	V
		Differential Current Sense Voltage: V <sub>IIN_SNSP</sub> - V <sub>IIN_SNSM</sub>	●	-80	80	mV
I <sub>IIN</sub>	Input Current	I <sub>IN_SNSP</sub> and I <sub>IN_SNSM</sub> Inputs			$\pm 10$	$\mu\text{A}$
	Differential Input Current	I <sub>IN_SNSPn</sub> and I <sub>IN_SNSMn</sub> Inputs,  V <sub>IN_DIFF</sub>   = 80mV			$\pm 0.1$	$\mu\text{A}$
TUE_ADC_IIN	Total Unadjusted Error	$20\text{mV} \leq  V_{IIN\_SNSP} - V_{IIN\_SNSM}  \leq 80\text{mV}$	●		$\pm 0.6$	% of Reading
		$ V_{IIN\_SNSP} - V_{IIN\_SNSM}  \leq 20\text{mV}$	●		$\pm 120$	$\mu\text{V}$
V <sub>OS_IIN</sub>	Offset Error	V <sub>IIN_SNSP</sub> = V <sub>IIN_SNSM</sub>	●		$\pm 70$	$\mu\text{V}$

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_J = 25^\circ\text{C}$ .  $V_{VPWR} = 12\text{V}$ ,  $V_{VDD10} = V_{VDD33}, V_{VDD33}, V_{DD25}, \text{REFF},$  and  $\text{REFM}$  pins floating, unless otherwise indicated.  $C_{VDD33} = 100\text{nF}$ ,  $C_{VDD25} = 100\text{nF}$ , and  $C_{\text{REF}} = 100\text{nF}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMRR_IIN	DC CMRR	$3\text{V} \leq V_{\text{IIN\_SNSP}} \leq 60\text{V}$ $ V_{\text{IIN\_SNSP}} - V_{\text{IIN\_SNSM}}  = 80\text{mV}$	●		±4	μV/V
	AC CMRR	$ V_{\text{IIN\_SNSP}} - V_{\text{IIN\_SNSM}}  = 80\text{mV}$ , $V_{\text{IIN\_SNSP}} = 12\text{V} \pm 80\text{mV}$ , $f = 62.5\text{kHz}$		±25		μV/V
t <sub>CONV_IIN</sub>	Conversion Time			25		ms
t <sub>UPDATE</sub>	Update Rate			5.4		Hz

#### External Temperature Sensor Characteristics (READ\_TEMPERATURE\_1)

t <sub>CONV_TSENSE</sub>	Conversion Time	For One Channel, (Total Latency For All Channels Is 2 • 66ms)		66		ms	
I <sub>TSENSE_HI</sub>	T <sub>SENSE</sub> High Level Current		●	-90	-64	-40	μA
I <sub>TSENSE_LOW</sub>	T <sub>SENSE</sub> Low Level Current		●	-5.5	-4	-2.5	μA
TUE_TS	Total Unadjusted Error	Ideal Diode Assumed		±3		°C	
N_TS	Maximum Ideality Factor	READ_TEMPERATURE_1 = 175°C MFR_TEMP_1_GAIN = 1/N_TS			1.10		

#### Internal Temperature Sensor Characteristics (READ\_TEMPERATURE\_2)

TUE_TS2	Total Unadjusted Error			±1		°C
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#### V<sub>OUT</sub> Enable Output (V<sub>OUT\_EN</sub>[1:0]) Characteristics

I <sub>VOUT_ENn</sub>	Output Sinking Current	Mfr_config_vo_en_wpd_en = 0 $V_{\text{VOUT\_ENn}} = 0.4\text{V}$	●	3	5	8	mA
		Mfr_config_vo_en_wpd_en = 1 $V_{\text{VOUT\_ENn}} = 0.4\text{V}$	●	70	100	130	μA
	Output Leakage Current	$0\text{V} \leq V_{\text{VOUT\_ENn}} \leq 60\text{V}$	●		±1		μA
V <sub>OUT_VALID</sub>	Minimum VDD33 when V <sub>OUT_ENn</sub> Valid	$V_{\text{VOUT\_ENn}} \leq 0.4\text{V}$	●		1.2		V

#### General Purpose Output (AUXFAULTB) Characteristics

I <sub>AUXFAULTB</sub>	Output Sinking Current	$V_{\text{AUXFAULTB}} = 0.4\text{V}$	●	3	5	8	mA
	Output Leakage Current	$0\text{V} \leq V_{\text{AUXFAULTB}} \leq 60\text{V}$	●		±1		μA

#### Energy Meter Characteristics

TUE_ETB	Energy Meter Time-Base Error		●		±1	% of Reading
TUE_PIN	READ_PIN Total Unadjusted Error	$V_{\text{IIN\_SNSP}} - V_{\text{IIN\_SNSM}} = 50\text{mV}$	●		±1	% of Reading
TUE_EIN	Energy Meter Total Unadjusted Error	$V_{\text{IIN\_SNSP}} - V_{\text{IIN\_SNSM}} = 50\text{mV}$	●		±2	% of Reading

#### EEPROM Characteristics

Endurance	(Notes 12, 13)	$0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ During EEPROM Write Operations	●	10,000		Cycles	
Retention	(Notes 12, 13)	$T_J \leq 125^\circ\text{C}$	●	10		Years	
t <sub>MASS_WRITE</sub>	Mass Write Operation Time (Note 14)	STORE_USER_ALL, $0^\circ\text{C} < T_J < 85^\circ\text{C}$ During EEPROM Write Operations	●		200	4100	ms

#### Digital Inputs SCL, SDA, CONTROL0, CONTROL1, PGO, PG1, WDI/RESETB, FAULTB0, FAULTB1, WP

V <sub>IH</sub>	Input High Threshold Voltage	$1.62\text{V} \leq V_{\text{VDD10}} \leq 3.6\text{V}$	●	0.7 • $V_{\text{VDD10}}$		V
V <sub>IL</sub>	Input Low Threshold Voltage	$1.62\text{V} \leq V_{\text{VDD10}} \leq 3.6\text{V}$	●		0.3 • $V_{\text{VDD10}}$	V
V <sub>HYST</sub>	Input Hysteresis	FAULTBn, CONTROLn, PGn, WDI/RESETB, WP		20		mV
		SDA, SCL		80		mV

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_J = 25^\circ\text{C}$ .  $V_{VPWR} = 12\text{V}$ ,  $V_{VDD10} = V_{VDD33}$ ,  $V_{DD33}$ ,  $V_{DD25}$ , REFP, and REFM pins floating, unless otherwise indicated.  $C_{VDD33} = 100\text{nF}$ ,  $C_{VDD25} = 100\text{nF}$ , and  $C_{REF} = 100\text{nF}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{LEAK}$	Input Leakage Current	$0\text{V} \leq V_{PIN} \leq 3.6\text{V}$	●		$\pm 2$	$\mu\text{A}$
$t_{SP}$	Pulse Width of Spike Suppressed	FAULTBn, CONTROLn		10		$\mu\text{s}$
		SDA, SCL		98		ns
$t_{FAULT\_MIN}$	Minimum Low Pulse Width for Externally Generated Faults			180		ms
$t_{RESETB}$	Pulse Width to Assert Reset	$V_{WDI/RESETB} \leq 1.5\text{V}$	●	300		$\mu\text{s}$
$t_{WDI}$	Pulse Width to Reset Watchdog Timer	$V_{WDI/RESETB} \leq 1.5\text{V}$	●	0.3	200	$\mu\text{s}$
$f_{WDI}$	Watchdog Timer Interrupt Input Frequency		●		1	MHz
$C_{IN}$	Input Capacitance			10		pF

#### Digital Input SHARE\_CLK

$V_{IH}$	High Level Input Voltage		●	1.6		V
$V_{IL}$	Low Level Input Voltage		●		0.8	V
$f_{SHARE\_CLK\_IN}$	Input Frequency Operating Range		●	90	110	kHz
$t_{LOW}$	Assertion Low Time	$V_{SHARE\_CLK} < 0.8\text{V}$	●	0.825	1.11	$\mu\text{s}$
$t_{RISE}$	Rise Time	$V_{SHARE\_CLK} < 0.8\text{V}$ to $V_{SHARE\_CLK} > 1.6\text{V}$	●		450	ns
$I_{LEAK}$	Input Leakage Current	$0\text{V} \leq V_{SHARE\_CLK} \leq V_{VDD33} + 0.3\text{V}$	●		$\pm 1$	$\mu\text{A}$
$C_{IN}$	Input Capacitance			10		pF

#### Digital Outputs SDA, ALERTB, SHARE\_CLK, FAULTB0, FAULTB1, PWRGD, PG0, PG1

$V_{OL}$	Digital Output Low Voltage	$I_{SINK} = 3\text{mA}$	●		0.4	V	
$f_{SHARE\_CLK\_OUT}$	Output Frequency Operating Range	5.49k $\Omega$ Pull-Up to $V_{DD33}$	●	90	100	110	kHz

#### Digital Inputs ASELO,ASEL1

$V_{IH}$	Input High Threshold Voltage		●	$V_{VDD33} - 0.5$		V
$V_{IL}$	Input Low Threshold Voltage		●		0.5	V
$I_{H,IL}$	High, Low Input Current	$ASEL[1:0] = 0\text{V}$ , $V_{VDD33}$	●		$\pm 95$	$\mu\text{A}$
$I_{HIZ}$	Hi-Z Input Current		●		$\pm 24$	$\mu\text{A}$
$C_{IN}$	Input Capacitance			10		pF

#### Serial Bus Timing Characteristics

$f_{SCL}$	Serial Clock Frequency (Note 15)		●	10	400	kHz
$t_{LOW}$	Serial Clock Low Period (Note 15)		●	1.3		$\mu\text{s}$
$t_{HIGH}$	Serial Clock High Period (Note 15)		●	0.6		$\mu\text{s}$
$t_{BUF}$	Bus Free Time Between Stop and Start (Note 15)		●	1.3		$\mu\text{s}$
$t_{HD,STA}$	Start Condition Hold Time (Note 15)		●	600		ns
$t_{SU,STA}$	Stop Condition Setup Time (Note 15)		●	600		ns
$t_{SU,STO}$	Stop Condition Setup Time (Note 15)		●	600		ns

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_J = 25^\circ\text{C}$ .  $V_{VPWR} = 12\text{V}$ ,  $V_{VDD10} = V_{VDD33}$ ,  $V_{DD33}$ ,  $V_{DD25}$ , REFP, and REFM pins floating, unless otherwise indicated.  $C_{VDD33} = 100\text{nF}$ ,  $C_{VDD25} = 100\text{nF}$ , and  $C_{REF} = 100\text{nF}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{HD,DAT}$	Data Hold Time (LTC2971 Receiving Data) (Note 15)		●	0		ns
	Data Hold Time (LTC2971 Transmitting Data) (Note 15)		●	300	900	ns
$t_{SU,DA}$	Data Setup Time (Note 15)		●	100		ns
$t_{SP}$	Pulse Width of Spike Suppressed (Note 15)			98		ns
$t_{TIMEOUT\_BUS}$	Time Allowed to Complete any PMBus Command After Which Time SDA Will Be Released and Command Terminated	Mfr_config_all_longer_pmbus_timeout = 0	●	25	35	ms
		Mfr_config_all_longer_pmbus_timeout = 1	●	200	280	ms

### Additional Digital Timing Characteristics

$t_{OFF\_MIN}$	Minimum Off-Time for Any Channel			100		ms
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**Note 1:** Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. Exposure to any Absolute Maximum Rating for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified. If power is supplied to the chip via the  $V_{DD33}$  pin only, connect  $V_{PWR}$  and  $V_{DD33}$  pins together.

**Note 3:** The ADC total unadjusted error includes all error sources. First, a two-point analog trim is performed to achieve a flat reference voltage ( $V_{REF}$ ) over temperature. This results in minimal temperature coefficient, but the absolute voltage can still vary. To compensate for this, a high resolution, drift-free, and noiseless digital trim is applied at the output of the ADC, resulting in a very high accuracy measurement.

**Note 4:** Hysteresis in the output voltage is created by package stress that differs depending on whether IC was previously at a higher or lower temperature. Output voltage is always measured at  $25^\circ\text{C}$ , but the IC is cycled to  $125^\circ\text{C}$  or  $-40^\circ\text{C}$  before successive measurements. Hysteresis is roughly proportional to the square of the temperature change.

**Note 5:** Internal circuitry processes the absolute value of  $V_{OUT\_SNS} - GND_{SNS}$ . Thus, all digital voltages read and programmed are positive.

**Note 6:** Channels with negative range lack IMON capability. On these channels, setting Mfr\_config\_imon\_sel to 1 does not harm the part but returns incorrect results.

**Note 7:** The current sense resolution is determined by the L11 format, the values of IOUT\_CAL\_GAIN, and the magnitude of the current being measured. See [Table 3](#) for details.

**Note 8:** The nominal time between successive ADC conversions (latency of the ADC) for any given channel is  $t_{UPDATE\_ADC}$ .

**Note 9:**  $V_{OUT\_SNS}$ ,  $GND_{SNS}$ , and  $I_{OUT\_SNS}$  input currents are characterized by input current and input differential current. Input current is defined as current into a single device pin (see Note 2). Input differential current is defined as  $(I^+ - I^-)$  where  $I^+$  is the current into the positive device pin and  $I^-$  is the current into the negative device pin.

**Note 10:** Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to full-scale code, 1023.

**Note 11:** While READ\_VIN operates with  $0\text{V} \leq V_{VIN\_SNS} \leq 60\text{V}$ , the valid READ\_IIN, READ\_PIN, and MFR\_EIN operating range is  $3\text{V} \leq V_{IIN\_SNSP/M} \leq 60\text{V}$ .

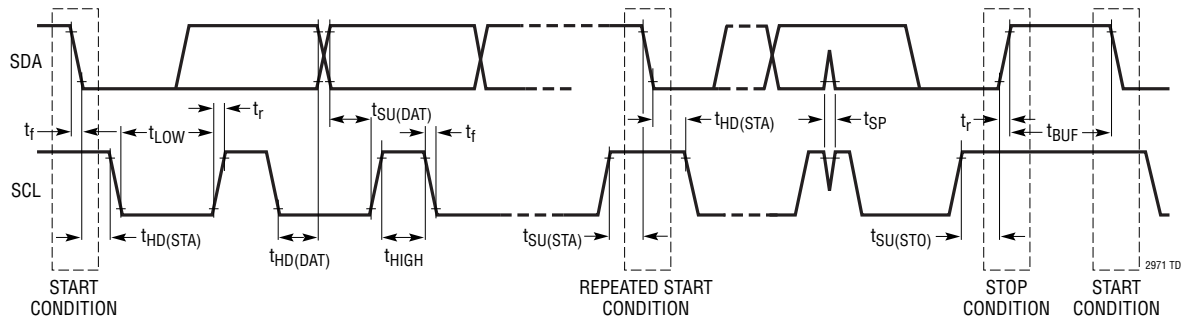
**Note 12:** EEPROM endurance and retention will be degraded when  $T_J > 125^\circ\text{C}$ .

**Note 13:** EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

**Note 14:** The LTC2971 will not acknowledge any PMBus commands, except for MFR\_COMMON, when a STORE\_USER\_ALL command is being executed. See also OPERATION section.

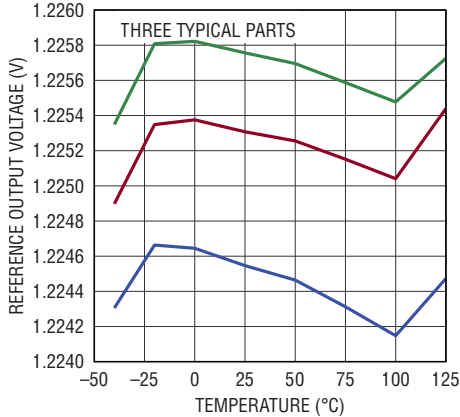
**Note 15:** Maximum capacitive load,  $C_B$ , for SCL and SDA is 400pF. Data and clock rise time ( $t_r$ ) and fall time ( $t_f$ ) are:  $(20 + 0.1 \cdot C_B)$  (ns)  $< t_r < 300\text{ns}$  and  $(20 + 0.1 \cdot C_B)$  (ns)  $< t_f < 300\text{ns}$ .  $C_B$  = capacitance of one bus line in pF. SCL and SDA external pullup voltage,  $V_{I0}$ , is  $3.13\text{V} < V_{I0} < 3.6\text{V}$ .

# PMBUS TIMING DIAGRAM

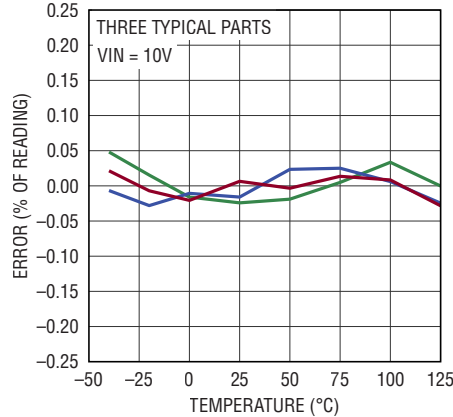


**TYPICAL PERFORMANCE CHARACTERISTICS**

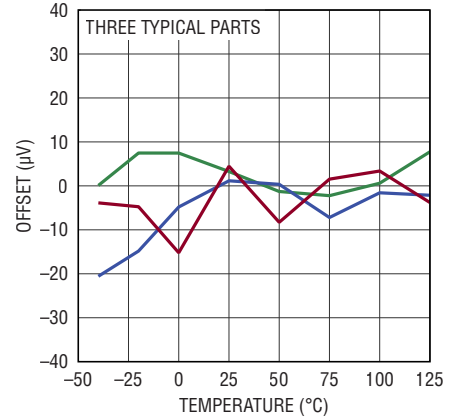
**Reference Voltage vs Temperature**



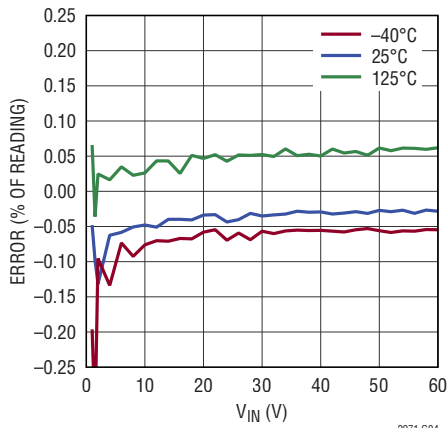
**ADC READ\_VOUT ADC Total Unadjusted Error vs Temperature**



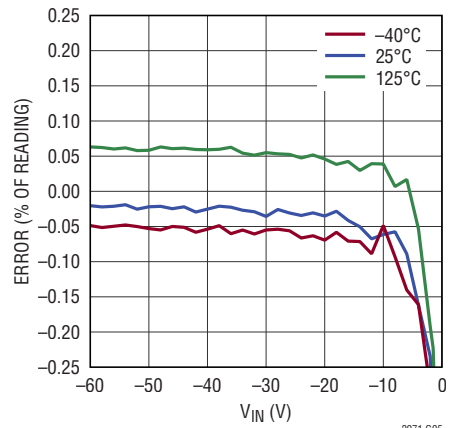
**ADC READ\_IOUT Input Referred Offset Voltage vs Temperature**



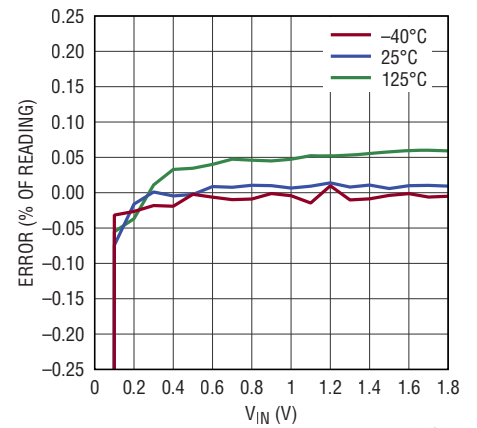
**+60V Channel READ\_VOUT Total Unadjusted Error vs Input Voltage**



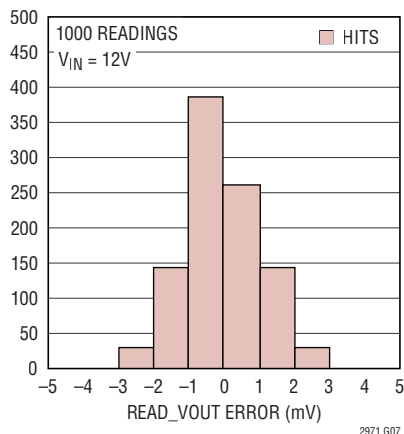
**-60V Channel READ\_VOUT Total Unadjusted Error vs Input Voltage**



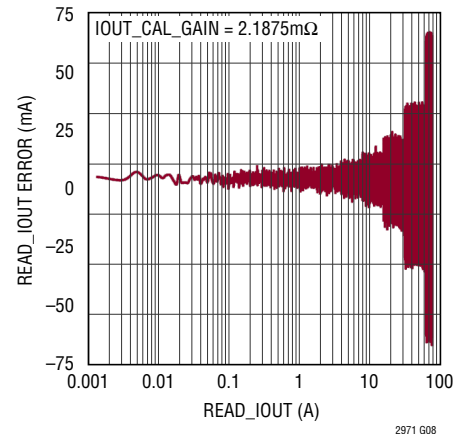
**+1.8V Channel READ\_VOUT Total Unadjusted Error vs Input Voltage**



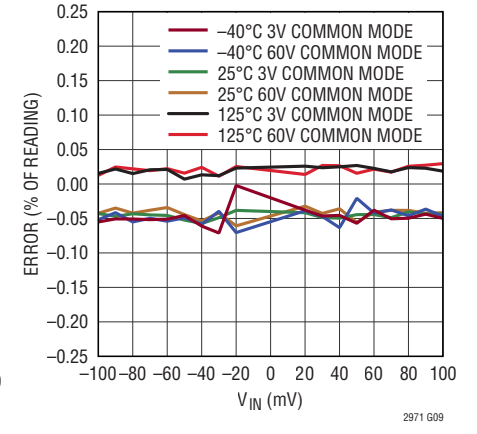
**ADC READ\_VOUT Noise Histogram**



**ADC READ\_IOUT Error vs READ\_IOUT**

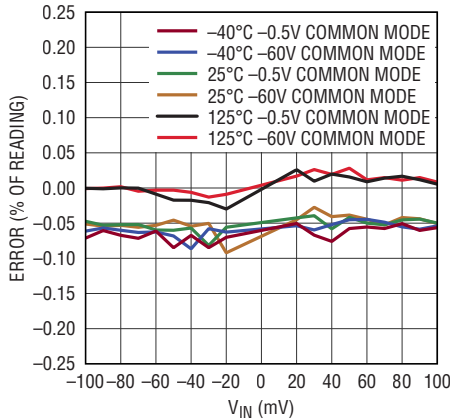


**+60V Channel MFR\_READ\_IOUT Total Unadjusted Error vs Input Voltage**



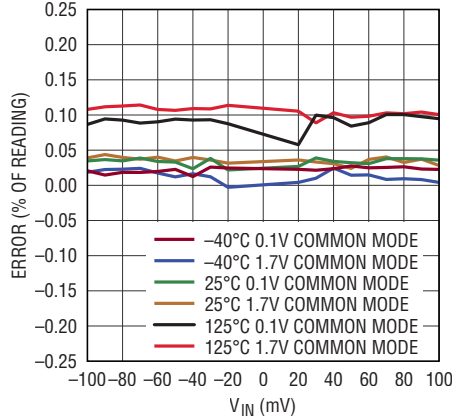
# TYPICAL PERFORMANCE CHARACTERISTICS

**-60V Channel MFR\_READ\_IOUT  
Total Unadjusted Error vs Input  
Voltage**



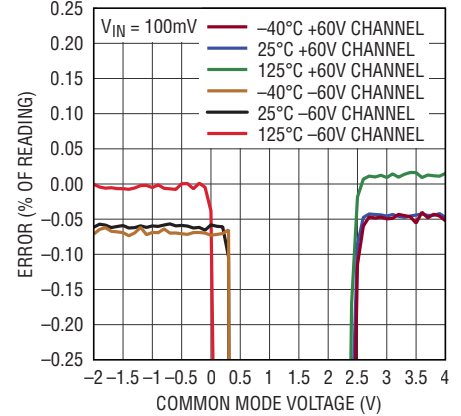
2971 G10

**+1.8V Channel MFR\_READ\_IOUT  
Total Unadjusted Error vs Input  
Voltage**



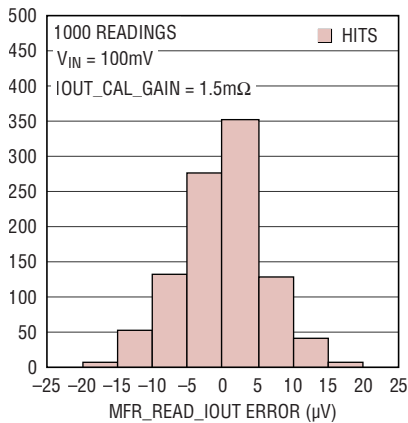
2971 G11

**MFR\_READ\_IOUT  
Total Unadjusted Error vs  
Low Common Mode Voltage**



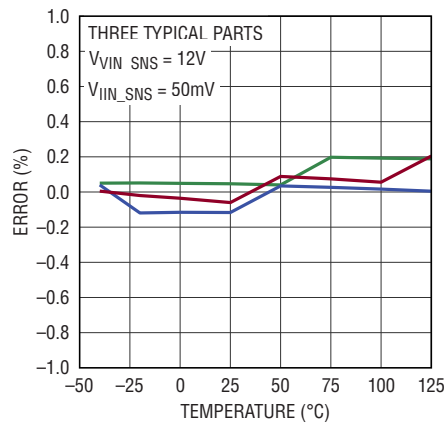
2971 G12

**ADC MFR\_READ\_IOUT Noise  
Histogram**



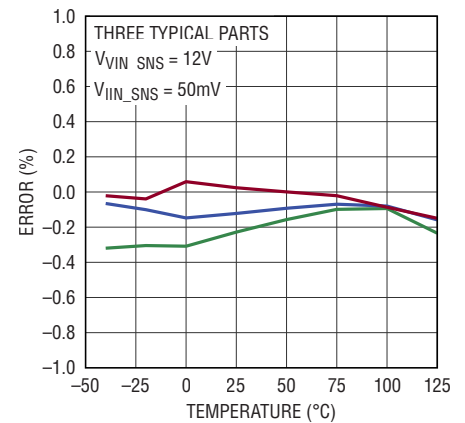
2971 G13

**Power Measurement Error**



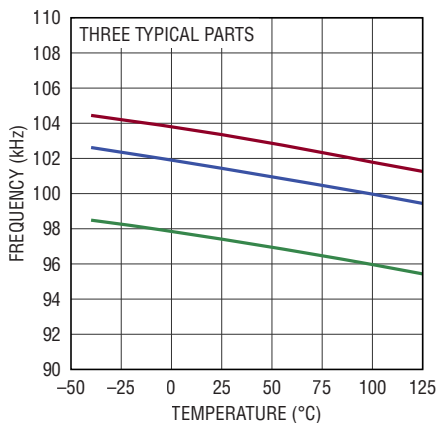
2971 G14

**Energy Measurement Error**



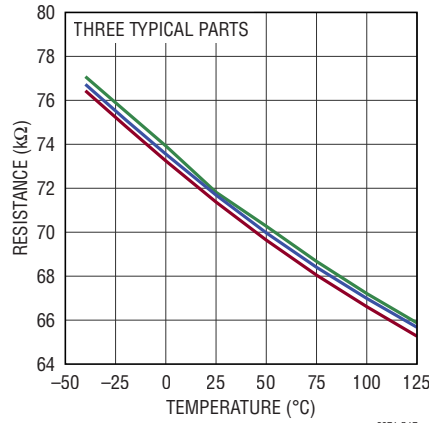
2971 G15

**SHARE\_CLK Output Frequency vs  
Temperature**



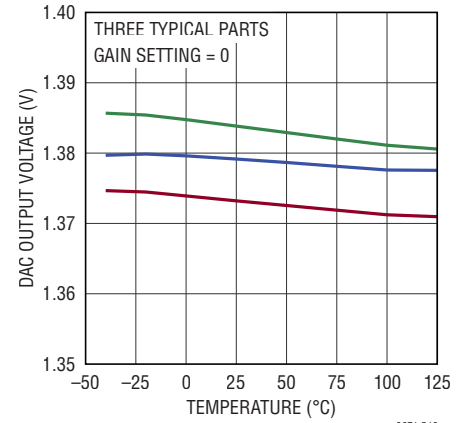
2971 G16

**VDDIO Input Resistance vs  
Temperature**



2971 G17

**DAC Full-Scale Voltage vs  
Temperature, Gain Setting = 0**

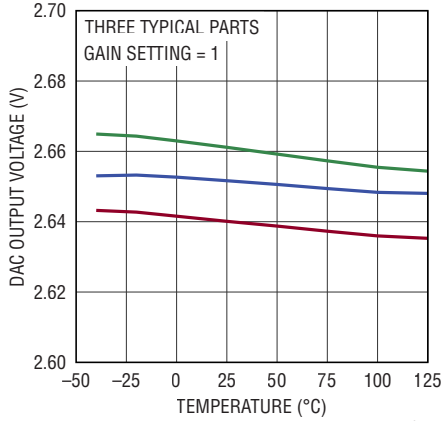


2971 G18

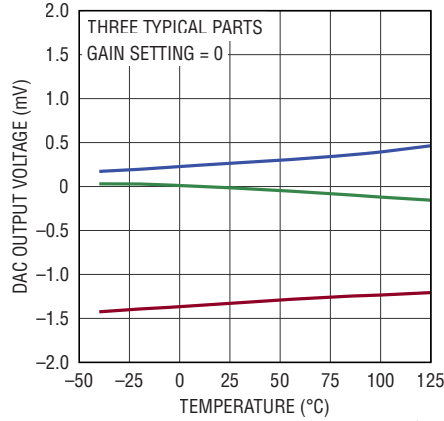


**TYPICAL PERFORMANCE CHARACTERISTICS**

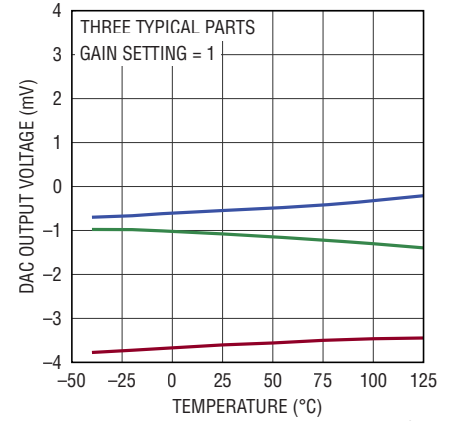
**DAC Full-Scale Voltage vs Temperature, Gain Setting = 1**



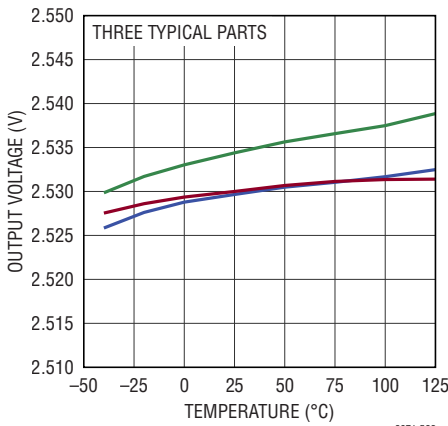
**DAC Offset Voltage vs Temperature, Gain Setting = 0**



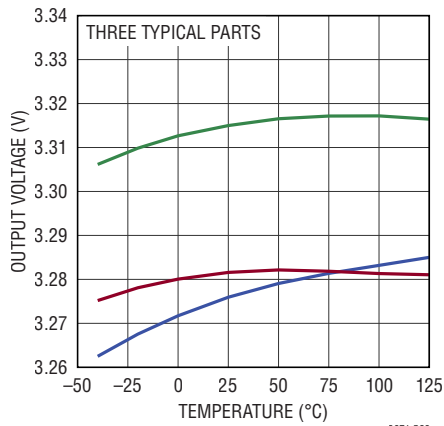
**DAC Offset Voltage vs Temperature, Gain Setting = 1**



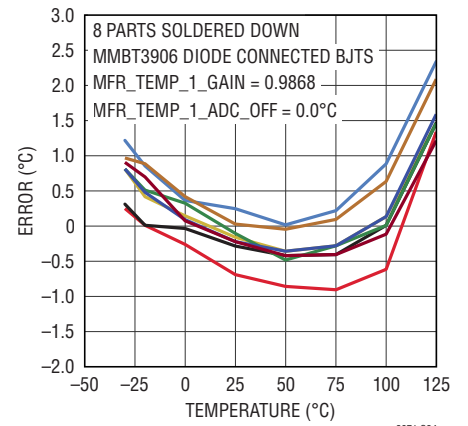
**VDD25 Regulator Output Voltage vs Temperature**



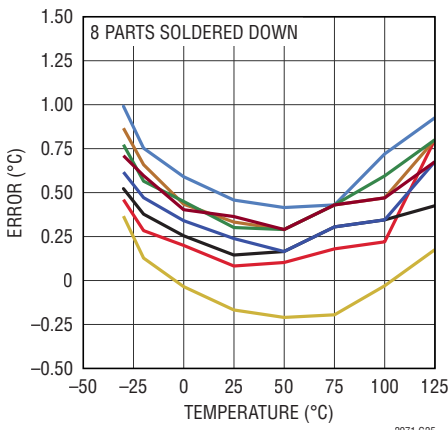
**VDD33 Regulator Output Voltage vs Temperature**



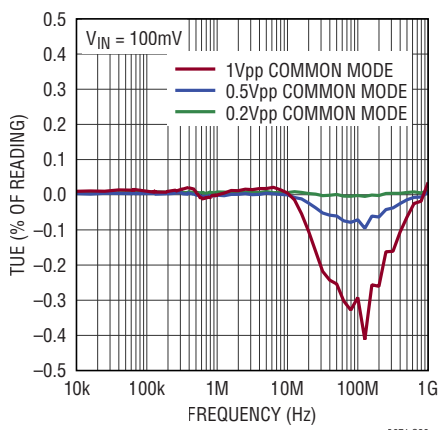
**External Temperature READ\_TEMPERATURE\_1 Error vs Temperature**



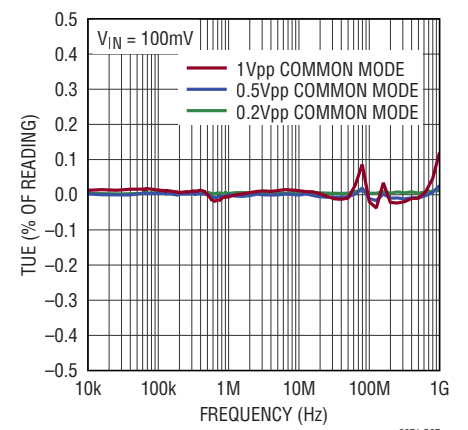
**READ\_TEMPERATURE\_2 Error vs Temperature**



**+60V Channel MFR\_READ\_IOUT Total Unadjusted Error vs AC Common Mode**

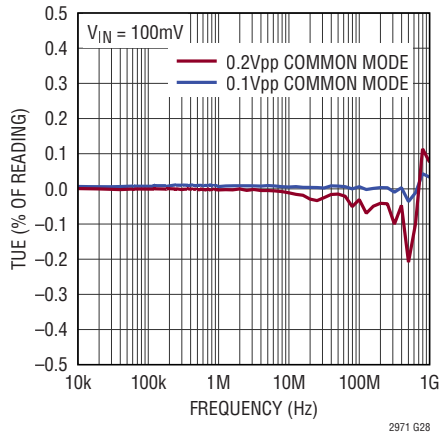


**-60V Channel MFR\_READ\_IOUT Total Unadjusted Error vs AC Common Mode**

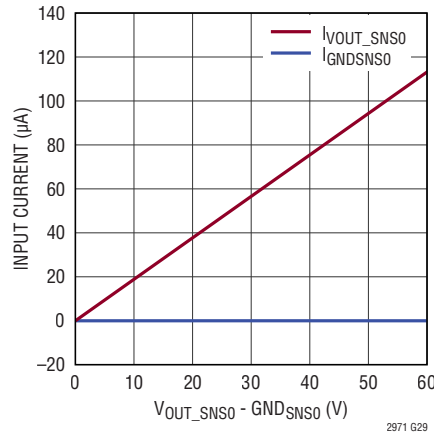


# TYPICAL PERFORMANCE CHARACTERISTICS

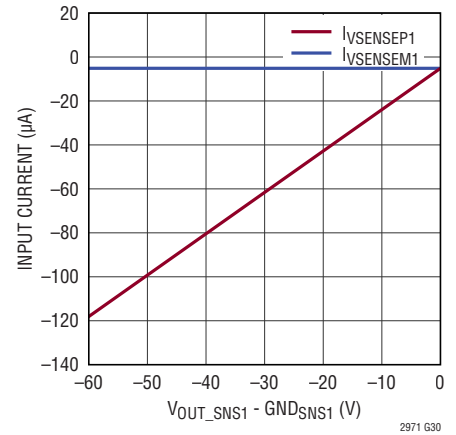
**+1.8V Channel MFR\_READ\_IOUT Total Unadjusted Error vs AC Common Mode**



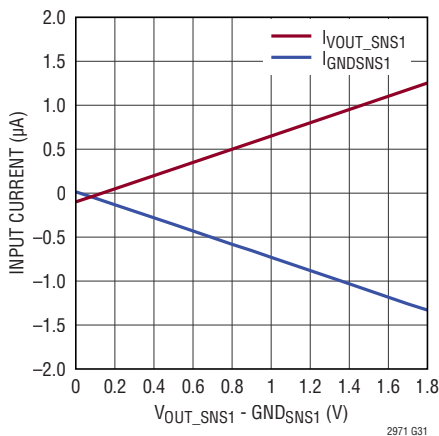
**+60V Channel Voltage Sense Input Currents vs Differential Input Voltage**



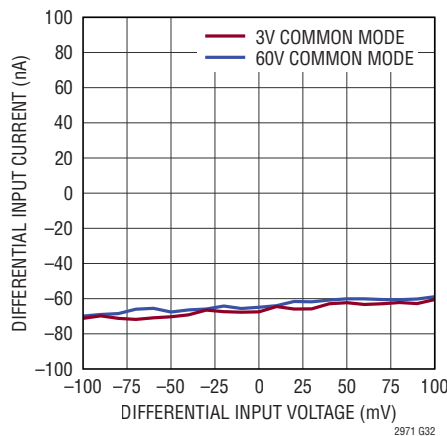
**-60V Channel Voltage Sense Input Currents vs Differential Input Voltage**



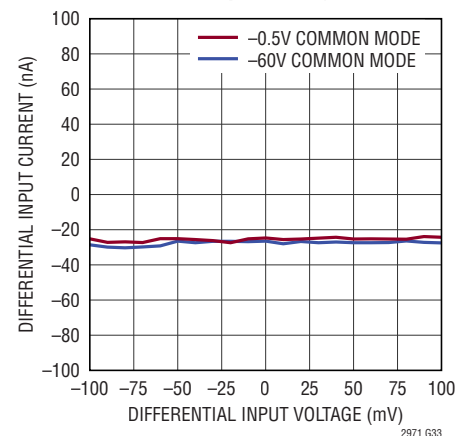
**+1.8V Channel Voltage Sense Input Currents vs Differential Input Voltage**



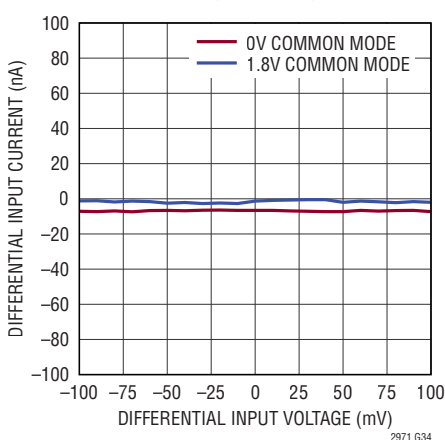
**+60V Channel Current Sense Differential Input Current vs Differential Input Voltage**



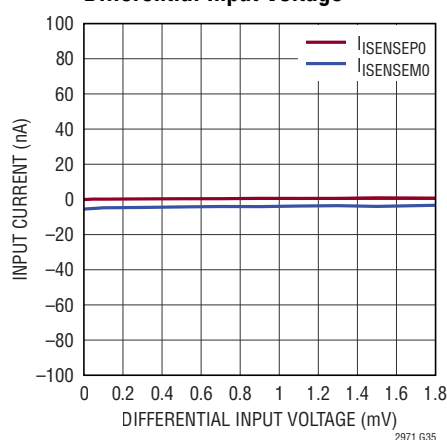
**-60V Channel Current Sense Differential Input Current vs Differential Input Voltage**



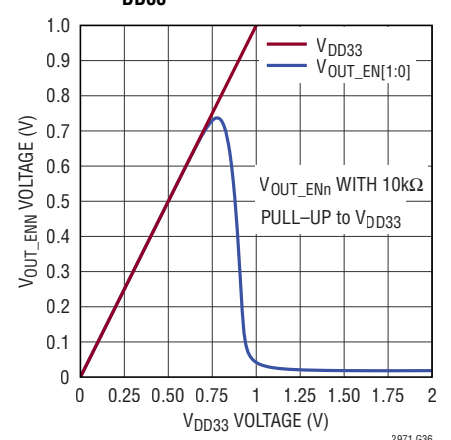
**+1.8V Channel Current Sense Differential Input Current vs Differential Input Voltage**



**IMON Sense Input Current vs Differential Input Voltage**



**VOUT\_EN[1:0] Output Voltage vs VDD33**



## PIN FUNCTIONS

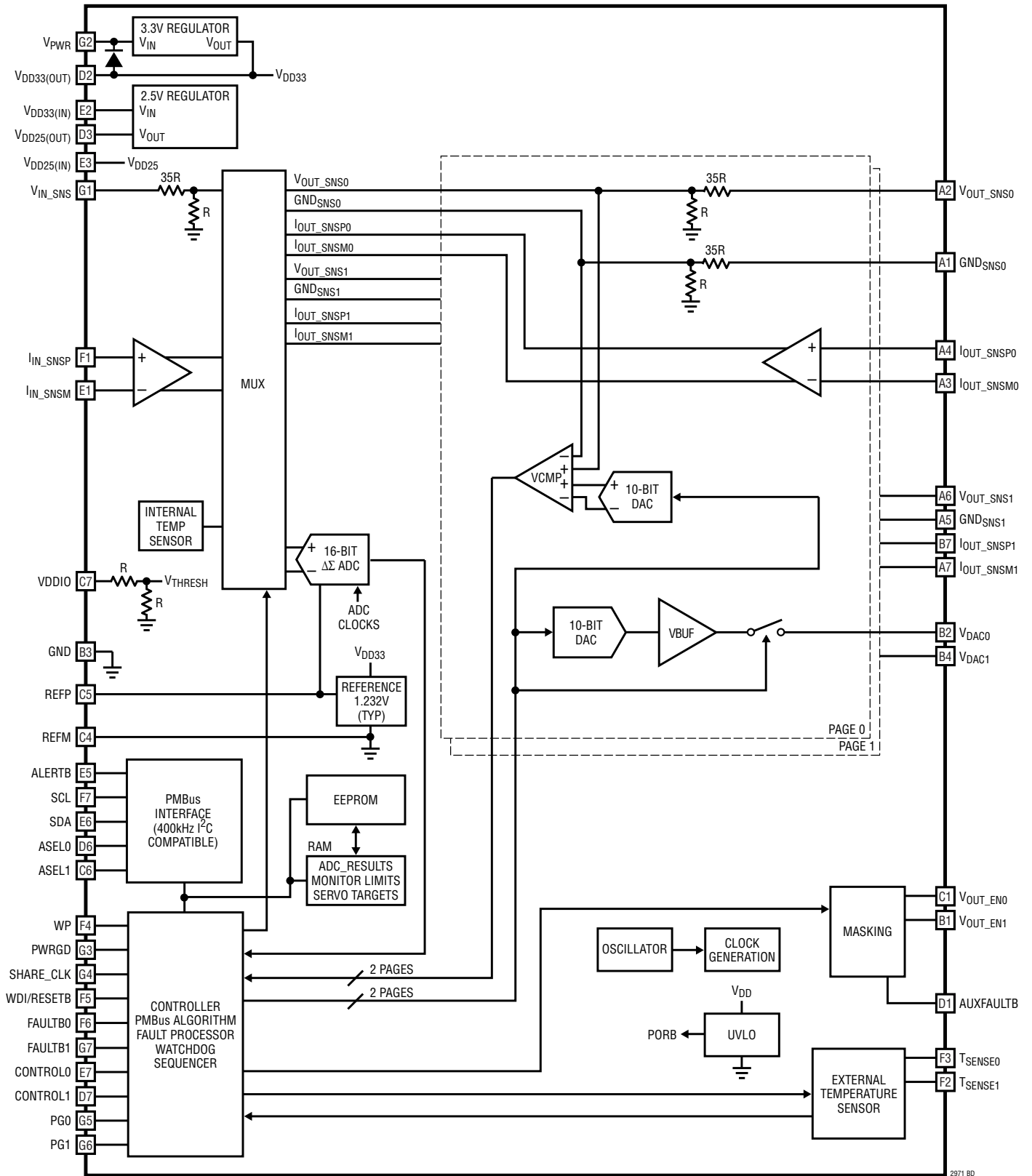
PIN NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
V <sub>OUT_SNS0</sub>	A2	In	DC/DC Converter Differential Output Voltage-0 Sensing Pin
GND <sub>SNS0</sub>	A1	In	DC/DC Converter Differential Output Voltage-0 Ground Sensing Pin
V <sub>OUT_EN0</sub>	C1	Out	DC/DC Converter Enable-0 Pin
V <sub>OUT_EN1</sub>	B1	Out	DC/DC Converter Enable-1 Pin
AUXFAULTB	D1	Out	Auxiliary Fault Output Pin. Can be configured to pull low when OV/UV detected.
DNC	B6	Do Not Connect	Do Not Connect. Leave this pin floating.
V <sub>IN_SNS</sub>	G1	In	V <sub>IN</sub> Sense Input. This voltage is compared against the V <sub>IN</sub> On and Off voltage thresholds in order to determine when to enable and disable, respectively, the downstream DC/DC converters.
V <sub>PWR</sub>	G2	In	V <sub>PWR</sub> Serves as the Unregulated Power Supply Input to the Chip. If a 4.5V to 60V supply voltage is unavailable, short V <sub>PWR</sub> to V <sub>DD33</sub> and power the chip directly from a 3.3V supply. Bypass to GND with a 0.1µF capacitor.
V <sub>DD33</sub>	D2	In/Out	If shorted to V <sub>PWR</sub> , It serves as 3.13 to 3.47V supply input pin. Otherwise it is a 3.3V internally regulated voltage output. If using the internal regulator to provide V <sub>DD33</sub> , do not connect to V <sub>DD33</sub> pins of any other devices. Bypass to GND with a 0.1µF capacitor.
V <sub>DD33</sub>	E2	In	Input for Internal 2.5V Sub-Regulator. Short this pin to pin D2. If using the internal regulator to provide V <sub>DD33</sub> , do not connect to V <sub>DD33</sub> pins of any other devices.
V <sub>DD25</sub>	D3	In/Out	2.5V Internally Regulated Voltage Output. Bypass to GND with a 0.1µF capacitor. Do not connect to V <sub>DD25</sub> pins of any other devices.
V <sub>DD25</sub>	E3	In	2.5V Supply Voltage Input. Short this pin to pin D3. Do not connect to V <sub>DD25</sub> pins of any other devices.
T <sub>SENSE0</sub>	F3	In/Out	External Temperature Current Output and Voltage Input for Channel 0. Maximum allowed capacitance is 1µF.
T <sub>SENSE1</sub>	F2	In/Out	External Temperature Current Output and Voltage Input for Channel 1. Maximum allowed capacitance is 1µF.
PWRGD	G3	Out	Power-Good Open Drain Output. Indicates when selected outputs are power good. Can be used as system power-on reset.
SHARE_CLK	G4	In/Out	Bidirectional Clock Sharing Pin. Connect a 5.49kΩ pull-up resistor to V <sub>DD33</sub> . Connect to all other SHARE_CLK pins in the system.
PG0	G5	In/Out	Configurable Open-Drain Output and Digital Input for Channel 0. Connect a 10kΩ pull-up resistor to V <sub>DDIO</sub> .
PG1	G6	In/Out	Configurable Open-Drain Output and Digital Input for Channel 1. Connect a 10kΩ pull-up resistor to V <sub>DDIO</sub> .
WDI/RESETB	F5	In	Watchdog Timer Interrupt and Chip Reset Input. Connect a 10kΩ pull-up resistor to V <sub>DD33</sub> . Rising edge resets watchdog counter. Holding this pin low for more than t <sub>RESETB</sub> resets the chip.
FAULTB0	F6	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-0. Connect a 10kΩ pull-up resistor to V <sub>DDIO</sub> .
FAULTB1	G7	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-1. Connect a 10kΩ pull-up resistor to V <sub>DDIO</sub> .
WP	F4	In	Digital Input. Active High Write-Protect Input Pin
SDA	E6	In/Out	PMBus Bidirectional Serial Data Pin
SCL	F7	In	PMBus Serial Clock Input Pin (400kHz Maximum)
ALERTB	E5	Out	Open-Drain Output. Generates an interrupt request in a fault/warning situation.
CONTROL0	E7	In	Control Pin 0 Input
CONTROL1	D7	In	Control Pin 1 Input
V <sub>DDIO</sub>	C7	In	Sets the Input Threshold of all digital inputs, except SHARE_CLK, ASEL[1:0], VOUT_EN[1:0] and AUXFAULTB, to approximately 45% of V <sub>DDIO</sub> . Connect to a supply voltage between 1.62V and 3.6V. Connect all of the LTC2971 pins pull-up resistors to this pin except WDI/RESETB, SHARE_CLK and VOUT_EN[1:0]. Connect these pins pull-up resistors to V <sub>DD33</sub> .

## PIN FUNCTIONS

PIN NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
ASEL0	D6	In	Ternary Address Select Pin 0 Input. Connect to $V_{DD33}$ , GND or float to encode 1 of 3 logic states.
ASEL1	C6	In	Ternary Address Select Pin 1 Input. Connect to $V_{DD33}$ , GND or float to encode 1 of 3 logic states.
REFP	C5	Out	Reference Voltage Output. Needs 0.1 $\mu$ F decoupling capacitor to REFM.
REFM	C4	Out	Reference Return Pin. Needs 0.1 $\mu$ F decoupling capacitor to REFP.
$I_{OUT\_SNSP0}$	A4	In	DC/DC Converter Differential (+) Output Current-0 Sensing Pin
$I_{OUT\_SNSM0}$	A3	In	DC/DC Converter Differential (-) Output Current-0 Sensing Pin
$I_{OUT\_SNSP1}$	B7	In	DC/DC Converter Differential (+) Output Current-1 Sensing Pin
$I_{OUT\_SNSM1}$	A7	In	DC/DC Converter Differential (-) Output Current-1 Sensing Pin
GND	B3, B5, C2, C3, D4, D5, E4	Ground	
$V_{DAC0}$	B2	Out	DAC0 Output
$V_{DAC1}$	B4	Out	DAC1 Output
$I_{IN\_SNSP}$	F1	In	DC/DC Converter Differential (+) Input Current Sensing Pin.
$I_{IN\_SNSM}$	E1	In	DC/DC Converter Differential (-) Input Current Sensing Pin.
$V_{OUT\_SNS1}$	A6	In	DC/DC Converter Differential Output Voltage-1 Sensing Pin
$GND_{SNS1}$	A5	In	DC/DC Converter Differential Output Voltage-1 Ground Sensing Pin

\* Tie any unused  $V_{OUT\_SNSn}/GND_{SNSn}$ ,  $I_{OUT\_SNSPn}$ ,  $I_{OUT\_SNSMn}$  or  $T_{SENSEn}$  pins to GND. Refer to Unused ADC Sense Inputs in the [Applications Information](#) section.

**BLOCK DIAGRAM**



See Figure 30 for a Typical Application with a Simplified Block Diagram

## OPERATION

### LTC2971 OPERATION OVERVIEW

The LTC2971 is a PMBus programmable power supply controller, monitor, sequencer and voltage supervisor that can perform the following operations:

- Accept PMBus compatible programming commands.
- Provide DC/DC converter input voltage, output voltage, output current, output temperature, and LTC2971 internal temperature readback through the PMBus interface.
- Connect directly to a DC/DC converter's IMON pin or the DCR sense network for output current telemetry readback.
- Control the output of DC/DC converters that set the output voltage with a trim pin or DC/DC converters that set the output voltage using an external resistor feedback network.
- Sequence the startup of DC/DC converters via PMBus programming and the CONTROL input pins. The LTC2971 supports time-based sequencing and tracking sequencing. Cascade sequence ON with time based sequence OFF is also supported.
- Trim the DC/DC converter output voltage (typically in 0.02% steps), in closed-loop servo operating mode, autonomously or through PMBus programming.
- Margin the DC/DC converter output voltage to PMBus programmed limits.
- Trim or margin the DC/DC converter output voltage with direct access to the margin DAC.
- Supervise the DC/DC converter input voltage, output voltage and the inductor temperatures for overvalue/undervalue conditions with respect to PMBus programmed limits and generate appropriate faults and warnings.
- Accurately handle inductor self-heating transients using a proprietary algorithm. These self-heating effects are combined with external temperature sensor readings to improve accuracy of ADC current measurements.
- Respond to a fault condition by continuing operation indefinitely, latching-off after a programmable deglitch period, latching-off immediately or sequencing off after TOFF\_DELAY. Use retry mode to automatically recover from a latched-off condition. With retry enabled, MFR\_RETRY\_COUNT programs the number of retries (0 to 6 or infinite) for both pages.
- Optionally stop trimming the DC/DC converter output voltage after it reaches the initial margin or nominal target. Optionally allow trimming restart if target drifts outside of  $V_{OUT}$  warning limits.
- Store command register contents to EEPROM with CRC and ECC through PMBus programming.
- Restore EEPROM contents through PMBus programming or when  $V_{DD33}$  is applied on power-up.
- Generate interrupt requests by asserting the ALERTB pin in response to supported PMBus faults and warnings.
- Coordinate system wide fault responses for all DC/DC converters connected to the LTC2971 FAULTB0 and FAULTB1 pins.
- Propagate per-channel POWER GOOD status via the PG0 and PG1 pins, or configure these pins as general-purpose IOs.
- Synchronize sequencing delays or shutdown for multiple devices using the SHARE\_CLK pin.
- Software and hardware write protect the command registers.
- Disable the supervised DC/DC converters in response to output OV and UV faults.
- Log telemetry and status data to EEPROM in response to a faulted-off condition.
- Supervise an external microcontroller's activity for a stalled condition with a programmable watchdog timer and reset it if necessary.

## OPERATION

- Prevent a DC/DC converter from re-entering the ON state after a power cycle until a programmable interval (MFR\_RESTART\_DELAY) has elapsed and its output has decayed below a programmable threshold voltage (MFR\_VOUT\_DISCHARGE\_THRESHOLD).
- Read high side input current, input voltage, input power, and accumulated input energy.
- Record minimum and maximum input voltage, input current, input power, output voltages, output currents and output temperatures.
- Access user EEPROM data directly, without altering RAM space (Mfr\_ee\_unlock, Mfr\_ee\_erase, and Mfr\_ee\_data). Facilitates in-house bulk programming.
- Accommodate multiple hosts with Command Plus.

## EEPROM

The LTC2971 contains internal EEPROM (Nonvolatile Memory) with error-correcting-code (ECC) to store configuration settings and fault log information. EEPROM endurance, retention and mass write operation time are specified over the operating temperature range. See [Electrical Characteristics](#) and [Absolute Maximum Ratings](#) sections.

Read operations performed between  $-40^{\circ}\text{C}$  and  $125^{\circ}\text{C}$  will not degrade the EEPROM. Write operations above  $85^{\circ}\text{C}$  are possible but will degrade retention characteristics. It is recommended that the EEPROM not be written above  $85^{\circ}\text{C}$ . The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above  $85^{\circ}\text{C}$ , the slight degradation in the retention characteristics of the fault log will not take away the usefulness of the function.

The degradation in EEPROM retention for temperatures  $>125^{\circ}\text{C}$  can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[ \left( \frac{E_a}{k} \right) \left( \frac{1}{T_{\text{USE}} + 273} - \frac{1}{T_{\text{STRESS}} + 273} \right) \right]}$$

where:

AF = acceleration factor

$E_a$  = activation energy = 1.4eV

$k = 8.617 \cdot 10^{-5} \text{ eV}/^{\circ}\text{K}$

$T_{\text{USE}}$  =  $125^{\circ}\text{C}$  specified junction temperature

$T_{\text{STRESS}}$  = actual junction temperature  $^{\circ}\text{C}$

Example: Calculate the effect on retention when operating at a junction temperature of  $130^{\circ}\text{C}$  for 10 hours.

$T_{\text{STRESS}} = 130^{\circ}\text{C}$

$T_{\text{USE}} = 125^{\circ}\text{C}$

AF = 1.66

Equivalent operating time at  $125^{\circ}\text{C}$  = 16.6 hours.

So the overall retention of the EEPROM was degraded by an additional 6.6 hours as a result of operation at a junction temperature of  $130^{\circ}\text{C}$  for 10 hours. Note that the effect of this overstress is negligible when compared to the overall EEPROM retention rating of 87,600 hours at a junction temperature of  $125^{\circ}\text{C}$ .

## AUXFAULTB

The MFR\_CONFIG2\_LTC2971 and MFR\_CONFIG3\_LTC2971 commands can be used on a per channel basis to select which, if any, fault conditions will cause the AUXFAULTB pin to be driven low. The only fault types which can be propagated to the AUXFAULTB pin are over/under voltage faults.

## RESETB

Holding the WDI/RESETB pin low for more than  $t_{\text{RESETB}}$  will cause the LTC2971 to enter the power-on reset state. While in the power-on reset state, the device will not communicate on the I<sup>2</sup>C bus. Following the subsequent rising-edge of the WDI/RESETB pin, the LTC2971 will execute its power-on sequence per the user configuration stored in EEPROM. Connect WDI/RESETB to  $V_{\text{DD33}}$  with a 10k resistor. WDI/RESETB includes an internal 256 $\mu\text{s}$  deglitch filter so additional filter capacitance on this pin is not recommended.



## OPERATION

### V<sub>DDIO</sub>

The V<sub>DDIO</sub> pin defines the input threshold of the SDA, SCL, ALERTB, PWRGD, FAULTB[1:0], CONTROL[1:0], PG[1:0], WDI/RESETB, and WP pins to allow for lower voltage digital communication. An internal resistive divider at the V<sub>DDIO</sub> pin sets the internal threshold voltage to approximately 45% of the V<sub>DDIO</sub> pin voltage. The VOUT\_EN[1:0], AUXFAULTB, and SHARE\_CLK pins are not affected by the voltage at the V<sub>DDIO</sub> pin and should always be pulled up to V<sub>DD33</sub>.

### PMBus SERIAL DIGITAL INTERFACE

The LTC2971 communicates with a host (master) using the standard PMBus serial bus interface. The PMBus [Timing Diagram](#) shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC2971 is a slave device. The master can communicate with the LTC2971 using the following formats:

- Master transmitter, slave receiver
- Master receiver, slave transmitter

The following SMBus commands are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read
- Alert Response Address

Figures 1 to 13 illustrate the aforementioned SMBus protocols. All transactions support PEC (packet error check) and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the SMBus timeout may be extended using the Mfr\_config\_all\_longer\_pmbus\_timeout setting.

### PMBus

PMBus is an industry standard that defines a means of communication with power conversion devices. It is comprised of an industry standard SMBus serial interface and the PMBus command language.

The PMBus two wire interface is an incremental extension of the SMBus. SMBus is built upon I<sup>2</sup>C with some minor

differences in timing, DC parameters and protocol. The SMBus protocols are more robust than simple I<sup>2</sup>C byte commands because they provide timeouts to prevent bus hangs and optional Packet Error Checking (PEC) to ensure data integrity. In general, a master device that can be configured for I<sup>2</sup>C communication can be used for PMBus communication with little or no change to hardware or firmware.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.1: Section 5: Transport. This can be found at:

[www.pmbus.org](http://www.pmbus.org)

For a description of the differences between SMBus and I<sup>2</sup>C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B – Differences between SMBus and I<sup>2</sup>C. This can be found at:

[www.smbus.org](http://www.smbus.org)

When using an I<sup>2</sup>C controller to communicate with a PMBus part it is important that the controller be able to write a byte of data without generating a stop. This will allow the controller to properly form the repeated start of a PMBus read command by concatenating a start command byte write with an I<sup>2</sup>C read.

### Device Address

The I<sup>2</sup>C/SMBus address of the LTC2971 equals the base address + N where N is a number from 0 to 8. N can be configured by setting the ASELO and ASEL1 pins to V<sub>DD33</sub>, GND or FLOAT. See [Table 1](#). Using one base address and the nine values of N, nine LTC2971s can be connected together to control eighteen outputs. The base address is stored in the MFR\_I2C\_BASE\_ADDRESS register. The base address can be written to any value, but generally should not be changed unless the desired range of addresses overlap existing addresses. Ensure that the address range does not overlap with other I<sup>2</sup>C/SMBus device or global addresses, including I<sup>2</sup>C/SMBus multiplexers and bus buffers. This will bring you great happiness.

The LTC2971 always responds to its global address and the SMBus Alert Response address regardless of the state of its ASEL pins and the MFR\_I2C\_BASE\_ADDRESS register.

## OPERATION

### Processing Commands

The LTC2971 uses a dedicated processing block to ensure quick response to all of its commands. There are a few exceptions where the part will NACK a subsequent command

because it is still processing the previous command. These are summarized in the following tables. MFR\_COMMON is a special command that may always be read even when the part is busy. This provides an alternate method for a host to determine if the LTC2971 is busy.

### EEPROM Related Commands

COMMAND	TYPICAL DELAY*	COMMENT
STORE_USER_ALL	$t_{\text{MASS\_WRITE}}$	See Electrical Characterization table. The LTC2971 will not accept any commands while it is transferring register contents to the EEPROM. The command byte will be NACKed. MFR_COMMON may always be read.
RESTORE_USER_ALL	30ms	The LTC2971 will not accept any commands while it is transferring EEPROM data to command registers. The command byte will be NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_CLEAR	175ms	The LTC2971 will not accept any commands while it is initializing the fault log EEPROM space. The command byte will be NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_STORE	20ms	The LTC2971 will not accept any commands while it is transferring fault log RAM buffer to EEPROM space. The command byte will be NACKed. MFR_COMMON may always be read.
Internal Fault log	20ms	An internal fault log event is a one time event that uploads the contents of the fault log to EEPROM in response to a fault. Internal fault logging may be disabled. Commands received during this EEPROM write are NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_RESTORE	2ms	The LTC2971 will not accept any commands while it is transferring EEPROM data to the fault log RAM buffer. The command byte will be NACKed. MFR_COMMON may always be read.

\*The typical delay is measured from the command's stop to the next command's start.

### Other Commands

COMMAND	TYPICAL DELAY*	COMMENT
MFR_CONFIG	<50 $\mu$ s	The LTC2971 will not accept any commands while it is completing this command. The command byte will be NACKed. MFR_COMMON may always be read.
IOUT_CAL_GAIN and IOUT_CAL_OFFSET	<500 $\mu$ s	The LTC2971 will not accept any commands while it is completing this command. The command byte will be NACKed. MFR_COMMON may always be read.

\*The delay is measured from the command's stop to the next command's start.

### Other PMBus Timing Notes

COMMAND	COMMENT
CLEAR_FAULTS	The LTC2971 will accept commands while it is completing this command but the affected status flags will not be cleared for up to 500 $\mu$ s.

# OPERATION

**Table 1. LTC2971 Address Look-Up Table with MFR\_I2C\_BASE\_ADDRESS Set to 7-bit 0x5C**

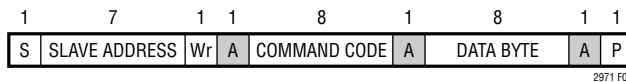
ADDRESS PINS		DESCRIPTION	HEX DEVICE ADDRESS		BINARY DEVICE ADDRESS							R/W
ASEL1	ASEL0		7-Bit	8-Bit	6	5	4	3	2	1	0	
X	X	Alert Response	0C	19	0	0	0	1	1	0	0	1
X	X	Global	5B	B6	1	0	1	1	0	1	1	0
L	L	N = 0	5C*	B8	1	0	1	1	1	0	0	0
L	NC	N = 1	5D	BA	1	0	1	1	1	0	1	0
L	H	N = 2	5E	BC	1	0	1	1	1	1	0	0
NC	L	N = 3	5F	BE	1	0	1	1	1	1	1	0
NC	NC	N = 4	60	C0	1	1	0	0	0	0	0	0
NC	H	N = 5	61	C2	1	1	0	0	0	0	1	0
H	L	N = 6	62	C4	1	1	0	0	0	1	0	0
H	NC	N = 7	63	C6	1	1	0	0	0	1	1	0
H	H	N = 8	64	C8	1	1	0	0	1	0	0	0

H = Tie to V<sub>DD33</sub>, NC = No Connect = Open or Float, L = Tie to GND, X = Don't Care  
 \*MFR\_I2C\_BASE\_ADDRESS = 7-bit 0x5C (Factory Default)

- S START CONDITION
- Sr REPEATED START CONDITION
- Rd READ (BIT VALUE OF 1)
- Wr WRITE (BIT VALUE OF 0)
- $\bar{A}$  NOT ACKNOWLEDGE (HIGH)
- A ACKNOWLEDGE (LOW)
- P STOP CONDITION
- PEC PACKET ERROR CODE
- MASTER TO SLAVE
- SLAVE TO MASTER
- ... CONTINUATION OF PROTOCOL

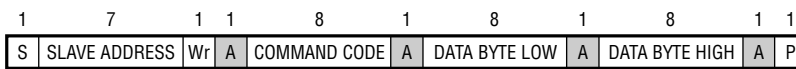
2971 F01

**Figure 1. PMBus Packet Protocol Diagram Element Key**



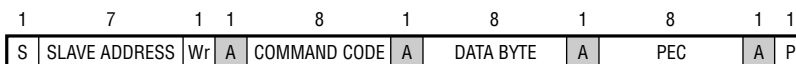
2971 F02

**Figure 2. Write Word Protocol Write Byte Protocol**



2971 F03

**Figure 3. Write Byte Protocol**



2971 F04

**Figure 4. Write Byte Protocol with PEC**

**OPERATION**

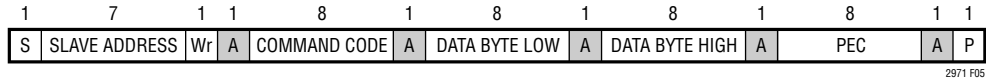


Figure 5. Write Word Protocol with PEC

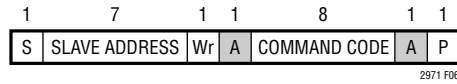


Figure 6. Send Byte Protocol

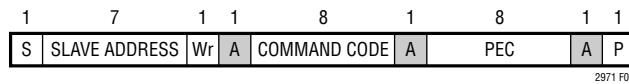


Figure 7. Send Byte Protocol with PEC

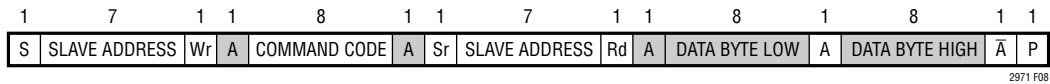


Figure 8. Read Word Protocol

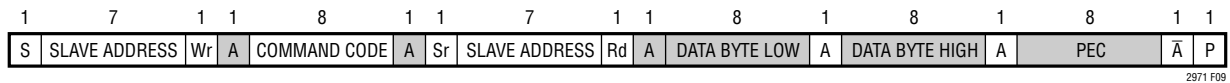


Figure 9. Read Word Protocol with PEC

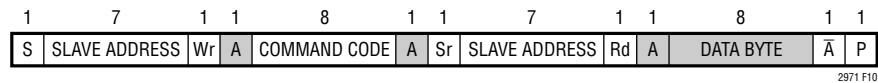


Figure 10. Read Byte Protocol

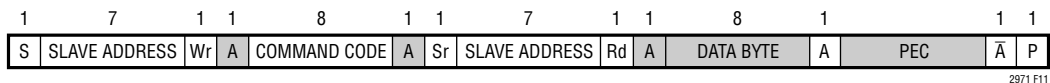


Figure 11. Read Byte Protocol with PEC

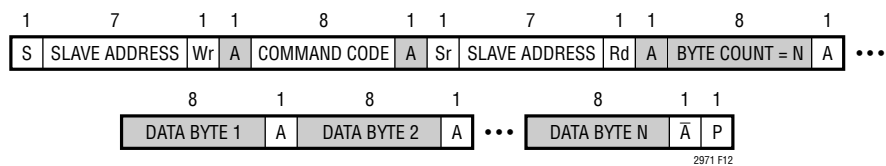


Figure 12. Block Read

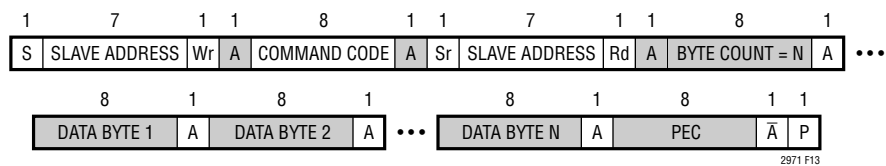


Figure 13. Block Read with PEC

## PMBus COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT (Note 1)	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX (Note 2)	REF PAGE
PAGE	0x00	Channel or page currently selected for any command that supports paging.	R/W Byte	N	Reg			0x00	<a href="#">33</a>
OPERATION	0x01	Operating mode control. On/Off, Margin High and Margin Low.	R/W Byte	Y	Reg		Y	0x00	<a href="#">39</a>
ON_OFF_CONFIG	0x02	CONTROL pin and PMBus on/off command setting.	R/W Byte	Y	Reg		Y	0x1E	<a href="#">40</a>
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	Y				NA	<a href="#">70</a>
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	<a href="#">34</a>
STORE_USER_ALL	0x15	Store entire operating memory to EEPROM.	Send Byte	N				NA	<a href="#">48</a>
RESTORE_USER_ALL	0x16	Restore entire operating memory from EEPROM.	Send Byte	N				NA	<a href="#">48</a>
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	<a href="#">90</a>
VOUT_MODE	0x20	Output voltage data format and mantissa exponent.	R Byte	Y	Reg			2 <sup>-10</sup> 0x16 2 <sup>-13</sup> 0x13	<a href="#">55</a>
VOUT_COMMAND	0x21	Servo target. Nominal DC/DC converter output voltage setpoint.	R/W Word	Y	L16	V	Y	12.0 0x3000 1.0 0x2000	<a href="#">55</a>
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	15.0 0x3C00 4.0 0x8000	<a href="#">55</a>
VOUT_MARGIN_HIGH	0x25	Margin high DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	12.6 0x3266 1.05 0x219A	<a href="#">55</a>
VOUT_MARGIN_LOW	0x26	Margin low DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	11.4 0x2D9A 0.95 0x1E66	<a href="#">55</a>
VIN_ON	0x35	Input voltage above which power conversion can be enabled.	R/W Word	N	L11	V	Y	10.0 0xD280	<a href="#">51</a>
VIN_OFF	0x36	Input voltage below which power conversion is disabled. Both V <sub>OUT_EN</sub> pins go off immediately or sequence off after TOFF_DELAY (See Mfr_config_track_enr).	R/W Word	N	L11	V	Y	9.0 0xD240	<a href="#">51</a>
IOUT_CAL_GAIN	0x38	The nominal resistance of the current sense element in mΩ.	R/W Word	Y	L11	mΩ	Y	1.0 0xBA00	<a href="#">56</a>
IOUT_CAL_OFFSET	0x39	Offset applied to the current sense measurement in Amps.	R/W Word	Y	L11	A	Y	0 0x8000	<a href="#">56</a>
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	13.2 0x34CD 1.1 0x2333	<a href="#">55</a>
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	<a href="#">66</a>
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	12.9 0x339A 1.075 0x2266	<a href="#">51</a>
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	11.1 0x2C66 0.925 0x1D9A	<a href="#">51</a>

## PMBus COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT (Note 1)	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX (Note 2)	REF PAGE
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit. Used for Ton_max_fault and PWRGD pin de-assertion.	R/W Word	Y	L16	V	Y	10.8 0x2B33 0.9 0x1CCD	<a href="#">55</a>
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0x7F	<a href="#">66</a>
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A		5.0 0xCA80	<a href="#">57</a>
OT_FAULT_LIMIT	0x4F	Overtemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	65.0 0xEA08	<a href="#">58</a>
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an overtemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	<a href="#">67</a>
OT_WARN_LIMIT	0x51	Overtemperature warning limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	60.0 0xE3C0	<a href="#">58</a>
UT_WARN_LIMIT	0x52	Undertemperature warning limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	0 0x8000	<a href="#">58</a>
UT_FAULT_LIMIT	0x53	Undertemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	-5.0 0xCD80	<a href="#">58</a>
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an undertemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	<a href="#">67</a>
VIN_OV_FAULT_LIMIT	0x55	Input overvoltage fault limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	15.0 0xD3C0	<a href="#">51</a>
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	N	Reg		Y	0x80	<a href="#">67</a>
VIN_OV_WARN_LIMIT	0x57	Input overvoltage warning limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	14.0 0xD380	<a href="#">51</a>
VIN_UV_WARN_LIMIT	0x58	Input undervoltage warning limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	0 0x8000	<a href="#">51</a>
VIN_UV_FAULT_LIMIT	0x59	Input undervoltage fault limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	0 0x8000	<a href="#">51</a>
VIN_UV_FAULT_RESPONSE	0x5A	Action to be taken by the device when an input undervoltage fault is detected.	R/W Byte	N	Reg		Y	0x00	<a href="#">67</a>
POWER_GOOD_ON	0x5E	Output voltage at or above which the PWRGD pin should be asserted.	R/W Word	Y	L16	V	Y	11.52 0x2E14 0.96 0x1EB8	<a href="#">55</a>
POWER_GOOD_OFF	0x5F	Output voltage at or below which the PWRGD pin should be de-asserted when Mfr_config_all_pwrGD_off_uses_uv is clear.	R/W Word	Y	L16	V	Y	11.28 0x2D1F 0.94 0x1E14	<a href="#">55</a>
TON_DELAY	0x60	Time from CONTROL pin and/or OPERATION command = ON to V <sub>OUT_ENn</sub> pin = ON.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	<a href="#">60</a>
TON_RISE	0x61	Time from when the V <sub>OUT_ENn</sub> pin goes high until the LTC2971 optionally soft-connects its DAC and begins to servo the output voltage to the desired value.	R/W Word	Y	L11	ms	Y	10.0 0xD280	<a href="#">60</a>
TON_MAX_FAULT_LIMIT	0x62	Maximum time from V <sub>OUT_ENn</sub> = ON assertion that an UV condition will be tolerated before a TON_MAX_FAULT condition results.	R/W Word	Y	L11	ms	Y	15.0 0xD3C0	<a href="#">60</a>

## PMBus Command Summary

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT (Note 1)	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX (Note 2)	REF PAGE
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	<a href="#">67</a>
TOFF_DELAY	0x64	Time from CONTROL pin and/or OPERATION command = OFF to V <sub>OUT_ENN</sub> pin = OFF	R/W Word	Y	L11	ms	Y	1.0 0xBA00	<a href="#">60</a>
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R Byte	Y	Reg			NA	<a href="#">71</a>
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R Word	Y	Reg			NA	<a href="#">71</a>
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R Byte	Y	Reg			NA	<a href="#">72</a>
STATUS_IOUT	0x7B	Output current fault and warning status.	R Byte	Y	Reg			NA	<a href="#">72</a>
STATUS_INPUT	0x7C	Input supply fault and warning status.	R Byte	N	Reg			NA	<a href="#">72</a>
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMPERATURE_1.	R Byte	Y	Reg			NA	<a href="#">73</a>
STATUS_CML	0x7E	Communication and memory fault and warning status.	R Byte	N	Reg			NA	<a href="#">73</a>
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R Byte	Y	Reg			NA	<a href="#">74</a>
READ_VIN	0x88	Input supply voltage.	R Word	N	L11	V		NA	<a href="#">77</a>
READ_IIN	0x89	DC/DC converter input current.	R Word	N	L11	A		NA	<a href="#">77</a>
READ_VOUT	0x8B	DC/DC converter output voltage.	R Word	Y	L16	V		NA	<a href="#">77</a>
READ_IOUT	0x8C	DC/DC converter output current.	R Word	Y	L11	A		NA	<a href="#">78</a>
READ_TEMPERATURE_1	0x8D	External diode junction temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	°C		NA	<a href="#">78</a>
READ_TEMPERATURE_2	0x8E	Internal junction temperature.	R Word	N	L11	°C		NA	<a href="#">78</a>
READ_POUT	0x96	DC/DC converter output power.	R Word	Y	L11	W		NA	<a href="#">79</a>
READ_PIN	0x97	DC/DC converter input power.	R Word	N	L11	W		NA	<a href="#">77</a>
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.1.	R Byte	N	Reg			0x11	<a href="#">90</a>
USER_DATA_00	0xB0	Manufacturer reserved for LTpowerPlay.	R/W Word	N	Reg		Y	NA	<a href="#">91</a>
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA	<a href="#">91</a>
USER_DATA_02	0xB2	OEM Reserved.	R/W Word	N	Reg		Y	NA	<a href="#">91</a>
USER_DATA_03	0xB3	Scratchpad location.	R/W Word	Y	Reg		Y	0x0000	<a href="#">91</a>
USER_DATA_04	0xB4	Scratchpad location.	R/W Word	N	Reg		Y	0x0000	<a href="#">91</a>
MFR_FIRST_FAULT	0xB5	First fault information.	R Word	N	Reg			NA	<a href="#">76</a>
MFR_INFO	0xB6	Manufacturer specific information.	R Word	N	Reg			NA	<a href="#">91</a>
MFR_STATUS_2	0xB7	Manufacturer specific status.	R Word	Y	Reg			NA	<a href="#">76</a>
MFR_T_SELF_HEAT	0xB8	Calculated temperature rise due to self-heating of output current sense device above value measured by external temperature sensor.	R Word	Y	L11	°C		NA	<a href="#">58</a>
MFR_IOUT_CAL_GAIN_TAU_INV	0xB9	Inverse of time constant for Mfr_t_self_heat changes scaled by $4 \cdot t_{CONV\_SENSE}$ .	R/W Word	Y	L11		Y	0.0 0x8000	<a href="#">58</a>



## PMBus COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT (Note 1)	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX (Note 2)	REF PAGE
MFR_IOUT_CAL_GAIN_THETA	0xBA	Thermal resistance from inductor core to point measured by external temperature sensor.	R/W Word	Y	L11	°C/W	Y	0.0 0x8000	<a href="#">58</a>
MFR_READ_IOUT	0xBB	Alternate data format for READ_IOUT. One LSB = 2.5mA.	R Word	Y	CF	2.5mA		NA	<a href="#">79</a>
MFR_LTC_RESERVED_2	0xBC	Manufacturer reserved.	R/W Word	Y	Reg			NA	<a href="#">91</a>
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA	<a href="#">49</a>
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA	<a href="#">49</a>
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA	<a href="#">49</a>
MFR_EIN	0xC0	Input Energy data bytes.	R Block	N	Reg			NA	<a href="#">51</a>
MFR_EIN_CONFIG	0xC1	Configuration register for energy and input current.	R/W Byte	N	Reg		Y	0x00	<a href="#">52</a>
MFR_SPECIAL_LOT	0xC2	Customer dependent codes that identify the factory programmed user configuration stored in EEPROM. Contact factory for default value.	R Byte	Y	Reg		Y	NA	<a href="#">91</a>
MFR_IIN_CAL_GAIN_TC	0xC3	Temperature coefficient applied to IIN_CAL_GAIN.	R/W Word	N	CF	ppm	Y	0x0000	<a href="#">53</a>
MFR_IIN_PEAK	0xC4	Maximum measured value of READ_IIN.	R Word	N	L11	A		NA	<a href="#">78</a>
MFR_IIN_MIN	0xC5	Minimum measured value of READ_IIN.	R Word	N	L11	A		NA	<a href="#">78</a>
MFR_PIN_PEAK	0xC6	Maximum measured value of READ_PIN.	R Word	N	L11	W		NA	<a href="#">78</a>
MFR_PIN_MIN	0xC7	Minimum measured value of READ_PIN.	R Word	N	L11	W		NA	<a href="#">78</a>
MFR_COMMAND_PLUS	0xC8	Alternate access to block read and other data. Commands for all additional hosts.	R/W Word	N	Reg			0x0000	<a href="#">35</a>
MFR_DATA_PLUS0	0xC9	Alternate access to block read and other data. Data for additional host 0.	R/W Word	N	Reg			0x0000	<a href="#">35</a>
MFR_DATA_PLUS1	0xCA	Alternate access to block read and other data. Data for additional host 1.	R/W Word	N	Reg			0x0000	<a href="#">35</a>
MFR_PG_CONFIG	0xCB	PG pin configuration.	R/W Word	Y	Reg		Y	0xC046	<a href="#">62</a>
MFR_CLEAR_ENERGY	0xCC	Clear MFR_EIN time and energy values.	Send Byte	N				NA	<a href="#">53</a>
MFR_DAC_STARTUP	0xCD	DAC output code used at start-up.	R/W Word	Y	Reg		Y	0x0000	<a href="#">55</a>
MFR_PG_GPO	0xCE	PG pin output data register.	R/W Byte	Y	Reg		Y	0x00	<a href="#">64</a>
MFR_CONFIG_LTC2971	0xD0	Configuration bits that are channel specific.	R/W Word	Y	Reg		Y	0x0080	<a href="#">40</a>
MFR_CONFIG_ALL_LTC2971	0xD1	Configuration bits that are common to both pages.	R/W Word	N	Reg		Y	0x007B	<a href="#">46</a>
MFR_FAULTB0_PROPAGATE	0xD2	Configuration that determines if a channel's faulted OFF state is propagated to the FAULTB0 pin.	R/W Byte	Y	Reg		Y	0x00	<a href="#">69</a>
MFR_FAULTB1_PROPAGATE	0xD3	Configuration that determines if a channel's faulted OFF state is propagated to the FAULTB1 pin.	R/W Byte	Y	Reg		Y	0x00	<a href="#">69</a>

## PMBus COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT (Note 1)	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX (Note 2)	REF PAGE
MFR_PWRGD_EN	0xD4	Configuration that maps WDI/RESETB status and individual channel power good to the PWRGD pin.	R/W Word	N	Reg		Y	0x0000	<a href="#">64</a>
MFR_FAULTB0_RESPONSE	0xD5	Action to be taken by the device when the FAULTB0 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	<a href="#">69</a>
MFR_FAULTB1_RESPONSE	0xD6	Action to be taken by the device when the FAULTB1 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	<a href="#">69</a>
MFR_IOUT_PEAK	0xD7	Maximum measured value of READ_IOUT.	R Word	Y	L11	A		NA	<a href="#">80</a>
MFR_IOUT_MIN	0xD8	Minimum measured value of READ_IOUT.	R Word	Y	L11	A		NA	<a href="#">81</a>
MFR_CONFIG2_LTC2971	0xD9	Configuration bits that are channel specific.	R/W Byte	N	Reg		Y	0x00	<a href="#">43</a>
MFR_CONFIG3_LTC2971	0xDA	Configuration bits that are channel specific.	R/W Byte	N	Reg		Y	0x00	<a href="#">43</a>
MFR_RETRY_DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	N	L11	ms	Y	200 0xF320	<a href="#">68</a>
MFR_RESTART_DELAY	0xDC	Delay from actual CONTROL active edge to virtual CONTROL active edge.	R/W Word	N	L11	ms	Y	400 0xFB20	<a href="#">61</a>
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT.	R Word	Y	L16	V		NA	<a href="#">80</a>
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN.	R Word	N	L11	V		NA	<a href="#">80</a>
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	<a href="#">80</a>
MFR_DAC	0xE0	The code of the 10-bit DAC.	R/W Word	Y	Reg			NA	<a href="#">56</a>
MFR_POWERGOOD_ASSERTION_DELAY	0xE1	PWRGD pin output assertion delay.	R/W Word	N	L11	ms	Y	100 0xEB20	<a href="#">64</a>
MFR_WATCHDOG_T_FIRST	0xE2	First watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	<a href="#">65</a>
MFR_WATCHDOG_T	0xE3	Watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	<a href="#">65</a>
MFR_PAGE_FF_MASK	0xE4	Configuration defining which channels respond to global page commands (PAGE=0xFF).	R/W Byte	N	Reg		Y	0x03	<a href="#">35</a>
MFR_PADS	0xE5	Current state of selected digital I/O pads.	R/W Word	N	Reg			NA	<a href="#">74</a>
MFR_I2C_BASE_ADDRESS	0xE6	Base value of the I <sup>2</sup> C/SMBus address byte.	R/W Byte	N	Reg		Y	0x5C	<a href="#">35</a>
MFR_SPECIAL_ID	0xE7	Manufacturer code for identifying the LTC2971.	R Word	N	Reg		Y	LTC2971 0x032X LTC2971-1 0x033X LTC2971-2 0x034X LTC2971-3 0x035X	<a href="#">90</a>
MFR_IIN_CAL_GAIN	0xE8	The nominal resistance of the input current sense element in mΩ.	R/W Word	N	L11	mΩ	Y	1.0 0xBA00	<a href="#">53</a>
MFR_VOUT_DISCHARGE_THRESHOLD	0xE9	Coefficient used to multiply VOUT_COMMAND in order to determine V <sub>OUT</sub> off threshold voltage.	R/W Word	Y	L11		Y	2.0 0xC200	<a href="#">55</a>
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA	<a href="#">82</a>
MFR_FAULT_LOG_RESTORE	0xEB	Command a transfer of the fault log previously stored in EEPROM back to RAM.	Send Byte	N				NA	<a href="#">82</a>

## PMBus COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT (Note 1)	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX (Note 2)	REF PAGE
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks.	Send Byte	N				NA	<a href="#">82</a>
MFR_FAULT_LOG_STATUS	0xED	Fault logging status.	R Byte	N	Reg		Y	NA	<a href="#">82</a>
MFR_FAULT_LOG	0xEE	Fault log data bytes. This sequentially retrieved data is used to assemble a complete fault log.	R Block	N	Reg		Y	NA	<a href="#">82</a>
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			NA	<a href="#">75</a>
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient applied to IOUT_CAL_GAIN.	R/W Word	Y	CF	ppm	Y	0x0000	<a href="#">57</a>
MFR_RETRY_COUNT	0xF7	Retry count for all faulted off conditions that enable retry.	R/W Byte	N	Reg		Y	0x07	<a href="#">68</a>
MFR_TEMP_1_GAIN	0xF8	Inverse of external diode temperature non ideality factor. One LSB = $2^{-14}$ .	R/W Word	Y	CF		Y	1 0x4000	<a href="#">58</a>
MFR_TEMP_1_OFFSET	0xF9	Offset value for the external temperature.	R/W Word	Y	L11	°C	Y	0 0x8000	<a href="#">58</a>
MFR_IOUT_SENSE_VOLTAGE	0xFA	Absolute value of the voltage between I <sub>OUT_SNSPn</sub> and I <sub>OUT_SNSMn</sub> . One LSB = 3.05µV or 91.5µV.	R Word	Y	CF	3.05µV		NA	<a href="#">80</a>
MFR_VOUT_MIN	0xFB	Minimum measured value of READ_VOUT.	R Word	Y	L16	V		NA	<a href="#">80</a>
MFR_VIN_MIN	0xFC	Minimum measured value of READ_VIN.	R Word	N	L11	V		NA	<a href="#">80</a>
MFR_TEMPERATURE_1_MIN	0xFD	Minimum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	<a href="#">81</a>

### Note 1: Data Formats

L11	Linear_5s_11s	<p>PMBus data field b[15:0]. Value = <math>Y \cdot 2^N</math> where <math>N = b[15:11]</math> is a 5-bit two's complement integer and <math>Y = b[10:0]</math> is an 11-bit two's complement integer. Example: READ_VIN = 10V For <math>b[15:0] = 0xD280 = 1101\_0010\_1000\_0000b</math> Value = <math>640 \cdot 2^{-6} = 10</math> See PMBus Rev 1.1 Spec Part II: Paragraph 7.1.</p>
L16	Linear_16u	<p>PMBus data field b[15:0]. Value = <math>Y \cdot 2^N</math> where <math>Y = b[15:0]</math> is an unsigned integer and <math>N = Vout\_mode\_parameter</math> is a 5-bit two's complement exponent that is hardwired to -10 decimal. The LTC2971-3 Channel 1 has a -13 decimal. Example: VOUT_COMMAND = 4.75V For <math>b[15:0] = 0x1300 = 0001\_0011\_0000\_0000b</math> Value = <math>4864 \cdot 2^{-10} = 4.75</math> See PMBus Rev 1.1 Spec Part II: Paragraph 8.3.1.</p>
Reg	Register	<p>PMBus data field b[15:0] or b[7:0]. Bit field meaning is defined in detailed PMBus Command Register Description.</p>
CF	Custom Format	<p>PMBus data field b[15:0]. Value is defined in detailed PMBus Command Register Description. This is often an unsigned or two's complement integer scaled by an MFR specific constant.</p>

**Note 2:** When two default values are shown, the first default value applies to LTC2971, LTC2971-1, LTC2971-2, and LTC2971-3 Channel 0. The second default value applies to LTC2971-3 Channel 1.

## PMBus COMMAND DESCRIPTION

### ADDRESSING AND WRITE PROTECT

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
PAGE	0x00	Channel or page currently selected for any command that supports paging.	R/W Byte	N	Reg			0x00	<a href="#">33</a>
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	<a href="#">34</a>
MFR_I2C_BASE_ADDRESS	0xE6	Base value of the I <sup>2</sup> C/SMBus address byte.	R/W Byte	N	Reg		Y	0x5C	<a href="#">35</a>
MFR_PAGE_FF_MASK	0xE4	Configuration defining which channels respond to global page commands (PAGE=0xFF).	R/W Byte	N	Reg		Y	0x03	<a href="#">35</a>
MFR_COMMAND_PLUS	0xC8	Alternate access to block read and other data. Commands for all additional hosts.	R/W Word	N	Reg				<a href="#">35</a>
MFR_DATA_PLUS0	0xC9	Alternate access to block read and other data. Data for additional host 0.	R/W Word	N	Reg				<a href="#">35</a>
MFR_DATA_PLUS1	0xCA	Alternate access to block read and other data. Data for additional host 1.	R/W Word	N	Reg				<a href="#">35</a>

### PAGE

The LTC2971 has two pages that correspond to the two DC/DC converter channels that can be managed. Each DC/DC converter channel can be uniquely programmed by first setting the appropriate page.

Setting PAGE = 0xFF allows a simultaneous write to both pages for PMBus commands that support global page programming. The only commands that support PAGE = 0xFF are CLEAR\_FAULTS, OPERATION and ON\_OFF\_CONFIG. See MFR\_PAGE\_FF\_MASK for additional options. Reading any paged PMBus register with PAGE = 0xFF returns unpredictable data and will trigger a CML fault. Writes to paged commands that do not support PAGE = 0xFF with PAGE = 0xFF will be ignored and generate a CML fault.

### PAGE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Page	Page operation. 0x00: All PMBus commands address channel/page 0. 0x01: All PMBus commands address channel/page 1. 0xXX: All non specified values reserved. 0xFF: A single PMBus write/send to commands that support this mode will simultaneously address all channel/pages with MFR_PAGE_FF_MASK enabled.

## PMBus COMMAND DESCRIPTION

### WRITE\_PROTECT

The WRITE\_PROTECT command provides protection against accidental programming of the LTC2971 command registers. All supported commands may have their parameters read, regardless of the WRITE\_PROTECT setting, and the EEPROM contents can also be read regardless of the WRITE\_PROTECT settings.

There are two levels of protection:

- Level 1: Nothing can be changed except the level of write protection itself. Values can be read from both pages. This setting can be stored to EEPROM.
- Level 2: Nothing can be changed except for the level of protection, channel ON/OFF state, clearing of faults and energy, and PG pin general-purpose output force states. Values can be read from both pages. This setting can be stored to EEPROM.

#### WRITE\_PROTECT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Write_protect[7:0]	1000_0000b: Level 1 Protection – Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, STORE_USER_ALL and MFR_COMMAND_PLUS commands. 0100_0000b: Level 2 Protection – Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, STORE_USER_ALL, OPERATION, MFR_COMMAND_PLUS, MFR_PAGE_FF_MASK, MFR_CLEAR_ENERGY, MFR_PG_GPO, and CLEAR_FAULTS commands. 0000_0000b: Enable writes to all commands. xxxx_xxxx b: All other values reserved.

### WRITE PROTECT Pin

The WP pin allows the user to write-protect the LTC2971's configuration registers. The WP pin is active high, and when asserted it provides Level 2 protection: all writes are disabled except to the WRITE\_PROTECT, PAGE, MFR\_EE\_UNLOCK, STORE\_USER\_ALL, OPERATION, MFR\_COMMAND\_PLUS, MFR\_PAGE\_FF\_MASK, CLEAR\_FAULTS, MFR\_PG\_GPO, and MFR\_CLEAR\_ENERGY commands. The most restrictive setting between the WP pin and WRITE\_PROTECT command will override. For example if WP = 1 and WRITE\_PROTECT = 0x80, then the WRITE\_PROTECT command overrides, since it is the most restrictive.

WP Pin State	WRITE_PROTECT Command Value	Write Protect Level
Low	0x00	No write protection
	0x40	Level 2
	0x80	Level 1
High	0x00	Level 2
	0x40	Level 2
	0x80	Level 1

## PMBus COMMAND DESCRIPTION

### ***MFR\_PAGE\_FF\_MASK***

The MFR\_PAGE\_FF\_MASK command is used to select which channels respond when the global page command (PAGE = 0xFF) is in use.

#### **MFR\_PAGE\_FF\_MASK Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:2]	Reserved	Always returns 0000b
b[1]	Mfr_page_ff_mask_chan1	Channel 1 masking of global page command (PAGE=0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses
b[0]	Mfr_page_ff_mask_chan0	Channel 0 masking of global page command (PAGE = 0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses

### ***MFR\_I2C\_BASE\_ADDRESS***

The MFR\_I2C\_BASE\_ADDRESS command determines the base value for the I<sup>2</sup>C/SMBus address byte. Offsets of 0 to 8 are added to this base address to generate the device I<sup>2</sup>C/SMBus address. The part responds to the device address. For example, with the factory default MFR\_I2C\_BASE\_ADDRESS of 0x5C, with both ASEL1 and ASEL0 High (Offset N = 8), the device address would be 0x5C + 8 = 0x64.

#### **MFR\_I2C\_BASE\_ADDRESS Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7]	Reserved	Read only, always returns 0.
b[6:0]	I2C_base_address	This 7-bit value determines the base value of the 7-bit I <sup>2</sup> C/SMBus address. See Device Address in the <a href="#">Operation</a> section.

### ***MFR\_COMMAND\_PLUS***

#### ***MFR\_DATA\_PLUS0 and MFR\_DATA\_PLUS1***

#### ***MFR\_STATUS\_PLUS0, and MFR\_STATUS\_PLUS1***

Similar to the PAGE register, these registers allow the user to indirectly address memory. These registers are useful to advanced users for reading or writing memory as described below.

Command Plus operations use a sequence of word commands to support the following:

- An alternate method for reading block data using sequential standard word reads.
- A peek operation that allows up to two additional hosts to read an internal register using PMBus word protocol where each host has a unique page.
- A poke operation that allows up to two additional hosts to write an internal register using PMBus word protocol where each host has a unique page.
- Peek, Poke and Command Plus block reads do not interfere with normal PMBus accesses or page values set by PAGE. This enables multi master support for up to 3 hosts.

## PMBus COMMAND DESCRIPTION

### MFR\_COMMAND\_PLUS Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Mfr_command_plus_reserved	Reserved. Always returns 0.
b[14]	Mfr_command_plus_id	Command plus host ID 0: Mfr_command_plus pointer and page are cached and used for all Mfr_data_plus0 accesses. 1: Mfr_command_plus pointer and page are cached and used for all Mfr_data_plus1 accesses.
b[13:9]	Mfr_command_plus_page	Page to be used when peeking or poking via Mfr_data_plus0 or Mfr_data_plus1. Allowed values are 0 through 3. This page value is cached separately for Mfr_data_plus0 and Mfr_data_plus1 based on the value of Mfr_command_plus_id when this register is written.
b[8:0]	Mfr_command_plus_pointer	Internal memory location accessed by Mfr_data_plus0 or Mfr_data_plus1. Mfr_data_plus0 and Mfr_data_plus1 pointers are cached separately. Legal values are listed in the CMD Code column of the PMBus COMMAND SUMMARY table. All other values are reserved, except for the special poke enable/disable values listed in the Enabling And Disabling Poke <a href="#">Operations</a> section, and the command values listed below for Mfr_status_plus0 and Mfr_status_plus1.

### MFR\_DATA\_PLUS0 and MFR\_DATA\_PLUS1 Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_data_plus0 Mfr_data_plus1	A read from this register returns data referenced by the last matching Mfr_command_plus write. More specifically, writes to Mfr_command_plus by host 0 update Mfr_data_plus0, and writes to Mfr_command_plus by host1 update Mfr_data_plus1. Multiple sequential reads while pointer = Mfr_fault_Log return the complete contents of the block read buffer. Block reads beyond the end of buffer return zeros.  A write to this register will transfer the data to the location referenced by the last matching Mfr_command_plus_pointer when the Poke operation protocol described in the Poke <a href="#">Operation</a> Using Mfr_data_plus0 section is followed.

### MFR\_STATUS\_PLUS0 and MFR\_STATUS\_PLUS1 Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:2]	Reserved	
b[1]	Mfr_status_plus_poke_failed0 Mfr_status_plus_poke_failed1	Status of most recent poke for matching host. 0: Last poke operation did not fail. 1: Last poke operation failed because pokes were not enabled as described in Enabling and Disabling Poke <a href="#">Operations</a> section.
b[0]	Mfr_status_plus_block_peek_failed0 Mfr_status_plus_block_peek_failed1	Status of most recent block peek for matching host. 0: Last block peek was not aborted. 1: Last block peek was aborted due to an intervening fault log EEPROM write, MFR_FAULT_LOG_STORE command, or standard PMBus block read of MFR_FAULT_LOG. The intervening operation is always completed cleanly.

MFR\_STATUS\_PLUS0 is at command location 0x2C, and MFR\_STATUS\_PLUS1 is at command location 0x2D. These correspond to reserved PMBus command locations. These two status registers can only be read via Command Plus peeks.

### Reading Fault Log Using Command Plus and MFR\_DATA\_PLUS0

Write Mfr\_command\_plus\_pointer = 0xEE with Mfr\_command\_plus\_page = 0 and Mfr\_command\_plus\_id = 0.

Read data from Mfr\_data\_plus0; each read returns the next data word of the MFR\_FAULT\_LOG command:

- The first word read is Byte\_count[15:0] = 0x00FF.



## PMBus COMMAND DESCRIPTION

- The next set of words read is the Preamble with 2 bytes packed into a word. Refer to the Fault Log section for details.
- The next set of words read is the Cyclical Loop Data with 2 bytes per word. Refer to the Fault Log section for details.
- Extra reads return zero.
- Interleaved PMBus word and byte commands do not interfere with an ongoing Command Plus block read.
- Interleaved PMBus block reads of MFR\_FAULT\_LOG will interrupt this command.

Check status to be sure the data just read was all valid:

- Write `Mfr_command_plus_pointer = 0x2C` with `Mfr_command_plus_page = 0` and `Mfr_command_plus_id = 0`.
- Read data from `Mfr_data_plus0` and confirm that `Mfr_status_plus_block_peek_failed0 = 0`.

### Reading Energy Using MFR\_COMMAND\_PLUS and MFR\_DATA\_PLUS0

Write `Mfr_command_plus_pointer = 0xC0` with `Mfr_command_plus_page = 0` and `Mfr_command_plus_id = 0`.

Read data from `Mfr_data_plus_0`; each read returns the next data word of the MFR\_EIN command:

- `Byte_count[15:0] = 0x000C`
- `Energy_value[15:0]`
- `Energy_value[31:16]`
- `Energy_value[47:32]`
- `Energy_time[15:0]`
- `Energy_time[31:16]`
- `Energy_time[47:32]`

### Peek Operation Using MFR\_DATA\_PLUS0

Internal words and bytes may be read using Command Plus:

Write `Mfr_command_plus_pointer = CMD_CODE` with `Mfr_command_plus_page = page` and `Mfr_command_plus_id = 0`.

The `CMD_CODE`'s are listed in the PMBus COMMAND SUMMARY table.

Read data from `Mfr_data_plus0`. Data is always read using a word read. Byte data is returned with upper byte set to 0.

### Enabling and Disabling Poke Operations

Poke operations to `Mfr_data_plus0` are enabled by writing `Mfr_command_plus = 0x0BF6`.

Poke operations to `Mfr_data_plus0` are disabled by writing `Mfr_command_plus = 0x01F6`.

Poke operations to `Mfr_data_plus1` are enabled by writing `Mfr_command_plus = 0x4BF6`.

Poke operations to `Mfr_data_plus1` are disabled by writing `Mfr_command_plus = 0x41F6`.

## PMBus COMMAND DESCRIPTION

### Poke Operation Using Mfr\_data\_plus0

Internal words and bytes may be written using Command Plus:

Enable poke access for Mfr\_data\_plus0. This need only be done once after a power-up or WDI reset.

Write Mfr\_command\_plus\_pointer = CMD\_CODE with Mfr\_command\_plus\_page = page and Mfr\_command\_plus\_id = 0.

The CMD\_CODEs are listed in the PMBus COMMAND SUMMARY table.

Write the new data value to MFR\_DATA\_PLUS0

Optionally check status to be sure data was written as desired:

- Write Mfr\_command\_plus\_pointer = 0x2C with Mfr\_command\_plus\_page = 0 and Mfr\_command\_plus\_id = 0.
- Read data from Mfr\_data\_plus0 and confirm that Mfr\_status\_plus\_poke\_failed0 = 0.

### Command Plus Operations Using MFR\_DATA\_PLUS1

All the previous operations may be accessed via Mfr\_data\_plus1 by substituting Mfr\_command\_plus\_id value with a 1. Poke operations must be enabled for Mfr\_data\_plus1.

## ON/OFF CONTROL, MARGINING AND CONFIGURATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
OPERATION	0x01	Operating mode control. On/Off, Margin High and Margin Low.	R/W Byte	Y	Reg		Y	0x00	<a href="#">39</a>
ON_OFF_CONFIG	0x02	CONTROL pin and PMBus ON/OFF command setting.	R/W Byte	Y	Reg		Y	0x12	<a href="#">40</a>
MFR_CONFIG_LTC2971	0xD0	Configuration bits that are channel specific.	R/W Word	Y	Reg		Y	0x0080	<a href="#">40</a>
MFR_CONFIG2_LTC2971	0xD9	Configuration bits that are channel specific.	R/W Byte	N	Reg		Y	0x00	<a href="#">43</a>
MFR_CONFIG3_LTC2971	0xDA	Configuration bits that are channel specific.	R/W Byte	N	Reg		Y	0x00	<a href="#">43</a>
MFR_CONFIG_ALL_LTC2971	0xD1	Configuration bits that are common to both pages.	R/W Word	N	Reg		Y	0x007B	<a href="#">46</a>

## PMBus COMMAND DESCRIPTION

### OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the CONTROL pin and ON\_OFF\_CONFIG. This command register responds to the global page command (PAGE = 0xFF). The contents and functions of the data byte are shown in the following tables. A minimum  $t_{OFF\_MIN}$  wait time must be observed between any OPERATION commands used to turn the unit off and then back on.

#### OPERATION Data Contents (On\_off\_config\_use\_pmbus = 1)

SYMBOL	Action	Operation_control[1:0]	Operation_margin[1:0]	Operation_fault[1:0]	Reserved (Read Only)
BITS		b[7:6]	b[5:4]	b[3:2]	b[1:0]
FUNCTION	Turn off immediately	00	XX	XX	00
	Sequence on	10	00	XX	00
	Margin low (ignore faults and warnings)	10	01	01	00
	Margin low	10	01	10	00
	Margin high (ignore faults and warnings)	10	10	01	00
	Margin high	10	10	10	00
	Sequence off with margin to nominal	01	00	XX	00
	Sequence off with margin low (ignore faults and warnings)	01	01	01	00
	Sequence off with margin low	01	01	10	00
	Sequence off with margin high (ignore faults and warnings)	01	10	01	00
	Sequence off with margin high	01	10	10	00
	Reserved	All remaining combinations			

#### OPERATION Data Contents (On\_off\_config\_use\_pmbus = 0)

##### On or Off

SYMBOL	Action	Operation_control[1:0]	Operation_margin[1:0]	Operation_fault[1:0]	Reserved (Read Only)
BITS		b[7:6]	b[5:4]	b[3:2]	b[1:0]
FUNCTION	Output at nominal	00, 01 or 10	00	XX	00
	Margin low (ignore faults and warnings)	00, 01 or 10	01	01	00
	Margin low	00, 01 or 10	01	10	00
	Margin high (ignore faults and warnings)	00, 01 or 10	10	01	00
	Margin high	00, 01 or 10	10	10	00
	Reserved	All remaining combinations			

## PMBus COMMAND DESCRIPTION

### ON\_OFF\_CONFIG

The ON\_OFF\_CONFIG command configures the combination of CONTROL pin input and PMBus commands needed to turn the LTC2971 on/off, including the power-on behavior, as shown in the following table. This command register responds to the global page command (PAGE = 0xFF). After the part has initialized, an additional comparator monitors VIN\_SNS. The VIN\_ON threshold must be exceeded before the output power sequencing can begin. After V<sub>IN</sub> is initially applied, the part will typically require t<sub>INIT</sub> to initialize and begin the TON\_DELAY timer. The readback of voltages and currents may require an additional wait for t<sub>UPDATE\_ADC</sub>. A minimum t<sub>OFF\_MIN</sub> wait time must be observed for any CONTROL pin used toggle to turn the unit off and then back on.

#### ON\_OFF\_CONFIG Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:5]	Reserved	Don't care. Always returns 0.
b[4]	On_off_config_controlled_on	Control default autonomous power up operation. 0: Unit powers up regardless of the CONTROL pin or OPERATION value. Unit always powers up with sequencing. To turn unit on without sequencing, set TON_DELAY = 0. 1: Unit does not power up unless commanded by the CONTROL pin and/or the OPERATION command on the serial bus. If On_off_config[3:2] = 00, the unit never powers up.
b[3]	On_off_config_use_pmbus	Controls how the unit responds to commands received via the serial bus. 0: Unit ignores the <a href="#">Operation_control</a> [1:0]. 1: Unit responds to <a href="#">Operation_control</a> [1:0]. Depending on On_off_config_use_control, the unit may also require the CONTROL pin to be asserted for the unit to start.
b[2]	On_off_config_use_control	Controls how unit responds to the CONTROL pin. 0: Unit ignores the CONTROL pin. 1: Unit requires the CONTROL pin to be asserted to start the unit. Depending on On_off_config_use_pmbus the OPERATION command may also be required to instruct the device to start.
b[1]	Reserved	Not supported. Always returns 1.
b[0]	On_off_config_control_fast_off	CONTROL pin turn off action when commanding the unit to turn off. 0: Use the programmed TOFF_DELAY. 1: Turn off the output and stop transferring energy as quickly as possible. The device does not sink current in order to decrease the output voltage fall time.

### MFR\_CONFIG\_LTC2971

This command is used to configure various manufacturer specific operating parameters for each channel.

#### MFR\_CONFIG\_LTC2971 Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Mfr_config_track_en	Select if channel is a slave in a tracked power supply system. 0: Channel is not a slave in a tracked power supply system. 1: Channel is a slave in a tracked power supply system. Setting this bit disables UV detection during TOFF_DELAY.
b[14]	Mfr_config_cascade_on	Configures channel's control pin for cascade sequence ON. There is no provision for cascade sequence OFF. See description for time based sequence OFF options.

## PMBus COMMAND DESCRIPTION

### MFR\_CONFIG\_LTC2971 Data Contents

BIT(S)	SYMBOL	OPERATION
b[13:12]	Mfr_config_controln_sel	Selects the active control pin input (CONTROL0 , CONTROL1) for this channel. 00: Select CONTROL0 pin. 01: Select CONTROL1 pin. 10: Reserved. 11: Reserved.
b[11]	Mfr_config_fast_servo_off	Disables fast servo when margining or trimming output voltages: 0: fast-servo enabled. 1: fast-servo disabled.
b[10]	Mfr_config_supervisor_resolution	Selects voltage supervisor resolution: 0: high resolution = 35.2mV/LSB, range for $ V_{OUT\_SNSn} - GND_{SNSn} $ is 0V to 34V; = 1.6mV/LSB, range for LTC2971-3 $ V_{OUT\_SNS1} - GND_{SNS1} $ is 0V to 1.5V 1: low resolution = 70.4mV/LSB, range for $ V_{OUT\_SNSn} - GND_{SNSn} $ is 0V to 60V; = 3.2mV/LSB, range for LTC2971-3 $ V_{OUT\_SNS1} - GND_{SNS1} $ is 0V to 1.8V
b[9]	Reserved	Always returns 0.
b[8]	Mfr_config_imon_sel	Select input range of Current Sense Channel: 0: DCR Sense telemetry mode, Range for $V_{IOUT\_SNSPn} - V_{IOUT\_SNSMn}$ is -80mV to +80mV 1: Buffered IMON telemetry mode, Range for $V_{IOUT\_SNSPn} - V_{IOUT\_SNSMn}$ is -0.1V to +1.8V
b[7]	Mfr_config_servo_continuous	Select whether the UNIT should continuously servo $V_{OUT}$ after it has reached a new margin or nominal target. Only applies when Mfr_config_dac_mode = 00b. 0: Do not continuously servo $V_{OUT}$ after reaching initial target. 1: Continuously servo $V_{OUT}$ to target.
b[6]	Mfr_config_servo_on_warn	Control re-servo on warning feature. Only applies when Mfr_config_dac_mode = 00b and Mfr_config_servo_continuous = 0. 0: Do not allow the unit to re-servo when a $V_{OUT}$ warning threshold is met or exceeded. 1: Allow the unit to re-servo $V_{OUT}$ to nominal target if $V_{OUT} \geq V(V_{out\_ov\_warn\_limit})$ or $V_{OUT} \leq V(V_{out\_uv\_warn\_limit})$ .
b[5:4]	Mfr_config_dac_mode	Determines how DAC is used when channel is in the ON state and TON_RISE has elapsed. 00: Soft-connect (if needed) and servo to target. 01: DAC not connected. 10: DAC connected immediately using value from MFR_DAC command. If this is the configuration after a reset or RESTORE_USER_ALL, The value in MFR_DAC_STARTUP will be used to set the DAC output. 11: DAC is soft-connected. After soft-connect is complete MFR_DAC may be written.
b[3]	Reserved	Always set to 1.
b[2]	Mfr_config_vo_en_wpd_en	VOUT_EN current-limited pull-down enable. 0: Use a fast N-channel device to pull down VOUT_EN pin when the channel is off for any reason. 1: Use weak current-limited pull-down to discharge VOUT_EN pin when channel is off due to soft stop by the CONTROL pin and/or OPERATION command. If the channel is off due to a fault, use the fast pull-down on the VOUT_EN pin.

## PMBus COMMAND DESCRIPTION

### MFR\_CONFIG\_LTC2971 Data Contents

BIT(S)	SYMBOL	OPERATION
b[1]	Mfr_config_dac_gain	DAC buffer gain. 0: Select DAC buffer gain dac_gain_0 (1.38V full-scale). 1: Select DAC buffer gain dac_gain_1 (2.65V full-scale).
b[0]	Mfr_config_dac_pol	DAC output polarity. 0: Encodes negative (inverting) DC/DC converter trim input. 1: Encodes positive (non-inverting) DC/DC converter trim input.

### Cascade Sequence ON with Time-Based Sequence OFF

Cascade sequence ON allows a master power supply to sequence on a series of slave supplies by connecting each power supply's power good output, or the LTC2971's configured PG pin, to the control pin of the next power supply, or LTC2971 channel, in the chain. Please note that the LTC2971's PWRGD pin should not be used for cascade sequencing. Power good based cascade sequence OFF is not supported, OFF sequencing must be managed using immediate or time based sequence OFF. See also Tracking Based Sequencing section.

Cascade sequence ON is illustrated in [Figure 14](#). For each slave channel Mfr\_config\_cascade\_on is asserted high and the associated control input is connected to the power good output of the previous power supply. In this configuration each slave channel's startup is delayed until the previous supply has powered up.

Cascade sequence OFF is not directly supported. Options for reversing the sequence when turning the supplies off include:

- Using the OPERATION command to turn off all the channels with an appropriate off delay.
- Using the FAULT pin to bring all the channels down immediately or in sequence with an appropriate off delay.

When asserted, Mfr\_config\_cascade\_on enables a slave channel to honor fault retries even when its control pin is low. Additionally, if the system has faulted off after zero or a finite number of retries, an OPERATION command may be used to turn all cascade channels off then on to clear the faulted OFF state when the slave's control pin is low. For this reason we refer to the control pin as being redefined as a sequence pin.

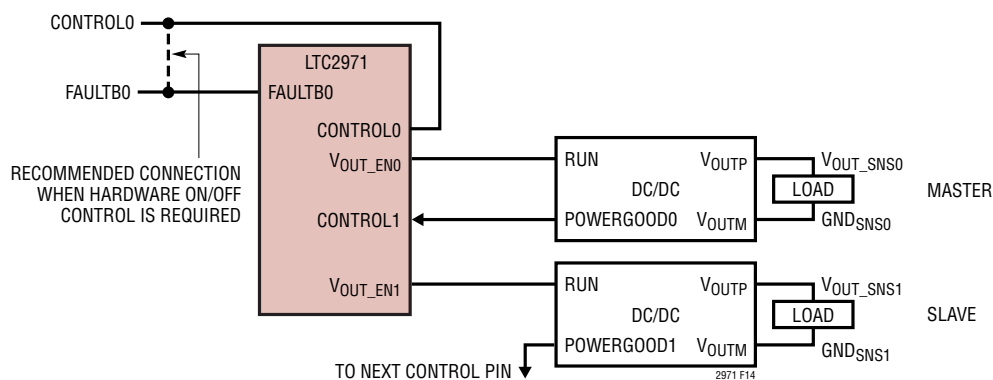


Figure 14. LTC2971 Configured to Cascade Sequence ON and Time-Base Sequence OFF

## PMBus COMMAND DESCRIPTION

The waveform of Figure 15 illustrates cascade sequence ON and time based sequence OFF using the configuration illustrated in Figure 14. In this example the FAULTB0 pin is used as a broadcast off signal. Turning the system off with the FAULTB0 requires all slave channels to be configured with `Mfr_faultb0_response_chann` asserted high. After the system is turned off, the LTC2971 will assert ALERTB with all slave channels indicating a `Status_mfr_fault0_in` event.

### MFR\_CONFIG2\_LTC2971

This command register determines whether  $V_{OUT}$  overvoltage faults from a given channel cause the AUXFAULTB pin to be pulled low.

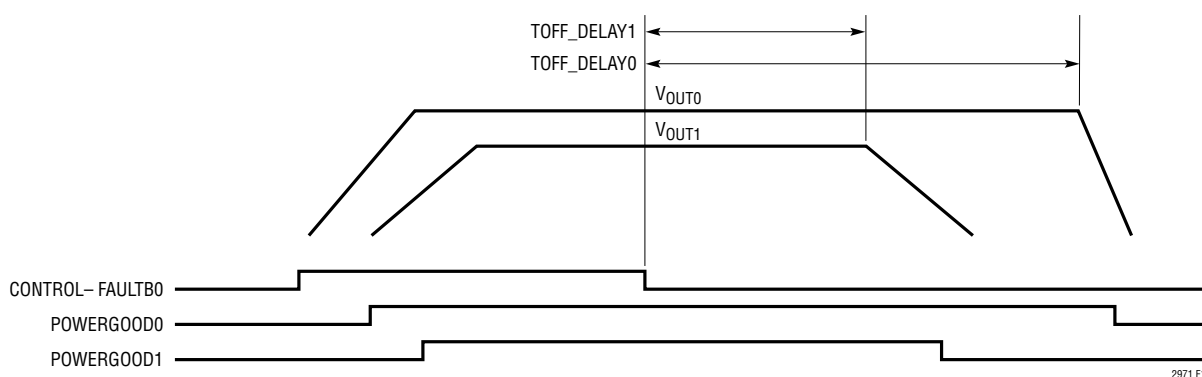


Figure 15. Cascade Sequence ON with Time Based Sequence Down on FAULT0

### MFR\_CONFIG2\_LTC2971 Data Contents

BIT(S)	SYMBOL	OPERATION
b[1]	<code>Mfr_auxfaultb_ov_fault_response_chan1</code>	Response to channel 1 $V_{OUT\_OV\_FAULT}$ . 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[0]	<code>Mfr_auxfaultb_ov_fault_response_chan0</code>	Response to channel 0 $V_{OUT\_OV\_FAULT}$ . 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.

### MFR\_CONFIG3\_LTC2971

This command register determines whether  $V_{OUT}$  undervoltage faults from a given channel cause the AUXFAULTB pin to be pulled low.

### MFR\_CONFIG3\_LTC2971 Data Contents

BIT(S)	SYMBOL	OPERATION
b[1]	<code>Mfr_auxfaultb_uv_fault_response_chan1</code>	Response to channel 1 $V_{OUT\_UV\_FAULT}$ . 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[0]	<code>Mfr_auxfaultb_uv_fault_response_chan0</code>	Response to channel 0 $V_{OUT\_UV\_FAULT}$ . 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.

## PMBus COMMAND DESCRIPTION

### Tracking Supplies On and Off

The LTC2971 supports tracking power supplies that are equipped with a tracking pin and configured for tracking. A tracking power supply uses a secondary feedback terminal (TRACK) to allow its output voltage to be scaled to an external master voltage. Typically the external voltage is generated by the supply with the highest voltage in the system, which is fed to the slave track pins (see [Figure 16](#)). Supplies that track a master supply must be enabled before the master supply comes up and disabled after the master supply comes down. Enabling the slave supplies when the master is down requires supervisors monitoring the slaves to disable UV detection. Both channels configured for tracking must track off together in response to a fault on any channel or any other condition that can bring one or more of the channels down. Prematurely disabling a slave channel via its RUN pin may cause that channel to shut down out of sequence (see [Figure 19](#))

An important feature of the LTC2971 is the ability to control, monitor and supervise DC/DC converters that are configured to track a master supply on and off.

The LTC2971 supports the following tracking features:

- Track channels on and off without issuing false UV events when the slave channels are tracking up or down.
- Track channels down in response to a fault from a slave or master.
- Track channels down when VIN\_SNS drops below VIN\_OFF, share clock is held low or RESTORE\_USER\_ALL is issued.
- Ability to reconfigure selected channels that are part of a tracking group to sequence up after the group has tracked up or sequence down before the group has tracked down.

### Tracking Implementation

The LTC2971 supports tracking through the coordinated programming of Ton\_delay, Ton\_rise, Toff\_delay and Mfr\_config\_track\_en. The master channel must be configured to turn on after all the slave channels have turned on and to turn off before all the slave channels turn off. Slaves that are enabled before the master will remain off until the tracking pin allows them to turn on. Slaves will be turned off via the tracking pin even though their run pin is still asserted. Ton\_rise must be extended on the slaves so that it ends relative to the rise of the TRACK pin and not the rise of the VOUT\_EN pin.

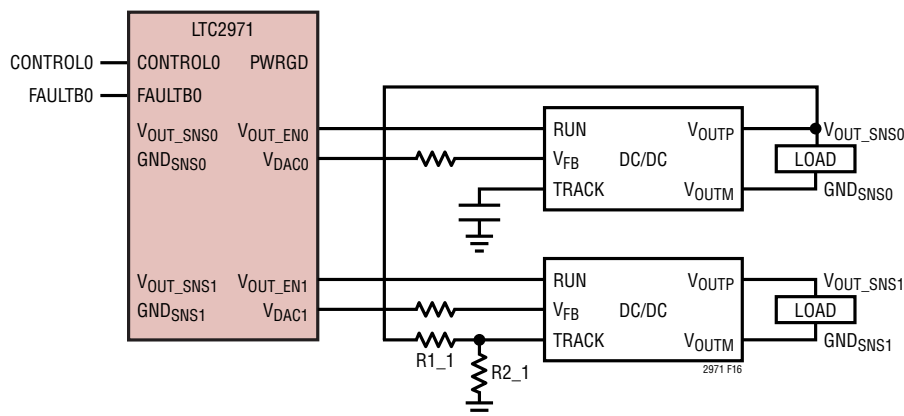


Figure 16. LTC2971 Configured to Control, Supervise and Monitor Power Supplies Equipped with Tracking Pin



## PMBus COMMAND DESCRIPTION

When `Mfr_config_track_en` is enabled the channel is reconfigured to:

- Sequence down on fault, `VIN_OFF`, `SHARE_CLK` low or `RESTORE_USER_ALL`.
- Ignore UV during `TOFF_DELAY`. Note that ignoring UV during `TON_RISE` and `TON_MAX_FAULT` always happens regardless of how this bit is set.

The following example illustrates configuring an LTC2971 with one master channel and one slave.

Master channel 0

`TON_DELAY = Ton_delay_master`

`TON_RISE = Ton_rise_master`

`TOFF_DELAY = Toff_delay_master`

`Mfr_config_track_en = 0`

Slave channel 1

`TON_DELAY = Ton_delay_slave`

`TON_RISE = Ton_delay_master + Ton_rise_slave`

`TOFF_DELAY = Toff_delay_master + T_off_delay_slave`

`Mfr_config_track_en = 1`

Where:

`Ton_delay_master – Ton_delay_slave > RUN to TRACK setup time`

`Toff_delay_slave > time for master supply to fall.`

The system response to a control pin toggle is illustrated in [Figure 17](#).

The system response to a UV fault on a slave channel is illustrated in [Figure 18](#).

## PMBus COMMAND DESCRIPTION

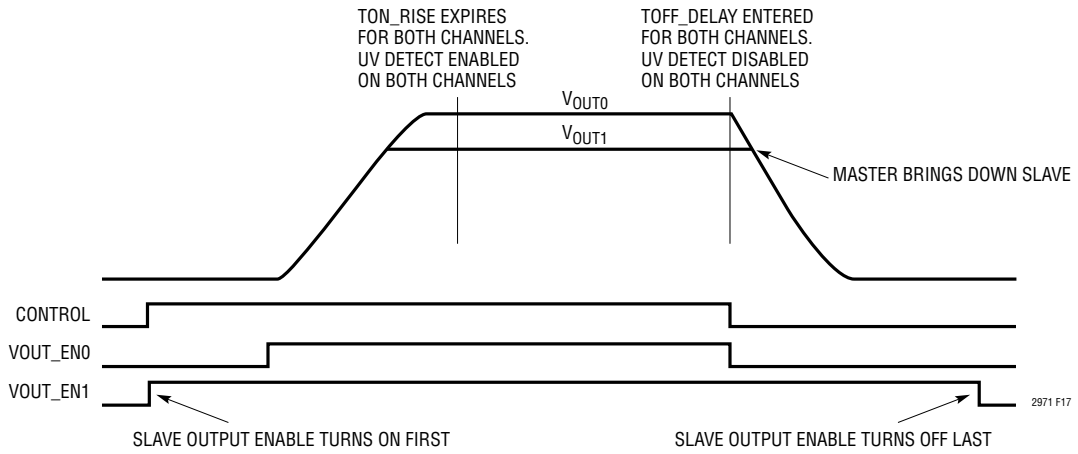
### MFR\_CONFIG\_ALL\_LTC2971

This command is used to configure parameters that are common to both channels on the IC. They may be set or reviewed from any PAGE setting.

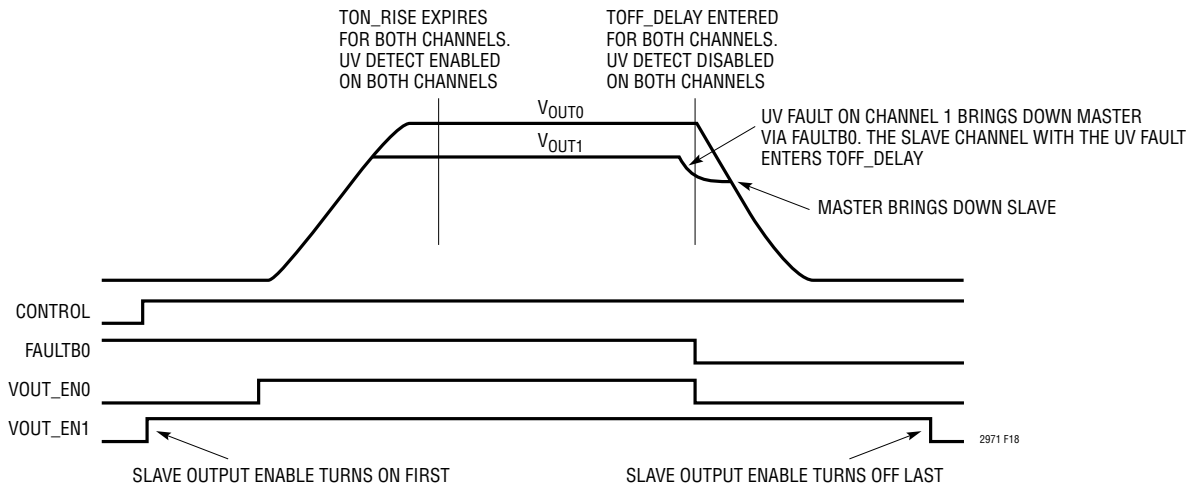
#### MFR\_CONFIG\_ALL\_LTC2971 Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:13]	Reserved	Don't care. Always returns 0.
b[12]	Mfr_config_all_en_short_cycle_fault	Enable short cycle fault detection. See Mfr_status_2_short_cycle_fault on page 76 for more information. 0: Issuing an ON before prior OFF is complete will not cause a fault. 1: Issuing an ON before prior OFF is complete will cause a fault.
b[11]	Mfr_config_all_pwrzd_off_uses_uv	Selects PWRGD de-assertion source for both channels. 0: PWRGD is de-asserted based on $V_{OUT}$ being below or equal to POWER_GOOD_OFF. This option uses the ADC. Response time is approximately 100ms to 200ms. 1: PWRGD is de-asserted based on $V_{OUT}$ being below or equal to VOUT_UV_LIMIT. This option uses the high speed supervisor. Response time is approximately 12 $\mu$ s.
b[10]	Reserved	Don't care.
b[9]	Reserved	Don't care. Always returns 0.
b[8]	Reserved	Don't care. Always returns 0.
b[7]	Mfr_config_all_fault_log_enable	Enable fault logging to EEPROM in response to Fault. 0: Fault logging to EEPROM is disabled. 1: Fault logging to EEPROM is enabled.
b[6]	Mfr_config_all_vin_on_clr_faults_en	Allow VIN_ON rising edge to clear all latched faults. 0: VIN_ON clear faults feature is disabled. 1: VIN_ON clear faults feature is enabled.
b[5]	Mfr_config_all_control1_pol	Selects active polarity of CONTROL1 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).
b[4]	Mfr_config_all_control0_pol	Selects active polarity of CONTROL0 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).
b[3]	Mfr_config_all_vin_share_enable	Allow this unit to hold Share-clock pin low when $V_{IN}$ has not risen above VIN_ON or has fallen below VIN_OFF. When enabled this unit will also turn both channels off in response to Share-clock being held low. 0: Share-clock inhibit is disabled. 1: Share-clock inhibit is enabled.
b[2]	Mfr_config_all_pec_en	PMBus packet error checking enable. 0: PEC is accepted but not required. 1: PEC is enabled.
b[1]	Mfr_config_all_longer_pmbus_timeout	Increase PMBus timeout interval by a factor of 8. Recommended for fault logging. 0: PMBus timeout is not multiplied by a factor of 8. 1: PMBus timeout is multiplied by a factor of 8.
b[0]	Reserved	Always set to 1.

# PMBus COMMAND DESCRIPTION



**Figure 17. Control Pin Tracking All Supplies Up And Down**



**Figure 18. Fault on Channel 1 Tracking All Supplies Down**

## PMBus COMMAND DESCRIPTION

### PROGRAMMING USER EEPROM SPACE

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
STORE_USER_ALL	0x15	Store entire operating memory to EEPROM.	Send Byte	N				NA	<a href="#">48</a>
RESTORE_USER_ALL	0x16	Restore entire operating memory from EEPROM.	Send Byte	N				NA	<a href="#">48</a>
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA	<a href="#">49</a>
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA	<a href="#">49</a>
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA	<a href="#">49</a>

#### ***STORE\_USER\_ALL and RESTORE\_USER\_ALL***

STORE\_USER\_ALL, RESTORE\_USER\_ALL commands provide access to User EEPROM space. Once a command is stored in User EEPROM, it will be restored with explicit restore command, when the part emerges from power-on reset after power is applied, or after toggling the Reset pin. While either of these commands is being processed, the part will indicate it is busy, see Response When Part Is Busy on page [50](#).

STORE\_USER\_ALL. Issuing this command will store all operating memory commands with a corresponding EEPROM memory location.

RESTORE\_USER\_ALL. Issuing this command will restore all commands from EEPROM Memory. It is recommended that this command not be executed while a unit is enabled since all monitoring is suspended while the EEPROM is transferred to operating memory, and intermediate values from EEPROM may not be compatible with the values initially stored in operating memory.

#### **Bulk Programming the User EEPROM Space**

The MFR\_EE\_UNLOCK, MFR\_EE\_ERASE and MFR\_EE\_DATA commands provide a method for 3rd party EEPROM programming houses and end users to easily program the LTC2971 independent of any order dependencies or delays between PMBus commands. All data transfers are directly to and from the EEPROM and do not affect the volatile RAM space currently configuring the device.

The first step is to program a master reference part with the desired configuration. MFR\_EE\_UNLOCK and MFR\_EE\_DATA are then used to read back all the data in User EEPROM space as sequential words. This information is stored to the master programming HEX file. Subsequent parts may be cloned to match the master part using MFR\_EE\_UNLOCK, MFR\_EE\_ERASE and MFR\_EE\_DATA to transfer data from the master HEX file. These commands operate directly on the EEPROM independent of the part configurations stored in RAM space. During EEPROM access the part will indicate that it is busy as described below.

In order to support simple programming fixtures the bulk programming features only uses PMBus word and byte commands. The MFR\_UNLOCK configures the appropriate access mode and resets an internal address pointer allowing a series of word commands to behave as a block read or write with the address pointer being incremented after each operation. PEC use is optional and is configured by the MFR\_EE\_UNLOCK operation.

## PMBus COMMAND DESCRIPTION

### ***MFR\_EE\_UNLOCK***

The MFR\_EE\_UNLOCK command prevents accidental EEPROM access in normal operation and configures the required EEPROM bulk programming mode for bulk initialization, sequential writes, or reads. MFR\_EE\_UNLOCK augments the protection provided by write protect. Upon unlocking the part for the required operation, an internal address pointer is reset allowing a series of MFR\_EE\_DATA reads or writes to sequentially transfer data, similar to a block read or block write. The MFR\_EE\_UNLOCK command can clear or set PEC mode based on the desired level of error protection. An MFR\_EE\_UNLOCK sequence consists of writing two or three unlock codes as described below. The following table documents the allowed sequences. Writing a non-supported sequence locks the part. Reading MFR\_EE\_UNLOCK returns the last byte written or zero if the part is locked.

#### **MFR\_EE\_UNLOCK Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:0]	Mfr_ee_unlock[7:0]	To unlock user EEPROM space for Mfr_ee_erase and Mfr_ee_data read or write operations with PEC allowed: Write 0x2B followed by 0xD4.  To unlock user EEPROM space for Mfr_ee_erase and Mfr_ee_data read or write operations with PEC required: Write 0x2B followed by 0xD5.  To unlock user and manufacturer EEPROM space for Mfr_ee_data read only operations with PEC allowed: Write 0x2B, followed by 0x91 followed by 0xE4.  To unlock user and manufacturer EEPROM space for Mfr_ee_data read only operations with PEC required: Write 0x2B, followed by 0x91 followed by 0xE5.

### ***MFR\_EE\_ERASE***

The MFR\_EE\_ERASE command is used to erase the entire contents of the user EEPROM space and configures this space to accept new program data. Writing values other than 0x2B will lock the part. Reads return the last value written.

#### **MFR\_EE\_ERASE Data contents**

BIT(S)	SYMBOL	OPERATION
b[7:0]	Mfr_ee_erase[7:0]	To erase the user EEPROM space and configure to accept new data: 1) Use the appropriate Mfr_ee_unlock sequence to configure for Mfr_ee_erase commands with or without PEC. 2) Write 0x2B to Mfr_ee_erase.  The part will indicate it is busy erasing the EEPROM by the mechanism detailed below.

### ***MFR\_EE\_DATA***

The MFR\_EE\_DATA command allows the user to transfer data directly to or from the EEPROM without affecting RAM space.

To read the user EEPROM space issue the appropriate Mfr\_ee\_unlock command and perform Mfr\_ee\_data reads until the EEPROM has been completely read. Extra reads will lock the part and return zero. The first read returns the 16-bit EEPROM packing revision ID that is stored in ROM. The second read returns the number of 16-bit words available; this is the number of reads or writes to access all memory locations. Subsequent reads return EEPROM data starting with lowest address.

To write to the user EEPROM space issue the appropriate Mfr\_ee\_unlock and Mfr\_ee\_erase commands followed by successive Mfr\_ee\_data word writes until the EEPROM is full. Extra writes will lock the part. The first write is to the lowest address.

## PMBus COMMAND DESCRIPTION

Mfr\_ee\_data reads and writes must not be mixed.

### MFR\_EE\_DATA Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_ee_data[15:0]	<p>To read user space</p> <ol style="list-style-type: none"> <li>1) Use the appropriate Mfr_ee_unlock sequence to configure for Mfr_ee_data commands with or without PEC.</li> <li>2) Read Mfr_ee_data[0] = PackingId (MFR Specific ID).</li> <li>3) Read Mfr_ee_data[1] = NumberOfUserWords (total number of 16-bit word available).</li> <li>4) Read Mfr_ee_data[2] through Mfr_ee_data[NumberOfWord+1] (User EEPROM data contents).</li> </ol> <p>To write user space</p> <ol style="list-style-type: none"> <li>1) Initialize the user memory using the sequence described for the MFR_EE_ERASE command.</li> <li>2) Use the appropriate Mfr_ee_unlock sequence to configure for Mfr_ee_data commands with or without PEC.</li> <li>3) Write Mfr_ee_data[0] through Mfr_ee_data[NumberOfWord-1] (User EEPROM data content to be written).</li> </ol> <p>The part will indicate it is busy erasing the EEPROM by the mechanism detailed below.</p>

### Response When Part Is Busy

The part will indicate it is busy accessing the EEPROM by the following mechanism:

- 1) Clearing Mfr\_common\_busyb of the MFR\_COMMON register. This byte can always be read and will never NACK a byte read request even if the part is busy.
- 2) NACKing commands other than MFR\_COMMON.

### MFR\_EE Erase and Write Programming Time

The program time per word is typically 0.51ms and will require spacing the I<sup>2</sup>C/SMBus writes at greater than 0.51ms to guarantee the write has completed. The Mfr\_ee\_erase command takes approximately 400ms. We recommend using MFR\_COMMON for handshaking.

### VIN\_ON, VIN\_OFF, VIN\_OV\_FAULT\_LIMIT, VIN\_OV\_WARN\_LIMIT, VIN\_UV\_WARN\_LIMIT and VIN\_UV\_FAULT\_LIMIT

These commands provide voltage supervising limits for the input voltage V<sub>IN\_SNS</sub>.

### INPUT VOLTAGE COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
VIN_ON	0x35	Input voltage above which power conversion can be enabled.	R/W Word	N	L11	V	Y	10.0 0xD280	<a href="#">51</a>
VIN_OFF	0x36	Input voltage below which power conversion is disabled. Both V <sub>OUT_ENn</sub> pins go off immediately or sequence off after TOFF_DELAY (See Mfr_config_track_en).)	R/W Word	N	L11	V	Y	9.0 0xD240	<a href="#">51</a>
VIN_OV_FAULT_LIMIT	0x55	Input overvoltage fault limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	15.0 0xD3C0	<a href="#">51</a>
VIN_OV_WARN_LIMIT	0x57	Input overvoltage warning limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	14.0 0xD380	<a href="#">51</a>
VIN_UV_WARN_LIMIT	0x58	Input undervoltage warning limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	0 0x8000	<a href="#">51</a>
VIN_UV_FAULT_LIMIT	0x59	Input undervoltage fault limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	0 0x8000	<a href="#">51</a>

Rev. 0

## PMBus COMMAND DESCRIPTION

### INPUT CURRENT AND ENERGY

COMMAND NAME		DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_EIN	0xC0	Input energy data bytes.	R Block	N	Reg			NA	<a href="#">51</a>
MFR_EIN_CONFIG	0xC1	Configuration register for energy and input current.	R/W Byte	N	Reg		Y	0	<a href="#">52</a>
MFR_IIN_CAL_GAIN_TC	0xC3	Temperature coefficient applied to IIN_CAL_GAIN.	R/W Word	N	CF	ppm	Y	0x0	<a href="#">53</a>
MFR_IIN_CAL_GAIN	0xE8	The nominal resistance of the current sense element in mΩ.	R/W Word	N	L11	mΩ	Y	1.0 0xBA00	<a href="#">53</a>
MFR_CLEAR_ENERGY	0xCC	Clear MFR_EIN time and energy values	Send Byte	N				NA	<a href="#">53</a>

### Energy Measurement and Reporting

Input energy measurement and monitoring supports the following:

- Input energy derived from the accumulated product of READ\_VIN and READ\_IIN.
- Reporting input energy value as a 48-bit integer in mJ. Returning value in Joules eliminates the need for the host to manage time.
- Reporting input energy time as a 48-bit integer in ms, where input energy time is the elapsed time since energy monitoring was last reset.
- Resetting time and energy accumulators whenever MFR\_EIN\_CONFIG or MFR\_CLEAR\_ENERGY is written.
- Wrapping of time and energy accumulators when full.
- An optional HD mode allowing the user to give priority to energy measurement by forcing the ADC to measure READ\_VIN and READ\_IIN between every other ADC measurement.
- Reporting energy and time values coherently.
- Ability to decrement energy to prevent rectification and accumulation of noise when the channel is off. Energy is not allowed to decrement below zero.

### ***MFR\_EIN***

Read only. This 12-byte data block returns the input energy value and time. Once the block read starts, MFR\_EIN updates are suspended until the block read completes. However, energy and time continue to accumulate internally during block reads.

## PMBus COMMAND DESCRIPTION

**Table 2. MFR\_EIN Data Block Contents**

DATA	BYTE*	DESCRIPTION
Energy_value [7:0]	0	Energy Value in mJ. This is the accumulated energy since Mfr_ein_config or Mfr_clear_energy was last written.
Energy_value [15:8]	1	
Energy_value [23:16]	2	
Energy_value [31:24]	3	
Energy_value [39:32]	4	
Energy_value [47:40]	5	
Energy_time [7:0]	6	Energy Time in ms. This is the elapsed time since Mfr_ein_config or Mfr_clear_energy was last written.
Energy_time [15:8]	7	
Energy_time [23:16]	8	
Energy_time [31:24]	9	
Energy_time [39:32]	10	
Energy_time [47:40]	11	

### ***MFR\_EIN\_CONFIG***

This command configures energy and input current related parameters.

**MFR\_EIN\_CONFIG Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:3]	Mfr_ein_config_reserved	Don't care. Always returns 0.
b[2]	Mfr_ein_config_hd	Optimize ADC polling sequence for higher definition input energy measurement. 0: Standard ADC polling sequence 1: Read_vin and Read_iin measurements are interleaved between every other ADC measurement.
b[1:0]	Mfr_ein_config_reserved	Don't care. Always returns 0.



## PMBus COMMAND DESCRIPTION

### ***MFR\_IIN\_CAL\_GAIN***

The MFR\_IIN\_CAL\_GAIN command is used to set the ratio of the voltage at the input current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the same value as the resistance of the sense resistor (units are expressed in mΩ). MFR\_IIN\_CAL\_GAIN is internally limited to values between 0.01mΩ to 1,000mΩ. The register readback value always returns what was last written and does not reflect internal limiting.

Calculations using IIN\_CAL\_GAIN are:

$$\text{READ\_IIN} = \frac{V_{\text{IIN\_SNSPn}} - V_{\text{IIN\_SNSMn}}}{(\text{MFR\_IIN\_CAL\_GAIN}) \cdot T_{\text{CORRECTION}}}$$

where:

$$T_{\text{CORRECTION}} = [1 + \text{MFR\_IIN\_CAL\_GAIN\_TC} \cdot 1\text{E-6} \cdot (\text{READ\_TEMPERATURE\_2} - 25.0)]$$

Note:

$T_{\text{CORRECTION}}$  is limited by hardware to a value between 0.25 and 4.0.

READ\_TEMPERATURE\_2 is the internal die temperature.

### ***MFR\_IIN\_CAL\_GAIN\_TC***

The MFR\_IIN\_CAL\_GAIN\_TC sets the temperature coefficient of the MFR\_IIN\_CAL\_GAIN register value in ppm/°C. This command uses the internal die temperature.

Refer to MFR\_IIN\_CAL\_GAIN for details on proper usage.

#### **MFR\_IIN\_CAL\_GAIN\_TC Data Contents**

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_iin_cal_gain_tc	16-bit twos complement integer representing the temperature coefficient. Value = Y where Y = b[15:0] is a twos complement number. Example: Mfr_iin_cal_gain_tc = 3900ppm For b[15:0] = 0x0F3C, Value = 3900

### ***MFR\_CLEAR\_ENERGY***

This send byte command clears the accumulated energy and time value in MFR\_EIN and can be written even when the LTC2971 is write-protected with level 2 protection. The LTC2971 may internally delay the application of this command by up to  $t_{\text{UPDATE\_ADC}}$ , in order to avoid corrupting an ongoing energy calculation.

## PMBus COMMAND DESCRIPTION

### OUTPUT VOLTAGE COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE (Note 2)	REF PAGE
VOUT_MODE	0x20	Output voltage data format and mantissa exponent.	R Byte	Y	Reg			2 <sup>-10</sup> 0x16 2 <sup>-13</sup> 0x13	55
VOUT_COMMAND	0x21	Servo target. Nominal DC/DC converter output voltage setpoint.	R/W Word	Y	L16	V	Y	12.0 0x3000 1.0 0x2000	55
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	15.0 0x3C00 4.0 0x8000	55
VOUT_MARGIN_HIGH	0x25	Margin high DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	12.6 0x3266 1.05 0x219A	55
VOUT_MARGIN_LOW	0x26	Margin low DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	11.4 0x2D9A 0.95 0x1E66	55
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	13.2 0x34CD 1.1 0x2333	55
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	12.9 0x339A 1.075 0x2266	55
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	11.1 0x2C66 0.925 0x1D9A	55
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit. Used for Ton_max_fault and PWRGD pin de-assertion.	R/W Word	Y	L16	V	Y	10.8 0x2B33 0.9 0x1CCD	55
POWER_GOOD_ON	0x5E	Output voltage at or above which the PWRGD pin should be asserted.	R/W Word	Y	L16	V	Y	11.52 0x2E14 0.96 0x1EB8	55
POWER_GOOD_OFF	0x5F	Output voltage at or below which the PWRGD pin should be de-asserted when Mfr_config_all_pwrgd_off_uses_uv is clear.	R/W Word	Y	L16	V	Y	11.28 0x2D1F 0.94 0x1E14	55
MFR_VOUT_DISCHARGE_THRESHOLD	0xE9	Coefficient used to multiply VOUT_COMMAND in order to determine V <sub>OUT</sub> off threshold voltage.	R/W Word	Y	L11		Y	2.0 0xC200	55
MFR_DAC	0xE0	Manufacturer register that contains the code of the 10-bit DAC.	R/W Word	N	Reg			0x0000	56
MFR_DAC_STARTUP	0xCD	DAC Output Code Used At Start-up	R/W Word	Y	Reg		Y	0x0000	56

**Note 2:** When two default values are shown, the first default value applies to LTC2971, LTC2971-1, LTC2971-2, and LTC2971-3 Channel 0. The second default value applies to LTC2971-3 Channel 1.

## PMBus COMMAND DESCRIPTION

### *VOUT\_MODE*

This command is read only and specifies the mode and exponent for all commands with a L16 data format. See Data Formats on page 27.

#### **VOUT\_MODE Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:5]	Vout_mode_type	Reports linear mode. Hard-wired to 000b.
b[4:0]	Vout_mode_parameter	Linear mode exponent. 5-bit two's complement integer. Hardwired to 0x16 (–10 decimal) (LTC2971, LTC2971-1, LTC2971-2, LTC2971-3 Page 0). Hardwired to 0x13 (–13 decimal) (LTC2971-3 Page 1).

### *VOUT\_COMMAND, VOUT\_MAX, VOUT\_MARGIN\_HIGH, VOUT\_MARGIN\_LOW, VOUT\_OV\_FAULT\_LIMIT, VOUT\_OV\_WARN\_LIMIT, VOUT\_UV\_WARN\_LIMIT, VOUT\_UV\_FAULT\_LIMIT, POWER\_GOOD\_ON and POWER\_GOOD\_OFF*

These commands provide various servo, margining and supervising limits for a channel's output voltage.

### *MFR\_VOUT\_DISCHARGE\_THRESHOLD*

This register contains the coefficient that multiplies *VOUT\_COMMAND* in order to determine the OFF threshold voltage for the associated output. If the output voltage has not decayed below *MFR\_VOUT\_DISCHARGE\_THRESHOLD* • *VOUT\_COMMAND* prior to the channel being commanded to enter/re-enter the ON state, the Status\_mfr\_discharge bit in the STATUS\_MFR\_SPECIFIC register will be set and the ALERTB pin will be asserted low. In addition, the channel will not enter the ON state until the output has decayed below its off-threshold voltage. Setting this to a value greater than 1.0 effectively disables DISCHARGE\_THRESHOLD checking, allowing the channel to turn back on even if it has not decayed at all.

Other channels can be held-off if a particular output has failed to discharge by using the bidirectional FAULTB<sub>n</sub> pins (refer to the MFR\_FAULTB<sub>n</sub>\_RESPONSE and MFR\_FAULTB<sub>n</sub>\_PROPOGATE registers).

### *MFR\_DAC\_STARTUP*

This command register programs the 10-bit DAC to a specific DAC code when a channel is enabled with the DAC set to connect immediately and servo is disabled (*MFR\_CONFIG\_LTC2971* b[5:4] = 10b). This value is loaded from EEPROM at power-on-reset or after a RESTORE\_USER\_ALL command. After loading, all subsequent DAC values are set by writing to the MFR\_DAC command register. If soft-connect mode is enabled, the value in this register is ignored.

#### **MFR\_DAC\_STARTUP Data Contents**

BIT(S)	SYMBOL	OPERATION
b[15:10]	Reserved	Read only, always returns 0.
b[9:0]	Mfr_dac_startup_val	DAC code value.

## PMBus COMMAND DESCRIPTION

### MFR\_DAC

This command register allows the user to directly program the 10-bit DAC. Manual DAC writes require the channel to be in the ON state, TON\_RISE to have expired and MFR\_CONFIG\_LTC2971 b[5:4] = 10b or 11b. Writing MFR\_CONFIG\_LTC2971 b[5:4] = 10b commands the DAC to hard connect with the value in Mfr\_dac\_direct\_val. Writing b[5:4] = 11b commands the DAC to soft connect. Once the DAC has soft connected, Mfr\_dac\_direct\_val returns the value that allowed the DAC to be connected without perturbing the power supply. MFR\_DAC writes are ignored when MFR\_CONFIG\_LTC2971 b[5:4] = 00b or 01b.

#### MFR\_DAC Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:10]	Reserved	Read only, always returns 0.
b[9:0]	Mfr_dac_direct_val	DAC code value.

### OUTPUT CURRENT COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
IOUT_CAL_GAIN	0x38	The nominal resistance of the current sense element in mΩ.	R/W Word	Y	L11	mΩ	Y	1.0 0xBA00	<a href="#">56</a>
IOUT_CAL_OFFSET	0x39	Offset applied to the current sense measurement in Amps.	R/W Word	Y	L11	A	Y	0.0 0x8000	<a href="#">56</a>
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A		5.0 0xCA80	<a href="#">57</a>
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient applied to IOUT_CAL_GAIN.	R/W Word	Y	CF	ppm	Y	0x0	<a href="#">57</a>

#### IOUT\_CAL\_GAIN and IOUT\_CAL\_OFFSET

The IOUT\_CAL\_GAIN command is used to set the ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the same value as the resistance of the resistor (units are expressed in mΩ). IOUT\_CAL\_GAIN is internally limited to values between 0.01mΩ to 1,000mΩ. The register readback value always returns what was last written and does not reflect internal limiting. IOUT\_CAL\_OFFSET is used to add a current offset from the READ\_IOUT results.

Calculations using IOUT\_CAL\_GAIN and IOUT\_CAL\_OFFSET are:

$$T_{\text{CORRECTION}} = (1 + \text{MFR\_IOUT\_CAL\_GAIN\_TC} \cdot 1\text{E-}6 \cdot (\text{READ\_TEMPERATURE\_1} + \text{MFR\_T\_SELF\_HEAT} - 25.0))$$

$$\text{READ\_IOUT} = \frac{V_{\text{IOUT\_SNSPn}} - V_{\text{IOUT\_SNSMn}}}{(\text{IOUT\_CAL\_GAIN}) \cdot T_{\text{CORRECTION}}} + \text{IOUT\_CAL\_OFFSET}$$

Note: T<sub>CORRECTION</sub> is limited by hardware to a value between 0.25 and 4.0.

READ\_TEMPERATURE\_2 is substituted for READ\_TEMPERATURE\_1 if the associated T<sub>SENSE</sub> network fails to detect a valid temperature. See READ\_TEMPERATURE\_1 for more information.

## PMBus COMMAND DESCRIPTION

### IOUT\_OC\_WARN\_LIMIT

The IOUT\_OC\_WARN\_LIMIT is measured by the LTC2971's ADC.

### MFR\_IOUT\_CAL\_GAIN\_TC

The MFR\_IOUT\_CAL\_GAIN\_TC is a paged command that sets the temperature coefficient of the IOUT\_CAL\_GAIN register value in ppm/°C. This command uses the temperature measured by the external temperature diode for the associated page.

Refer to IOUT\_CAL\_GAIN for details on proper usage.

#### MFR\_IOUT\_CAL\_GAIN\_TC Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_iout_cal_gain_tc	16-bit twos complement integer representing the temperature coefficient. Value = Y where Y = b[15:0] is a twos complement. Example: Mfr_iout_cal_gain_tc = 3900ppm For b[15:0] = 0x0F3C Value = 3900

## EXTERNAL TEMPERATURE COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
OT_FAULT_LIMIT	0x4F	Overtemperature fault limit setting for the external temperature sensor.	R/W Word	Y	L11	°C	Y	65.0 0xEA08	<a href="#">58</a>
OT_WARN_LIMIT	0x51	Overtemperature warning limit for the external temperature sensor	R/W Word	Y	L11	°C	Y	60.0 0xE3C0	<a href="#">58</a>
UT_WARN_LIMIT	0x52	Undertemperature warning limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	0 0x8000	<a href="#">58</a>
UT_FAULT_LIMIT	0x53	Undertemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	-5.0 0xCD80	<a href="#">58</a>
MFR_TEMP_1_GAIN	0xF8	Inverse of external diode temperature non ideality factor. One LSB = $2^{-14}$ .	R/W Word	Y	CF		Y	1 0x4000	<a href="#">58</a>
MFR_TEMP_1_OFFSET	0xF9	Offset value for the external temperature.	R/W Word	Y	L11	°C	Y	0 0x8000	<a href="#">58</a>
MFR_T_SELF_HEAT	0xB8	Calculated temperature rise due to self-heating of output current sense device above value measured by external temperature sensor.	R Word	Y	L11	°C		NA	<a href="#">58</a>
MFR_IOUT_CAL_GAIN_TAU_INV	0xB9	Inverse of time constant for Mfr_t_self_heat changes scaled by $4 \cdot t_{CONV\_SENSE}$ .	R/W Word	Y	L11		Y	0.0 0x8000	<a href="#">58</a>
MFR_IOUT_CAL_GAIN_THETA	0xBA	Thermal resistance from inductor core to point measured by external temperature sensor.	R/W Word	Y	L11	°C/W	Y	0.0 0x8000	<a href="#">58</a>

## PMBus COMMAND DESCRIPTION

### *OT\_FAULT\_LIMIT, OT\_WARN\_LIMIT, UT\_WARN\_LIMIT and UT\_FAULT\_LIMIT*

These commands provide supervising limits for temperature as measured by the external diode.

### *MFR\_TEMP\_1\_GAIN and MFR\_TEMP\_1\_OFFSET*

The MFR\_TEMP\_1\_GAIN command specifies the inverse of the temperature sensor ideality factor. The MFR\_TEMP\_1\_OFFSET allows an offset to be applied to the measured temperature.

Calculations using these paged commands are:

$$\text{READ\_TEMPERATURE\_1} = T_{\text{EXT}} \cdot \text{MFR\_TEMP\_1\_GAIN} - 273.15 + \text{MFR\_TEMP\_1\_OFFSET}$$

where:

$$T_{\text{EXT}} = \text{Measured external temperature in degrees Kelvin.}$$

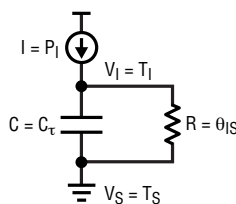
READ\_TEMPERATURE\_2 is substituted for READ\_TEMPERATURE\_1 if the associated T<sub>SENSE</sub> network fails to detect a valid temperature. Under these conditions MFR\_TEMP\_1\_GAIN and MFR\_TEMP\_1\_OFFSET will have no effect. See READ\_TEMPERATURE\_1 for more information.

#### MFR\_TEMP\_1\_GAIN Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_temp_1_gain[15:0]	16-bit integer representing inverse of temperature non-ideality factor. Value = $Y \cdot 2^{14}$ where $Y = b[15:0]$ is an unsigned integer. Example: MFR_TEMP_1_GAIN = 1.0 For b[15:0] = 0x4000 Value = $16384 \cdot 2^{-14} = 1.0$

### *MFR\_T\_SELF\_HEAT, MFR\_IOUT\_CAL\_GAIN\_TAU\_INV and MFR\_IOUT\_CAL\_GAIN\_THETA*

The LTC2971 uses an innovative (US patent 8920026) algorithm to dynamically model the temperature rise from the external temperature sensor to the inductor core. This temperature rise is called MFR\_T\_SELF\_HEAT and is used to calculate the final temperature correction required by IOUT\_CAL\_GAIN. The temperature rise is a function of the power dissipated in the inductor DCR, the thermal resistance from the inductor core to the remote temperature sensor and the thermal time constant of the inductor to board system. The algorithm simplifies the placement requirements for the external temperature sensor and compensates for the significant steady state and transient temperature error from the inductor core to the primary inductor heat sink.



- P<sub>1</sub> = CURRENT REPRESENTING THE POWER DISSIPATED BY THE INDUCTOR (V<sub>DCR</sub> • READ\_IOUT WHERE V<sub>DCR</sub> = (V<sub>IOUT\_SNSP</sub> - V<sub>IOUT\_SNSM</sub>))
- C<sub>t</sub> = CAPACITANCE REPRESENTING THERMAL HEAT CAPACITY OF THE INDUCTOR (INCLUDED IN MFR\_IOUT\_CAL\_GAIN\_TAU\_INV)
- T<sub>1</sub> = VOLTAGE REPRESENTING THE TEMPERATURE OF THE INDUCTOR
- θ<sub>IS</sub> = RESISTANCE REPRESENTING THE THERMAL RESISTANCE FROM THE DCR TO THE REMOTE TEMPERATURE SENSOR (MFR\_IOUT\_CAL\_GAIN\_THETA)
- T<sub>S</sub> = VOLTAGE REPRESENTING THE TEMPERATURE AT THE REMOTE TEMPERATURE SENSOR

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Figure 19. Electronic Analogy for Inductor Temperature Model

## PMBus COMMAND DESCRIPTION

The best way to understand the self-heating effect inside the inductor is to model the system using the circuit analogy of [Figure 19](#). The 1st order differential equation for the above model may be approximated by the following difference equation:

$$P_I - T_I/\theta_{IS} = C_\tau \Delta T_I/\Delta t \text{ (Eq1) (when } T_S = 0)$$

from which:

$$\Delta T_I = \Delta t (P_I \theta_{IS} - T_I)/(\theta_{IS} C_\tau) \text{ (Eq2) or}$$

$$\Delta T_I = (P_I \theta_{IS} - T_I) \cdot \tau_{INV} \text{ (Eq3)}$$

where

$$\tau_{INV} = \Delta t/(\theta_{IS} C_\tau) \text{ (Eq4)}$$

and  $\Delta t$  is the sample period of the external temperature ADC.

The LTC2971 implements the self-heating algorithm using Eq3 and Eq4 where:

$$\Delta T_I = \Delta MFR\_T\_SELF\_HEAT$$

$$P_I = READ\_IOUT \cdot (V_{IOUT\_SNSP} - V_{IOUT\_SNSM})$$

$$T_S = READ\_TEMPERATURE\_1$$

$$T_I = MFR\_T\_SELF\_HEAT + T_S$$

$$\Delta t = 4 \cdot t_{CONV\_SENSE} \text{ (One complete external temperature loop period)}$$

$$\tau_{INV} = MFR\_IOUT\_CAL\_GAIN\_TAU\_INV$$

$$\theta_{IS} = MFR\_IOUT\_CAL\_GAIN\_THETA$$

Initially self heat is set to zero. After each temperature measurement self heat is updated to be the previous value of self heat incremented or decremented by  $\Delta MFR\_T\_SELF\_HEAT$ .

The actual value of  $C_\tau$  is not required. The important quantity is the thermal time constant  $\tau_{INV} = (\theta_{IS} C_\tau)$ . For example, if an inductor has a thermal time constant  $\tau_{INV} = 5$  seconds then:

$$MFR\_IOUT\_CAL\_GAIN\_TAU\_INV = (4 \cdot t_{CONV\_SENSE})/5 = 4 \cdot 66\text{ms}/5\text{s} = 0.0528$$

Refer to the application section for more information on calibrating  $\theta_{IS}$  and  $\tau_{INV}$ .

READ\_TEMPERATURE\_2 is substituted for READ\_TEMPERATURE\_1 if the associated  $T_{SENSE}$  network fails to detect a valid temperature. Under these conditions  $T_S = READ\_TEMPERATURE\_2$  and the self-heating correction is applied using the internal die temperature. See READ\_TEMPERATURE\_1 for more information.

### MFR\_T\_SELF\_HEAT Data Content

Bit(s)	Symbol	Operation
b[15:0]	Mfr_t_self_heat	Values are limited to the range 0°C to 50°C.

### MFR\_IOUT\_CAL\_GAIN\_THETA Data Content

Bit(s)	Symbol	Operation
b[15:0]	Mfr_iout_cal_gain_theta	Values $\leq 0$ set MFR_T_SELF_HEAT to zero.

## PMBus COMMAND DESCRIPTION

### MFR\_IOUT\_CAL\_GAIN\_TAU\_INV Data Content

Bit(s)	Symbol	Operation
b[15:0]	Mfr_iout_cal_gain_tau_inv	Values $\leq 0$ set MFR_T_SELF_HEAT to zero. Values $\geq 1$ set MFR_T_SELF_HEAT to $\text{MFR\_IOUT\_CAL\_GAIN\_THETA} \cdot \text{READ\_IOUT} \cdot (V_{\text{IOUT\_SNSP}} - V_{\text{IOUT\_SNSM}})$ .

### SEQUENCING TIMING LIMITS AND CLOCK SHARING

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
TON_DELAY	0x60	Time from CONTROL pin and/or OPERATION command = ON to $V_{\text{OUT\_EN}n}$ pin = ON.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	<a href="#">60</a>
TON_RISE	0x61	Time from when the $V_{\text{OUT\_EN}n}$ pin goes high until the LTC2971 optionally soft-connects its DAC and begins to servo the output voltage to the desired value.	R/W Word	Y	L11	ms	Y	10.0 0xD280	<a href="#">60</a>
TON_MAX_FAULT_LIMIT	0x62	Maximum time from $V_{\text{OUT\_EN}n}$ pin on assertion that an UV condition will be tolerated before a TON_MAX_FAULT condition results.	R/W Word	Y	L11	ms	Y	15.0 0xD3C0	<a href="#">60</a>
TOFF_DELAY	0x64	Time from CONTROL pin and/or OPERATION command = OFF to $V_{\text{OUT\_EN}n}$ pin = OFF	R/W Word	Y	L11	ms	Y	1.0 0xBA00	<a href="#">60</a>
MFR_RESTART_DELAY	0xDC	Delay from actual CONTROL active edge to virtual CONTROL active edge.	R/W Word	N	L11	ms	Y	400 0xFB20	<a href="#">61</a>

### ***TON\_DELAY, TON\_RISE, TON\_MAX\_FAULT\_LIMIT and TOFF\_DELAY***

These commands share the same format and provide sequencing and timer fault and warning delays in ms.

TON\_DELAY sets the amount of time in milliseconds that a channel waits following the start of an ON sequence before its  $V_{\text{OUT\_EN}}$  pin enables a DC/DC converter. This delay is counted using SHARE\_CLK only.

TON\_RISE sets the amount of time in ms that elapses after the power supply has been enabled until the LTC2971's DAC soft connects and servos the output voltage to the desired level if Mfr\_dac\_mode = 00b. This delay is counted using SHARE\_CLK only.

TON\_MAX\_FAULT\_LIMIT is the maximum amount of time that the power supply being controlled by the LTC2971 can attempt to power up the output without reaching the  $V_{\text{OUT\_UV\_FAULT\_LIMIT}}$ . If it does not, then a TON\_MAX\_FAULT is declared. If the output reaches  $V_{\text{OUT\_UV\_FAULT\_LIMIT}}$  prior to TON\_MAX\_FAULT\_LIMIT, the LTC2971 unmask the  $V_{\text{OUT\_UV\_FAULT\_LIMIT}}$  threshold. (Note that a value of zero means there is no limit to how long the power supply can attempt to bring up its output voltage.) This delay is counted using SHARE\_CLK only.

TOFF\_DELAY is the amount of time that elapses after the CONTROL pin and/or OPERATION command is de-asserted until the channel is disabled (soft-off). This delay is counted using SHARE\_CLK if available, otherwise the internal oscillator is used.

TON\_DELAY and TOFF\_DELAY are internally limited to 13.1 seconds, and rounded to the nearest 10 $\mu$ s when smaller than 655ms, or rounded to the nearest 200 $\mu$ s when larger than 655ms. TON\_RISE and TON\_MAX\_FAULT\_LIMIT are internally limited to 655ms, and rounded to the nearest 10 $\mu$ s. The read value of these commands always returns what was last written and does not reflect internal limiting.



## PMBus COMMAND DESCRIPTION

### MFR\_RESTART\_DELAY

This command essentially sets the off time of a CONTROL pin initiated restart. If the CONTROL pin is toggled off for at least 10 $\mu$ s then on, all dependent channels are disabled, held off for a time = Mfr\_restart\_delay, then sequenced back on. CONTROL pin transitions whose OFF time exceeds Mfr\_restart\_delay are not affected by this command. A value of all zeros disables this feature. This delay is counted using SHARE\_CLK only.

This delay is internally limited to 13.1 seconds, and rounded to the nearest 200 $\mu$ s. The read value of this command always returns what was last written and does not reflect internal limiting.

### Clock Sharing

Multiple ADI PMBus devices can synchronize their clocks in an application by connecting together the open-drain SHARE\_CLK input/outputs to a pull-up resistor as a wired OR. In this case the fastest clock will take over and synchronize all other chips to its falling edge.

SHARE\_CLK can optionally be used to synchronize ON/OFF dependency on  $V_{IN}$  across multiple chips by setting the Mfr\_config\_all\_vin\_share\_enable bit of the MFR\_CONFIG\_ALL register. When configured this way the chip will hold SHARE\_CLK low when the unit is off for insufficient input voltage, and upon detecting that SHARE\_CLK is held low the chip will disable both channels after a brief deglitch period. When the SHARE\_CLK pin is allowed to rise, the chip will respond by beginning a start sequence. In this case the slowest VIN\_ON detection will take over and synchronize other chips to its start sequence.

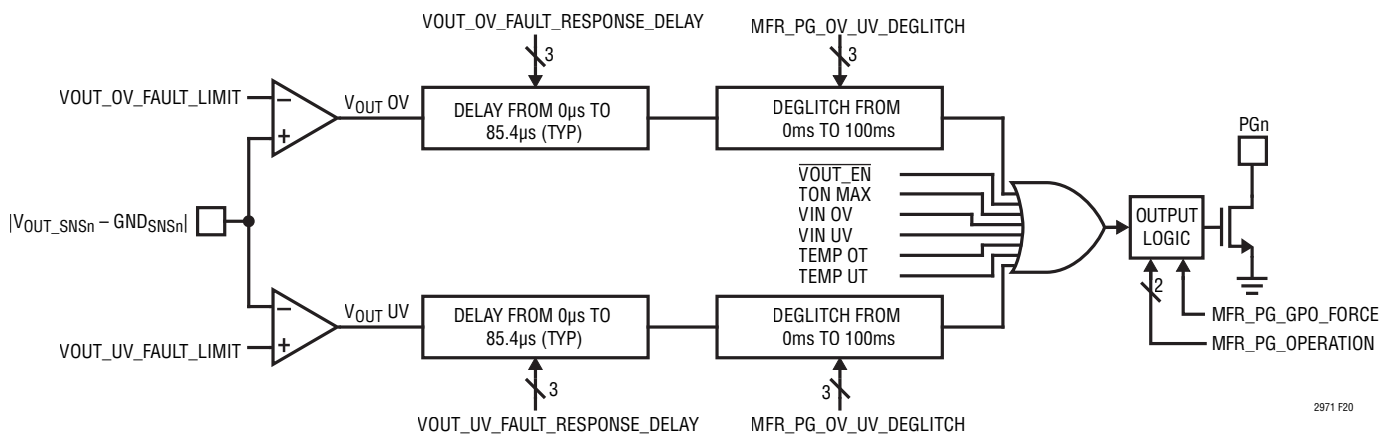
### WATCHDOG TIMER AND POWER GOOD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_PWRGD_EN	0xD4	Configuration that maps WDI/RESETB status and individual channel power good to the PWRGD pin.	R/W Word	N	Reg		Y	0x0000	<a href="#">64</a>
MFR_POWERGOOD_ASSERTION_DELAY	0xE1	Power-good output assertion delay.	R/W Word	N	L11	ms	Y	100 0xEB20	<a href="#">64</a>
MFR_WATCHDOG_T_FIRST	0xE2	First watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	<a href="#">65</a>
MFR_WATCHDOG_T	0xE3	Watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	<a href="#">65</a>
MFR_PG_CONFIG	0xCB	PG pin configuration	R/W Word	Y	Reg		Y	0xC046	<a href="#">62</a>
MFR_PG_GPO	0xCE	PG pin output data register	R/W Byte	Y	Reg		Y	0x00	<a href="#">64</a>

## PMBus COMMAND DESCRIPTION

### MFR\_PG\_CONFIG

The paged MFR\_PG\_CONFIG register defines the output operation of the per channel, open-drain, PG[1:0] pins. Fault signals selected to propagate to the PG pins are independent of their associated fault response masking. The  $V_{OUT}$  overvoltage and  $V_{OUT}$  undervoltage fast comparator signals are deglitched by the values set in the VOUT\_OV\_FAULT\_RESPONSE and VOUT\_UV\_FAULT\_RESPONSE registers respectively, in addition to the deglitching set by the MFR\_PG\_CONFIG register. Any programmed deglitching of the  $V_{OUT}$  overvoltage and undervoltage signals will be effectively disabled if the VOUT\_EN signal is also propagated to PG[1:0] pins. During a power-on-reset, WDI reset, or RESTORE\_USER\_ALL, the PG pins will pull low until the LTC2971 has completed its initialization and all NVM data has been loaded into operating memory regardless of the MFR\_PG\_CONFIG register contents. The MFR\_PG\_CONFIG register is write protected in both Level 1 and Level 2 protection. The PG pins can also be configured as general purpose outputs allowing the user to directly control the PG pin state with values written to the MFR\_PG\_GPO register. The input pin state of the PG pins can be detected by reading the MFR\_PADS register.



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\*SOME DETAILS OMITTED FOR CLARITY, ONLY ONE OF TWO CHANNELS SHOWN

**Figure 20. PG Output Pin Functional Block Diagram**

## PMBus COMMAND DESCRIPTION

### MFR\_PG\_CONFIG Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Mfr_pg_fault_sel_vout_ov	1: Output overvoltage mapped to PG pin with additional deglitching equal to Mfr_pg_ov_uv_deglitch. Only applies if Mfr_pg_operation=10b or 11b. 0: Output overvoltage not mapped to PG pin.
b[14]	Mfr_pg_fault_sel_vout_uv	1: Output undervoltage mapped to PG pin with additional deglitching equal to Mfr_pg_ov_uv_deglitch. Only applies if Mfr_pg_operation=10b or 11b. 0: Output overvoltage not mapped to PG pin.
b[13]	Mfr_pg_fault_sel_iout_oc	Not supported
b[12]	Mfr_pg_fault_sel_iout_uc	Not supported
b[11]	Mfr_pg_fault_sel_temp_ot	1: Overtemperature mapped to PG pin. Only applies if Mfr_pg_operation=10b or 11b. 0: Overtemperature not mapped to PG pin.
b[10]	Mfr_pg_fault_sel_temp_ut	1: Undertemperature mapped to PG pin. Only applies if Mfr_pg_operation=10b or 11b. 0: Undertemperature not mapped to PG pin.
b[9]	Mfr_pg_fault_sel_vin_ov	1: Input overvoltage mapped to PG pin. Only applies if Mfr_pg_operation=10b or 11b. 0: Input overvoltage not mapped to PG pin.
b[8]	Mfr_pg_fault_sel_vin_uv	1: Input undervoltage mapped to PG pin. Only applies if Mfr_pg_operation=10b or 11b. 0: Input undervoltage not mapped to PG pin.
b[7]	Mfr_pg_fault_sel_ton_max	1: TON_MAX_FAULT sequencing fault mapped to PG pin. Only applies if Mfr_pg_operation=10b or 11b. 0: TON_MAX_FAULT sequencing fault not mapped to PG pin.
b[6]	Mfr_pg_fault_sel_vout_en	1: Inverted output enable mapped to PG pin. 0: Inverted output enable not mapped to PG pin.
b[5]	Reserved	Reserved, always returns 0
b[4:2]	Mfr_pg_ov_uv_deglitch	Additional deglitch value for assertion and de-assertion of overvoltage and undervoltage signals to PG: 111b: 100ms 110b: 50ms 101b: 20ms 100b: 10ms 011b: 5ms 010b: 1ms 001b: 200µs 000b: There is no additional deglitch delay applied to the signal
b[1:0]	Mfr_pg_operation	11b: Active Hi-Z propagation of faults according to Mfr_pg_fault_sel 10b: Active low propagation of faults according to Mfr_pg_fault_sel 01b: Reserved 00b: Force PG pin to value set by Mfr_pg_gpo_force in MFR_PG_GPO register

## PMBus COMMAND DESCRIPTION

### ***MFR\_PG\_GPO***

The paged MFR\_PG\_GPO register defines the output logic state of the PG pins if Mfr\_pg\_operation equals 2'b00. This register is write protected during Level 1 protection only.

#### **MFR\_PG\_GPO Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:1]	Reserved	Reserved, always returns 0
b[0]	Mfr_pg_gpo_force	1: Force PG Hi-Z 0: Force PG Low

### ***MFR\_PWRGD\_EN***

This command register controls the mapping of the watchdog and channel power good status to the PWRGD pin.

#### **MFR\_PWRGD\_EN Data Contents**

BIT(S)	SYMBOL	OPERATION
b[15:9]	Reserved	Read only, always returns 0s.
b[8]	Mfr_pwrzd_en_wdog	Watchdog. 1 = Watchdog timer not-expired status is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = Watchdog timer does not affect the PWRGD pin.
b[7:2]	Reserved	Always returns 000000b.
b[1]	Mfr_pwrzd_en_chan1	Channel 1. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.
b[0]	Mfr_pwrzd_en_chan0	Channel 0. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.

### ***MFR\_POWERGOOD\_ASSERTION\_DELAY***

This command register allows the user to program the delay from when the internal power-good signal becomes valid until the PWRGD pin output is asserted. This delay is counted using SHARE\_CLK if available, otherwise the internal oscillator is used. This delay is internally limited to 13.1 seconds, and rounded to the nearest 200µs. The read value of this command always returns what was last written and does not reflect internal limiting.

The PWRGD pin de-assertion delay and threshold source is controlled by Mfr\_config\_all\_pwrzd\_off\_uses\_uv. Systems that require a fast PWRGD pin de-assertion should set Mfr\_config\_all\_pwrzd\_off\_uses\_uv = 1. This uses the VOUT\_UV\_FAULT\_LIMIT and the high speed comparator to de-assert the PWRGD pin. Systems that require a separate power good off threshold should set Mfr\_config\_all\_pwrzd\_off\_uses\_uv = 0. This uses the slower ADC polling loop and POWER\_GOOD\_OFF to de-assert the PWRGD pin.

## PMBus COMMAND DESCRIPTION

### Watchdog Operation

A non-zero write to the MFR\_WATCHDOG\_T register will reset the watchdog timer. Low-to-high transitions on the WDI/RESETB pin also reset the watchdog timer. If the timer expires, ALERTB is asserted and the PWRGD output is optionally de-asserted and then reasserted after MFR\_PWRGD\_ASSERTION\_DELAY ms. Writing 0 to either the MFR\_WATCH\_DOG\_T or MFR\_WATCHDOG\_T\_FIRST registers will disable the timer.

### MFR\_WATCHDOG\_T\_FIRST and MFR\_WATCHDOG\_T

The MFR\_WATCHDOG\_T\_FIRST register allows the user to program the duration of the first watchdog timer interval following assertion of the PWRGD pin, assuming the PWRGD pin reflects the status of the watchdog timer. If assertion of PWRGD is not conditioned by the watchdog timer's status, then MFR\_WATCHDOG\_T\_FIRST applies to the first timing interval after the timer is enabled. Writing a value of 0ms to the MFR\_WATCHDOG\_T\_FIRST register disables the watchdog timer. This delay is internally limited to 65 seconds and rounded to the nearest 1ms.

The MFR\_WATCHDOG\_T register allows the user to program watchdog timer intervals subsequent to the MFR\_WATCHDOG\_T\_FIRST timing interval. Writing a value of 0ms to the MFR\_WATCHDOG\_T register disables the watchdog timer. This delay is internally limited to 655ms and rounded to the nearest 10 $\mu$ s.

Both timers operate on an internal clock independent of SHARE\_CLK. The read value of both commands always returns what was last written and does not reflect internal limiting.

### FAULT RESPONSES

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	<a href="#">66</a>
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0x7F	<a href="#">66</a>
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an overtemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	<a href="#">67</a>
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an undertemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	<a href="#">67</a>
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	N	Reg		Y	0x80	<a href="#">67</a>
VIN_UV_FAULT_RESPONSE	0x5A	Action to be taken by the device when an input undervoltage fault is detected.	R/W Byte	N	Reg		Y	0x00	<a href="#">67</a>
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	<a href="#">67</a>
MFR_RETRY_DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	N	L11	ms	Y	200 0xF320	<a href="#">68</a>
MFR_RETRY_COUNT	0xF7	Retry count for all faulted off conditions that enable retry.	R/W Byte	N	Reg		Y	0x00	<a href="#">55</a>

## PMBus COMMAND DESCRIPTION

### Clearing Latched Faults

Latched faults are reset by toggling the CONTROL pin, using the OPERATION command, or removing and reapplying the bias voltage to the  $V_{IN\_SNS}$  pin. All fault and warning conditions result in the ALERTB pin being asserted low and the corresponding bits being set in the status registers. The CLEAR\_FAULTS command resets the contents of the status registers and de-asserts the ALERTB output. The CLEAR\_FAULTS does not clear a faulted OFF state nor allow a channel to turn back on.

### VOUT\_OV\_FAULT\_RESPONSE and VOUT\_UV\_FAULT\_RESPONSE

The fault response documented here is for voltages that are measured by the high speed supervisor. These voltages are measured over a short period of time and may require a deglitch period. Note that in addition to the response described by these commands, the LTC2971 will also:

- Set the appropriate bit(s) in the STATUS\_BYTE.
- Set the appropriate bit(s) in the STATUS\_WORD.
- Set the appropriate bit in the corresponding STATUS\_VOUT register, and
- Notify the host by pulling the ALERTB pin low.

### VOUT\_OV\_FAULT\_RESPONSE and VOUT\_UV\_FAULT\_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Vout_ov_fault_response_action, Vout_uv_fault_response_action	Response action: 00b: The unit continues operation without interruption. 01b: The unit continues operating for the delay time specified by bits[2:0] in increments of $t_{S\_VS}$ . See <a href="#">Electrical Characteristics</a> Table. If the fault is still present at the end of the delay time, the unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_config_track_en). After shutting down, the device responds according to the retry settings in bits [5:3]. 10b-11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_config_track_en). After shutting down, the device responds according to the retry settings in bits [5:3].
b[5:3]	Vout_ov_fault_response_retry, Vout_uv_fault_response_retry	Response retry behavior: 000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 001b-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Changing the value might not take effect until the next off-then-on sequence on that channel.
b[2:0]	Vout_ov_fault_response_delay, Vout_uv_fault_response_delay	This sample count determines the amount of time a unit is to ignore a fault after it is first detected. Use this delay to deglitch fast faults. 000b: There is no additional deglitch delay applied to fault detection. 001b-111b: The fault is deglitched for deglitch period of b[2:0] samples at a sampling period of $t_{S\_VS}$ (12.2 $\mu$ s typical).

## PMBus COMMAND DESCRIPTION

### *OT\_FAULT\_RESPONSE, UT\_FAULT\_RESPONSE, VIN\_OV\_FAULT\_RESPONSE and VIN\_UV\_FAULT\_RESPONSE*

The fault response documented here is for values that are measured by the ADC. Note that in addition to the response described by these commands, the LTC2971 will also:

- Set the appropriate bit(s) in the STATUS\_BYTE.
- Set the appropriate bit(s) in the STATUS\_WORD.
- Set the appropriate bit in the corresponding STATUS\_VIN or STATUS\_TEMPERATURE register, and
- Notify the host by pulling the ALERTB pin low.

### **OT\_FAULT\_RESPONSE, UT\_FAULT\_RESPONSE, VIN\_OV\_FAULT\_RESPONSE, VIN\_UV\_FAULT\_RESPONSE Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:6]	Ot_fault_response_action, Ut_fault_response_action, Vin_ov_fault_response_action, Vin_uv_fault_response_action	Response action: 00b: The unit continues operation without interruption. 01b-11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_config_track_enh). After shutting down, the device responds according to the retry settings in bits [5:3].
b[5:3]	Ot_fault_response_retry, Ut_fault_response_retry, Vin_ov_fault_response_retry, Vin_uv_fault_response_retry	Response retry behavior: 000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 001b-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Changing the value might not take effect until the next off-then-on sequence on that channel.
b[2:0]	Ot_fault_response_delay, Ut_fault_response_delay, Vin_ov_fault_response_delay, Vin_uv_fault_response_delay	Hard coded to 000b: There is no additional deglitch delay applied to fault detection.

### **TON\_MAX\_FAULT\_RESPONSE**

This command defines the LTC2971 response to a TON\_MAX\_FAULT. It may be used to protect against a short-circuited output at startup. After startup use VOUT\_UV\_FAULT\_RESPONSE to protect against a short-circuited output.

The device also:

- Sets the HIGH\_BYTE bit in the STATUS\_BYTE,
- Sets the V<sub>OUT</sub> bit in the STATUS\_WORD,
- Sets the TON\_MAX\_FAULT bit in the STATUS\_VOUT register, and
- Notifies the host by asserting ALERTB.

## PMBus COMMAND DESCRIPTION

### TON\_MAX\_FAULT\_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Ton_max_fault_response_action	Response action: 00b: The unit continues operation without interruption. 01b-11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_config_track_en). After shutting down, the device responds according to the retry settings in bits [5:3].
b[5:3]	Ton_max_fault_response_retry	Response retry behavior: 000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 001b-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Changing the value might not take effect until the next off-then-on sequence on that channel.
b[2:0]	Ton_max_fault_response_delay	Hard coded to 000b: There is no additional deglitch delay applied to fault detection.

### MFR\_RETRY\_DELAY

This command determines the retry interval when the LTC2971 is in retry mode in response to a fault condition. This delay is counted using SHARE\_CLK only. This delay is internally limited to 13.1 seconds, and rounded to the nearest 200µs. The read value of this command always returns what was last written and does not reflect internal limiting.

### MR\_RETRY\_COUNT

The MFR\_RETRY\_COUNT is a global command that sets the number of retries attempted when any channel faults off with its fault response retry field set to a non zero value.

In the event of multiple or recurring retry faults on the same channel the total number of retries equals MFR\_RETRY\_COUNT. If a channel has not been faulted off for at least 16 seconds, its retry counter is cleared. Toggling a channel's CONTROL pin off then on or issuing OPERATION off then on commands will synchronously clear the retry count.

### MFR\_RETRY\_COUNT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:3]	Reserved	Always returns zero.
b[2:0]	Mfr_retry_count [2:0]	0: No retries: 1-6: Number of retries. 7: Infinite retries. Changing the value might not take effect until the next off-then-on sequence on that channel.



## PMBus COMMAND DESCRIPTION

### SHARED EXTERNAL FAULTS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_FAULTB0_PROPAGATE	0xD2	Configuration that determines if a channel's faulted OFF state is propagated to the FAULTB0 pin.	R/W Byte	Y	Reg		Y	0x00	<a href="#">69</a>
MFR_FAULTB1_PROPAGATE	0xD3	Configuration that determines if a channel's faulted OFF state is propagated to the FAULTB1 pin.	R/W Byte	Y	Reg		Y	0x00	<a href="#">69</a>
MFR_FAULTB0_RESPONSE	0xD5	Action to be taken by the device when the FAULTB0 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	<a href="#">69</a>
MFR_FAULTB1_RESPONSE	0xD6	Action to be taken by the device when the FAULTB1 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	<a href="#">69</a>

### ***MFR\_FAULTB0\_PROPAGATE and MFR\_FAULTB1\_PROPAGATE***

These manufacturer specific commands enable channels that have faulted off to propagate that state to the appropriate fault pin. MFR\_FAULTB0\_PROPAGATE allows any channel's faulted OFF state to propagate to the FAULTB0 pin. MFR\_FAULTB1\_PROPAGATE allows any channel's faulted OFF state to propagate to the FAULTB1 pin.

Note that pulling a fault pin low will have no effect for channels that have MFR\_FAULTBn\_RESPONSE set to 0. The channel continues operation without interruption. This fault response is called Ignore (0x0) in LTpowerPlay.

#### **MFR\_FAULT0\_PROPAGATE Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:1]	Reserved	Don't care. Always returns 0.
b[0]	Mfr_faultb0_propagate	Enable fault propagation. 0: Channel's faulted OFF state does not assert FAULTB0 low. 1: Channel's faulted OFF state asserts FAULTB0 low.

#### **MFR\_FAULT1\_PROPAGATE Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:1]	Reserved	Don't care. Always returns 0.
b[0]	Mfr_faultb1_propagate	Enable fault propagation. 0: Channel's faulted OFF state does not assert FAULTB1 low. 1: Channel's faulted OFF state asserts FAULTB1 low.

### ***MFR\_FAULTB0\_RESPONSE and MFR\_FAULTB1\_RESPONSE***

These manufacturer specific commands share the same format and specify the response to assertions of the FAULTB pins. MFR\_FAULTB0\_RESPONSE determines which channels shut off when the FAULTB0 pin is asserted low and MFR\_FAULTB1\_RESPONSE determines which channels shut off when the FAULTB1 pin is asserted low. When a channel shuts off in response to a FAULTBn pin, the ALERTB pin is asserted low and the appropriate bit is set in the STATUS\_MFR\_SPECIFIC register. For a graphical explanation, see the switches on the left hand side of [Figure 27: Channel Fault Management Block Diagram](#).

Faults will not propagate for channels that have MFR\_FAULTBn\_RESPONSE set to 0: The channel continues operation without interruption. Note that this fault response is called No Action in LTpowerPlay.

## PMBus COMMAND DESCRIPTION

### MFR\_FAULTB0\_RESPONSE and MFR\_FAULTB1\_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:2]	Reserved	Read only, always returns 000000b.
b[1]	Mfr_faultb0_response_chan1, Mfr_faultb1_response_chan1	Channel 1 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding FAULTB pin is still asserted after 10 $\mu$ s. When the FAULTB pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[0]	Mfr_faultb0_response_chan0, Mfr_faultb1_response_chan0	Channel 0 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding FAULTB pin is still asserted after 10 $\mu$ s. When the FAULTB pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.

### FAULT WARNING AND STATUS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	Y				NA	<a href="#">70</a>
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R Byte	Y	Reg			NA	<a href="#">71</a>
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R Word	Y	Reg			NA	<a href="#">71</a>
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R Byte	Y	Reg			NA	<a href="#">72</a>
STATUS_IOUT	0x7B	Output current fault and warning status.	R Byte	Y	Reg			NA	<a href="#">72</a>
STATUS_INPUT	0x7C	Input supply fault and warning status.	R Byte	N	Reg			NA	<a href="#">72</a>
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMPERATURE_1.	R Byte	Y	Reg			NA	<a href="#">73</a>
STATUS_CML	0x7E	Communication and memory fault and warning status.	R Byte	N	Reg			NA	<a href="#">73</a>
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R Byte	Y	Reg			NA	<a href="#">74</a>
MFR_PADS	0xE5	Current state of selected digital I/O pads.	R/W Word	N	Reg			NA	<a href="#">74</a>
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			NA	<a href="#">75</a>
MFR_FIRST_FAULT	0xB6	First fault information	R Word	N	Reg				<a href="#">76</a>
MFR_STATUS_2	0xB7	Manufacturer Specific Status	R Word	Y	Reg			NA	<a href="#">75</a>

### CLEAR\_FAULTS

The CLEAR\_FAULTS command is used to clear status bits that have been set. This command clears all fault and warning bits in all unpagged status registers, and pagged status registers selected by the current PAGE setting. At the same time, the device negates (clears, releases) its contribution to ALERTB.

The CLEAR\_FAULTS command does not cause a unit that has latched off for a fault condition to restart. See Clearing Latched Faults for more information.

If the fault is present after the fault is cleared, the fault status bit will be set again and the host notified by the usual means.

Note: this command responds to the global page command. (PAGE=0xFF)

## PMBus COMMAND DESCRIPTION

### STATUS\_BYTE

The STATUS\_BYTE command returns the summary of the most critical faults or warnings which have occurred, as shown in the following table. STATUS\_BYTE is a subset of STATUS\_WORD and duplicates the same information.

#### STATUS\_BYTE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_byte_busy	Same as Status_word_busy.
b[6]	Status_byte_off	Same as Status_word_off.
b[5]	Status_byte_vout_ov	Same as Status_word_vout_ov.
b[4]	Status_byte_iout_oc	Not supported. Always returns 0.
b[3]	Status_byte_vin_uv	Same as Status_word_vin_uv.
b[2]	Status_byte_temp	Same as Status_word_temp.
b[1]	Status_byte_cml	Same as Status_word_cml.
b[0]	Status_byte_high_byte	Same as Status_word_high_byte.

### STATUS\_WORD

The STATUS\_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate detailed status register.

The low byte of the STATUS\_WORD is the same register as the STATUS\_BYTE command.

#### STATUS\_WORD Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Status_word_vout	An output voltage fault or warning has occurred. See STATUS_VOUT.
b[14]	Status_word_iout	An output current warning has occurred. See STATUS_IOUT.
b[13]	Status_word_input	An input voltage fault or warning has occurred. See STATUS_INPUT.
b[12]	Status_word_mfr	A manufacturer specific fault has occurred. See STATUS_MFR_SPECIFIC.
b[11]	Status_word_power_not_good	The PWRGD pin, if enabled, is negated. Power is not good.
b[10]	Status_word_fans	Not supported. Always returns 0.
b[9]	Status_word_other	Not supported. Always returns 0.
b[8]	Status_word_unknown	Not supported. Always returns 0.
b[7]	Status_word_busy	Device busy when PMBus command received. See OPERATION: Processing Commands.
b[6]	Status_word_off	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. The off-bit is clear if unit is allowed to provide power to the output.
b[5]	Status_word_vout_ov	An output overvoltage fault has occurred.
b[4]	Status_word_iout_oc	Not supported. Always returns 0.
b[3]	Status_word_vin_uv	A $V_{IN}$ undervoltage fault has occurred.
b[2]	Status_word_temp	A temperature fault or warning has occurred. See STATUS_TEMPERATURE.
b[1]	Status_word_cml	A communication, memory or logic fault has occurred. See STATUS_CML.
b[0]	Status_word_high_byte	A fault/warning not listed in b[7:1] has occurred or Status_word_power_not_good = 1.

## PMBus COMMAND DESCRIPTION

### STATUS\_VOUT

The STATUS\_VOUT command returns the summary of the output voltage faults or warnings which have occurred, as shown in the following table:

#### STATUS\_VOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_vout_ov_fault	Overvoltage fault.
b[6]	Status_vout_ov_warn	Overvoltage warning.
b[5]	Status_vout_uv_warn	Undervoltage warning.
b[4]	Status_vout_uv_fault	Undervoltage fault.
b[3]	Status_vout_max_warn	VOUT_MAX warning. An attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command.
b[2]	Status_vout_ton_max_fault	TON_MAX_FAULT sequencing fault.
b[1]	Status_vout_toff_max_warn	Not supported. Always returns 0.
b[0]	Status_vout_tracking_error	Not supported. Always returns 0.

### STATUS\_IOUT

The STATUS\_IOUT command returns the summary of the output current faults or warnings which have occurred, as shown in the following table:

#### STATUS\_IOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_iout_oc_fault	Not supported. Always returns 0.
b[6]	Status_iout_oc_uv_fault	Not supported. Always returns 0.
b[5]	Status_iout_oc_warn	Overcurrent warning.
b[4]	Status_iout_uc_fault	Not supported. Always returns 0.
b[3]	Status_curr_share_fault	Not supported. Always returns 0.
b[2]	Status_pout_power_limiting	Not supported. Always returns 0.
b[1]	Status_pout_overpower_fault	Not supported. Always returns 0.
b[0]	Status_pout_overpower_warn	Not supported. Always returns 0.

### STATUS\_INPUT

The STATUS\_INPUT command returns the summary of the  $V_{IN}$  faults or warnings which have occurred, as shown in the following table:

#### STATUS\_INPUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_input_ov_fault	$V_{IN}$ overvoltage fault.
b[6]	Status_input_ov_warn	$V_{IN}$ overvoltage warning.
b[5]	Status_input_uv_warn	$V_{IN}$ undervoltage warning.
b[4]	Status_input_uv_fault	$V_{IN}$ undervoltage fault.
b[3]	Status_input_off	Unit is off for insufficient input voltage.
b[2]	IIN overcurrent fault	Not supported. Always returns 0.
b[1]	IIN overcurrent warn	Not supported. Always returns 0.
b[0]	PIN overpower warn	Not supported. Always returns 0.

## PMBus COMMAND DESCRIPTION

### STATUS\_TEMPERATURE

The STATUS\_TEMPERATURE command returns the summary of the temperature faults or warnings which have occurred, as shown in the following table. Note that this information is paged and refers to the temperature of the associated external diode.

#### STATUS\_TEMPERATURE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_temperature_ot_fault	Overtemperature fault.
b[6]	Status_temperature_ot_warn	Overtemperature warning.
b[5]	Status_temperature_ut_warn	Undertemperature warning.
b[4]	Status_temperature_ut_fault	Undertemperature fault.
b[3]	Reserved	Reserved. Always returns 0.
b[2]	Reserved	Reserved. Always returns 0.
b[1]	Reserved	Reserved. Always returns 0.
b[0]	Reserved	Reserved. Always returns 0.

### STATUS\_CML

The STATUS\_CML command returns the summary of the communication, memory and logic faults or warnings which have occurred, as shown in the following table:

#### STATUS\_CML Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_cml_cmd_fault	1 = An illegal or unsupported command fault has occurred. 0 = No fault has occurred.
b[6]	Status_cml_data_fault	1 = Illegal or unsupported data received. 0 = No fault has occurred.
b[5]	Status_cml_pec_fault	1 = A packet error check fault has occurred. Note: PEC checking is always active in the LTC2971. Any extra byte received before a STOP will set Status_cml_pec_fault unless the extra byte is a matching PEC byte. 0 = No fault has occurred.
b[4]	Status_cml_memory_fault	1 = A fault has occurred in the EEPROM. 0 = No fault has occurred.
b[3]	Status_cml_processor_fault	Not supported, always returns 0.
b[2]	Reserved	Reserved, always returns 0.
b[1]	Status_cml_pmbus_fault	1 = A communication fault other than ones listed in this table has occurred. This is a catch all category for illegally formed I <sup>2</sup> C/SMBus commands (Example: An address byte with read =1 received immediately after a START). 0 = No fault has occurred.
b[0]	Status_cml_unknown_fault	Not supported, always returns 0.

## PMBus COMMAND DESCRIPTION

### STATUS\_MFR\_SPECIFIC

The STATUS\_MFR\_SPECIFIC command returns manufacturer specific status flags. Bits marked CHANNEL = All are not paged. Bits marked STICKY = Yes stay set until a CLEAR\_FAULTS is issued or the channel is commanded on by the user. Bits marked ALERT = Yes pull ALERTB low when the bit is set. Bits marked OFF = Yes indicate that the event can be configured elsewhere to turn the channel off.

#### STATUS\_MFR\_SPECIFIC Data Contents

BIT(S)	SYMBOL	OPERATION	CHANNEL	STICKY	ALERT	OFF
b[7]	Status_mfr_discharge	1 = A $V_{OUT}$ discharge fault occurred while attempting to enter the ON state. 0 = No $V_{OUT}$ discharge fault has occurred.	Current Page	Yes	Yes	Yes
b[6]	Status_mfr_fault1_in	This channel attempted to turn on while the FAULTB1 pin was asserted low, or this channel has shut down at least once in response to a FAULTB1 pin asserting low since the last CONTROL pin toggle, OPERATION command ON/OFF cycle or CLEAR_FAULTS command.	Current Page	Yes	Yes	Yes
b[5]	Status_mfr_fault0_in	This channel attempted to turn on while the FAULTB0 pin was asserted low, or this channel has shut down at least once in response to a FAULTB0 pin asserting low since the last CONTROL pin toggle, OPERATION command ON/OFF cycle or CLEAR_FAULTS command.	Current Page	Yes	Yes	Yes
b[4]	Status_mfr_servo_target_reached	Servo target has been reached.	Current Page	No	No	No
b[3]	Status_mfr_dac_connected	DAC is connected and driving $V_{DAC}$ pin.	Current Page	No	No	No
b[2]	Status_mfr_dac_saturated	A previous servo operation terminated with maximum or minimum DAC value.	Current Page	Yes	No	No
b[1]	Status_mfr_auxfaultb_faulted_off	AUXFAULTB has been de-asserted due to a $V_{OUT}$ or $I_{OUT}$ fault.	All	No	No	No
b[0]	Status_mfr_watchdog_fault	1 = A watchdog fault has occurred. 0 = No watchdog fault has occurred.	All	Yes	Yes	No

### MFR\_PADS

The MFR\_PADS command provides read-only access of digital pads (pins). The input values are before any deglitching logic.

#### MFR\_PADS Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Mfr_pads_pwrpd_drive	0 = PWRGD pad is being driven low by this chip. 1 = PWRGD pad is not being driven low by this chip.
b[14]	Mfr_pads_alertb_drive	0 = ALERTB pad is being driven low by this chip. 1 = ALERTB pad is not being driven low by this chip.
b[13:12]	Mfr_pads_faultb_drive[1:0]	bit[1] used for FAULTB0 pad, bit[0] used for FAULTB1 pad as follows: 0 = FAULTB pad is being driven low by this chip. 1 = FAULTB pad is not being driven low by this chip.
b[11:10]	Mfr_pads_pg_drive[1:0]	bit[1] used for PG1 pad, bit[0] used for PG0 pad as follows: 0 = $PG_n$ pad is being driven low by this chip 1 = $PG_n$ pad is not being driven low by this chip
b[9:8]	Mfr_pads_asel1[1:0]	11: Logic high detected on ASEL1 input pad. 10: ASEL1 input pad is floating. 01: Reserved. 00: Logic low detected on ASEL1 input pad.

## PMBus COMMAND DESCRIPTION

### MFR\_PADS Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Mfr_pads_asel0[1:0]	11: Logic high detected on ASELO input pad. 10: ASELO input pad is floating. 01: Reserved. 00: Logic low detected on ASELO input pad.
b[5]	Mfr_pads_control1	1: Logic high detected on CONTROL1 pad. 0: Logic low detected on CONTROL1 pad.
b[4]	Mfr_pads_control0	1: Logic high detected on CONTROL0 pad. 0: Logic low detected on CONTROL0 pad.
b[3:2]	Mfr_pads_faultb[1:0]	bit[1] used for FAULTB0 pad, bit[0] used for FAULTB1 pad as follows: 1: Logic high detected on FAULTB pad. 0: Logic low detected on FAULTB pad.
b[1]	Mfr_pads_pg1	1: Logic high detected on PG1 pad. 0: Logic low detected on PG1 pad.
b[0]	Mfr_pads_pg0	1: Logic high detected on PG0 pad. 0: Logic low detected on PG0 pad.

### MFR\_COMMON

This command returns status information for the alert, device busy, share-clock pin (SHARE\_CLK) and the write-protect pin (WP).

This is the only command that may still be read when the LTC2971 is busy processing an EEPROM or other command. It may be polled by the host to determine when the LTC2971 is available to process a PMBus command. A busy device will always acknowledge its address but will NACK the command byte and set Status\_byte\_busy and Status\_word\_busy when it receives a command that it cannot immediately process.

### MFR\_COMMON Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Mfr_common_alertb	Returns alert status. 1: ALERTB is de-asserted high. 0: ALERTB is asserted low.
b[6]	Mfr_common_busyb	Returns device busy status. 1: The device is available to process PMBus commands. 0: The device is busy and will NACK PMBus commands.
b[5:2]	Reserved	Read only, always returns 1s.
b[1]	Mfr_common_share_clk	Returns the status of the share-clock pin. 1: Share-clock pin is being held low. 0: Share-clock pin is active.
b[0]	Mfr_common_write_protect	Returns the status of the write-protect pin. 1: Write-protect pin is high. 0: Write-protect pin is low.

## PMBus COMMAND DESCRIPTION

### MFR\_STATUS\_2

This command returns additional manufacturer specific fault and state information. Bits marked Sticky = Yes are set by the appropriate event and not cleared until the user issues a CLEAR\_FAULTS command or turns the channel back on. Bits marked ALERT = YES assert ALERTB low when they are set. Bits marked Channel = All are not paged.

#### MFR\_STATUS\_2 Data Contents

BIT(S)	SYMBOL	OPERATION	STICKY	ALERT	CHANNEL
b[15:3]	Mfr_status_2_reserved	Read only, always returns 0.			
b[2]	Mfr_status_2_shortcycle_fault	1: This channel was commanded on by user before it finished sequencing off. 0: No short cycle fault has occurred on this channel.	Yes	Yes	Current Page
b[1]	Mfr_status_2_vinen_drive	1: AUXFAULTB pad is being driven low by this chip. 0: AUXFAULTB pad is not being driven low by this chip.	No	No	All
b[0]	Mfr_status_2_vin_caused_off	1: This channel was turned off due to VIN_SNS dropping below the VIN_OFF threshold. 0: VIN_SNS has not caused this channel to turn off.	Yes	No	Current Page

### MFR\_FIRST\_FAULT

The MFR\_FIRST\_FAULT register contains a value that indicates the first observed fault by the LTC2971 that caused a channel to fault off. This value is stored in the fault log and is cleared to 0x0000 by sending either the CLEAR\_FAULTS command or cycling a channel off then on. This register will capture the first observed fault regardless of whether fault logging is enabled. The LTC2971 will store an additional byte into the fault log, FirstFaultTime, that is a snapshot copy of the least significant 8 bits of the shared-timer value at the time the first fault was detected. Using the FirstFaultTime value a user can pinpoint a first fault occurrence to within 200µs of all LTC2971 devices with connected SHARE\_CLK pins. The FirstFaultTime value will be reset whenever the MFR\_FIRST\_FAULT is cleared.

#### MFR\_FIRST\_FAULT Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:12]	Mfr_first_fault_page	The page of the first observed fault: 0xF: Global 0x1: Channel 1 0x0: Channel 0 All other values reserved
b[11:8]	Mfr_first_fault_bit_num	Bit number of the status register indicated by Mfr_first_fault_cmd that contains the first observed fault condition
b[7:0]	Mfr_first_fault_cmd	The PMBus command of the status register that contains the first observed fault condition: 0x80: STATUS_MFR_SPECIFIC 0x7D: STATUS_TEMPERATURE 0x7C: STATUS_INPUT 0x7A: STATUS_VOUT 0x00: None All other values reserved



## PMBus COMMAND DESCRIPTION

### TELEMETRY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
READ_VIN	0x88	Input supply voltage.	R Word	N	L11	V		NA	<a href="#">77</a>
READ_IIN	0x89	DC/DC converter input current.	R Word	Y	L11	A		NA	<a href="#">77</a>
READ_PIN	0x97	DC/DC converter input power.	R Word	Y	L11	W		NA	<a href="#">77</a>
READ_VOUT	0x8B	DC/DC converter output voltage.	R Word	Y	L16	V		NA	<a href="#">77</a>
READ_IOUT	0x8C	DC/DC converter output current.	R Word	Y	L11	A		NA	<a href="#">78</a>
READ_TEMPERATURE_1	0x8D	External diode junction temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	°C		NA	<a href="#">78</a>
READ_TEMPERATURE_2	0x8E	Internal junction temperature.	R Word	N	L11	°C		NA	<a href="#">78</a>
READ_POUT	0x96	DC/DC converter output power.	R Word	Y	L11	W		NA	<a href="#">79</a>
MFR_READ_IOUT	0xBB	Alternate data format for READ_IOUT. One LSB = 2.5mA.	R Word	Y	CF	2.5mA		NA	<a href="#">79</a>
MFR_IIN_PEAK	0xC4	Maximum measured value of READ_IIN	R Word	Y	L11	A		NA	<a href="#">78</a>
MFR_IIN_MIN	0xC5	Minimum measured value of READ_IIN.	R Word	Y	L11	A		NA	<a href="#">78</a>
MFR_PIN_PEAK	0xC6	Maximum measured value of READ_PIN.	R Word	Y	L11	W		NA	<a href="#">78</a>
MFR_PIN_MIN	0xC7	Minimum measured value of READ_PIN.	R Word	Y	L11	W		NA	<a href="#">78</a>
MFR_IOUT_SENSE_VOLTAGE	0xFA	Absolute value of $V_{IOUT\_SNSP} - V_{IOUT\_SNSM}$ . One LSB = 3.05μV or 91.5μV.	R Word	Y	CF	μV		NA	<a href="#">80</a>
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN.	R Word	N	L11	V		NA	<a href="#">80</a>
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT.	R Word	Y	L16	V		NA	<a href="#">80</a>
MFR_IOUT_PEAK	0xD7	Maximum measured value of READ_IOUT.	R Word	Y	L11	A		NA	<a href="#">80</a>
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	<a href="#">80</a>
MFR_VIN_MIN	0xFC	Minimum measured value of READ_VIN.	R Word	N	L11	V		NA	<a href="#">80</a>
MFR_VOUT_MIN	0xFB	Minimum measured value of READ_VOUT.	R Word	Y	L16	V		NA	<a href="#">80</a>
MFR_IOUT_MIN	0xD8	Minimum measured value of READ_IOUT.	R Word	Y	L11	A		NA	<a href="#">81</a>
MFR_TEMPERATURE_1_MIN	0xFD	Minimum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	<a href="#">81</a>

### **READ\_VIN**

This command returns the most recent ADC measured value of the input voltage at the  $V_{IN\_SNS}$  pin.

### **READ\_IIN**

This command returns the most recent ADC measured value of the input current derived from the voltage difference between the  $I_{IN\_SNSP}$  and  $I_{IN\_SNSM}$  pins.

### **READ\_PIN**

This command returns the most recent ADC measured value of the input power in watts. This is the product of READ\_IIN and READ\_VIN.

### **READ\_VOUT**

This command returns the most recent ADC measured value of the channel's output voltage.

## PMBus COMMAND DESCRIPTION

### ***READ\_IOUT***

This command returns the most recent ADC measured value of the channel's output current.

### ***MFR\_IIN\_PEAK***

This command returns the maximum ADC measured value of the input current. This register is reset to 0x7C00 ( $-2^{25}$ ) when the LTC2971 emerges from power-on reset, when a CLEAR\_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

### ***MFR\_IIN\_MIN***

This command returns the minimum ADC measured value of the input current. This register is reset to 0x7BFF (approximately  $2^{25}$ ) when the LTC2971 emerges from power-on reset, when a CLEAR\_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

### ***MFR\_PIN\_PEAK***

This command returns the maximum ADC measured value of the input power. This register is reset to 0x7C00 ( $-2^{25}$ ) when the LTC2971 emerges from power-on reset, when a CLEAR\_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

### ***MFR\_PIN\_MIN***

This command returns the minimum ADC measured value of the input power. This register is reset to 0x7BFF (approximately  $2^{25}$ ) when the LTC2971 emerges from power-on reset, when a CLEAR\_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

### ***READ\_TEMPERATURE\_1***

This command returns the most recent measured value of the external diode temperature in °C. This value is used for all temperature related operations and calculations. This command is paged. READ\_TEMPERATURE\_2 is substituted for READ\_TEMPERATURE\_1 if the associated T<sub>SENSE</sub> network fails to detect a valid temperature.

The T<sub>SENSE</sub> network will fail to detect a valid temperature under the following conditions:

- The T<sub>SENSE</sub> pin is shorted to a constant voltage.

- The sense diode has an ideality factor greater than N<sub>TS</sub> max.

Floating the T<sub>SENSE</sub> pin is not recommended and may return unpredictable temperature values.

### ***READ\_TEMPERATURE\_2***

This command returns the most recent ADC measured value of junction temperature in °C as determined by the LTC2971's internal temperature sensor. This register is for information purposes and does not generate any faults, warnings, or affect any other registers or internal calculations unless it is used as READ\_TEMPERATURE\_1. This command is not paged.

READ\_TEMPERATURE\_2 is substituted for READ\_TEMPERATURE\_1 if a channel's T<sub>SENSE</sub> network fails to detect a valid temperature.

## PMBus COMMAND DESCRIPTION

### READ\_POUT

This command returns the most recent ADC measured value of the channel's output power in watts.

### MFR\_READ\_IOUT

This command returns the most recent ADC measured value of the channel's output current, using a custom format that provides better numeric representation granularity than the READ\_IOUT command for currents whose absolute value is between 2A and 82A.

#### MFR\_READ\_IOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_read_iout[15:0]	Channel output current expressed in custom format for improved resolution at high currents. Value = $Y \cdot 2.5$ where $Y = b[15:0]$ is a signed two's-complement number. Example: MFR_READ_IOUT = 5mA For b[15:0] = 0x0002 Value = $2 \cdot 2.5 = 5\text{mA}$

The granularity of the returned value is always 2.5mA, and the return value is limited to  $\pm 81.92\text{A}$ . The READ\_IOUT command provides the best resolution for currents less than 2A and must be used for currents larger than 82A. Note that the accuracy of the returned value is always limited by the ADC Characteristics listed in the [Electrical Characteristics](#) section.

**Table 3. Comparison of Granularity Due to Numeric Format**

CURRENT RANGE	READ_IOUT GRANULARITY	MFR_READ_IOUT GRANULARITY
$31.25\text{mA} \leq I_{\text{OUT}} < 62.5\text{mA}$	61 $\mu\text{A}$	2.5mA
$62.5\text{mA} \leq I_{\text{OUT}} < 125\text{mA}$	122 $\mu\text{A}$	2.5mA
$125\text{mA} \leq I_{\text{OUT}} < 250\text{mA}$	244 $\mu\text{A}$	2.5mA
$250\text{mA} \leq I_{\text{OUT}} < 500\text{mA}$	488 $\mu\text{A}$	2.5mA
$0.5\text{A} \leq I_{\text{OUT}} < 1\text{A}$	977 $\mu\text{A}$	2.5mA
$1\text{A} \leq I_{\text{OUT}} < 2\text{A}$	1.95mA	2.5mA
$2\text{A} \leq I_{\text{OUT}} < 4\text{A}$	3.9mA	2.5mA
$4\text{A} \leq I_{\text{OUT}} < 8\text{A}$	7.8mA	2.5mA
$8\text{A} \leq I_{\text{OUT}} < 16\text{A}$	15.6mA	2.5mA
$16\text{A} \leq I_{\text{OUT}} < 32\text{A}$	31.3mA	2.5mA
$32\text{A} \leq I_{\text{OUT}} < 64\text{A}$	62.5mA	2.5mA
$64\text{A} \leq I_{\text{OUT}} < 82\text{A}$	125mA	2.5mA
$82\text{A} \leq I_{\text{OUT}} < 128\text{A}$	125mA	Saturated
$128\text{A} \leq I_{\text{OUT}} < 256\text{A}$	250mA	Saturated

## PMBus COMMAND DESCRIPTION

### ***MFR\_IOUT\_SENSE\_VOLTAGE***

This command returns the absolute value of the voltage measured between  $I_{OUT\_SNSPn}$  and  $I_{OUT\_SNSMn}$  during the last READ\_IOUT ADC conversion without any temperature correction.

#### **MFR\_IOUT\_SENSE\_VOLTAGE Data Contents**

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_iout_sense_voltage	<p>Absolute value of raw voltage conversion measured between <math>I_{OUT\_SNSPn}</math> and <math>I_{OUT\_SNSMn}</math>.</p> <p>Value = <math>Y \cdot X \cdot 2^{-13}</math> where <math>Y = b[15:0]</math> is an unsigned integer and <math>X = 0.025</math> or <math>0.75</math> if <code>mfr_config_imon_sel = 0</code> or <code>1</code> respectively, resulting in an LSB of <math>3.05\mu\text{V}</math> or <math>91.5\mu\text{V}</math>.</p> <p>Example:</p> <p><code>mfr_config_imon_sel = 0</code>  <code>MFR_IOUT_SENSE_VOLTAGE = 1.544mV</code>            For <code>b[15:0] = 0x1FA = 506</code>            Value = <math>506 \cdot 0.025 \cdot 2^{-13} = 1.544\text{mV}</math></p>

### ***MFR\_VIN\_PEAK***

This command returns the maximum ADC measured value of the input voltage. This register is reset to `0x7C00` ( $-2^{25}$ ) when the LTC2971 emerges from power-on reset, when a CLEAR\_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

### ***MFR\_VOUT\_PEAK***

This command returns the maximum ADC measured value of the channel's output voltage. This register is reset to `0xF800` (0.0) when the LTC2971 emerges from power-on reset, when a CLEAR\_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

### ***MFR\_IOUT\_PEAK***

This command returns the maximum ADC measured value of the channel's output current. This register is reset to `0x7C00` ( $-2^{25}$ ) when the LTC2971 emerges from power-on reset, when a CLEAR\_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

### ***MFR\_TEMPERATURE\_1\_PEAK***

This command returns the maximum measured value of the external diode temperature in  $^{\circ}\text{C}$ . This register is reset to `0x7C00` ( $-2^{25}$ ) when the LTC2971 emerges from power-on reset, when a CLEAR\_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

### ***MFR\_VIN\_MIN***

This command returns the minimum ADC measured value of the input voltage. This register is reset to `0x7BFF` (approximately  $2^{25}$ ) when the LTC2971 emerges from power-on reset, when a CLEAR\_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

### ***MFR\_VOUT\_MIN***

This command returns the minimum ADC measured value of the channel's output voltage. This register is reset to `0xFFFF` (7.9999) when the LTC2971 emerges from power-on reset, when a CLEAR\_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

## PMBus COMMAND DESCRIPTION

### MFR\_IOUT\_MIN

This command returns the minimum ADC measured value of the channel's output current. This register is reset to 0x7BFF (approximately  $2^{25}$ ) when the LTC2971 emerges from power-on reset, when a CLEAR\_FAULTS command is executed to the page, or the channel goes through an off-to-on transition.

### MFR\_TEMPERATURE\_1\_MIN

This command returns the minimum measured value of the external diode temperature in °C. This register is reset to 0x7BFF (approximately  $2^{25}$ ) when the LTC2971 emerges from power-on reset, when a CLEAR\_FAULTS command is executed to the page, or the channel goes through an off-to-on transition.

### FAULT LOGGING

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA	<a href="#">82</a>
MFR_FAULT_LOG_RESTORE	0xEB	Command a transfer of the fault log previously stored in EEPROM back to RAM.	Send Byte	N				NA	<a href="#">82</a>
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks.	Send Byte	N				NA	<a href="#">82</a>
MFR_FAULT_LOG_STATUS	0xED	Fault logging status.	R Byte	N	Reg		Y	NA	<a href="#">82</a>
MFR_FAULT_LOG	0xEE	Fault log data bytes. This sequentially retrieved data is used to assemble a complete fault log.	R Block	N	Reg		Y	NA	<a href="#">82</a>

### Fault Log Operation

A conceptual diagram of the fault log is shown in [Figure 21](#). The fault log provides black box capability for the LTC2971. During normal operation the contents of the status registers, the output voltage/current/temperature readings, the input voltage readings, as well as peak and min values of these quantities, are stored in a continuously updated buffer in RAM. You can think of the operation as being similar to a strip chart recorder. When a fault occurs, the contents are written into EEPROM for non volatile storage. The EEPROM fault log is then locked. The part can be powered down with the fault log available for reading at a later time.

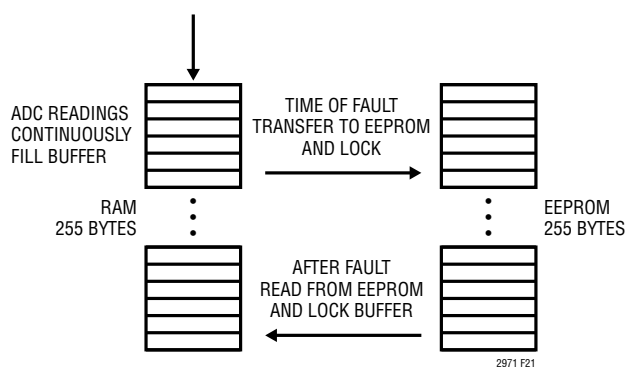


Figure 21. Fault Logging

## PMBus COMMAND DESCRIPTION

### ***MFR\_FAULT\_LOG\_STORE***

This command allows the user to transfer data from the RAM buffer to EEPROM.

### ***MFR\_FAULT\_LOG\_RESTORE***

This command allows the user to transfer a copy of the fault-log data from the EEPROM to the RAM buffer. After a restore the RAM buffer is locked until a successful Mfr\_fault\_log read.

### ***MFR\_FAULT\_LOG\_CLEAR***

This command initializes the EEPROM block reserved for fault logging. Any previous fault log stored in EEPROM will be erased by this operation and logging of the fault log RAM to EEPROM will be enabled. Make sure that Mfr\_fault\_log\_status\_ram = 0 before issuing the MFR\_FAULT\_LOG\_CLEAR command.

### ***MFR\_FAULT\_LOG\_STATUS***

This register is used to manage fault log events. The Mfr\_fault\_log\_status\_eeprom bit is set after a MFR\_FAULT\_LOG\_STORE command or a faulted-off event triggers a transfer of the fault log from RAM to EEPROM. This bit is cleared by a MFR\_FAULT\_LOG\_CLEAR command.

Mfr\_fault\_log\_status\_ram is set after a MFR\_FAULT\_LOG\_RESTORE to indicate that the data in the RAM has been restored from EEPROM and not yet read using a MFR\_FAULT\_LOG command. This bit is cleared only by a successful execution of an MFR\_FAULT\_LOG command.

#### **MFR\_FAULT\_LOG\_STATUS Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:2]	Reserved	Read only, always returns 0s.
b[1]	Mfr_fault_log_status_ram	Fault log RAM status: 0: The fault log RAM allows updates. 1: The fault log RAM is locked until the next Mfr_fault_log read.
b[0]	Mfr_fault_log_status_eeprom	Fault log EEPROM status: 0: The transfer of the fault log RAM to the EEPROM is enabled. 1: The transfer of the fault log RAM to the EEPROM is inhibited.

### ***MFR\_FAULT\_LOG***

Read only. This 2040-bit (255-byte) data block contains a copy of the RAM buffer fault log. The RAM buffer is continuously updated after each ADC conversion as long as Mfr\_fault\_log\_status\_eeprom is clear.

With Mfr\_config\_fault\_log\_enable = 1 and Mfr\_fault\_log\_status\_eeprom = 0, the RAM buffer is transferred to EEPROM whenever an LTC2971 fault causes a channel to latch off or a MFR\_FAULT\_LOG\_STORE command is received. This transfer is delayed until the ADC has updated its READ values for both channels when Mfr\_config\_all\_fast\_fault\_log is clear, otherwise it happens within 24ms. This optional delay can be used to ensure that the slower ADC monitored values are all updated for the case where a fast supervisor detected fault initiates the transfer to EEPROM.

Mfr\_fault\_log\_status\_eeprom is set high after the RAM buffer is transferred to EEPROM and not cleared until a Mfr\_fault\_log\_clear is received, even if the LTC2971 is reset or powered down. Fault log EEPROM transfers are not initiated as a result of Status\_mfr\_discharge events.

## PMBus COMMAND DESCRIPTION

During a Mfr\_fault\_log read, data is returned one byte at a time as defined in Table 4. The fault log data is partitioned into two sections. The first section is referred to as the preamble and contains the Position\_last pointer, time information and peak and min values. The second section contains a chronological record of telemetry and requires Position\_last for proper interpretation. The fault log stores approximately 300ms seconds of telemetry. To prevent timeouts during block reads, it is recommended that Mfr\_config\_all\_longer\_pmbus\_timeout be set to 1.

**Table 4. Data Block Contents**

DATA	BYTE*	DESCRIPTION
Position_last[7:0]	0	Position of fault log pointer when fault occurred.
Reserved	1	Always returns 0x00.
SharedTime[7:0]	2	41-bit share-clock counter value when fault occurred. Counter LSB is in 200µs increments. This counter is cleared at power-up or after the LTC2971 is reset.
SharedTime[15:8]	3	
SharedTime[23:16]	4	
SharedTime[31:24]	5	
SharedTime[39:32]	6	
SharedTime[40]	7	
Mfr_first_fault[7:0]	8	Least significant 8 bits of the share-clock counter captured at the time the first fault is detected.
Mfr_first_fault[15:8]	9	
FirstFaultTime	10	
Mfr_vout_peak0[7:0]	11	
Mfr_vout_peak0[15:8]	12	
Mfr_vout_min0[7:0]	13	
Mfr_vout_min0[15:8]	14	
Mfr_temperature_peak0[7:0]	15	
Mfr_temperature_peak0[15:8]	16	
Mfr_temperature_min0[7:0]	17	
Mfr_temperature_min0[15:8]	18	
Mfr_iout_peak0[7:0]	19	
Mfr_iout_peak0[15:8]	20	
Mfr_iout_min0[7:0]	21	
Mfr_iout_min0[15:8]	22	
Mfr_vin_peak[7:0]	23	
Mfr_vin_peak[15:8]	24	
Mfr_vin_min[7:0]	25	

**Table 4. Data Block Contents**

DATA	BYTE*	DESCRIPTION
Mfr_vin_min[15:8]	26	
Mfr_iin_peak[7:0]	27	
Mfr_iin_peak[15:8]	28	
Mfr_iin_min[7:0]	29	
Mfr_iin_min[15:8]	30	
Mfr_pin_peak[7:0]	31	
Mfr_pin_peak[15:8]	32	
Mfr_pin_min[7:0]	33	
Mfr_pin_min[15:8]	34	
Mfr_vout_peak1[7:0]	35	
Mfr_vout_peak1[15:8]	36	
Mfr_vout_min1[7:0]	37	
Mfr_vout_min1[15:8]	38	
Mfr_temperature_peak1[7:0]	39	
Mfr_temperature_peak1[15:8]	40	
Mfr_temperature_min1[7:0]	41	
Mfr_temperature_min1[15:8]	42	
Mfr_iout_peak1[7:0]	43	
Mfr_iout_peak1[15:8]	44	
Mfr_iout_min1[7:0]	45	
Mfr_iout_min1[15:8]	46	
Status_vout0[7:0]	47	
Status_iout0[7:0]	48	
Status_mfr_specific0[7:0]	49	
Mfr_status_2_0[7:0]	50	Reserved bits[15:8] not stored
Status_vout1[7:0]	51	
Status_iout1[7:0]	52	
Status_mfr_specific1[7:0]	53	
Mfr_status_2_1[7:0]	54	
		55 bytes for preamble
Fault_log [Position_last]	55	
Fault_log [Position_last-1]	56	
...		
Fault_log [Position_last-170]	237	
Reserved	238-254	
		Number of loops: (238 – 55)/36 = 5.08

\*Note that PMBus data byte numbers start at 1 rather than 0. Position\_last is the first byte returned after BYTE\_COUNT = 0xFF. See block read protocol.

## PMBus COMMAND DESCRIPTION

The data returned between bytes 55 and 237 of the previous table is interpreted using Position\_last and the following table. The key to identifying the data located in byte 55 is to locate the DATA corresponding to POSITION = Position\_last in the next table. Subsequent bytes are identified by decrementing the value of POSITION. For example: If Position\_last = 9 then the first data returned in byte position 55 of a block read is Status\_temperature of page 0 followed by Read\_temperature\_1[15:8] of page 0 followed by Read\_temperature\_1[7:0] of page 0 and so on. See [Table 5](#).

**Table 5. Interpreting Cyclical Loop Data**

POSITION	DATA
0	Read_temperature_2[7:0]
1	Read_temperature_2[15:8]
2	Read_vout0[7:0]
3	Read_vout0[15:8]
4	Status_vout0[7:0]
5	Status_mfr_specific0[7:0]
6	Mfr_status_2_0[7:0]
7	Read_temperature_1_0[7:0]
8	Read_temperature_1_0[15:8]
9	Status_temperature0[7:0]
10	Status_iout0[7:0]
11	Read_iout0[7:0]
12	Read_iout0[15:8]

**Table 5. Interpreting Cyclical Loop Data**

POSITION	DATA
13	Read_pout0[7:0]
14	Read_pout0[15:8]
15	Read_vin[7:0]
16	Read_vin[15:8]
17	Status_input[7:0]
18	0x0
19	Read_iin[7:0]
20	Read_iin[15:8]
21	Read_pin[7:0]
22	Read_pin[15:8]
23	Read_vout1[7:0]
24	Read_vout1[15:8]
25	Status_vout1[7:0]
26	Status_mfr_specific1[7:0]
27	Mfr_status_2_1[7:0]
28	Read_temperature_1_1[7:0]
29	Read_temperature_1_1[15:8]
30	Status_temperature1[7:0]
31	Status_iout1[7:0]
32	Read_iout1[7:0]
33	Read_iout1[15:8]
34	Read_pout1[7:0]
35	Read_pout1[15:8]
	Total Bytes = 36



## PMBus COMMAND DESCRIPTION

### MFR\_FAULT\_LOG Read Example

The following table fully decodes a sample fault log read with Position\_last = 4 to help clarify the cyclical nature of the operation.

#### Data Block Contents

PREAMBLE INFORMATION			
BYTE NUMBER DECIMAL	BYTE NUMBER HEX	DATA	DESCRIPTION
0	00	Position_last[7:0] = 4	Position of fault-log pointer when fault occurred.
1	01	Reserved	Always returns 0x00.
2	02	SharedTime[7:0]	41-bit share-clock counter value when fault occurred. Counter LSB is in 200µs increments.
3	03	SharedTime[15:8]	
4	04	SharedTime[23:16]	
5	05	SharedTime[31:24]	
6	06	SharedTime[39:32]	
7	07	SharedTime[40]	
8	08	Mfr_first_fault[7:0]	
9	09	Mfr_first_fault[15:8]	
10	0A	FirstFaultTime	
11	0B	Mfr_vout_peak0[7:0]	
12	0C	Mfr_vout_peak0[15:8]	
13	0D	Mfr_vout_min0[7:0]	
14	0E	Mfr_vout_min0[15:8]	
15	0F	Mfr_temperature_peak0[7:0]	
16	10	Mfr_temperature_peak0[15:8]	
17	11	Mfr_temperature_min0[7:0]	
18	12	Mfr_temperature_min0[15:8]	
19	13	Mfr_iout_peak0[7:0]	
20	14	Mfr_iout_peak0[15:8]	
21	15	Mfr_iout_min0[7:0]	
22	16	Mfr_iout_min0[15:8]	
23	17	Mfr_vin_peak_[7:0]	
24	18	Mfr_vin_peak_[15:8]	
25	19	Mfr_vin_min_[7:0]	
26	1A	Mfr_vin_min_[15:8]	

#### PREAMBLE INFORMATION

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	DATA	DESCRIPTION
27	1B	Mfr_iin_peak[7:0]	
28	1C	Mfr_iin_peak[15:8]	
29	1D	Mfr_iin_min[7:0]	
30	1E	Mfr_iin_min[15:8]	
31	1F	Mfr_pin_peak[7:0]	
32	20	Mfr_pin_peak[15:8]	
33	21	Mfr_pin_min[7:0]	
34	22	Mfr_pin_min[15:8]	
35	23	Mfr_vout_peak1[7:0]	
36	24	Mfr_vout_peak1[15:8]	
37	25	Mfr_vout_min1[7:0]	
38	26	Mfr_vout_min1[15:8]	
39	27	Mfr_temperature_peak1[7:0]	
40	28	Mfr_temperature_peak1[15:8]	
41	29	Mfr_temperature_min1[7:0]	
42	2A	Mfr_temperature_min1[15:8]	
43	2B	Mfr_iout_peak1[7:0]	
44	2C	Mfr_iout_peak1[15:8]	
45	2D	Mfr_iout_min1[7:0]	
46	2E	Mfr_iout_min1[15:8]	
47	2F	Status_vout0[7:0]	
48	30	Status_iout0[7:0]	
49	31	Status_mfr_specific0[7:0]	
50	32	Mfr_status_2_0[7:0]	
51	33	Status_vout1[7:0]	
52	34	Status_iout1[7:0]	
53	35	Status_mfr_specific1[7:0]	
54	36	Mfr_status_2_1[7:0]	End of Preamble

## PMBus COMMAND DESCRIPTION

### CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	DATA LOOP 0	36 BYTES PER LOOP
55	37	4	Status_vout0[7:0]	Position_last
56	38	3	Read_vout0[15:8]	
57	39	2	Read_vout0[7:0]	
58	40	1	Read_temperature_2[15:8]	
59	41	0	Read_temperature_2[7:0]	

### CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	DATA LOOP 1	36 BYTES PER LOOP
60	3C	35	Read_pout1[15:8]	
61	3D	34	Read_pout1[7:0]	
62	3E	33	Read_iout1[15:8]	
63	3F	32	Read_iout1[7:0]	
64	40	31	Status_iout1[7:0]	
65	41	30	Status_temperature2[7:0]	
66	42	29	Read_temperature_1_1[15:8]	
67	43	28	Read_temperature_1_1[7:0]	
68	44	27	Mfr_status_2_1[7:0]	
69	45	26	Status_mfr_specific1[7:0]	
70	46	25	Status_vout1[7:0]	
71	47	24	Read_vout1[15:8]	
72	48	23	Read_vout1[7:0]	
73	49	22	Read_pin[15:8]	
74	4A	21	Read_pin[7:0]	
75	4B	20	Read_in[15:8]	
76	4C	19	Read_in[7:0]	
77	4D	18	0x0	
78	4E	17	Status_input[7:0]	
79	4F	16	Read_vin[15:8]	
80	50	15	Read_vin[7:0]	
81	51	14	Read_pout0[15:8]	
82	52	13	Read_pout0[7:0]	
83	53	12	Read_iout0[15:8]	

### CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	DATA LOOP 1	36 BYTES PER LOOP
84	54	11	Read_iout0[7:0]	
85	55	10	Status_iout0[7:0]	
86	56	9	Status_temperature0[7:0]	
87	57	8	Read_temperature_1_0[15:8]	
88	58	7	Read_temperature_1_0[7:0]	
89	59	6	Mfr_status_2_0[7:0]	
90	5A	5	Status_mfr_specific0[7:0]	
91	5B	4	Status_vout0[7:0]	
92	5C	3	Read_vout0[15:8]	
93	5D	2	Read_vout0[7:0]	
94	5E	1	Read_temperature_2[15:8]	
95	5F	0	Read_temperature_2[7:0]	

### CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	DATA LOOP 2	36 BYTES PER LOOP
96	60	35	Read_pout1[15:8]	
97	61	34	Read_pout1[7:0]	
98	62	33	Read_iout1[15:8]	
99	63	32	Read_iout1[7:0]	
100	64	31	Status_iout1[7:0]	
101	65	30	Status_temperature2[7:0]	
102	66	29	Read_temperature_1_1[15:8]	
103	67	28	Read_temperature_1_1[7:0]	
104	68	27	Mfr_status_2_1[7:0]	
105	69	26	Status_mfr_specific1[7:0]	
106	6A	25	Status_vout1[7:0]	
107	6B	24	Read_vout1[15:8]	
108	6C	23	Read_vout1[7:0]	
109	6D	22	Read_pin[15:8]	

## PMBus COMMAND DESCRIPTION

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	DATA LOOP 2	36 BYTES PER LOOP
110	6E	21	Read_pin[7:0]	
111	6F	20	Read_in[15:8]	
112	70	19	Read_in[7:0]	
113	71	18	0x0	
114	72	17	Status_input[7:0]	
115	73	16	Read_vin[15:8]	
116	74	15	Read_vin[7:0]	
117	75	14	Read_pout0[15:8]	
118	76	13	Read_pout0[7:0]	
119	77	12	Read_iout0[15:8]	
120	78	11	Read_iout0[7:0]	
121	79	10	Status_iout0[7:0]	
122	7A	9	Status_temperature0[7:0]	
123	7B	8	Read_temperature_1_0[15:8]	
124	7C	7	Read_temperature_1_0[7:0]	
125	7D	6	Mfr_status_2_0[7:0]	
126	7E	5	Status_mfr_specific0[7:0]	
127	7F	4	Status_vout0[7:0]	
128	80	3	Read_vout0[15:8]	
129	81	2	Read_vout0[7:0]	
130	82	1	Read_temperature_2[15:8]	
131	83	0	Read_temperature_2[7:0]	

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	DATA LOOP 3	36 BYTES PER LOOP
133	85	35	Read_pout1[15:8]	
134	86	34	Read_pout1[7:0]	
135	87	33	Read_iout1[15:8]	
136	88	32	Read_iout1[7:0]	
137	89	31	Status_iout1[7:0]	
138	8A	30	Status_temperature2[7:0]	

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	DATA LOOP 3	36 BYTES PER LOOP
139	8B	29	Read_temperature_1_1[15:8]	
140	8C	28	Read_temperature_1_1[7:0]	
141	8D	27	Mfr_status_2_1[7:0]	
142	8E	26	Status_mfr_specific1[7:0]	
143	8F	25	Status_vout1[7:0]	
144	90	24	Read_vout1[15:8]	
145	91	23	Read_vout1[7:0]	
146	92	22	Read_pin[15:8]	
147	93	21	Read_pin[7:0]	
148	94	20	Read_in[15:8]	
149	95	19	Read_in[7:0]	
150	96	18	0x0	
151	97	17	Status_input[7:0]	
152	98	16	Read_vin[15:8]	
153	99	15	Read_vin[7:0]	
154	9A	14	Read_pout0[15:8]	
155	9B	13	Read_pout0[7:0]	
156	9C	12	Read_iout0[15:8]	
157	9D	11	Read_iout0[7:0]	
158	9E	10	Status_iout0[7:0]	
159	9F	9	Status_temperature0[7:0]	
160	A0	8	Read_temperature_1_0[15:8]	
161	A1	7	Read_temperature_1_0[7:0]	
162	A2	6	Mfr_status_2_0[7:0]	
163	A3	5	Status_mfr_specific0[7:0]	
164	A4	4	Status_vout0[7:0]	
165	A5	3	Read_vout0[15:8]	
166	A6	2	Read_vout0[7:0]	
167	A7	1	Read_temperature_2[15:8]	
168	A8	0	Read_temperature_2[7:0]	

## PMBus COMMAND DESCRIPTION

### CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	DATA LOOP 4	36 BYTES PER LOOP
169	A9	35	Read_pout1[15:8]	
170	AA	34	Read_pout1[7:0]	
171	AB	33	Read_iout1[15:8]	
172	AC	32	Read_iout1[7:0]	
173	AD	31	Status_iout1[7:0]	
174	AE	30	Status_temperature2[7:0]	
175	AF	29	Read_temperature_1_1[15:8]	
176	B0	28	Read_temperature_1_1[7:0]	
177	B1	27	Mfr_status_2_1[7:0]	
178	B2	26	Status_mfr_specific1[7:0]	
179	B3	25	Status_vout1[7:0]	
180	B4	24	Read_vout1[15:8]	
181	B5	23	Read_vout1[7:0]	
182	B6	22	Read_pin[15:8]	
183	B7	21	Read_pin[7:0]	
184	B8	20	Read_in[15:8]	
185	B9	19	Read_in[7:0]	
186	BA	18	0x0	
187	BB	17	Status_input[7:0]	
188	BC	16	Read_vin[15:8]	
189	BD	15	Read_vin[7:0]	
190	BE	14	Read_pout0[15:8]	
191	BF	13	Read_pout0[7:0]	
192	C0	12	Read_iout0[15:8]	
193	C1	11	Read_iout0[7:0]	
194	C2	10	Status_iout0[7:0]	
195	C3	9	Status_temperature0[7:0]	

### CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	DATA LOOP 4	36 BYTES PER LOOP
196	C4	8	Read_temperature_1_0[15:8]	
197	C5	7	Read_temperature_1_0[7:0]	
198	C6	6	Mfr_status_2_0[7:0]	
199	C7	5	Status_mfr_specific0[7:0]	
200	C8	4	Status_vout0[7:0]	
201	C9	3	Read_vout0[15:8]	
202	CA	2	Read_vout0[7:0]	
203	CB	1	Read_temperature_2[15:8]	
204	CC	0	Read_temperature_2[7:0]	

### CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	DATA LOOP 5	36 BYTES PER LOOP
205	CD	35	Read_pout1[15:8]	
206	CE	34	Read_pout1[7:0]	
207	CF	33	Read_iout1[15:8]	
208	D0	32	Read_iout1[7:0]	
209	D1	31	Status_iout1[7:0]	
210	D2	30	Status_temperature2[7:0]	
211	D3	29	Read_temperature_1_1[15:8]	
212	D4	28	Read_temperature_1_1[7:0]	
213	D5	27	Mfr_status_2_1[7:0]	
214	D6	26	Status_mfr_specific1[7:0]	
215	D7	25	Status_vout1[7:0]	
216	D8	24	Read_vout1[15:8]	
217	D9	23	Read_vout1[7:0]	
218	DA	22	Read_pin[15:8]	
219	DB	21	Read_pin[7:0]	
220	DC	20	Read_in[15:8]	
221	DD	19	Read_in[7:0]	

## PMBus COMMAND DESCRIPTION

### CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	DATA LOOP 5	36 BYTES PER LOOP
222	DE	18	0x0	
223	DF	17	Status_input[7:0]	
224	E0	16	Read_vin[15:8]	
225	E1	15	Read_vin[7:0]	
226	E2	14	Read_pout0[15:8]	
227	E3	13	Read_pout0[7:0]	
228	E4	12	Read_iout0[15:8]	
229	E5	11	Read_iout0[7:0]	
230	E6	10	Status_iout0[7:0]	
231	E7	9	Status_temperature0[7:0]	
232	E8	8	Read_temperature_1_0[15:8]	
233	E9	7	Read_temperature_1_0[7:0]	
234	EA	6	Mfr_status_2_0[7:0]	
235	EB	5	Status_mfr_specific0[7:0]	
236	EC	4	Status_vout0[7:0]	
237	ED	3	Read_vout0[15:8]	Last valid fault log byte

### RESERVED BYTES

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	DATA	36 BYTES PER LOOP	Notes
238	EE	0x00		Bytes EE – FE Return 0x00 But Must Be Read
239	EF	0x00		
240	F0	0x00		
241	F1	0x00		
242	F2	0x00		
243	F3	0x00		
244	F4	0x00		
245	F5	0x00		
246	F6	0x00		
247	F7	0x00		
248	F8	0x00		
249	F9	0x00		
250	FA	0x00		
251	FB	0x00		
252	FC	0x00		
253	FD	0x00		
254	FE	0x00		
				Use One Block Read Command to Read 255 Bytes Total, from 0x00 to 0xFE

## PMBus COMMAND DESCRIPTION

### IDENTIFICATION/INFORMATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	<a href="#">90</a>
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.1.	R Byte	N	Reg			0x11	<a href="#">90</a>
MFR_SPECIAL_ID	0xE7	Manufacturer code for identifying the LTC2971.	R Word	N	Reg		Y	LTC2971 0x032X LTC2971-1 0x033X LTC2971-2 0x034X LTC2971-3 0x035X	<a href="#">90</a>
MFR_SPECIAL_LOT	0xE8	Customer dependent codes that identify the factory programmed user configuration stored in EEPROM. Contact factory for default value.	R Byte	Y	Reg		Y		<a href="#">91</a>
MFR_INFO	0xB6	Manufacturer Specific Information	R Word	N	Reg			NA	<a href="#">91</a>

### CAPABILITY

The CAPABILITY command provides a way for a host system to determine some key capabilities of the LTC2971.

#### CAPABILITY Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Capability_pec	Hard coded to 1 indicating Packet Error Checking is supported. Reading the Mfr_config_all_pec_en bit will indicate whether PEC is currently required.
b[6:5]	Capability_scl_max	Hard coded to 01b indicating the maximum supported bus speed is 400kHz.
b[4]	Capability_smb_alert	Hard coded to 1 indicating this device does have an ALERTB pin and does support the SMBus Alert Response Protocol.
b[3:0]	Reserved	Always returns 0.

### PMBUS\_REVISION

#### PMBUS\_REVISION Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	PMBus_rev	Reports the PMBus standard revision compliance. This is hard-coded to 0x11 for revision 1.1.

### MFR\_SPECIAL\_ID

This register contains the manufacturer ID for the LTC2971. Always returns 0x032X (LTC2971), 0x033X (LTC2971-1), 0x034X (LTC2971-2) or 0x035X (LTC2971-3). The last nibble is adjusted by the manufacturer.

## PMBus COMMAND DESCRIPTION

### MFR\_SPECIAL\_LOT

These paged registers contain information that identifies the user configuration that was programmed at the factory. Contact the factory to request a custom factory programmed user configuration and special lot number.

### MFR\_INFO

The MFR\_INFO register contains manufacturer specific information and is updated after a power-on reset, a RESTORE\_USER\_ALL command, or an EEPROM bulk read operation.

#### MFR\_INFO Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:6]	Reserved	Reserved
b[5]	Mfr_info_ecc_user	EEPROM ECC status. 0: Corrections made in the EEPROM user space 1: No corrections made in the EEPROM user space
b[4:0]	Reserved	Reserved

### USER SCRATCHPAD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
USER_DATA_00	0xB0	Manufacturer reserved for LTpowerPlay.	R/W Word	N	Reg		Y	N/A	<a href="#">91</a>
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	N/A	<a href="#">91</a>
USER_DATA_02	0xB2	OEM Reserved.	R/W Word	N	Reg		Y	N/A	<a href="#">91</a>
USER_DATA_03	0xB3	Scratchpad location.	R/W Word	Y	Reg		Y	0x0000	<a href="#">91</a>
USER_DATA_04	0xB4	Scratchpad location.	R/W Word	N	Reg		Y	0x0000	<a href="#">91</a>
MFR_LTC_RESERVED_2	0xBC	Manufacturer reserved.	R/W Word	Y	Reg			NA	<a href="#">91</a>

### USER\_DATA\_00, USER\_DATA\_01, USER\_DATA\_02, USER\_DATA\_03, USER\_DATA\_04 and MFR\_LTC\_RESERVED\_2

These registers are provided as user scratchpad and additional manufacturer reserved locations.

USER\_DATA\_03 and USER\_DATA\_04 are available for user scratchpad use. These 10 bytes (1 unpagged word plus 2 pagged words) might be used for traceability or revision information such as serial number, board model number, assembly location, or assembly date.

## APPLICATIONS INFORMATION

### OVERVIEW

The LTC2971 is a 2-channel Power System Management IC that is capable of sequencing, margining, trimming, supervising output voltage for OV/UV conditions, fault management, voltage/current/temperature readback for two DC/DC converter channels, and readback of high side input current, input voltage, input power, input energy, and junction temperature. Multiple Analog Devices Power System Managers can coordinate operation using the SHARE\_CLK, FAULTB, and CONTROL pins. The LTC2971 utilizes a PMBus compliant interface and command set.

### POWERING THE LTC2971

The LTC2971 can be powered two ways. In one method, power from an external 4.5V to 60V supply is applied to the  $V_{PWR}$  pin. See Figure 22. An internal linear regulator converts  $V_{PWR}$  to 3.3V, which drives the LTC2971's internal circuitry. High  $V_{PWR}$  levels cause excessive internal power dissipation and self-heating. Although the LTC2971 works with 60V  $V_{PWR}$  levels, it is advised to use an external switching regulator to drop  $V_{PWR}$  for external supplies above 24V.

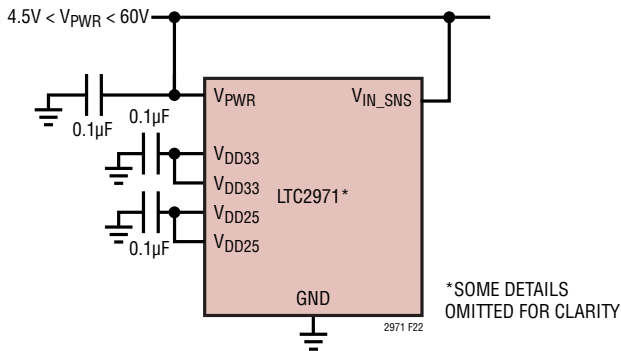


Figure 22. Powering LTC2971 from External 4.5V to 60V Supply

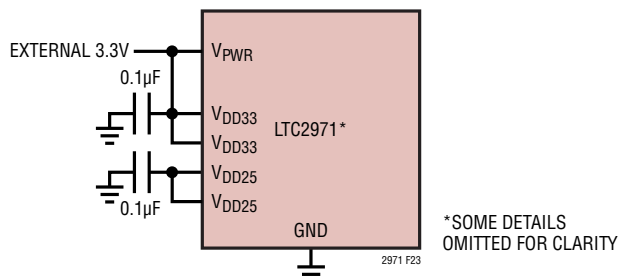


Figure 23. Powering LTC2971 from External 3.3V Supply

Alternatively, power from an external 3.13V to 3.47V supply is applied to the  $V_{DD33}$  and  $V_{PWR}$  pins. See Figure 23. All functionality is available when using this method, and internal power is minimized.

### SETTING COMMAND REGISTER VALUES

The command register settings described herein are intended as a reference and for the purpose of understanding the registers in a software development environment. In actual practice, the LTC2971 can be completely configured for stand-alone operation with the DC1613 USB to I<sup>2</sup>C/SMBus/PMBus controller and LTpowerPlay using intuitive menu driven objects.

### MEASURING INPUT CURRENT

The LTC2971 is capable of measuring the current of the input power source. The device also measures the input supply voltage, enabling it to calculate input power. The LTC2971 has an accurate internal time base allowing the chip to calculate input energy since energy is the product of power and time. The units for each of the measured parameters are amps, volts, watts, and millijoules.

Input current is measured by placing a sense resistor,  $R_{SENSE}$ , in series with the desired current load path as shown in Figure 24. If  $R_{SENSE}$  has low thermal drift characteristics, the MFR\_IIN\_CAL\_GAIN\_TC register value may be set to zero. Otherwise, choose a setting for the MFR\_IIN\_CAL\_GAIN\_TC value in units of ppm/°C to correct for  $R_{SENSE}$  thermal drift.

For best results, it is recommended to locate  $R_{SENSE}$  close to and isothermal with the LTC2971.

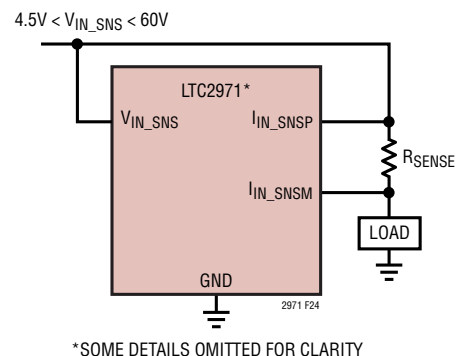


Figure 24. Measuring Input Current



## APPLICATIONS INFORMATION

The  $R_{SENSE}$  value should be chosen to encompass the maximum input signal in the  $\pm 80\text{mV}$  input range. After selecting  $R_{SENSE}$ , write its value in  $\text{m}\Omega$  to the  $\text{MFR\_IIN\_CAL\_GAIN}$  register, and  $\text{READ\_IIN}$  will return the sensed current in amps.

### MEASURING INPUT VOLTAGE

$\text{READ\_VIN}$  returns input voltage on the  $V_{\text{IN\_SNS}}$  pin.  $\text{TUE\_VIN}$  reflects  $\text{READ\_VIN}$  measurement error.

### MEASURING INPUT POWER

$\text{READ\_PIN}$  returns input power in watts calculated from the product of the most recent  $V_{\text{VIN\_SNS}}$  and  $I_{\text{IN\_SNS}}$  measurements. Although the [Electrical Characteristics](#) table only specifies  $\text{READ\_PIN}$  Total Unadjusted Error ( $\text{TUE\_PIN}$ ) under typical conditions,  $\text{TUE\_PIN}$  is actually bounded by the sum of  $\text{TUE\_IIN}$  and  $\text{TUE\_VIN}$ .

$$\text{TUE\_PIN} \leq \text{TUE\_IIN} + \text{TUE\_VIN}$$

For example, if  $15\text{mV} < |V_{\text{IIN\_SNS}}| < 50\text{mV}$ ,  $\text{TUE\_IIN} \leq 1\%$  and  $\text{TUE\_PIN}$  is less than  $1\% (\text{TUE\_IIN}) + 0.5\% (\text{TUE\_VIN}) = 1.5\%$ .

Since current sense ranges include positive and negative inputs,  $\text{READ\_PIN}$  returns signed values indicating power transfer magnitude and direction.

### MEASURING INPUT ENERGY

The 12 byte data block,  $\text{MFR\_EIN}$ , contains a 48-bit accumulated energy measurement in mJ,  $\text{Energy\_value}[47:0]$ , and a 48-bit elapsed time in milliseconds since energy began accumulating,  $\text{Energy\_time}[47:0]$ . Refer to [INPUT CURRENT AND ENERGY](#) and [MFR\\_COMMAND\\_PLUS](#) sections of the [PMBUS COMMAND DESCRIPTION](#) for accumulated energy and elapsed time data access details.  $\text{Energy\_value}$  can accumulate up to  $(2^{48}-1)$  mJ of energy before wrapping. Energy can accumulate for  $(2^{48}-1)$  ms, or about 8925 years, before  $\text{Energy\_time}$  wraps. Accumulation of negative power measurements decreases  $\text{Energy\_value}$ , and the energy meter saturates when it reaches 0 millijoules.

The energy meter time base error ( $\text{TUE\_ETB}$ ) specifies error in the internal energy time base accuracy:  $\text{Energy\_time}$  is accurate with maximum error of  $\text{TUE\_ETB}$ . Accumulated energy includes errors from current sense measurements, voltage sense measurements, and the internal time base.  $\text{Energy\_value}$  error ( $\text{TUE\_EIN}$ ) is bounded by the summation of  $\text{TUE\_IIN}$ ,  $\text{TUE\_VIN}$ , and  $\text{TUE\_ETB}$ :

$$\text{TUE\_EIN} \leq \text{TUE\_IIN} + \text{TUE\_VIN} + \text{TUE\_ETB}$$

For example, if  $V_{\text{IIN\_SNS}} = 20\text{mV}$ ,  $\text{TUE\_IIN}$  is less than 1% error,  $\text{TUE\_VIN}$  is less than 0.5% error, and  $\text{TUE\_ETB}$  is less than 1% error. Therefore the energy measurement error ( $\text{TUE\_EIN}$ ) is less than 2.5%.

## SEQUENCE, SERVO, MARGIN AND RESTART OPERATIONS

### Command Units On or Off

Three control parameters determine how a particular channel is turned on and off: The  $\text{CONTROL}$  pins, the  $\text{OPERATION}$  command and the value of the input voltage measured at the  $V_{\text{IN\_SNS}}$  pin ( $V_{\text{IN}}$ ). In all cases,  $V_{\text{IN}}$  must exceed  $\text{VIN\_ON}$  in order to enable the device to respond to the  $\text{CONTROL}$  pins or  $\text{OPERATION}$  commands. When  $V_{\text{IN}}$  drops below  $\text{VIN\_OFF}$  an immediate OFF or sequence off after  $\text{TOFF\_DELAY}$  of both channels will result (See [Mfr\\_config\\_track\\_enr](#)). Refer to the  $\text{OPERATION}$  section in the data sheet for a detailed description of the  $\text{ON\_OFF\_CONFIG}$  command.

Some examples of typical ON/OFF configurations are:

1. A DC/DC converter may be configured to turn on any time  $V_{\text{IN}}$  exceeds  $\text{VIN\_ON}$ .
2. A DC/DC converter may be configured to turn on only when it receives an  $\text{OPERATION}$  command.
3. A DC/DC converter may be configured to turn on only via the  $\text{CONTROL}$  pin.
4. A DC/DC converter may be configured to turn on only when it receives an  $\text{OPERATION}$  command and the  $\text{CONTROL}$  pin is asserted.

## APPLICATIONS INFORMATION

### ON Sequencing

The TON\_DELAY command sets the amount of time that a channel will wait following the start of an ON sequence before its  $V_{OUT\_EN}$  pin will enable a DC/DC converter. Once the DC/DC converter has been enabled, the TON\_RISE value determines the time at which the device soft-connects the DAC and servos the DC/DC converter output to the VOUT\_COMMAND value. The TON\_MAX\_FAULT\_LIMIT value determines the time at which the device checks for an undervoltage condition. If a TON\_MAX\_FAULT occurs, the channel can be configured to disable the DC/DC converter and propagate the fault to other channels using the bidirectional FAULTB pins. Figure 25 shows a typical on-sequence using the CONTROL pin. Note that overvoltage faults are checked against the VOUT\_OV\_FAULT\_LIMIT value at all times the device is powered up and not in a reset state nor margining while ignoring OVs.

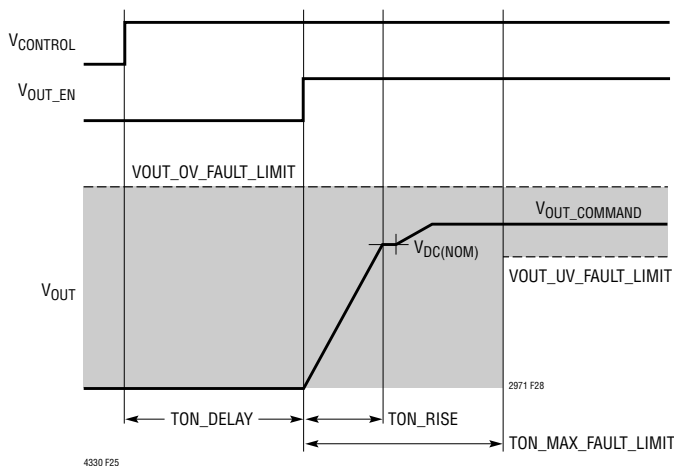


Figure 25. Typical ON Sequence Using Control Pin

### ON State Operation

Once a channel has reached the ON state, the OPERATION command can be used to command the DC/DC converter's output to margin high, margin low, or return to a nominal output voltage indicated by VOUT\_COMMAND. The user also has the option of configuring a channel to continuously trim the output of the DC/DC converter to the VOUT\_COMMAND voltage, or the channel's  $V_{DACn}$  output can be placed in a high impedance state thus allowing the DC/DC converter output voltage to go to its nominal value,

$V_{DCn(NOM)}$ . Refer to the MFR\_CONFIG\_LTC2971 command for details on how to configure the output voltage servo.

### Servo Modes

The ADC, DAC and internal processor comprise a digital servo loop that can be configured to operate in several useful modes. The servo target refers to the desired output voltage.

Continuous/non-continuous trim mode: MFR\_CONFIG\_LTC2971 b[7]. In continuous trim mode, the servo will update the DAC in a closed loop fashion each time it takes a  $V_{OUT}$  reading. The update rate is determined by the time it takes to step through the ADC MUX which is no more than  $t_{UPDATE\_ADC}$ . See [Electrical Characteristics](#) table Note 6. In non-continuous trim mode, the servo will drive the DAC until the ADC measures the output voltage desired and then stop updating the DAC.

As part of continuous/noncontinuous trim mode, fast servo mode can be used to speed up large output transitions, such as margin commands, or ON events. To use, set Mfr\_config\_fast\_servo\_off = 0. When enabled, fast servo is started by a change to the target voltage or a new soft connect. The DAC is ramped one LSB every  $t_{S\_VDAC}$  period until it is near the new target voltage, at which point slow servo mode is entered to avoid overshoot.

Non-continuous servo on warn mode: MFR\_CONFIG\_LTC2971 b[7] = 0, b[6] = 1. When in non-continuous mode, the LTC2971 will re-trim (re-servo) the output if the output drifts beyond the OV or UV warn limits.

### DAC Modes

The DACs that drive the  $V_{DACn}$  pins can operate in several useful modes. See MFR\_CONFIG\_LTC2971.

- Soft-connect. Using the ADI patented soft-connect feature, the DAC output is driven to within 1LSB of the voltage at the DC/DC's feedback node before connecting, to avoid introducing transients on the output. This mode is used when servoing the output voltage. During startup, the LTC2971 waits until TON\_RISE has expired before connecting the DAC. This is the most common operating mode.
- Disconnected. DAC output is high Z.

## APPLICATIONS INFORMATION

- DAC manual with soft-connect. Non servo mode. The DAC soft connects to the feedback node. Soft-connect drives the DAC code to match the voltage at the feedback node. After connection, the DAC is moved by writing DAC codes to the MFR\_DAC.
- DAC manual with hard connect. Non servo mode. The DAC hard connects to the feedback node using the current value in MFR\_DAC. After connection, the DAC is moved by writing DAC codes to the MFR\_DAC.

### Margining

The LTC2971 margins and trims the output of a DC/DC converter by forcing a voltage across an external resistor connected between the DAC output and the feedback node or the trim pin. Preset limits for margining are stored in the VOUT\_MARGIN\_HIGH/LOW registers. Margining is actuated by writing the appropriate bits to the OPERATION register.

Margining requires the DAC to be connected. Margin requests that occur when the DAC is disconnected will be ignored.

### Off Sequencing

An off sequence is initiated using the CONTROL pin or the OPERATION command. The TOFF\_DELAY value determines the amount of time that elapses from the beginning of the off sequence until each channel's V<sub>OUT\_EN</sub> pin is pulled low, thus disabling its DC/DC converter.

### V<sub>OUT</sub> Off Threshold Voltage

The MFR\_VOUT\_DISCHARGE\_THRESHOLD command register allows the user to specify the OFF threshold that the output voltage must decay below before the channel can enter/re-enter the ON state. The OFF threshold voltage is specified by multiplying MFR\_VOUT\_DISCHARGE\_THRESHOLD and VOUT\_COMMAND. In the event that an output voltage has not decayed below its OFF threshold before attempting to enter the ON state, the channel will continue to be held off, the appropriate bit is set in the STATUS\_MFR\_SPECIFIC register, and the ALERTB pin will be asserted low. When the output voltage has decayed below its OFF threshold, the channel can enter the ON state.

### Automatic Restart via MFR\_RESTART\_DELAY Command and CONTROL Pin

An automatic restart sequence can be initiated by driving the CONTROL pin to the OFF state for >10 $\mu$ s and then releasing it. The automatic restart disables both V<sub>OUT\_EN</sub> pins that are mapped to a particular CONTROL pin for a time period = MFR\_RESTART\_DELAY and then starts all DC/DC Converters according to their respective TON\_DELAYS. (see Figure 26). V<sub>OUT\_EN</sub> pins are mapped to one of the CONTROL pins by the MFR\_CONFIG\_LTC2971 command. This feature allows a host that is about to reset to restart the power in a controlled manner after it has recovered.

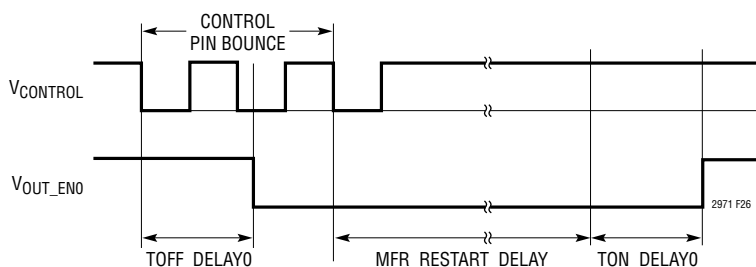


Figure 26. Off Sequence with Automatic Restart

## APPLICATIONS INFORMATION

### FAULT MANAGEMENT

#### Output Overvoltage and Undervoltage Faults

The high-speed voltage supervisor OV and UV fault thresholds are configured using the VOUT\_OV\_FAULT\_LIMIT and VOUT\_UV\_FAULT\_LIMIT commands, respectively. The VOUT\_OV\_FAULT\_RESPONSE and VOUT\_UV\_FAULT\_RESPONSE commands determine the responses to OV/UV faults. Fault responses can range from disabling the DC/DC converter immediately, waiting to see if the fault condition persists for some interval before disabling the DC/DC converter, or allowing the DC/DC converter to continue operating in spite of the fault. If a DC/DC converter is disabled, the LTC2971 can be configured to retry one to six times, retry continuously without limitation, or latch-off. The retry interval is specified using the MFR\_RETRY\_DELAY command. Latched faults are reset by toggling the CONTROL pin, using the OPERATION command, or removing and reapplying the bias voltage to the V<sub>IN\_SNS</sub> pin. All fault and warning conditions result in the ALERTB pin being asserted low and the corresponding bits being set in the status registers. The CLEAR\_FAULTS command resets the contents of the status registers and de-asserts the ALERTB output.

#### Output Overvoltage, Undervoltage, and Overcurrent Warnings

OV, UV, and OC warning thresholds are processed by the LTC2971's ADC. These thresholds are set by the VOUT\_OV\_WARN\_LIMIT, VOUT\_UV\_WARN\_LIMIT, and IOUT\_OC\_WARN\_LIMIT commands, respectively. Note that there is no I<sub>OUT</sub> UC warning threshold. If a warning occurs, the corresponding bits are set in the status registers and the ALERTB output is asserted low. Note that a warning will never cause a V<sub>OUT\_EN</sub> output pin to disable a DC/DC converter.

#### Configuring the AUXFAULTB Output

The AUXFAULTB output may be used to indicate an output OV or UV fault. Use the MFR\_CONFIG2\_LTC2971 and MFR\_CONFIG3\_LTC2971 registers to configure the AUXFAULTB pin to assert low in response to VOUT\_OV or VOUT\_UV fault conditions. The AUXFAULTB output will stop pulling low when the LTC2971 is commanded to re-enter the ON state following a faulted-off condition.

## APPLICATIONS INFORMATION

### Multi-Channel Fault Management

Multi-channel fault management is handled using the bidirectional FAULTB pins. [Figure 27](#) illustrates the connections between channels and the FAULTB pins.

- The MFR\_FAULTB<sub>n</sub>\_PROPAGATE command acts like a programmable switch that allows faulted\_off conditions from a particular channel (PAGE) to propagate to either FAULTB output. The MFR\_FAULTB<sub>n</sub>\_RESPONSE
- A FAULTB pin can also be asserted low by an external driver in order to initiate an immediate off-sequence after a 10µs deglitch delay.

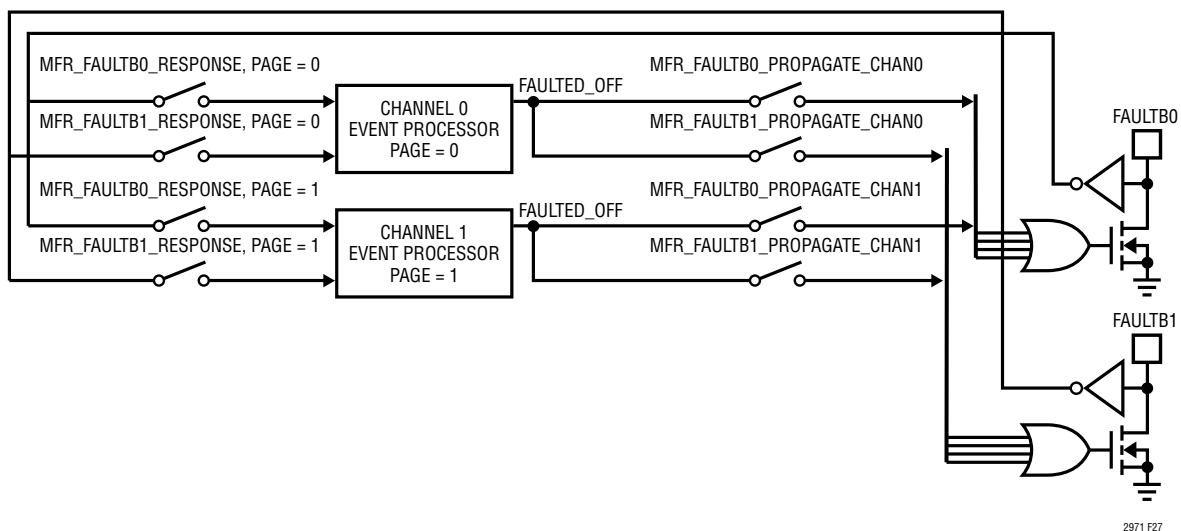


Figure 27. Channel Fault Management [Block Diagram](#)

## APPLICATIONS INFORMATION

### INTERCONNECT BETWEEN MULTIPLE ADI POWER MANAGERS

Figure 28 shows how to interconnect the pins in a typical multi-LTC2971 array.

- All  $V_{IN\_SNS}$  lines should be tied together in a star type connection at the point where  $V_{IN}$  is to be sensed. This will minimize timing errors for the case where the `ON_OFF_CONFIG` is configured to start the LTC2971 based on  $V_{IN}$  and ignore the `CONTROL` line and the `OPERATION` command. In multi-part applications that are sensitive to timing differences, it is recommended that the `Vin_share_enable` bit of the `MFR_CONFIG_ALL_LTC2971` register be set high in order to allow `SHARE_CLK` to synchronize on/off sequencing in response to the `VIN_ON` and `VIN_OFF` thresholds.
- Connecting all `AUXFAULTB` lines together will allow selected faults on any DC/DC converter's output in the array to shut off a common input switch.

- `ALERTB` is typically one line in an array of PMBus converters. The LTC2971 allows a rich combination of faults and warnings to be propagated to the `ALERTB` pin.
- `WDI/RESETB` can be used to put the LTC2971 in the power-on reset state. Pull `WDI/RESETB` low for at least  $t_{RESETB}$  to enter this state.
- The `FAULTB` lines can be connected together to create fault dependencies. Figure 28 shows a configuration where a fault on any `FAULTB` will pull all others low. This is useful for arrays where it is desired to abort a startup sequence in the event any channel does not come up (see Figure 29).
- `PWRGD` reflects the status of the outputs that are mapped to it by the `MFR_PWRGD_EN` command. Figure 28 shows all the `PWRGD` pins connected together, but any combination may be used.

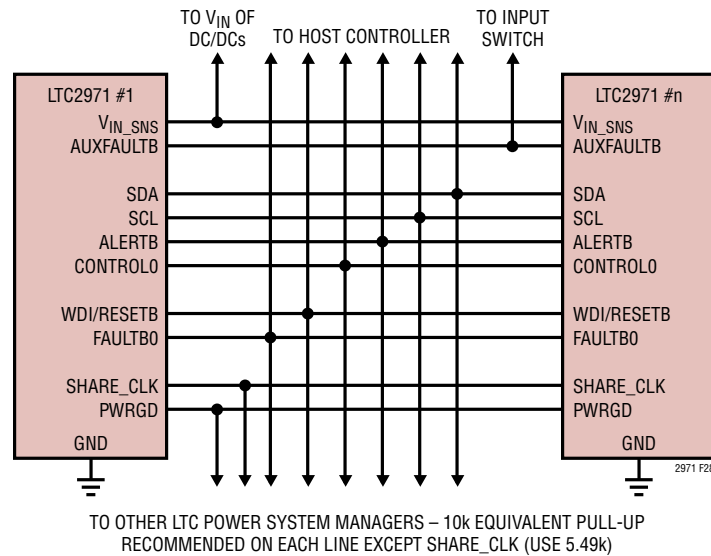


Figure 28. Typical Connections Between Multiple ADI Power System Managers

## APPLICATIONS INFORMATION

### APPLICATION CIRCUITS

#### Trimming and Margining DC/DC Converters with External Feedback Resistors and Positive $V_{FB}$

Figure 30 shows a typical application circuit for trimming/margining a power supply with an external feedback network. The  $V_{OUT\_SNS0}$  and  $GND_{SNS0}$  differential inputs sense the load voltage directly, and a correction voltage is developed on the  $V_{DAC0}$  pin by the closed-loop servo algorithm. The DAC output is connected to the DC/DC converter's feedback node through resistor  $R_{30}$ . Set  $Mfr\_config\_dac\_pol$  to 0.  $V_{FB}$  is a positive voltage. Positive voltage converters typically set  $V_{RET}$  to 0V. Some inverting DC/DC converters use this topology with  $V_{RET}$  tied to a positive voltage greater than  $V_{FB}$ .

#### Four-Step Resistor Selection Procedure for DC/DC Converters with External Feedback Resistors and Positive $V_{FB}$

The following four-step procedure should be used to calculate the resistor values required for the application circuit shown in Figure 30.

1. Set  $R_{20}$  to a value that keeps current through the feedback network relative to the output current small yet causes negligible DC error from  $I_{FB}$ .
2. Solve for  $R_{10}$ .

$$R_{10} = R_{20} \cdot \left( \frac{V_{FB} - V_{RET}}{V_{DC(NOM)} - V_{FB}} \right) \quad (1)$$

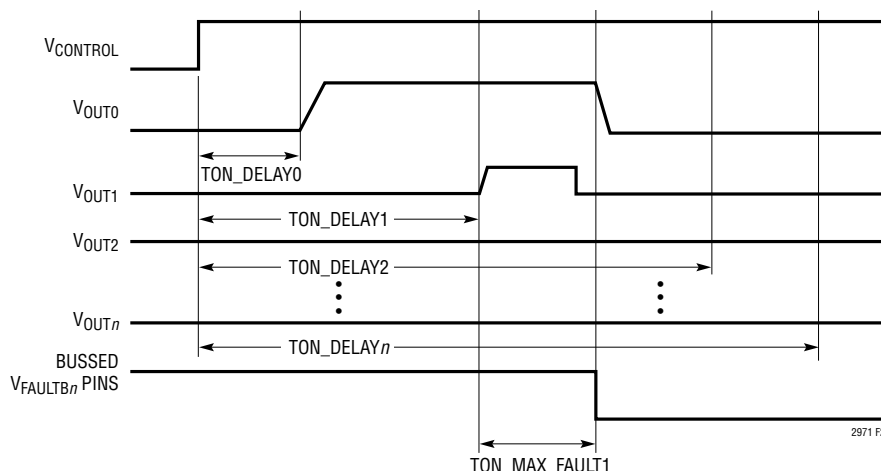


Figure 29. Aborted On-Sequence Due to Channel 1 Short



## APPLICATIONS INFORMATION

3. Set R30 so that the positive margining percentage,  $\Delta_{UP}\%$ , occurs when  $V_{DAC}=0V$ .

$$R30 < (R20 \parallel R10) \cdot \left( \frac{100}{\Delta_{UP}\%} \right) \quad (2)$$

To avoid the DAC output buffer's resistance change near 0V, R30 should be 10% less than its maximum value.

4. Set Mfr\_config\_dac\_gain so that the full-scale DAC setting,  $V_{FS\_VDAC}$ , of 1.38V or 2.65V encompasses the negative margining percentage,  $\Delta_{DOWN}\%$ .

$$V_{FS\_VDAC} > V_{DC(NOM)} \cdot \left( \frac{\Delta_{DOWN}\%}{100} \right) \cdot \left( \frac{R30}{R20} \right) + V_{FB} \quad (3)$$

When both settings work, choose the lower setting for better resolution.

### Trimming and Margining DC/DC Converters with a Trim Pin

Some DC/DC converter bricks use a trim pin and single resistor,  $R_{TRIM}$ , to set  $V_{DC}$ , and have an  $R_{TRIM}$  equation similar to:

$$R_{TRIM} = \frac{R20}{\frac{V_{DC(NOM)}}{V_{FB}} - 1} = R20 \cdot \left( \frac{V_{FB}}{V_{DC(NOM)} - V_{FB}} \right) \quad (4)$$

These converters use the same circuit as [Figure 30](#) with R20 included internally,  $V_{RET}=0V$ , and  $R_{TRIM}=R10$ . Thus, the previous section's equations work with R20 set. Other bricks vary this topology with R10 present internally, an internal resistor in series with  $R_{TRIM}$ , or  $V_{RET}$  non-zero. Consult ADI Field Application Engineering.

### Trimming and Margining DC/DC Converters with External Feedback Resistors and Negative $V_{FB}$

Some inverting regulator topologies use a negative  $V_{FB}$ . [Figure 31](#) shows a typical application circuit for trimming/margining a power supply with negative  $V_{FB}$  with an external feedback network. The Thevenin termination using  $V_{RET}$  causes  $V_{DAC}$  to see a positive voltage,  $V_P$ . The LTC2971's  $V_{REFP}$  functions as a suitable  $V_{RET}$ .

### Five-Step Resistor Selection Procedure for DC/DC Converters with External Feedback Resistors and Negative $V_{FB}$

The following five-step procedure should be used to calculate the resistor values required for the application circuit shown in [Figure 31](#).

1. Set R20 to a value that keeps current through the feedback network relative to the output current small yet causes negligible DC error from  $I_{FB}$ .
2. Set  $V_P$ , the voltage to which the DAC must soft-connect.

$$V_P = V_{FS\_VDAC} \cdot \left( \frac{\Delta_{UP}\%}{\Delta_{UP}\% + \Delta_{DOWN}\%} \right) \quad (5)$$

Note that for equal up/down margining,  $V_P$  is the DAC's midscale voltage. Mfr\_config\_dac\_gain chooses a full-scale DAC setting,  $V_{FS\_VDAC}$ , of 1.38V or 2.65V. Set Mfr\_config\_dac\_gain so that  $V_P < V_{RET}$ .

3. Solve for R10.

$$R10 = R20 \cdot \left( \frac{V_P - V_{FB}}{V_{FB} - V_{DC(NOM)}} \right) \quad (6)$$

4. Solve for R40.

$$R40 = R20 \cdot \left( \frac{V_{RET} - V_P}{V_{FB} - V_{DC(NOM)}} \right) \quad (7)$$

5. Set R30 so that the DC/DC converter output spans the minimum and maximum margining voltages over the DAC's range.

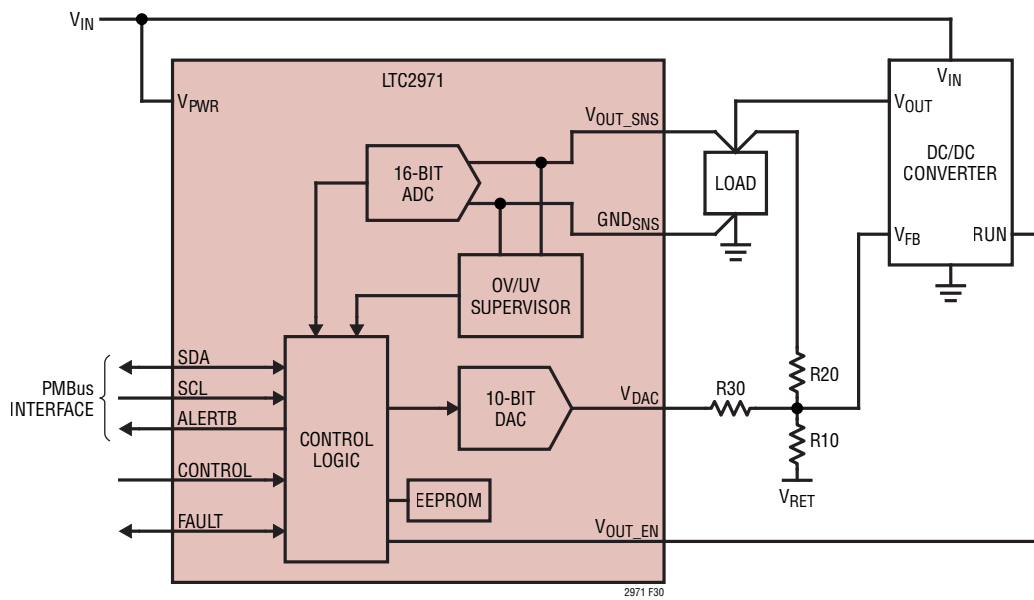
$$R30 < (R10 \parallel R40) \cdot \left[ \left( \frac{R20}{R10} \right) \cdot \left| \frac{-V_{FS\_VDAC}}{V_{DC(NOM)}} \right| \cdot \left( \frac{100}{\Delta_{UP}\% + \Delta_{DOWN}\%} \right) - 1 \right] \quad (8)$$

To avoid the DAC output buffer's resistance change near 0V, R30 should be 10% less than its maximum value.

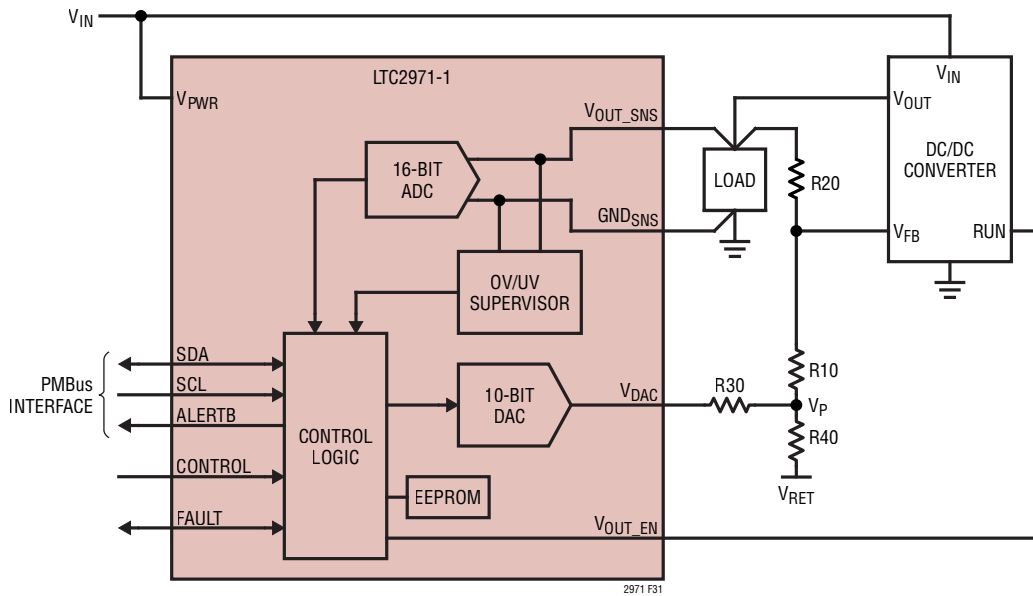
These equations also work for a positive DC/DC converter with  $V_{FB} > 0V$  and  $V_{RET}$  set to 0V, and make maximum use of the DAC range and thus optimize margining resolution versus [Figure 30](#)'s topology at the expense of one additional resistor.



**APPLICATIONS INFORMATION**



**Figure 30. Application Circuit for DC/DC Converters with External Feedback Resistors and Positive  $V_{FB}$**



**Figure 31. Application Circuit for DC/DC Converters with External Feedback Resistors and Negative  $V_{FB}$**

## APPLICATIONS INFORMATION

### Trimming and Margining Inverting DC/DC Converters with External Feedback Resistors and Current FBX

Some inverting DC/DC converters force a current,  $I_{INT}$ , out of an FBX pin. An external resistor is placed between FBX and OUT. An internal loop forces  $V_{DC}$  so that  $V_{FBX}=0V$ . [Figure 32](#) shows a typical application circuit for trimming/margining a power supply with external feedback resistors and a current FBX. The Thevenin termination using  $V_{RET}$  causes  $V_{DAC}$  to see a positive voltage,  $V_P$ . The LTC2971's  $V_{REFP}$  functions as a suitable  $V_{RET}$ .

### Four-Step Resistor Selection Procedure for Inverting DC/DC Converters with External Feedback Resistors and Current FBX

The following four-step procedure should be used to calculate the resistor values required for the application circuit shown in [Figure 32](#).

1. Set  $V_P$ , the voltage to which the DAC must soft-connect.

$$V_P = V_{FS\_VDAC} \cdot \left( \frac{\Delta_{UP}\%}{\Delta_{UP}\% + \Delta_{DOWN}\%} \right) \quad (9)$$

Add about  $0.1 \cdot (\Delta_{UP}\% + \Delta_{DOWN}\%)$  to the target  $\Delta_{UP}\%$  and  $\Delta_{DOWN}\%$  to avoid the DAC output buffer's resistance change near 0V.

Note that for equal up/down margining,  $V_P$  is the DAC's midscale voltage. Set `Mfr_config_dac_gain` so that  $V_P < V_{RET}$ .

2. Solve for R20.

$$R20 = \frac{|V_{DC(NOM)}|}{I_{INT}} \cdot \left( 1 - \frac{\Delta_{UP}\%}{100} \right) \quad (10)$$

3. Solve for R10.

$$R10 = \frac{V_P}{I_{INT}} \cdot \left( \frac{100}{\Delta_{UP}\%} - 1 \right) \quad (11)$$

4. Solve for R40.

$$R40 = R10 \cdot \left( \frac{V_{RET}}{V_P} - 1 \right) \quad (12)$$

## APPLICATIONS INFORMATION

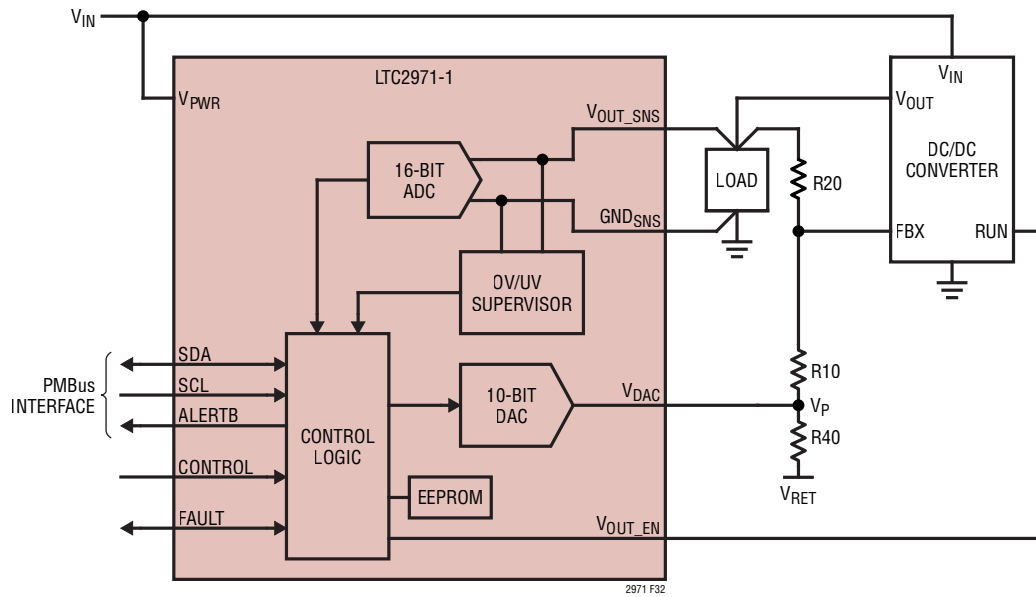


Figure 32. Application Circuit for DC/DC Converters with External Feedback Resistors and Current FBX

## APPLICATIONS INFORMATION

### Measuring Output with a Sense Resistor

A circuit for measuring current with a sense resistor is shown in [Figure 33](#).

Refer to Anti-Aliasing Filter Considerations for details about the optional filter network of R40, R50, and C30.

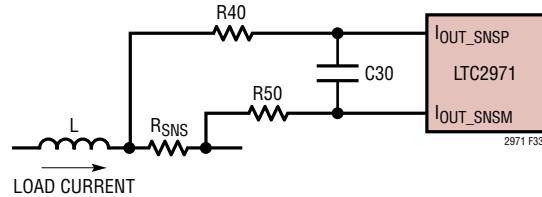


Figure 33. Sense Resistor Current Sensing Circuits

### Measuring Output with Inductor DCR

[Figure 34](#) shows the circuit for applications that require DCR current sense. A first order R-C filter is required to reduce ripple voltage to the differential range specification of  $\pm 80\text{mV}$ . The I\_OUT\_SNS internal anti-aliasing filter filters the remaining ripple to a negligible error. A value of  $250\Omega$  is suggested for R<sub>CM</sub> in order to minimize offset errors due to input bias current mismatch. C<sub>CM</sub> should be selected to provide cancellation of the zero created by the DCR and inductance, i.e.  $C_{CM} \geq L / (DCR \cdot R_{CM})$ . The optional C<sub>CM</sub> in parallel with the I\_OUT\_SNSM R<sub>CM</sub> matches the impedances between I\_OUT\_SNSP and I\_OUT\_SNSM.

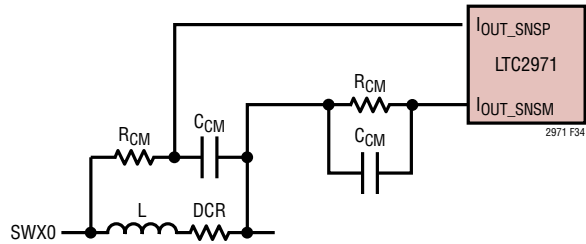


Figure 34. DCR Current Sensing Circuits

### Single Phase Design Example

As a design example for a DCR current sense application, assume  $L = 2.2\mu\text{H}$ ,  $DCR = 10\text{m}\Omega$ , and  $F_{SW} = 500\text{kHz}$ .

Let  $R_{CM} = 250\Omega$  and solve for C<sub>CM</sub>:

$$C_{CM} \geq \frac{2.2\mu\text{H}}{10\text{m}\Omega \cdot 250\Omega} = 880\text{nF}$$

### Measuring Multiphase Currents

For current sense applications with more than one phase, R-C averaging may be employed. [Figure 35](#) shows an example of this approach for a 3-phase system with DCR current sensing. The current sense waveforms are averaged together. Because the R<sub>CM</sub> resistors for the three phases are in parallel, the value of R<sub>CM</sub> must be multiplied by the number of phases. Also note that since the DCRs are effectively in parallel, the value for IOUT\_CAL\_GAIN will be equal to the inductor's DCR divided by the number of phases. Care should be taken in the layout of the multiphase inductors to keep the PCB trace resistance from the DC side of each inductor to the summing node balanced in order to provide the most accurate results.

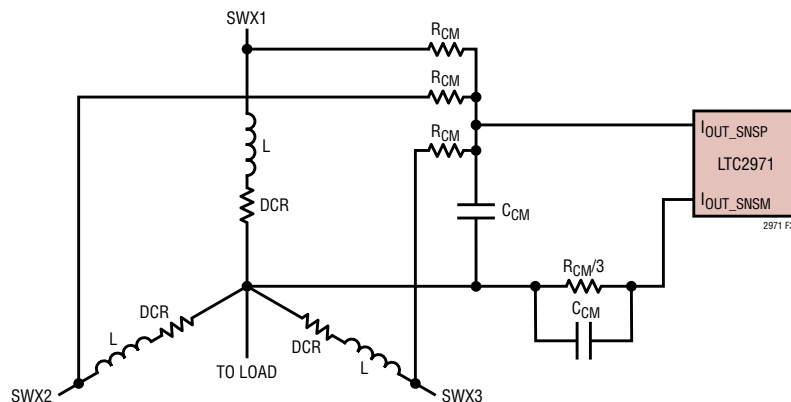


Figure 35. Multiphase DCR Current Sensing Circuits

## APPLICATIONS INFORMATION

### Multiphase Design Example

Using the same values for inductance and DCR from the previous design example, the value for  $R_{CM}$  will be  $750\Omega$  for a three phase DC/DC converter if  $C_{CM}$  is left at  $880nF$ . Similarly, the value for  $I_{OUT\_CAL\_GAIN}$  will be  $DCR/3 = 3.33m\Omega$ .

### Measuring Output Current in Buffered IMON Telemetry Mode

The LTC2971 can interface to power supplies that output a signal proportional to their internally measured output current by setting  $Mfr\_config\_imon = 1$ . This mode increases the  $I_{OUT\_SNS}$  input range from  $\pm 80mV$  to  $-0.1V$  to  $1.8V$ . Regulators whose IMON pin outputs a current proportional to the average load current will require a resistor to convert this current to a voltage for digitizing by the LTC2971 ADC. Figure 36 shows the LTC2971 connecting to the IMON pin of the LT<sup>®</sup>3086 LDO regulator.

### LT3086 IMON Design Example

The LT3086 will output a current equal to  $I_{IMON} = I_{OUT}/1000$ . If the desired  $V_{IMON}$  is  $1.0V$  for a total output

current of  $I_{OUT} = 2.0A$  then  $R_{IMON} = V_{IMON}/I_{IMON} = 500\Omega$  and  $I_{OUT\_CAL\_GAIN}$  should be programmed to  $500m\Omega$ .

### Anti-Aliasing Filter Considerations

All LTC2971 ADC inputs are internally filtered with a  $6kHz$  second order low pass anti-aliasing filter. Additionally the delta sigma ADC includes a  $62.5kHz$  sinc<sup>3</sup> filter. If additional filtering is necessary, add external filters of  $R_{40}$ ,  $R_{50}$  and  $C_{30}$  as shown in Figure 37 for  $V_{OUT\_SNS}$ . Use the same network for other ADC inputs. Set the filter's corner frequency to  $< 1/10$  the DC/DC converter's switching frequency. This offers a good compromise between voltage ripple and filter delay. When filtering  $V_{OUT\_SNS}$  and  $V_{IN\_SNS}$ , keep  $R_{40} = R_{50} \leq 250\Omega$  to minimize ADC gain errors due to the  $500k\Omega$  input resistance, and select a value for capacitor  $C_{30}$  that doesn't add too much additional response time to the supervisor, e.g.  $\tau = 10\mu s$  ( $R = 50\Omega$ ,  $C = 0.1\mu F$ ). Make sure the voltage rating of  $C_{30}$  is high enough to withstand the large voltage present. When filtering  $I_{OUT\_SNS}$  and  $I_{IN\_SNS}$ , keep  $R_{40} = R_{50} \leq 250\Omega$  to minimize ADC offset errors due to the  $100nA$  input bias current mismatch.

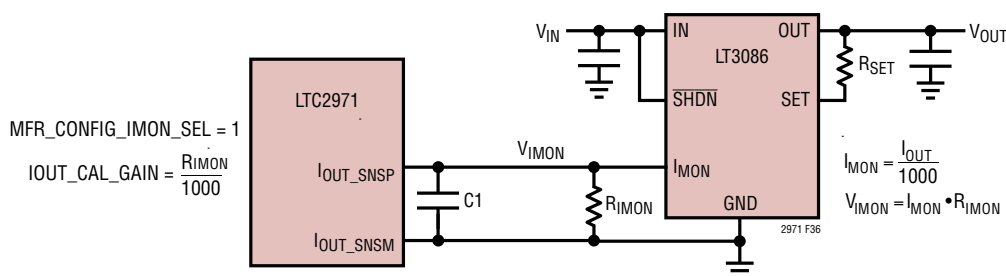


Figure 36. IMON Current Sensing

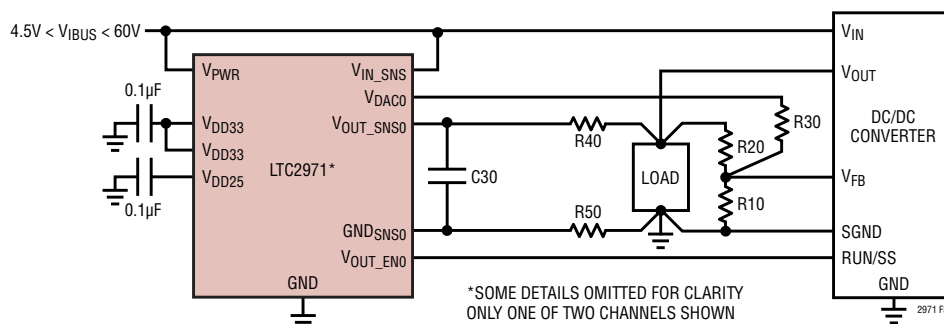


Figure 37. Anti-Aliasing Filter on  $V_{SENSE}$  Lines

## APPLICATIONS INFORMATION

### Connecting the DC1613 USB to I<sup>2</sup>C/SMBus/PMBus Controller to the LTC2971 in System

The DC1613 USB to I<sup>2</sup>C/SMBus/PMBus Controller can be interfaced to the LTC2971s on the user's board for programming, telemetry and system debug. The controller, when used in conjunction with LTpowerPlay software, provides a powerful way to debug an entire power system. Failures are quickly diagnosed using telemetry, fault status registers and the fault log. The final configuration can be quickly developed and stored to the LTC2971's EEPROM.

Figure 38 and Figure 39 illustrate application schematics for powering, programming and communicating with one or more LTC2971's via the ADI I<sup>2</sup>C/SMBus/PMBus controller regardless of whether or not system power is present.

Figure 38 shows the recommended schematic to use when the LTC2971 is powered by 3.3V. The LTC4412

ideal OR'ing circuit allows either the controller or system to power the LTC2971.

Because of the controller's limited current sourcing capability, only the LTC2971s, their associated pull-up resistors and the I<sup>2</sup>C/SMBus pull-up resistors should be powered from the ORed 3.3V supply. In addition, any device sharing I<sup>2</sup>C/SMBus bus connections with the LTC2971 should not have body diodes between the SDA/SCL pins and its V<sub>DD</sub> node because this will interfere with bus communication in the absence of system power.

The ADI controller's I<sup>2</sup>C/SMBus connections are opto-isolated from the PC's USB. The 3.3V from the controller and the LTC2971's V<sub>DD33</sub> pin can be paralleled because the ADI LDOs that generate these voltages can be back driven and draw <10μA. The controller's 3.3V current limit is 100mA.

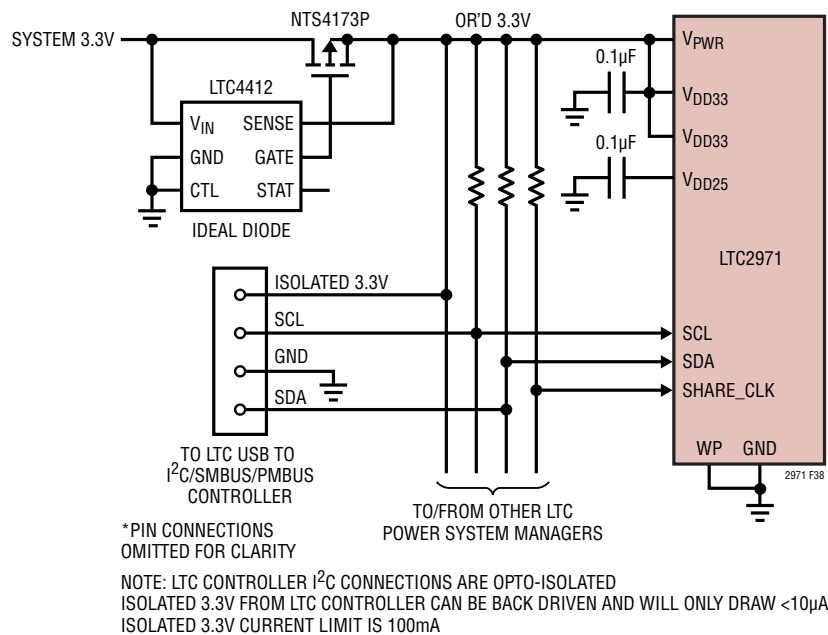


Figure 38. ADI Controller Connections When LTC2971 Is Powered from 3.3V

## APPLICATIONS INFORMATION

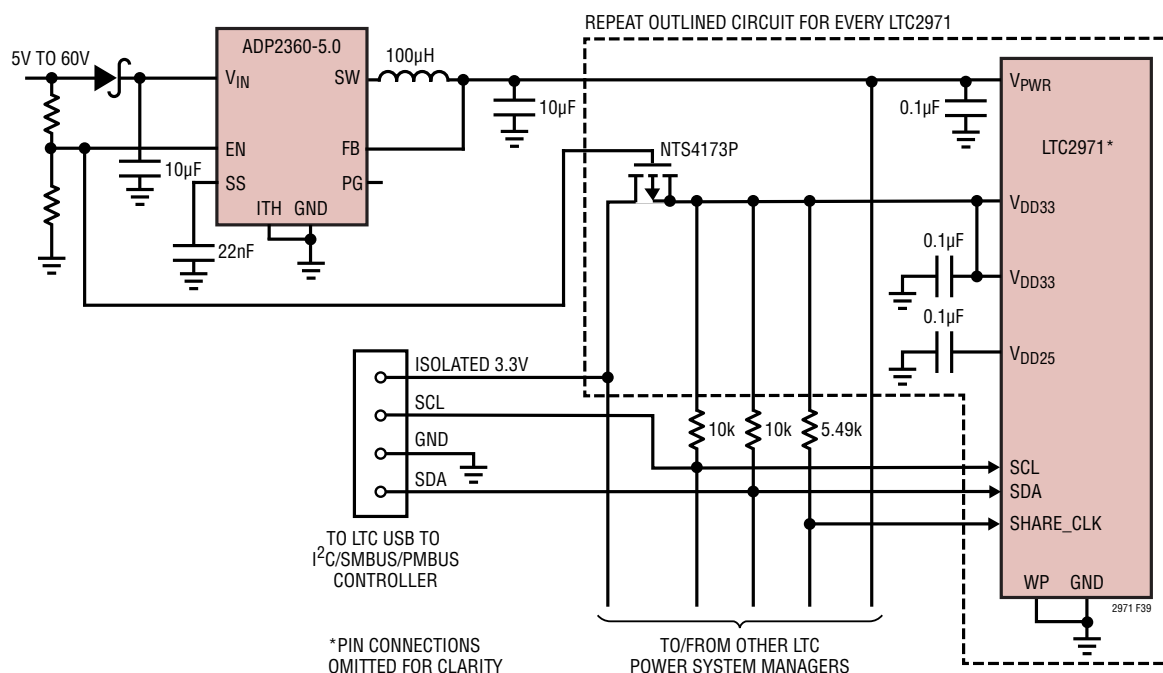


Figure 39. ADI Controller Connections When  $V_{PWR}$  Is Used

Figure 39 shows the recommended schematic to use when the LTC2971 is powered from 5V to 60V. An external switching regulator generates a local 5V supply to power the LTC2971. This saves power and avoids self-heating the LTC2971. The Schottky diode in series with the buck switching regulator satisfies the  $V_{PWR}$  current ABSMAX when the external supply is grounded.

### ACCURATE DCR TEMPERATURE COMPENSATION

Using the DC resistance of the inductor as a current shunt element has several advantages—no additional power loss, lower circuit complexity and cost. However, the strong temperature dependence of the inductor resistance and the difficulty in measuring the exact inductor core temperature introduce errors in the current measurement. For copper, a change of inductor temperature of only  $1^{\circ}\text{C}$  corresponds to approximately 0.39% current gain change. Figure 40 shows a sample layout using the integrated DC/DC converter LTC3601 (right) and its corresponding thermal image (left). The converter is providing 1.8V, 1.5A to the output load.

Heat dissipation in the inductor under high load conditions creates transient and steady state thermal gradients between the inductor and the temperature sensor, and the sensed temperature does not accurately represent the inductor core temperature. This temperature gradient is clearly visible in the thermal image of Figure 40. In addition, transient heating/cooling effects have to be accounted for in order to reduce the transient errors introduced when load current changes are faster than heat transfer time constants of the inductor. Both of these problems are addressed by introducing two additional parameters: the thermal resistance  $\theta_{IS}$  from the inductor core to the on-board temperature sensor, and the inductor thermal time constant  $\tau$ . The thermal resistance  $\theta_{IS}$  [ $^{\circ}\text{C}/\text{W}$ ], is used to calculate the steady state difference between the sensed temperature  $T_S$  and the internal inductor temperature  $T_I$  for a given power dissipated in the inductor  $P_I$ :

$$T_I - T_S = \theta_{IS} P_I = \theta_{IS} V_{DCR} I_{OUT} \quad (1.1)$$

## APPLICATIONS INFORMATION

The additional temperature rise is used for a more accurate estimate of the inductor DC resistance  $R_I$ :

$$R_I = R_0 (1 + \alpha [T_S - T_{REF} + \theta_{IS} V_{DCR} I_{OUT}]) \quad (1.2)$$

In these equations,  $V_{DCR}$  is the inductor DC voltage drop,  $I_{OUT}$  is the RMS value of the output current,  $R_0$  is the inductor DC resistance at the reference temperature  $T_{REF}$  and  $\alpha$  is the temperature coefficient of the resistance. Since most inductors are made of copper, we can expect a temperature coefficient close to  $\alpha_{CU} = 3900\text{ppm}/^\circ\text{C}$ . For a given  $\alpha$ , the remaining parameters  $\theta_{IS}$  and  $R_0$  can be calibrated at a single temperature using only two load currents:

$$R_0 = \frac{(R_2 - R_1)(P_2 + P_1) - (R_2 + R_1)(P_2 - P_1)}{\alpha(T_2 - T_1)(P_2 + P_1) - (P_2 - P_1)(2 + \alpha[T_1 + T_2 - 2T_{REF}])} \quad (1.3)$$

$$\theta_{IS} = \frac{1}{\alpha R_0} \frac{\alpha(R_1 + R_2)(T_2 - T_1) - (R_2 - R_1)(2 + \alpha[T_1 + T_2 - 2T_{REF}])}{\alpha(T_2 - T_1)(P_2 + P_1) - (P_2 - P_1)(2 + \alpha[T_1 + T_2 - 2T_{REF}])} \quad (1.4)$$

The inductor resistance,  $R_K = V_{DCR(K)}/I_{OUT(K)}$ , power dissipation  $P_K = V_{DCR(K)} I_{OUT(K)}$  and the sensed temperature  $T_K$ , ( $K = 1, 2$ ) are recorded for each load current. To increase the accuracy in calculating  $\theta_{IS}$ , the two load currents should be chosen around  $I_1 = 10\%$  and  $I_2 = 90\%$  of the current range of the system.

The inductor thermal time constant  $\tau$  models the first order thermal response of the inductor and allows accurate DCR compensation during load transients. During a transition from low to high load current, the inductor resistance increases due to the self-heating. If we apply a single load step from the low current  $I_1$  to the higher current  $I_2$ , the voltage across the inductor will change instantaneously from  $I_1 R_1$  to  $I_2 R_1$  and then slowly approach  $I_2 R_2$ . Here  $R_1$  is the steady state resistance at the given temperature and load current  $I_1$ , and  $R_2$  is the slightly higher DC resistance at  $I_2$ , due to the inductor self-heating. Note that the electrical time constant  $\tau_{EL} = L/R$  is several orders of magnitude shorter than the thermal one, and “instantaneous” is relative to the thermal time constant. The two settled regions give us the data sets  $(I_1, T_1, R_1, P_1)$  and  $(I_2, T_2, R_2, P_2)$  and the two-point calibration technique (1.3 – 1.4) is used to extract the steady-state parameters  $\theta_{IS}$  and  $R_0$  (given a previously characterized average  $\alpha$ ). The relative current error calculated using the steady-state expression (1.2) will peak immediately after the load step, and then decay to zero with the inductor thermal time constant  $\tau$ .

$$\frac{\Delta I}{I}(t) = \alpha \theta_{IS} (V_2 \cdot I_2 - V_1 \cdot I_1) e^{-t/\tau} \quad (1.5)$$

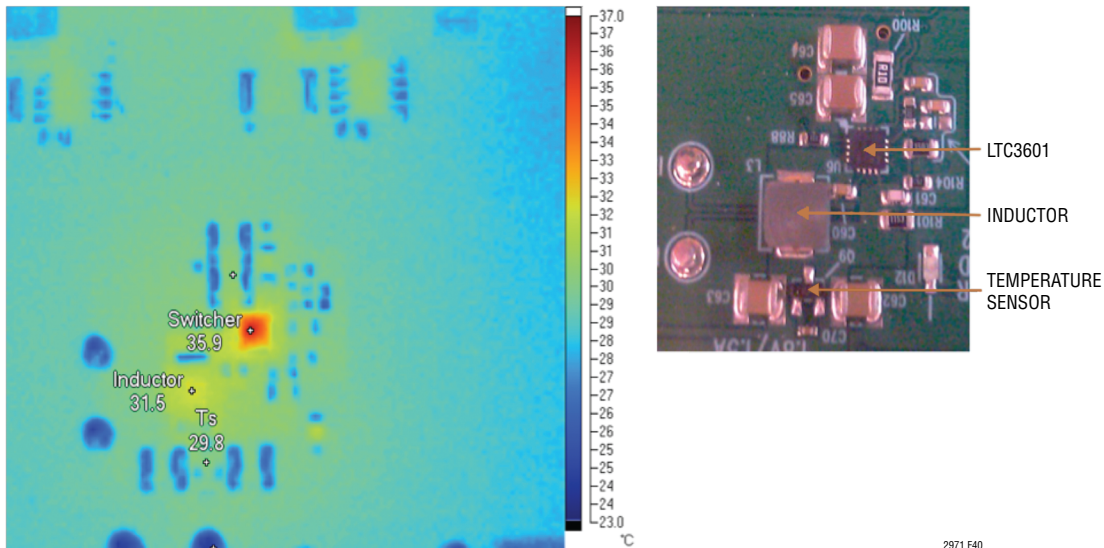


Figure 40. Thermal Image of a DC/DC Converter Showing the Difference Between the Actual Inductor Temperature and the Temperature Sensing Point

2971 F40



## APPLICATIONS INFORMATION

The time constant  $\tau$  is calculated from the slope of the best-fit line  $y = \ln(\Delta I/I) = a_1 + a_2 t$ :

$$\tau = -\frac{1}{a_2} \quad (1.6)$$

In summary, a single load current step is all that is needed to calibrate the DCR current measurement. The stable portions of the response give us the thermal resistance  $\theta_{IS}$  and nominal DC resistance  $R_0$ , and the settling characteristic is used to measure the inductor thermal time constant  $\tau$ .

To get the best performance, the temperature sensor has to be as close as possible to the inductor and away from other significant heat sources. For example in [Figure 40](#), the bipolar sense transistor is close to the inductor and away from the switcher. Connecting the collector of the PNP to the local power ground plane assures good thermal contact to the inductor, while the base and emitter should be routed to the LTC2971 separately, and the base connected to the signal ground close to LTC2971.

### LTpowerPlay: AN INTERACTIVE GUI FOR POWER MANAGERS

[Figure 41](#) shows LTpowerPlay interfacing to the LTC2971. LTpowerPlay is a powerful Windows based development environment that supports Analog Devices power manager ICs with EEPROM, including the LTC2971. The software supports a variety of different tasks. You can use LTpowerPlay to evaluate Analog Devices ICs by connecting to a demo board system. LTpowerPlay can also be used in an offline mode (with no hardware present) in order to build a multi-chip configuration file that can be saved and re-loaded at a later time. LTpowerPlay provides unprecedented diagnostic and debug features. It becomes a valuable diagnostic tool during board bring-up to program the power management scheme in a system. LTpowerPlay utilizes Analog Devices' DC1613 USB-to-I<sup>2</sup>C/SMBus/PMBus Controller to communicate with one of many potential targets including the DC2875 demo board set or a customer target system. The software also provides an automatic update feature to keep the software current

with the latest set of device drivers and documentation. A great deal of context sensitive help is available within LTpowerPlay along with several tutorial demos. [Complete information is available here.](#)

## PCB ASSEMBLY AND LAYOUT SUGGESTIONS

### Bypass Capacitor Placement

The LTC2971 requires 0.1 $\mu$ F bypass capacitors between the  $V_{DD33}$  pins and GND, the  $V_{DD25}$  pin and GND, the REFP pin and REFM pin. If the chip is being powered from the  $V_{PWR}$  input, then that pin should also be bypassed to GND by a 0.1 $\mu$ F capacitor. In order to be effective, these capacitors should be made of a high quality ceramic dielectric such as X5R or X7R and be placed as close to the chip as possible.

### PCB Board Layout

The LTC2971's high voltage pins are conveniently placed around the periphery of the package to allow plenty of space for nearby traces and vias. Follow high voltage spacing rules when routing these signals.

Mechanical stress on a PC board and soldering-induced stress can cause the LTC2971's reference voltage and the voltage drift to shift. A simple way to reduce the stress-related shifts is to mount the IC near the short edge of the PC board, or in a corner. The board acts as a stress boundary, or a region where the flexure of the board is minimal.

The LTC2971's current sense amplifiers have very low offsets enabling accurate current, power, and energy readings. PC Board routing to current sense inputs may create a thermal voltage offset if differential routing paths cross dissimilar metal boundaries in the presence of a thermal gradient. To minimize thermal voltages, route differential current sense inputs as close together as possible, and minimize vias. If vias are necessary, match the number and location of vias in the positive and negative current sense paths to minimize the temperature difference.

## APPLICATIONS INFORMATION

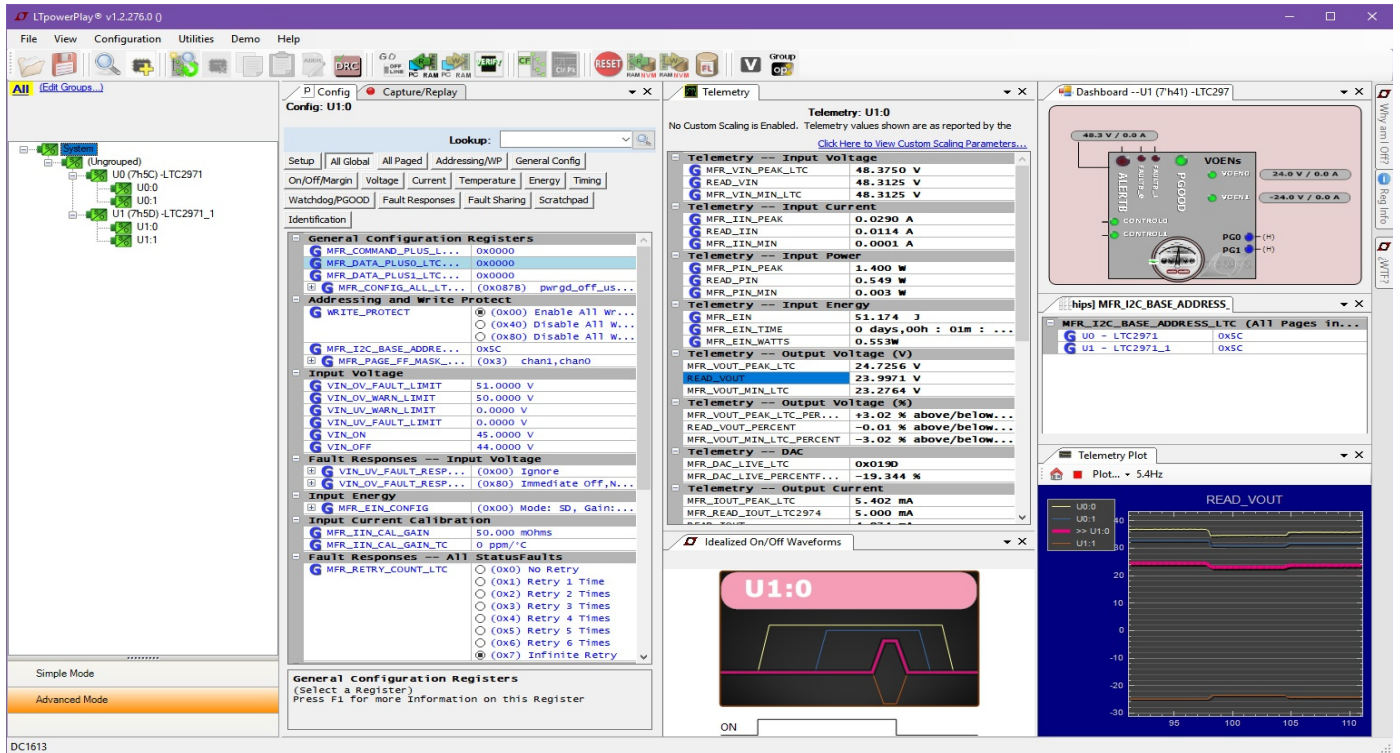


Figure 41. LTpowerPlay Snapshot

## APPLICATIONS INFORMATION

### Unused ADC Sense Inputs

Connect all unused ADC sense inputs ( $V_{OUT\_SNSn}$ ,  $GND_{SNSn}$ ,  $I_{OUT\_SNSPn}$ ,  $I_{OUT\_SNSMn}$ ,  $I_{IN\_SNSP}$ ,  $I_{IN\_SNSM}$ , or  $T_{SENSEn}$ ) to GND. In a system where the inputs are connected to removable cards and may be left floating in certain situations, connect the inputs to GND using 100k resistors. Place the 100k resistors before any filter components, as shown in [Figure 42](#), to prevent loading of the filter.

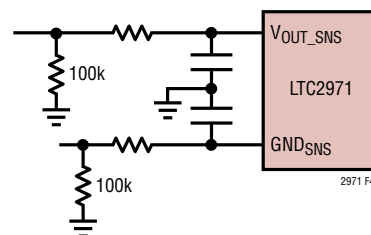


Figure 42. Connecting Unused Inputs to GND

### DESIGN CHECKLIST

#### ABSMAX

Verify that the absolute maximum rating of all pins are not exceeded.

When using the DC1613 USB to I<sup>2</sup>C Controller, use an external Schottky diode or other means to ensure reverse path current from  $V_{DD33}$  to  $V_{PWR}$  does not exceed the  $V_{PWR}$  current rating.

Shorting  $V_{OUT}$  to GND with a high value sense resistor can violate the  $I_{OUT\_SNSP}$  to  $I_{OUT\_SNSM}$  ABSMAX. The filter network in [Figure 33](#) can also protect against this case.

#### I<sup>2</sup>C

The LTC2971 must be configured for a unique address.

The address select pins ( $ASELn$ ) are tri-level; Check [Table 1](#).

Check addresses for collision with other devices on the bus and any global addresses.

#### Output Enables

Use appropriate pull-up resistors on both  $V_{OUT\_ENn}$  pins.

#### External Temperature Sense

Verify the PNP sense transistor is close to the inductor and away from other significant heat sources.

Verify the PNP sense transistor collector connects to a ground plane near the PNP, the emitter routes to the LTC2971, and the base connects to signal ground near the LTC2971.

### Logic Signals

Tie  $V_{DDIO}$  to a supply voltage between 1.5V and 3.6V.

Connect all SHARE\_CLK pins in the system together and pull-up to  $V_{DD33}$  with a 5.49k resistor.

Do not leave CONTROL $n$  pins floating. Pull up to  $V_{DDIO}$  with a 10k resistor.

Tie WDI/RESETB to  $V_{DD33}$  with a 10k resistor. Do not connect a capacitor to the WDI/RESETB pin.

Tie WP to either  $V_{DDIO}$  or GND. Do not leave floating.

Do not leave the FAULTB $n$  pins floating. Pull up to  $V_{DDIO}$  with a 10k resistor.

### Unused Inputs

Connect all unused  $V_{OUT\_SNSn}$ ,  $GND_{SNSn}$ ,  $I_{OUT\_SNSPn}$ ,  $I_{OUT\_SNSMn}$ ,  $I_{IN\_SNSP}$ ,  $I_{IN\_SNSM}$ , and  $T_{SENSEn}$  pins to GND. Do not float unused inputs.

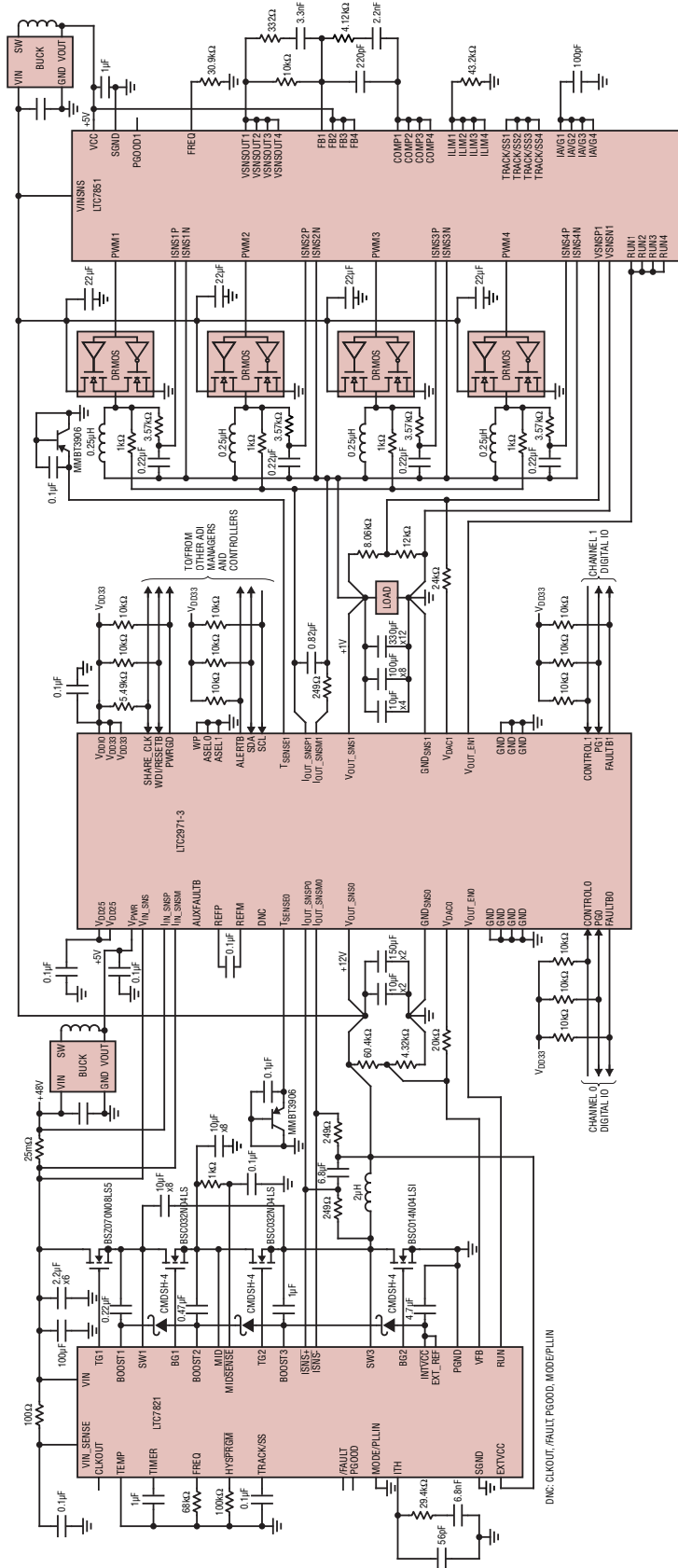
### DAC Outputs

Select appropriate resistor for desired margin range. Refer to the resistor selection tool in LTpowerPlay for assistance.

For a more complete list of design considerations and a schematic checklist, see the Design Checklist on the [LTC2971](#) product page.

TYPICAL APPLICATION

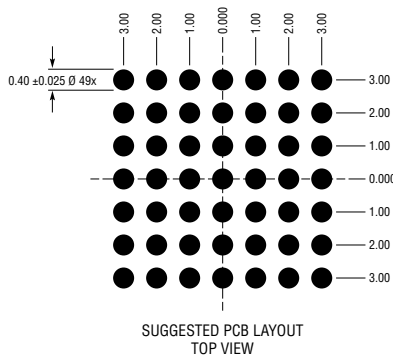
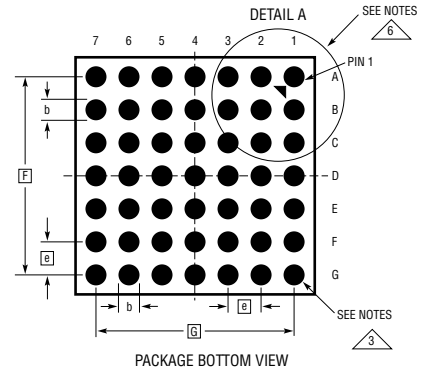
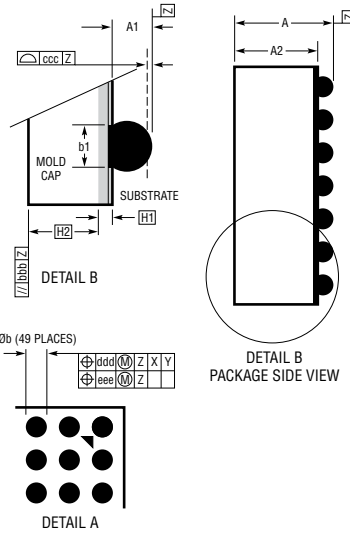
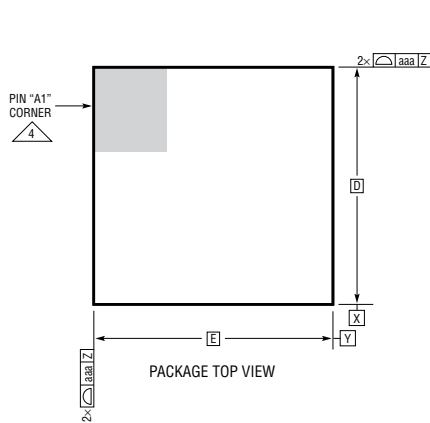
LTC2971-3 +48V to +1V



2971 TA02  
 DMC: CLKIN, CLKOUT, VSNSP2-4, VSNSN2-4, P600D2-4

# PACKAGE DESCRIPTION

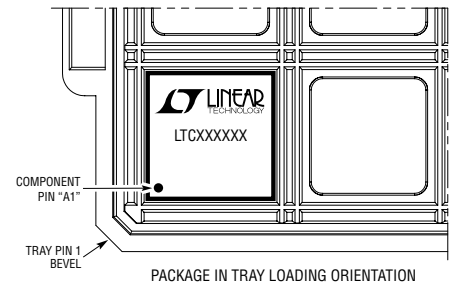
## BGA Package 49-Lead (7.00mm × 7.00mm × 1.44mm) (Reference LTC DWG # 05-08-1615 Rev 0)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.24	1.44	1.64	
A1	0.30	0.40	0.50	BALL HT
A2	0.94	1.04	1.14	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		7.00		
E		7.00		
e		1.00		
F		6.00		
G		6.00		
H1	0.29	0.34	0.39	SUBSTRATE THK
H2	0.65	0.70	0.75	MOLD CAP HT
aaa			0.15	
bbb			0.20	
ccc			0.20	
ddd			0.15	
eee			0.08	

TOTAL NUMBER OF BALLS: 49

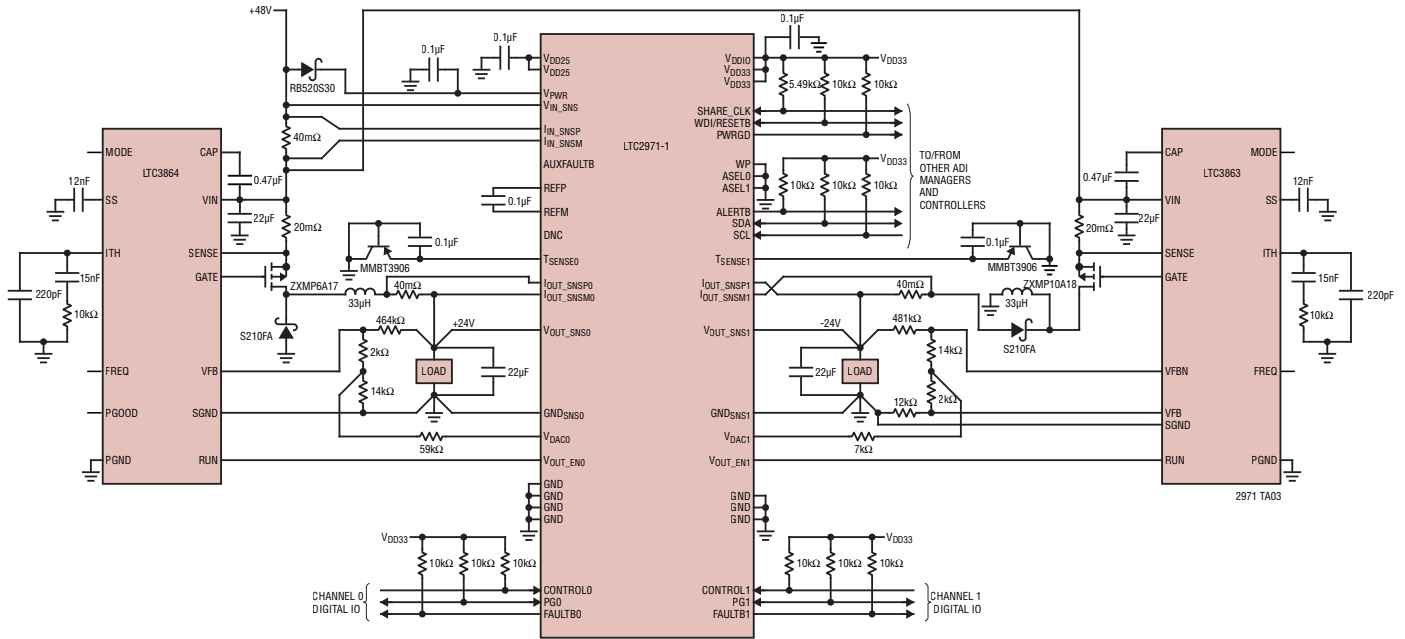
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. ALL DIMENSIONS ARE IN MILLIMETERS
  3. BALL DESIGNATION PER JEP95
  4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
  5. PRIMARY DATUM -Z- IS SEATING PLANE
  6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



BGA 49 1017 REV 0

## TYPICAL APPLICATION

### LTC2971-1 +48V to ±24V with Wide Margining Range



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LTC2972</a>	2-Channel Power System Manager Featuring Accurate Input Current and Energy Measurement	0.25% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision, Monitor Input Current and Accumulate Energy
<a href="#">LTC2975</a>	4-Channel Power System Manager Featuring Accurate Input Current and Energy Measurement	0.25% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision, Monitor Input Current (1%) and Accumulate Energy
<a href="#">LTC2970</a>	Dual I <sup>2</sup> C Power Supply Monitor and Margining Controller	5V to 15V, ±0.5% TUE 14-Bit ADC, 8-Bit DAC, Temperature Sensor
<a href="#">LTC2974</a>	4-Channel Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision
<a href="#">LTC2977</a>	8-Channel Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Temperature Monitoring and Supervision
<a href="#">LTC2980</a>	16-Channel PMBus Power System Manager	Dual LTC2977
<a href="#">LTM<sup>®</sup>2987</a>	16-Channel μModule <sup>®</sup> PMBus Power System Manager	Dual LTC2977 with Integrated Passive Components
<a href="#">LTC3889</a>	60V Dual Output Step-Down DC/DC Controller	0.5% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision
<a href="#">LTC7880</a>	60V Dual Output Step-Up DC/DC Controller	0.5% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision
<a href="#">LTC3884</a>	Single Output PolyPhase Step-Down DC/DC Controller with Sub-Milliohm DCR Sensing	0.5% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision
<a href="#">LTM4700</a>	Dual 50A or Single 100A μModule Regulator with Digital Power System Management	0.5% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision

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