LTC1773 Low Input Voltage Synchronous Current Mode Step-Down DC/DC Converter

DESCRIPTION

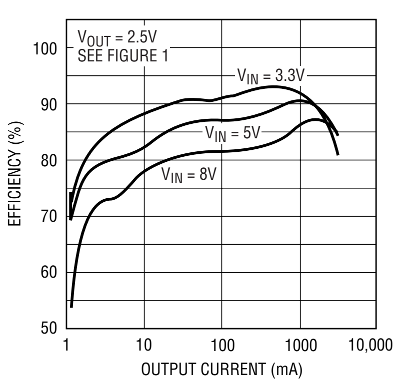
Demo board DC309 is a step-down (buck) regulator using the LTC®1773. The exclusive use of surface mount components results in a highly efficient application in a very small board space. It is ideal for cell phones and other portable electronics operating from one or two Li-Ion cells or three to six NiCd cells. DC309 is capable of providing 2.5A at an output voltage of 1.8V with an input supply of 3.3V. This demo board highlights the capabilities of the LTC1773, which uses a current mode PWM architecture to synchronously drive an external pair of P- and N-channel power MOSFETs. The result is a high performance power supply that has low output voltage ripple. A constant operating frequency of 550kHz makes the LTC1773 attractive for noise-sensitive applications while allowing for smaller external components such as the inductor and the output capacitor. In addition, its high efficiency over a wide load current range and its low quiescent current make the LTC1773 ideal for battery-powered applications. In dropout, the external P-channel MOSFET is turned on continuously (100% duty cycle), providing low dropout operation when V_{IN} approaches V_{OUT}. Under light load conditions, efficiency can be improved by activating Burst Mode™ operation, which is done by connecting the SYNC/FCB pin to V_{IN} or leaving it floating. Tying this pin to ground will force continuous operation, regardless of the load. The SYNC/FCB pin can also be used to synchronize the LTC1773 to frequencies of up to 750kHz. At input voltages below 2.5V, the LTC1773's undervoltage lockout feature is activated, shutting down the output. Soft-start is provided by connecting an external capacitor to the RUN/SS pin. **Gerber files for this circuit board are available. Call the LTC factory.**

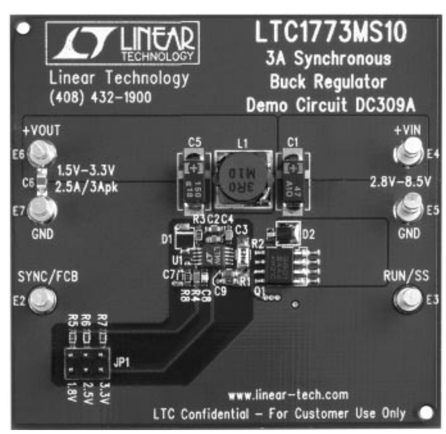
PERFORMANCE SUMMARY

SYMBOL	PARAMETER	CONDITIONS	VALUE
V_{IN}	Input Supply Voltage Range	V_{OUT} = 1.8V	2.8V to 8.5V
V_{OUT}	Output Voltage	I_{OUT} = 1A I_{OUT} = 1A I_{OUT} = 1A I_{OUT} = 1A	3.3V ±0.066V 2.5V ±0.050V 1.8V ±0.036V 1.5V ±0.030V

TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

Efficiency



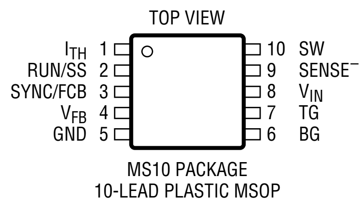


dc309fa

PERFORMANCE SUMMARY

SYMBOL	PARAMETER	CONDITIONS	VALUE
V_{FB}	Feedback Voltage		0.8V ±0.012V
I_Q	Supply Current Burst Mode Operation Shutdown	 V_{IN} = 5V, I_{OUT} = 0 V_{IN} = 5V, $V_{RUN/SS}$ = 0V	 130µA 10µA
I_{OUT}	Maximum Output Current	V_{IN} = 5V, V_{OUT} = 2.5V (Q1 = Si9801DY)	3A
ΔV_{OUT}	Typical Load Regulation	0mA < I_{OUT} < 3A, V_{IN} = 8.5V	–1%
V_{RIPPLE}	Typical Output Ripple	I_{OUT} = 3A, V_{IN} = 5V I_{OUT} = 100mA, Burst Mode Operation	40mV$_{P-P}$ 60mV$_{P-P}$
f_{SYNC}	Maximum Synchronizable Frequency	V_{OUT} = 2.5V, V_{IN} ≤ 8.5V V_{OUT} = 1.8V, V_{IN} ≤ 7V V_{OUT} = 1.5V, V_{IN} ≤ 6V	750kHz 750kHz 750kHz

PACKAGE AND SCHEMATIC DIAGRAMS



LTC1773EMS

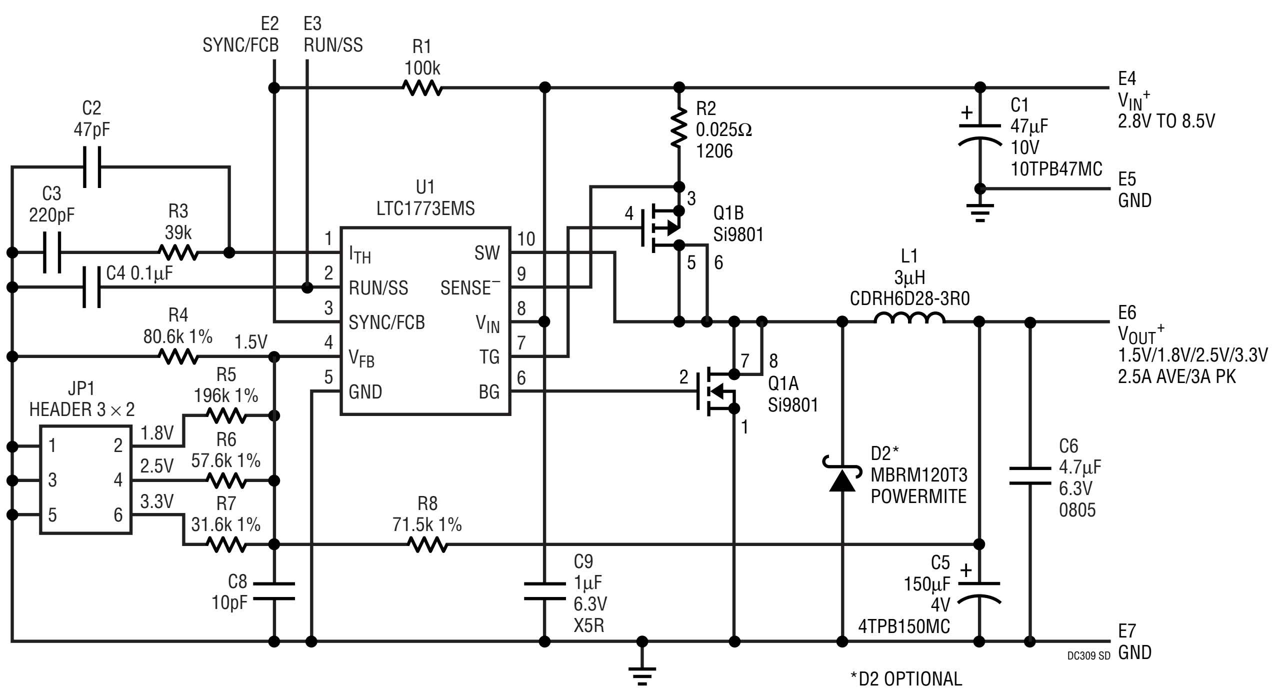


Figure 1. LTC1773 Low Input Voltage Synchronous Current Mode Step-Down DC/DC Converter

PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1	1	10TPB47MC	47µF 10V POSCAP Capacitor	Sanyo	(619) 661-6835
C2	1	06035A470JAT1A	47pF 50V NPO Ceramic Capacitor	AVX	(843) 946-0362
C3	1	06035A221JAT1A	220pF 50V NPO Ceramic Capacitor	AVX	(843) 946-0362
C4	1	EMK107BJ104MA	0.1µF 16V X5R Ceramic Capacitor	Taiyo Yuden	(408) 573-4150
C5	1	4TPB150MC	150µF 4V POSCAP Capacitor	Sanyo	(619) 661-6835
C6	1	JMK212BJ475MG	4.7µF 6.3V X5R Ceramic Capacitor	Taiyo Yuden	(408) 573-4150
C7	0		Don't Stuff		
C8	1	06035A100JAT2A	10pF 50V 5% NPO	AVX	(843) 946-0362
C9	1	JMK107BJ105MA	1µF 6.3V Y5V Ceramic Capacitor	Taiyo Yuden	(408) 573-4150
D1	0	MMSD914T1	Switching Diode (Don't Stuff)	ON Semiconductor	(602) 244-6600
D2	1	MBRM120T3	20V 1A Schottky Diode (Optional)	ON Semiconductor	(602) 244-6600
E1 to E6	6	2501-2	0.094" Turret Testpoint	Mill-Max	(516) 922-6000
JP1	1	2202S-06-G1	3-Pin 2-Row 0.079cc Header	Comm-Con	(626) 301-4200
JP1	1	CCIJ2MM-138G	0.079" Center Shunt	Comm-Con	(626) 301-4200
L1	1	CDRH6D28-3R0	3µH Inductor	Sumida	(847) 956-0667
Q1	1	Si9801DY	Dual N- and P-Channel MOSFET	Siliconix	(800) 554-5565
R1	1	CR16-104JM	100k 5% Chip Resistor	AAC	(800) 508-1521
R2	1	LRF1206-01-R025-J	0.025Ω Chip Resistor	IRC	(361) 992-7900
R3	1	CR16-393JM	39k 5% Chip Resistor	AAC	(800) 508-1521
R4	1	CR16-8062FM	80.6k 1% Chip Resistor	AAC	(800) 508-1521
R5	1	CR16-1963FM	196k 1% Chip Resistor	AAC	(800) 508-1521
R6	1	CR16-5762FM	57.6k 1% Chip Resistor	AAC	(714) 255-9186
R7	1	CR16-3162FM	31.6k 1% Chip Resistor	AAC	(714) 255-9186
R8	1	CR16-7152FM	71.5k 1% Chip Resistor	AAC	(714) 255-9186
U1	1	LTC1773EMS	IC	LTC	(408) 432-1900

QUICK START GUIDE

The DC309 demonstration board is easy to set up to evaluate the performance of the LTC1773. Please follow the procedure outlined below for proper operation.

1. Move jumper JP1 to the appropriate position for the required output voltage. The board is set up for a default output voltage of 1.5V if no jumper is used. To avoid possible damage to the LTC1773 device, make sure V_{IN} is off when moving the jumper JP1.
2. To shut down the circuit, connect the RUN/SS terminal to ground.
3. For synchronized operation, connect the clock signal between the SYNC/FCB and GND terminals. Do not apply more than the input voltage (V_{IN}) on the SYNC/FCB terminal.
4. For Burst Mode operation at low load currents, float the SYNC/FCB terminal or connect it to V_{IN}. Grounding this terminal will force continuous operation regardless of load current.
5. Connect the input power supply to the V_{IN} and GND terminals.
6. Connect the load between the V_{OUT} and GND terminals. Refer to Figure 2 for proper measurement equipment setup.

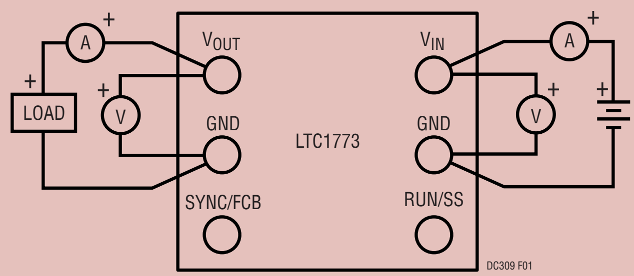


Figure 2. Proper Measurement Setup

COMPONENT SELECTION

Quick Components Selection Guide

COMPONENTS	I_{OUT} = 1A	I_{OUT} = 2.5A	I_{OUT} = 3A	I_{OUT} = 5A
R2	0.05Ω	0.025Ω	0.02Ω	0.015Ω
Q1	Si6803 or Si6801	Si9801	Si9803 and Si9804	2x Si9803 and Si9804
L1	6µH	3µH	3µH	1µH

The circuit shown in Figure 1 operates from an input voltage between 2.8V and 8.5V. Output voltages of 1.5V, 1.8V, 2.5V and 3.3V can be easily set by moving jumper JP1 to the appropriate position; make sure V_{IN} is off when doing this.

This demonstration circuit has been optimized for efficiency and physical footprint. For other requirements, please contact the factory. This demonstration circuit is intended for the evaluation of the LTC1773 switching regulator IC and was not designed for any other purpose.

External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, L can be chosen, followed by the external power MOSFETs. Finally, C_{IN} and C_{OUT} are selected.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1773 current comparator has a maximum threshold of $100mV/R_{SENSE}$. The current comparator threshold sets the peak inductor current, yielding a maximum average output current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Allowing a margin for variations in the LTC1773 and external component values yields:

$$R_{SENSE} = 70mV/I_{MAX}$$

Inductor Value Calculation

The inductor selection will depend on the operating frequency of the LTC1773. The internal preset frequency is 550kHz, but can be externally synchronized to frequencies of up to 750kHz.

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. However,

COMPONENT SELECTION

operating at a higher frequency generally results in lower efficiency because of external gate charge losses.

The inductor value has a direct effect on ripple current. The ripple current, ΔI_L, decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of lower inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{MAX})$.

Power MOSFET and Schottky Diode Selection

Two external power MOSFETs must be selected for use with the LTC1773: a P-channel MOSFET for the top (main) switch, and an N-channel MOSFET for the bottom (synchronous) switch.

This board is laid out with MOSFET footprints for three different output load requirements. For 1A or less applications, use the 8-pin TSSOP footprint on the back for complementary 1A MOSFETs in one package. For 2.5A applications, use the SO-8 footprint on the front for complementary 3A MOSFETs in one package. This is the default MOSFET footprint used on the board. For applications requiring more output current, use single packaged SO-8 MOSFETs (P-channel on the front and N-channel on the back).

The peak-to-peak gate drive levels are set by the V_{IN} voltage. Therefore, for $V_{IN} > 5V$, logic-level threshold MOSFETs should be used. But for $V_{IN} < 5V$, sublogic-level threshold MOSFETs ($V_{GS(TH)} < 3V$) should be used. In these applications, make sure that the V_{IN} to the LTC1773 is less than 8V because the absolute maximum VGS rating of a lot of these sublogic threshold MOSFETs is 8V.

Selection criteria for the power MOSFETs include the "ON" resistance, $R_{DS(ON)}$, reverse transfer capacitance, CRSS, input voltage, maximum output current and total gate charge.

A Schottky diode can be placed in parallel with the synchronous MOSFET to improve efficiency. It conducts during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. A 1.5A Schottky is generally a good size for 5A to 8A regulators due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance. The diode may be omitted if the efficiency loss can be tolerated.

C_{IN} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{MAX} \frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

C_{OUT} Selection

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisfied the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \cong \Delta I_L\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases

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with input voltage. With $\Delta I_L = 0.4I_{OUT(MAX)}$ and allowing for 2/3 of the ripple due to ESR, the output ripple will be less than 50mV at max V_{IN} assuming:

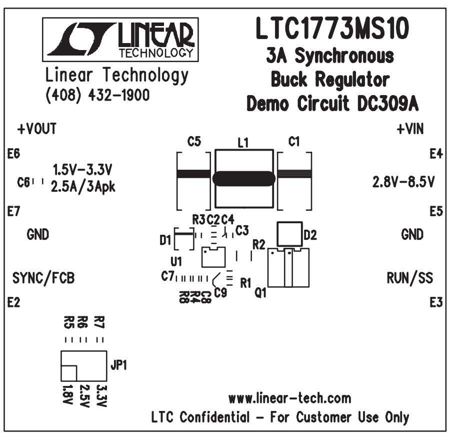
C_{OUT} required ESR < 2 R_{SENSE}

$C_{OUT} > 1/(8fR_{SENSE})$

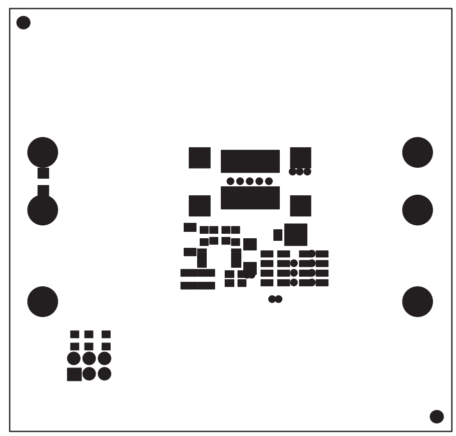
The first condition relates to the ripple current into the ESR of the output capacitance while the second term guarantees that the output voltage does not significantly discharge during the operating frequency period due to ripple current. The choice of using smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated for by using capacitors of very low ESR to maintain the ripple voltage at or below 50mV. The I_{TH} pin OPTI-LOOP™ compensation components can be optimized to provide stable, high performance transient response regardless of the output capacitors selected.

OPTI-LOOP is a trademark of Linear Technology Corporation.

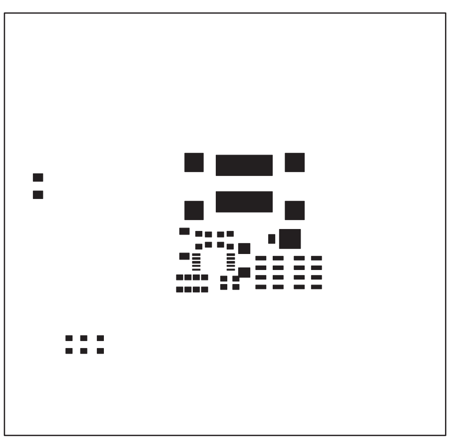
PCB LAYOUT AND FILM



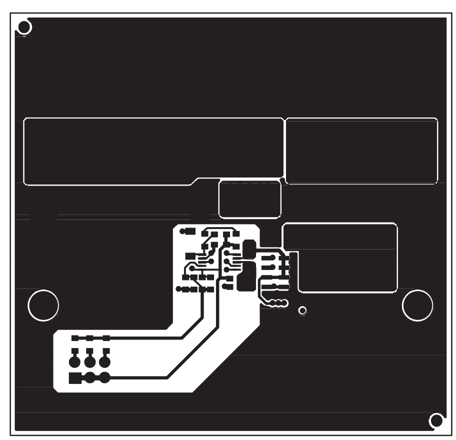
Component Side Silkscreen



Component Side Solder Mask

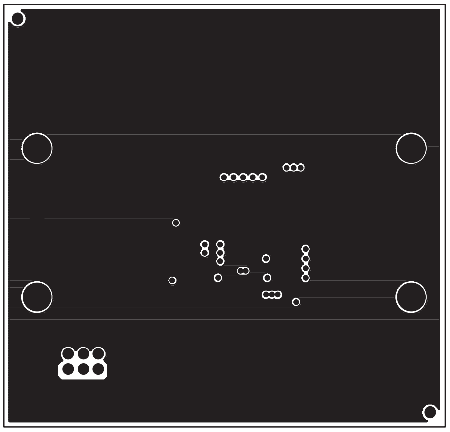


Component Side Paste Mask

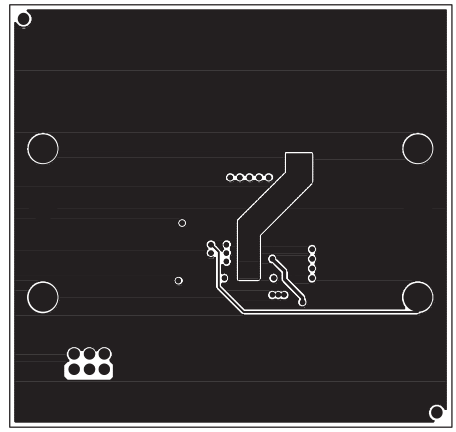


Layer 1 Component Side

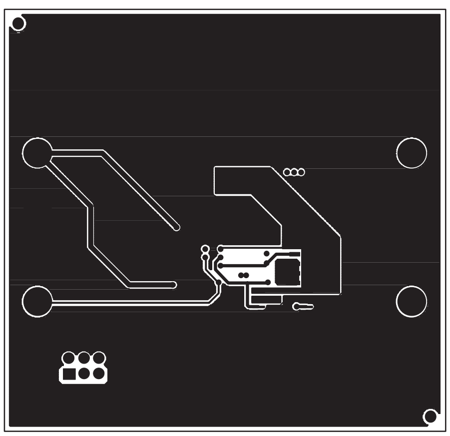
PCB LAYOUT AND FILM



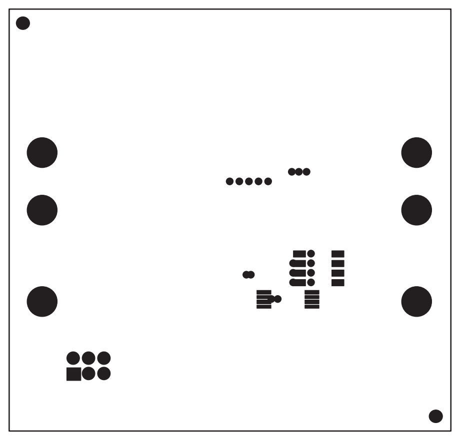
Layer 2 GND



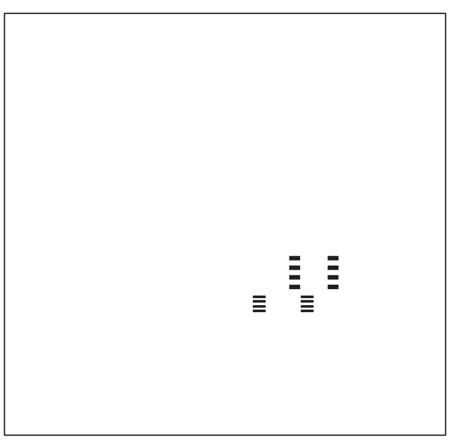
Layer 3 GND, $+V_{IN}$



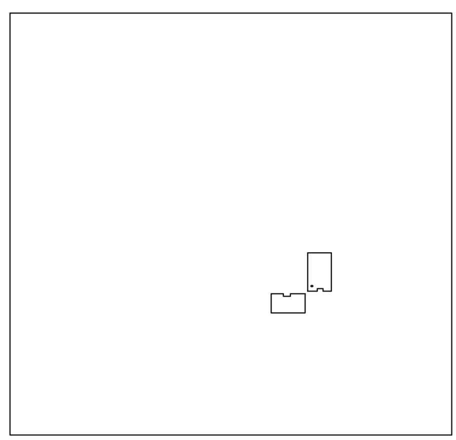
Layer 4 Solder Side



Solder Side Solder Mask

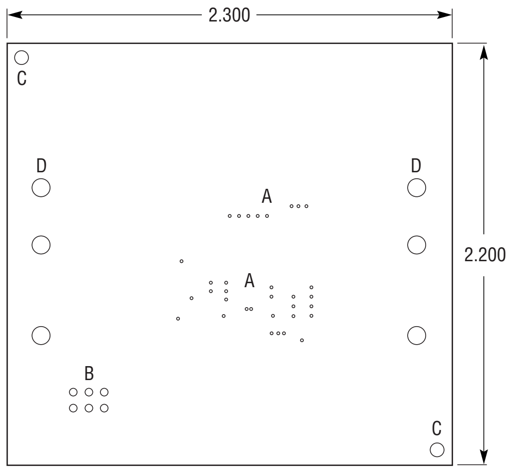


Solder Side Paste Mask



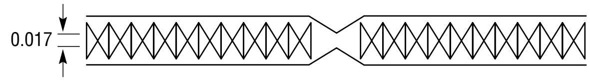
Solder Side Silkscreen

PC FAB DRAWING



NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: FR4 OR EQUIVALENT EPOXY,
   2 OZ COPPER CLAD, THICKNESS 0.062 ±0.006
   TOTAL OF 4 LAYERS
2. FINISH: ALL PLATED HOLES 0.001 MIN/0.0015 MAX
   COPPER PLATE, ELECTRODEPOSITED TIN-LEAD COMPOSITION
   BEFORE REFLOW, SOLDER MASK OVER BARE COPPER (SMOBC)
3. SOLDER MASK: BOTH SIDES USING LPI OR EQUIVALENT
4. SILKSCREEN: USING WHITE NONCONDUCTIVE EPOXY INK
5. ALL DIMENSIONS IN INCHES
6. SCORING



SYMBOL	DIAMETER	NUMBER OF HOLES	PLATED
A	0.015	33	PLTD
B	0.040	6	PLTD
C	0.072	2	NPLTD
D	0.094	6	PLTD
	TOTAL HOLES	47	

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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