## DESCRIPTION

Demonstration circuit 684A is a 48V Hot Swap ${ }^{\text {TM }}$ controller featuring the LT4256-3 in a 2 A application. The LT4256-3 is ideally suited for demanding power distribution control in $12 \mathrm{~V}, 24 \mathrm{~V}$ and 48 V applications for hot board insertion protection, high side power switching, and electronic circuit breaker functions. The LT4256-3 provides a rich set of features to support Hot Swap applications including:

- Overvoltage Shutdown
- Undervoltage Lockout
- Foldback Inrush Current Limiting
- Overcurrent Circuit Breaker with Programmable Cutout Time
- Programmable Output Voltage Ramp Rate
- Selectable Auto Retry or Latchoff on Overcurrent Faults
- Power Good Monitor
- Open MOSFET Detection

Available in a 16-lead SSOP package, the LT4256-3 is showcased on demonstration circuit 684A configured for a 48V, 2 A application. By changing a few passive components, 12 V and 24 V applications can easily be evaluated at up to 10A provided the thermal considerations of pass FET Q1 are taken into account.

Design files for this circuit board are available at http://www.linear.com/demo/DC684A
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## PERFORMANCE SUMMARY

Specifications are at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| PARAMETER | CONDITION | VALUE |
| :--- | :--- | :--- |
| Minimum Input Voltage | Determined by UVLO | 37 V |
| Maximum Input Voltage | Determined by TVS D2 Breakdown Voltage | 76 V |
| Undervoltage L to H Threshold | UVLO Pin Threshold $4 \mathrm{~V} \pm 1 \%$ | $36.3 \mathrm{~V} \pm 1.5 \%$ |
| Overvoltage L to H Threshold | OVLO Pin Threshold $4 \mathrm{~V} \pm 1 \%$ | $72.5 \mathrm{~V} \pm 1.5 \%$ |
| Power Good L to H Threshold | FB L to H Threshold $4.45 \mathrm{~V} \pm 1 \%$ | $44.9 \mathrm{~V} \pm 1.5 \%$ |
| Power Good H to L Threshold | FB H to L Threshold $3.99 \mathrm{~V} \pm 1 \%$ | $40.2 \mathrm{~V} \pm 1.5 \%$ |
| Current Breaker Trip Point | $\left(\mathrm{V}_{\text {CC }}-\mathrm{V}_{\text {SENSE }}\right)=55 \mathrm{mV} \pm 20 \%$ | $2.75 \mathrm{~A} \pm 20 \%$ |
| Open Circuit Detection Threshold | $\left(V_{\text {CC }}-V_{\text {SENSE }}\right)<3 \mathrm{mV}$ | $<150 \mathrm{~mA}$ |

## DEMO MANUAL DC684A

## QUICK START PROCEDURE

Demonstration circuit 684A is easy to set up to evaluate the performance of the LT4256-3. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:
Demonstration circuit 684A has two user configurable jumper options:

- J1 Retry: Set to ON for auto retry or OFF for latchoff on overcurrent faults.
- J2 LED Function: Select PWRGD or VOUT PRESENT. In the former position, LED D6 will only illuminate when the output voltage crosses the 44.9 V threshold. In the latter position, D6 will illuminate whenever Q1 is enhanced.

With power off, connect a nominal 48 V power supply capable of supplying 3A to the VIN and GND turrets.
Connect a logic level supply to the turrets labeled VLOGIC and GND to monitor the PWRGD state on the turret labeled PWRGD. This same supply can also be connected
to the turret Vmicro to monitor the OPEN pin on the turret labeled OPEN
NOTE: The OPEN and PWRGD pins are provided with separate supplies to facilitate connection of the PWRGD to a DC/DC power converter which may require a different voltage than the system processor which would monitor the OPEN state.

Connect a suitable load to the VOUT and GND turrets. This load can be an electronic load or power resistors (24W at 100 W for 2 A at 48 V ) can be used.
NOTE: Because the LT4256 incorporates foldback current limiting, the nominal startup current supplied to the load is 700 mA and can be as low as 500 mA . This current limit increases linearly until the FB pin exceeds 2 V (VOUT > 20V). An electronic constant current load set to 2A will not permit the circuit to turn on unless it is gated on by the PWRGD signal (as would be the case with a DC/DC converter controlled by the PWRGD signal). Resistive loading will not have this problem.


Figure 1. Proper Measurement Equipment Setup

## DEMO MANUAL DC684A

## คUICK START PROCEDURE

Turn on the power supplies, verify the input voltage is 48 V . Verify the output voltage and the load current, the OPEN turret should present a logic LOW if the load current is $>150 \mathrm{~mA}$ and the PWRGD turret should present a logic HIGH. LED D5 and D6 should be illuminated.

With the circuit functioning, additional evaluations can now be performed. Test the undervoltage lockout and PWRGD functionality by reducing the input voltage below 35V. Observe the trip points of the PWRGD and undervoltage lockout. Increase the input voltage back to 48 V and again observe the trip point of the PWRGD.
The overvoltage function can also be tested, but be aware that if resistive loads are used, the value must be increased to $36 \Omega$ to prevent an overcurrent fault. This test can also be performed without a load.

Overcurrent faults can be evaluated by increasing the output load current and observing the overcurrent trip point.
Circuit Testing Notes: As in all high current testing, it is a good idea to use twisted pair power leads to minimize circuit inductance. Under step loads, significant voltage spikes can occur as a result of this inductance causing false overvoltage or undervoltage trips. If there is significant lead length between the power supply and the DC684A, add additional bulk capacitance across the VIN and GND turrets. This capacitance may also be needed if stepping the load results in significant voltage steps on the input, particularly if performing tests of the circuit breaker function.

## DEMO MANUAL DC684A

## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| Required Circuit Components |  |  |  |  |
| 1 | 1 | CL | CAP, ELECTROLYTIC 10ヶF 100V 20\% | SANY0 100CV10FS |
| 2 | 1 | C1 | CAP, X7R 0.01~F 100V 10\% 1206 | AVX 12061C103KATMA |
| 3 | 1 | C2 | CAP, X7R 0.033 F F 50V 5\% 0805 | AVX 08055C333JAT |
| 4 | 1 | C3 | CAP, X7R 0.1 $\mu \mathrm{F} 50 \mathrm{~V} 10 \% 0603$ | TDK C1608X7R1H104K |
| 5 | 1 | C4 | CAP, X5R 1^F 25V 20\% 1206 | TAIYO YUDEN TMK316BJ105ML |
| 6 | 1 | D1 | DIODE, DUAL, ZENER 300mW | DIODES INC. AZ23C11 |
| 7 | 1 | D2 | DIODE, TRANSIENT VOLTAGE SUPPRESSOR | DIODES INC. SMAT70A |
| 8 | 1 | D3 | DIODE, 1N4148W SOD123 | DIODES INC. 1N4148W |
| 9 | 1 | D4 | DIODE, S1G 1A SMA | DIODES INC. S1G |
| 10 | 2 | D5, D6 | LED, GREEN | PANASONIC LN1351C-(TR) |
| 11 | 2 | JP2, JP1 | HEADER, 3PIN, 2mm | COMM CON 2802S-03G2 |
| 12 | 2 | JP2, JP1 | SHUNT | COMM CON CCIJ2MM-138G |
| 13 | 4 | J1, J3, J4, J5 | JACK, BANANA | KEYSTONE 575-4 |
| 14 | 1 | Q1 | XSTR, HEXFET POWER MOSFET | INT. RECT. IRF540NS |
| 15 | 1 | R1 | RES, 64.9k 1\% 1/4W 1206 | AAC CRL18-6492FM |
| 16 | 3 | R2, R3, R9 | RES, 4.02k 1\% 1/10W 0603 | AAC CR16-4021FM |
| 17 | 2 | R11, R4 | RES, 10k 5\% 1/2W 2010 | AAC CR12-103JM |
| 18 | 1 | R5 | RES, $0.02 \Omega 5 \% 1 \mathrm{~W} 2512$ | IRC LRF2512-01-R020-J |
| 19 | 1 | R6 | RES, $10 \Omega 1 \% 1 / 10 \mathrm{~W} 0603$ | AAC CR16-10R0FM |
| 20 | 1 | R7 | RES, $100 \Omega 5 \% 1 / 10 \mathrm{~W} 0603$ | AAC CR16-101JM |
| 21 | 1 | R8 | RES, 36.5k 1\% 1/4W 1206 | AAC CRL18-3652FM |
| 22 | 2 | R10, R12 | RES, 10k 5\% 1/10W 0603 | AAC CR16-103JM |
| 23 | 9 | TP2, TP6, TP7-TP13 | TURRET | MILL-MAX 2501-2 |
| 24 | 1 | U1 | IC, LT4256-3CGN HOT SWAP CONTROLLER | LINEAR TECH. LT4256-3CGN |
| 25 | 0 | U1-ALTERNATE | IC, LT4254CGN HOT SWAP CONTROLLER | LINEAR TECH. LT4254CGN |

## DEMO MANUAL DC684A

## SCHEMATIC DIAGRAM



## DEMO MANUAL DC684A

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Mailing Address:

Linear Technology<br>1630 McCarthy Blvd.<br>Milpitas, CA 95035

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