LTC2704
Quad 16-Bit V_{OUT} Softspan DAC

DESCRIPTION

Demonstration circuit DC752A-B features the LTC2704-16 Quad 16-bit SoftSpan™ V_{OUT} DAC. This device features six output ranges, 0V to 5V, 0V to 10V, ±5V, ±10V, ±2.5V and –2.5V to 7.5V that are independently settable for each channel. Each DAC has an offset adjust input pin and a com-

pensation pin to allow optimization of transient response.

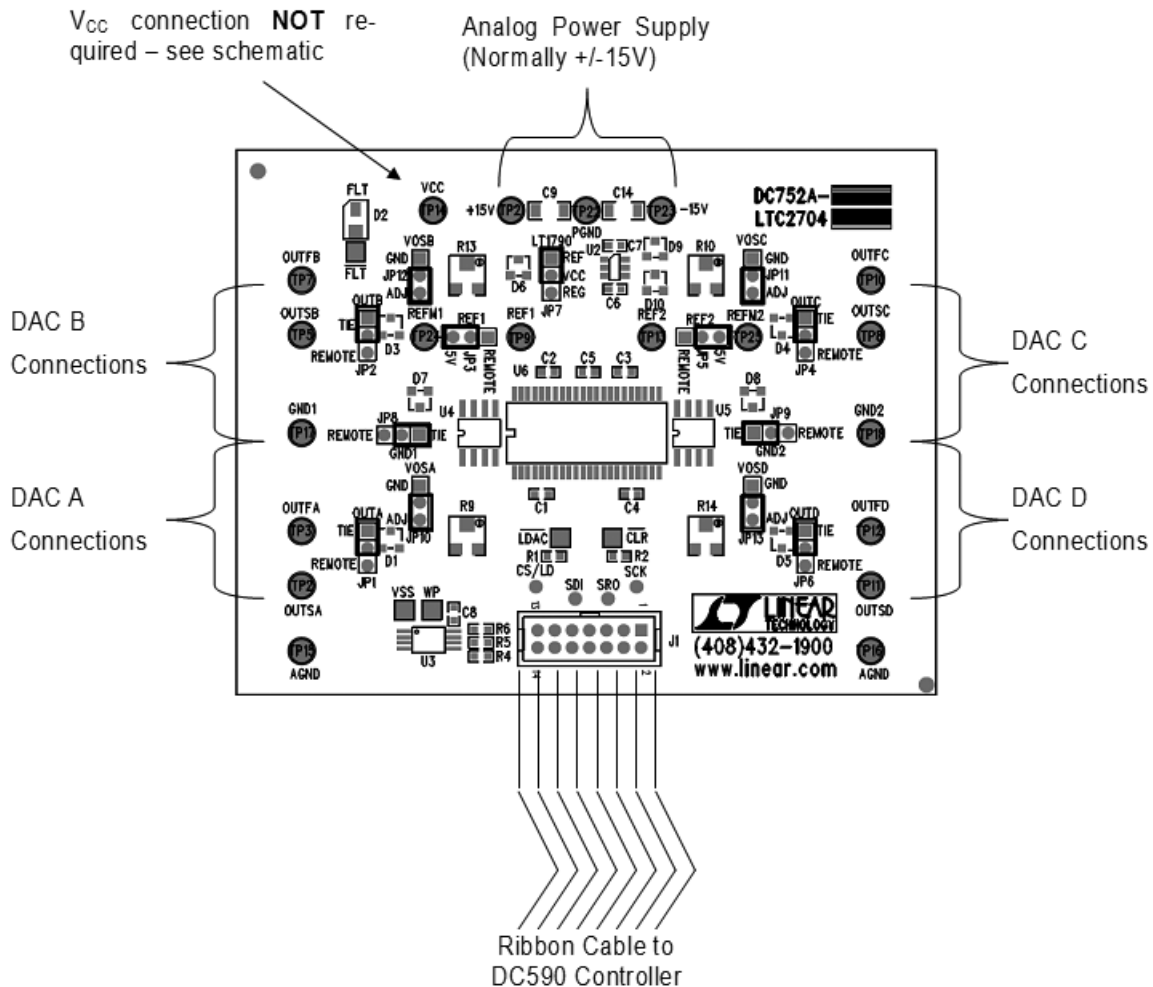**Design files for this circuit board are available at http://www.linear.com/demo**

Figure 1. Connection Diagram

QUICK START PROCEDURE

Connect a clean ±15V power supply to the turret posts at the top of the DC752A board. Connect J1 to a DC590 USB serial controller using the supplied 14-conductor ribbon cable. Connect DC590 to a host PC with a standard USB A/B cable. Run the QuikEval™ evaluation software supplied with DC590 or download it from www.linear.com/software. The correct control panel will be loaded automatically. The software automatically sets the LTC2704 outputs according to the entries in the control panel. A square wave option is available to test settling time.

Additional software documentation may be available from the Help menu item, as features may be added periodically.
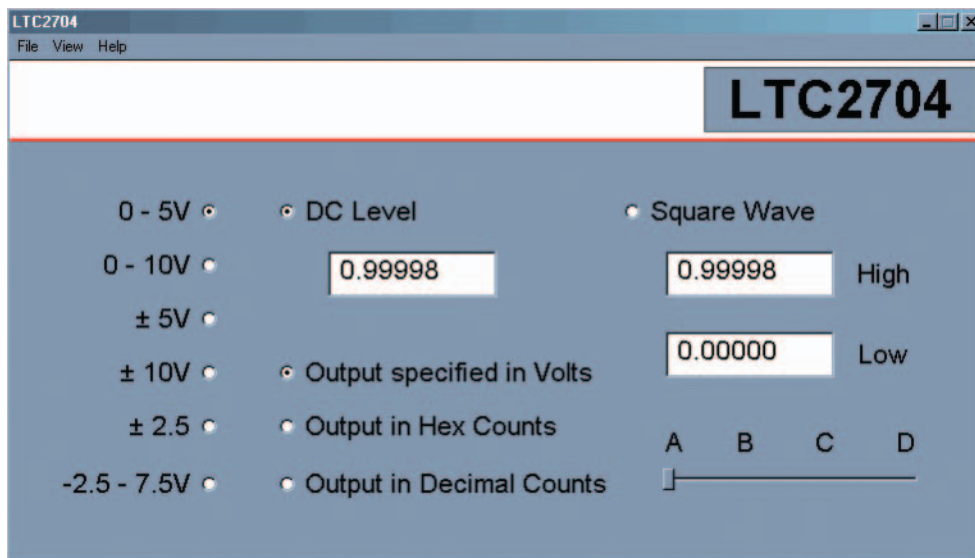

Figure 2. Software Screenshot

HARDWARE SETUP

JUMPERS

JP8, JP9: Tie points for GND1 and GND2, respectively. The default selection is TIE for both jumpers. This connects all DAC grounds to the analog ground plane, and is suitable for most applications that do not have large return currents into the GND1 and GND2 turrets. Alternatively, selecting REMOTE allows GND1 and GND2 to differ by as much as ±300mV from analog ground.

JP1, JP2, JP4, JP6: Sense connections for DACA, DACB, DACC, and DACD, respectively. Selecting TIE connects OUTFx (output force) output directly to OUTSx (output sense). Selecting REMOTE allows for remote sensing of the output voltage. This also allows a power gain stage such as the LT1970 to be added with no degradation of accuracy.

JP3 (REF1): Voltage reference selection for DACA and DACB, either 5V for the onboard LT1236 reference or REMOTE if an external reference source is connected to the REF1 turret post.

JP5 (REF2): Voltage reference selection for DACC and DACD, either 5V for the onboard LT1236 reference or REMOTE if an external reference source is connected to the REF2 turret post.

JP10 (VOSA), JP12 (VOSB), JP11 (VOSC), JP13 (VOSD): offset adjustment selection for DACA, DACB, DACC, and DACD, respectively. If no offset adjustment is required, select GND. Selecting ADJ connects the offset pin to the associated 10-turn pot, allowing adjustment of the DAC's offset.

JP7: Select source for 5V V_{CC} supply. Normally this should be left in the REF position for lowest noise operation. The REG position selects the 5V regulated supply from the 14-pin QuikEval connector. To apply an external supply, remove JP7 completely.

ANALOG CONNECTIONS (TURRET POSTS)

OUTFA, OUTFB, OUTFC, OUTFD: DAC voltage outputs.

OUTSA, OUTSB, OUTSC, OUTSD: DAC feedback inputs. The LTC2704 RFB inputs have a nominal 10k resistance, so resistance between this point an the load or buffer output must be kept low.

REF1, REF2: DAC Reference voltage. If the onboard LT1236 references are selected, the voltage may be measured at these points. If a remote reference is selected, then an external reference must be applied to these points.

REFM1, REFM2: Inverted reference output from the LTC2704. Do not drive these points with an external source.

POWER AND GROUND CONNECTIONS

Analog Power: The +15V, –15V, and GND turret posts are the analog supplies for the internal DAC amplifiers. These should be connected to a well regulated, low noise power supply.

**V_{CC}:** Connection to V_{CC}. See schematic and description for JP7.

Grounding: Separate power and signal grounds are provided. Signal ground is connected to the exposed ground planes at the top and bottom edges of the board, and to the two turrets labeled AGND. Use signal ground as the reference point for measurements and connections to external circuits. Any large currents drawn from the DAC outputs should be returned to the power ground turret closest to pin 1 on the 14-pin header. In this situation, GND1 and GND2 can be used to sense the ground voltage at the load, compensating for return resistance between the load and power ground return. The maximum difference in voltage between the load and power ground should be less than 300mV.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	4	C1, C2, C3, C4	Cap., NPO 27pF 25V 5%	AVX 06033A270JAT1A
2	5	C5, C6, C8, C10, C13	Cap., X7R 0.1µF 16V 20%	AVX 0603YC104MAT2A
3	3	C7, C11, C12	Cap., X5R 4.7µF 6.3V 20%	TDK C1608X5R0J475MT
4	2	C9, C14	Cap., X5R 4.7µF 25V 20%	Taiyo Yuden TMK316BJ475ML
5	4	C15, C16, C17, C18	Cap., X7R 0.1µF 25V 10%	Taiyo Yuden TMK107BJ104KA
6	4	D1, D3, D4, D5	Diode, Dual Switching Diode	ON Semi. BAV99LT1
7	1	D2	LED, GRN	Panasonic LN1351-C-TR
8	6	D6, D7, D8, D9, D10, D11	Schottky (Dual) Diode, BAT54S	Zetex BAT54S
9	13	JP1-JP13	Headers, 3 Pins 2mm Ctrs.	CommConn Con Inc. 2802S-03G2
10	13	XJP1-XJP13	Shunt, 2 Pins 2mm Ctrs.	CommConn Con Inc. CCIJ2MM-138GW
11	1	J1	Headers, 14 Pin 2mm Ctrs.	Molex 87331-1420
12	2	R2, R1	Res., Chip 10k 0.1W 5%	AAC CR16-103JM
13	1	R3	Res., Chip 1k 0.06W 5%	AAC CR16-102JM
14	3	R4, R5, R6	Res., Chip 4.99k 0.1W 1%	AAC CR16-4991FM
15	4	R9, R10, R13, R14	Pot. 11 Turns 20k	Bourns 3224W-1-203E
16	0	TP1, TP4, TP6, TP19, TP20 (Opt)	Testpoint	
17	20	TP2, TP3, TP5, TP7-TP18, TP21-TP25	Turret, Testpoint	Mill Max 2308-2
18	1	U2	I.C., µPWR LDO	Linear Technology Corp. LT1790ACS6-5
19	1	U3	EEPROM, Serial	MICROCHIP, 24LC025-I /ST
20	2	U4, U5	I.C., Precision Ref.	Linear Technology Corp. LT1236ACS8-5
21	1	U6	I.C., SoftSpan DAC	Linear Technology Corp. LTC2704CGW-16

SCHEMATIC DIAGRAM
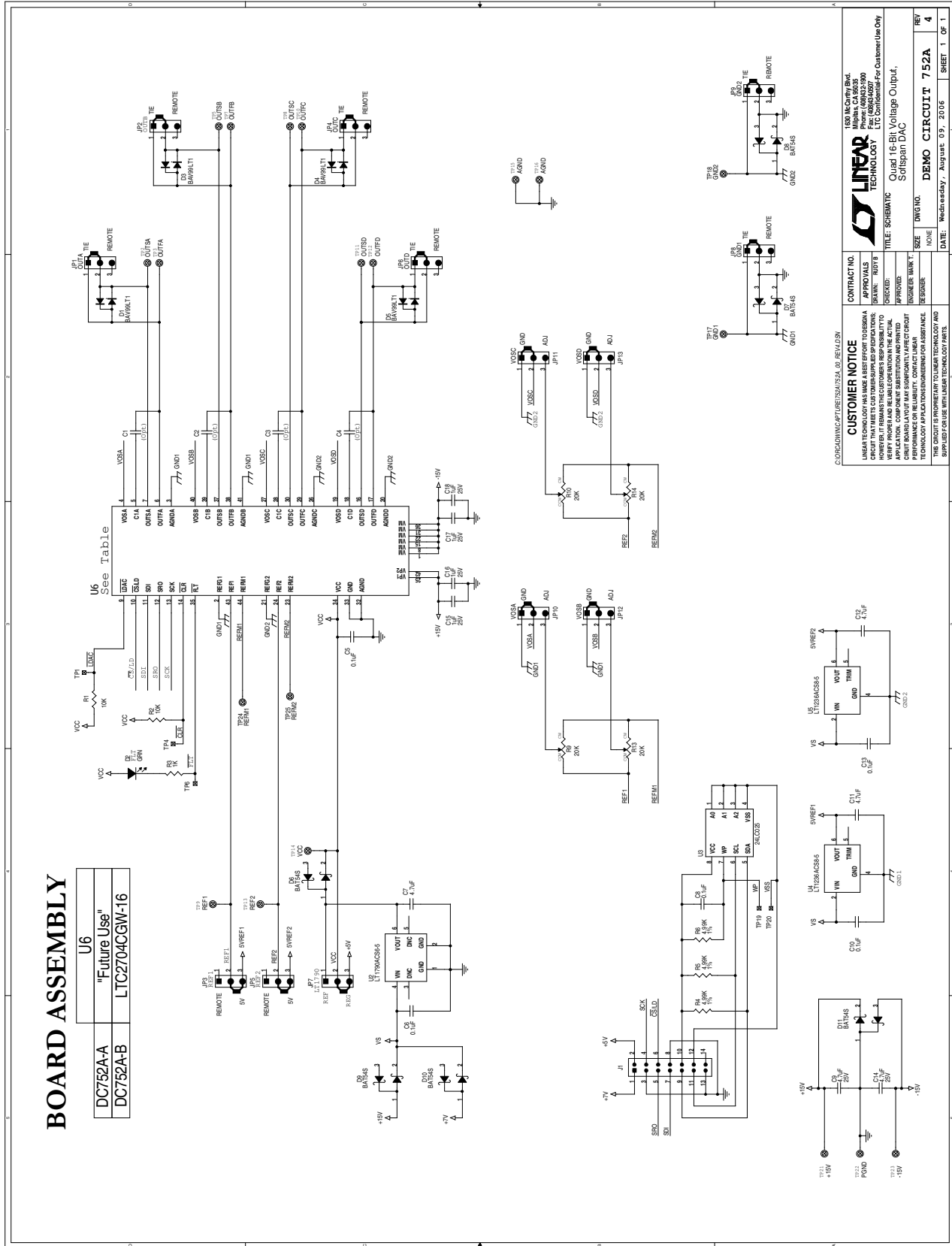
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