## DESCRIPTION

The LTC ${ }^{\otimes} 2446$ is a $4-/ 8$-channel, high speed, 24 -bit $\Delta \Sigma$ ADC with ten selectable speed/resolution modes from $6.9 \mathrm{~Hz} / 280 \mathrm{n} \mathrm{V}_{\text {RMS }}$ to $3.5 \mathrm{kHz} / 25 \mu \mathrm{~V}_{\text {RMS }}$. Key DC specifications include 5ppm INL, $5 \mu \mathrm{~V}$ offset, 10ppm full-scale error and $20 \mathrm{nV} /{ }^{\circ} \mathrm{C}$ offset drift. In the $6.9 \mathrm{~Hz} / 200 \mathrm{n} V_{\text {RMS }}$ mode, input normal mode rejection of 50 Hz and 60 Hz noise is better than 87 dB . The accuracy (offset, full-scale, linearity, drift) and power dissipation are independent of the speed selected. The LTC2446 also has four reference inputs dedicated to the four differential input channels and corresponding pairs of single-ended input channels. This allows the inputs to have different reference sources, facilitating independent ratiometric measurements on each channel.

The DC847A is a member of Linear Technology's QuikEval ${ }^{\text {TM }}$ family of demonstration boards. It is designed to allow easy evaluation of the LTC2446 and may be connected directly to the target application's analog signals while using the DC590 USB serial controller board and supplied software to measure performance. The exposed ground planes allow proper grounding to prototype circuitry. After evaluating with LTC's software, the digital signals can be connected to the application's processor/controller for development of the serial interface.

## Design files for this circuit board are available at http://www.linear.com/demo

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## BOARD LAYOUT



Figure 1. DC847A Connection Diagram

## DEMO MANUAL DC847A

## QUICK START PROCEDURE

- Connect the DC847A to a DC590 USB serial controller using the supplied 14-conductor ribbon cable.
- Connect the DC590 to a host PC with a standard USB A/B cable.
- Run the evaluation software supplied with the DC590 or download it from www.linear.com/software. The correct program will be loaded automatically.
- Click the slider at the bottom of the strip chart display to change the oversample ratio (OSR) which will, in turn, change the data output rate.

Tools are available for logging data, changing reference voltage, changing the number of points in the strip chart and histogram, and changing the number of points averaged for the DVM display.

- Click the Collect button to start reading the input voltage.


Figure 2. QuikEval Software Screenshot

## DEMO MANUAL DC847A

## HARDUARE SGTUP

## JUMPERS

JP1, JP3: Select the source for REF ${ }^{+}$and REF $^{-}$, respectively. REF ${ }^{+}$can be 5 V from the onboard LT1236 reference (default) or supplied externally. REF ${ }^{-}$can be ground (OV, default) or supplied externally.

JP2: Select the source for the analog COM input, either tied to ground or supplied externally to the COM turret post.
JP4: Trigger Mode; either normal (default) or externally triggered.

JP7: Trigger Input Signal. Pin 1 is a 5V Iogic signal, Pin 2 is ground. When trigger mode is selected on JP4, a rising edge starts a new conversion. Note that since a conversion cannot be terminated once started, this signal can only be used to slow down the conversion rate.

## CONNECTION TO THE DC590 SERIAL CONTROLLER

J2: Power and Digital Interface Connector. Connect to the DC590 serial controller with the supplied 14-conductor ribbon cable.

## ANALOG CONNECTIONS

Analog signal connections are made via the row of turret posts along the edge of the board. Also, if you are connecting the board to an existing circuit, the exposed ground planes along the edges of the board may be used to form a solid connection between grounds.

GND: Ground turrets are connected directly to the internal analog ground plane.
PWR GND: Power Ground; connected to the power return trace.
$V_{C C}$ : Supply for the ADC. Do not draw any power from this point. External power may be applied to this point after disabling the switching supply on the DC590. If the DC590 serial controller is being used, the voltage must be regulated 5 V only, as the isolation circuitry will also be powered from this supply. See the DC590 Quick Start Guide for details.

REF ${ }^{+}$, REF ${ }^{-}$: Turrets Connected to the LTC2446 Global Reference Pins (REF ${ }^{+}$and REF $^{-}$). If the onboard reference is being used, the reference voltage may be monitored from this point. An external reference may be connected to these terminals if JP1 and JP3 are configured for external reference.

REF01 ${ }^{+}$, REF01 $^{-}$, REF23 $^{+}$, REF23${ }^{-}$, etc.: Dedicated Reference Inputs for Each Input Channel.

Note: The REF ${ }^{+}$, REF ${ }^{-}$, REF01 ${ }^{+}$, REF01 ${ }^{-}$, REF23 ${ }^{+}$, REF23 $^{-}$, etc. terminals are decoupled to ground with $0.1 \mu F$ and $10 \mu F$ capacitors. Thus, any source connected to these terminals must be able to drive a capacitive load and have very low impedance at DC. Examples are series references that require an output capacitor and C-Ioad stable op amps, such as the LT1219 and LT1368.

CHO-CH7: These are the differential inputs to the LTC2446. They may be configured either as single-ended inputs with respect to the COM pin, oradjacent pairs may be configured as differential inputs ( $\mathrm{CH} 0-1, \mathrm{CH} 2-3$, etc.).

Note: Channels $0-3$ have $1 \mu \mathrm{~F}$ capacitors from the inputs to ground. Channels 4-7 do not have capacitors installed, however, there are pads for these capacitors on the back of the board. The reason for this is that some applications benefit from a large capacitance at the inputs while others require no capacitance.

## experiments

Input Noise

Solder a short wire from the CH 0 to CH 1 . Set the demo software to OSR32768 (6.8 samples per second) and check the 2 X box. Noise should be approximately 0.056 ppm of $V_{\text {REF }}(280 n V)$. Next, select different oversample ratios. Measured noise for each oversample ratio should be close to values given in the LTC2446 data sheet.

## Common Mode Rejection

Tie the two inputs (still connected together from previous experiment) to ground through a short wire and note the indicated voltage. Tie the inputs to REF ${ }^{+}$; the difference should be less than $5 \mu \mathrm{~V}$ due to the 120 dB CMRR of the LTC2446.

## DEMO MANUAL DC847A

## EXP $\in$ RImenTS

## Input Normal Mode Rejection

The LTC2446's SINC ${ }^{4}$ digital filter is trimmed to strongly reject both 50 Hz and 60 Hz line noise when operated with the internal conversion clock and oversample ratio 32768 (6.8 samples per second). To measure input normal mode rejection, connect COM to a 2.5 V source such as an LT1790-2.5 reference or a power supply. Connect any other input ( $\mathrm{CHO}-\mathrm{CH} 15$ ) to the same supply through a 10k $\Omega$ resistor. Apply a 10Hz, 2 V peak-to-peak sine wave to the input through a $1 \mu \mathrm{~F}$ capacitor.
Select OSR32768 ( 6.8 samples per second) and 2X mode in the demo software and start taking data. The input noise
will be quite large, and the graph of output vs time should show large variations.

Next, slowly increase the frequency to 55 Hz . The noise should be almost undetectable in the graph. Note that the indicated noise in ppm may still be above that of the data sheet specification because the inputs are not connected to a DC source.

Change the OSR to 16384 ( 13.75 samples per second). The noise will increase substantially, as the first notch at this OSR is at 110 Hz . Increase the signal generator frequency to 110 Hz ; the noise will drop again.

## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| Required Circuit Components |  |  |  |  |
| 1 | 4 | C3, C7, C10, C13 | CAP., CHIP, X7R, $0.01 \mu \mathrm{~F}, 16 \mathrm{~V}$ | AVX, 0603YC103KAT1A, 0603 |
| 2 | 3 | C11, C14, C15 | CAP., CHIP, X7R, $0.1 \mu \mathrm{~F}, 16 \mathrm{~V}$ | AVX, 0603YC104MAT1A, 0603 |
| 3 | 13 | $\begin{aligned} & \mathrm{C} 1, \mathrm{C} 4, \mathrm{C} 6, \mathrm{C} 16-\mathrm{C} 20, \mathrm{C} 23, \\ & \text { C24, C27-C29 } \end{aligned}$ | CAP., CHIP, X5R, $1 \mu \mathrm{~F}, 10 \mathrm{~V}$ | TAIYO YUDEN, LMK107BJ105MG, 0603 |
| 4 | 3 | C2, C9, C12 | CAP., CHIP, X5R, 4.7 $\mu$ F, 6.3V | TAIYO YUDEN, JMK212BJ475MG, 0805 |
| 5 | 1 | C8 | CAP., CHIP, X5R, 10 F , 6.3 V | TDK, C2012X5R0J106M, 0805 |
| 6 | 0 | C21, C22, C25, C26 | OPT. |  |
| 7 | 24 | TP1-TP6, TP8, TP10-TP12, TP14-TP27 | TURRET, TESTPOINT, 0.064" | MILL-MAX, 2308-2 |
| 8 | 0 | TP13, TP28, TP29 | OPT. (SURFACE MOUNT PAD ONLY) |  |
| 9 | 4 | JP1-JP4 | HEADER, 3-PIN, 1 ROW, 0.079" | COMM-CON, 2802S-03G2 |
| 10 | 4 | FOR (JP1-JP4) | SHUNT, 0.079", CENTER | COMM-CON, CCIJ2MM-138GW |
| 11 | 0 | JP7 | OPT. |  |
| 12 | 0 | J1 (0PT.) | CONN., SMA COAXIAL, STRAIGHT JACK | CONNEX, 132134 |
| 13 | 1 | J2 | HEADER, VERTICAL DUAL, $2 \times 7,0.079{ }^{\prime \prime}$ | MOLEX, 87831-1420 |
| 14 | 1 | R7 | RES., CHIP, 100, 5\% | AAC, CR16-101JM, 0603 |
| 15 | 3 | R8, R9, R10 | RES., CHIP, 4.99k, 1\% | VISHAY, CRCW0603 |
| 16 | 2 | R5, R11 | RES., CHIP, 10k, 5\% | AAC, CR16-103JM, 0603 |
| 17 | 0 | R6 | OPT. |  |
| 18 | 1 | U1 | I.C., 24-BIT 4-/8-CHANNEL DELTA SIGMA ADCs | LINEAR TECHNOLOGY, LTC2446UHF, 38QFN |
| 19 | 1 | U4 | I.C., PRECISION REFERENCE | LINEAR TECHNOLOGY, LT1236ACS8-5, S08 |
| 20 | 1 | U3 | I.C., SERIAL EEPROM | MICROCHIP, 24LCO25-I/ST, TSSOP-8 |
| 21 | 1 | U2 | I.C., NONINVERTING MULTIPLEXER | FAIRCHILD, NC7SZ157P6X, SC70 |
| 22 | 1 | U5 | I.C., SINGLE D FLIP-FLOP | ON SEMI., NL17SZ74US, US8 |

## DEMO MANUAL DC847A

## SCHEMATIC DIAGRAM



Figure 3. DC847A 24-Bit High Speed 4-/8-Channel Delta Sigma ADC

## DEMO MANUAL DC847A

## DEMONSTRATION BOARD IMPORTANT NOTICE

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

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