DEMO MANUAL DC996

# LTC2208/LTC2208-14/LTC2217/ LTC2216/LTC2215 16-Bit/14-Bit 80Msps tol30Msps ADCs 

## DESCRIPTIOn

Demonstration circuit 996 supports a family of 16-14-bit 80Msps to 130Msps ADCs. Each assembly features one of the following devices: LTC ${ }^{2208, ~ L T C 2208-14, ~ L T C 2217, ~}$ LTC2216, LTC2215 high speed, high dynamic range ADCs.
This demonstration circuit only supports LVDS operation. For demonstration of CMOS output signaling, please see DC854.

Other members of this family include the LTC2207, a 105Msps 16-bit CMOS-only version of this device, as well as lower speed versions and single-ended clock versions. These $7 \mathrm{~mm} \times 7 \mathrm{~mm}$ QFN devices are supported by Demonstration Circuits 918 and 919 (for single-ended clock input).

Several versions of the 996 demo board supporting the LTC2208 16-bit, LTC2217 16-bit and LTC2208-14 14-bit series of A/D converters are listed in Table 1. Depending on the required resolution, sample rate and input frequency, the DC996 is supplied with the appropriate ADC and with an optimized inputcircuit. The circuitry on the analog inputs is optimized for analog input frequencies below 70 MHz or from 70 MHz to 140 MHz . For higher input frequencies, contact the factory for support.
Design files for this circuit board are available at http://www.linear.com/demo
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Table 1. DC996 Variants

| DC996 VARIANTS | ADC PART NUMBER | RESOLUTION | MAXIMUM SAMPLE RATE | INPUT FREQUENCY |
| :---: | :---: | :---: | :---: | :---: |
| $996 \mathrm{~B}-\mathrm{A}$ | LTC2208 | $16-\mathrm{Bit}$ | 130 Msps | 1 MHz to 70 MHz |
| $996 \mathrm{~B}-\mathrm{B}$ | LTC2208 | $16-\mathrm{Bit}$ | 130 Msps | 70 MHz to 140 MHz |
| $996 \mathrm{~B}-\mathrm{C}$ | LTC2208-14 | 14 -Bit | 130 Msps | 1 MHz to 70 MHz |
| $996 \mathrm{~B}-\mathrm{D}$ | LTC2208-14 | $14-\mathrm{Bit}$ | 130 Msps | 70 MHz to 140 MHz |
| $996 \mathrm{~B}-\mathrm{E}$ | LTC2217 | $16-\mathrm{Bit}$ | 105 Msps | 1 MHz to 70 MHz |
| $996 \mathrm{~B}-\mathrm{F}$ | LTC2217 | $16-\mathrm{Bit}$ | 105 Msps | 70 MHz to 140 MHz |
| $996 \mathrm{~B}-\mathrm{G}$ | LTC2216 | $16-\mathrm{Bit}$ | 80 Msps | 1 MHz to 70 MHz |
| $996 \mathrm{~B}-\mathrm{H}$ | LTC2216 | $16-\mathrm{Bit}$ | 80 Msps | 70 MHz to 140 MHz |
| $996 \mathrm{~B}-\mathrm{I}$ | LTC2215 | $16-\mathrm{Bit}$ | 65 Msps | 1 MHz to 70 MHz |
| $996 \mathrm{~B}-\mathrm{J}$ | LTC2215 | $16-\mathrm{Bit}$ | 65 Msps | 70 MHz to 140 MHz |
| $996 \mathrm{~A}-\mathrm{P}$ | LTC2208 | $16-\mathrm{Bit}$ | 130 Msps | $>140 \mathrm{MHz}$ |
| $996 \mathrm{~A}-Q$ | LTC2208-14 | $14-\mathrm{Bit}$ | 130 Msps | $>140 \mathrm{MHz}$ |

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PERFORMARCE SUMMARY ( $\left.\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$

| PARAMETER | CONDITION | VALUE |
| :--- | :--- | :--- |
| Supply Voltage | Depending On Sampling Rate and the A/D Converter Provided, <br> This Supply Must Provide Up To 700mA. | Optimized for 3.3V <br> $[3.15 \mathrm{~V} \Leftrightarrow 3.45 \mathrm{~V}$ Min/Max] |
| Analog Input Range | Depending on PGA Pin Voltage | 1.5 V P-p to $2.25 \mathrm{~V}_{\text {P-p }}$ |
| Logic Input Voltages | Minimum Logic High <br> Maximum Logic Low | 2 V <br> 0.8 V |
| Logic Output Voltages (Differential) | Nominal Logic Levels (100 Load) <br> Minimum Logic levels (100 Load) | $350 \mathrm{mV} / 2.1 \mathrm{~V}$ Common Mode <br> $247 \mathrm{mV} / 2.1 \mathrm{~V}$ Common Mode |
| Sampling Frequency (Convert Clock Frequency) | See Table 1 |  |
| Convert Clock Level | $50 \Omega$ Source Impedance, AC-Coupled or Ground Referenced <br> (Convert Clock Input Is Capacitor Coupled On Board and <br> Terminated with 50 .) | $2 \mathrm{~V}_{\text {P-p } \Leftrightarrow 2.5 \mathrm{~V} \text { P-p Sine Wave or }}^{\text {Square wave }}$ |
| Resolution | See Table 1 |  |
| Input frequency range | See Table 1 |  |
| SFDR | See Applicable Data Sheet |  |
| SNR | See Applicable Data Sheet |  |

## PUICK START PROCEDURE

Demonstration circuit 996 is easy to set up to evaluate the performance of the LTC2208/LTC2208-14/LTC2217 A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow this procedure:

## Setup

If a DC890 QuikEval ${ }^{\text {TM }}$ II Data Acquisition and Collection System was supplied with the DC996 demonstration circuit, follow the DC890 Quick Start Guide to install the required software and for connecting the DC890 to the DC996 and to a PC.

## DC996 Demonstration Circuit Board Jumpers

The DC996 demonstration circuit board should have the following jumper settings as default: (as per Figure 1).
Figure 1 shows DC996A, the DC996B is shown in Figure 7.
J2: Mode ( $\mathrm{V}_{\mathrm{CC}}$ ) 2's Complement CDS Off
J3: SHDN: (Run) Dither (Off)
J4: Rand (Off) PGA 1x
J9: Unused power connector

## Applying Power and Signals to the DC996 Demonstration Circuit

Apply 3.3V across the pins marked " +3.3 V " and "PWR GND" on the DC996. The DC996 demonstration circuit requires up to 700 mA depending on the sampling rate and the A/D converter supplied. If a DC890 is used to acquire data from the DC996, the DC890 must be provided with an external $6 \mathrm{~V} \pm 0.5 \mathrm{~V} 1 \mathrm{~A}$ supply on turrets $\mathrm{G7}(+)$ and G1(-) or the adjacent 2.1 mm power jack to support the power requirements of the Xilinx Spartan 3 FPGA active terminations used to terminate the LVDS repeaters on the DC996. The DC890 will not activate the LVDS mode unless the DC890 detects external power present.
If external power is not present the DC890 will not configure the FPGA for LVDS terminations as this would result in exceeding the USB 500mA limit. The DC890 contains an onboard electronic circuit breaker which will shut off the DC890 if external power is removed while the FPGA is configured for LVDS active terminations.

## PUICK START PROCEDURE



Figure 1. DC996A Setup (Zoom for Detail). See Figure 7 for DC996B

## Encode Clock

Note: This is not a logic-compatible input. It is terminated with $50 \Omega$. Apply an encode clock to the SMA connector on the DC996 demonstration circuit board marked "J7 ENCODE INPUT". This is a transformer-coupled input, terminated on the secondary side in two steps, $100 \Omega$ at the transformer with final termination at the $\operatorname{ADC}$ at $100 \Omega$.
For the best noise performance, the ENCODE INPUT must be driven with a very low jitter source. When using a sinusoidal generator, the amplitude should often be as large as possible, up to $3 V_{\text {p-p }}$ or 13 dBm . Using bandpass filters on the clock and the analog input will improve the
noise performance by reducing the wideband noise power of the signals. Data sheet FFT plots are taken with 10 -pole LC filters made by TE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broad band noise. Low phase noise Agilent 8644B generators are used with TE bandpass filters for both the clock input and the analog input.
Apply the analog input signal of interest to the SMA connectors on the DC996 demonstration circuit board marked "J5 ANALOG INPUT". These inputs are capacitive coupled to Balun transformers ETC1-1-13, or directly coupled through flux-coupled transformers ETC1-1T.

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## DUICK START PROCEDURE

An internally generated conversion clock output is available on J 1 which could be collected via a logic analyzer, or other data collection system if populated with a SAMTEC MEC8-150 type connector or collected by the DC890 Data Acquisition Board using the PScope ${ }^{\text {TM }}$ System Software provided or downloaded from the Linear Technology website at http://www.linear.com/designtools/software/. If a DC890 was provided, follow the DC890 Quick Start Guide and the instructions below.

To start the data collection software if "PScope.exe", is installed (by default) in\Program Files\LTC\PScope<br>, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

Ifthe DC996 demonstration circuit is properly connected to the DC890, PScope should automatically detect the DC996, and configure itself accordingly. If necessary the procedure below explains how to manually configure PScope.
Under the Configure menu, go to ADC Configuration. Check the Config Manually box and use the following configuration options:

- 16-Bit (or 14-Bit if using LTC2208-14)
- Alignment: Left-16
- Bipolar (2's complement)
- Positive clock edge
- Type: LVDS

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC890 Quick Start Guide and in the online help available within the PScope program itself.

## Analog Input Network

For optimal distortion and noise performance the RC network on the analog inputs should be optimized for the analog input frequencies of interest. At this point in time, the circuit in Figure 3 for input frequencies below 70 MHz . For input frequencies from 70 MHz to 140 MHz , the circuit in Figure 2 is used. These two input networks cover a broad bandwidth and are not optimized for operation at a specific input frequency.

For higher frequencies, a single balun (ETC1-1-13) is populated on a DC996A board.
In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present $50 \Omega$ outside the passband.

The DC996A board has provision for a bandpass filter prior to the balun. This may be populated if the board is customized for a given frequency band. (Figure 5)

In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full-scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where operational amplifiers may be unable to deliver the combination of low noise figure and high IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower $Q$ filter used between the amplifier and the demo circuit.

For advice on drive circuits or for input frequencies greater than 220MHz, or for higher order bandpass filtering prior to the ADC, contact the factory for support.

## PUICK START PROCEDURE



Figure 2. Analog Front-End Circuit For 70MHz+


Figure 3. Analog Front-End Circuit For 1MHz $<\mathrm{A}_{\text {IN }}<70 \mathrm{MHz}$
For input frequencies less than 5 MHz , or greater than 150 MHz , other input networks may be more appropriate. Please consult the factory for suggestions on drivers and networks if your signal sources extend outside these ranges, or if you experience difficulties driving these suggested networks.

As this board has a black solder mask, in order to improve the thermal performance, Figure 4 is a picture of the top side in colors that are easier to digest. The dielectric under the input network (bluish pads) is 20 mils, otherwise, dielectric thickness is 6 mils.

This board is used only for 200MHz+ applications. The input network of Figure 5 is devised to be populated with a bandpass filter.

Gerber or PDF files of this board are available.
If the higher frequency board is ordered without requesting a bandpass filter, C 6 is a counterpart to C 7 , providing a DC block, C23 is a $0 \Omega$ resistor.

If this is populated as a BP filter, The reactance of L1 and L 3 , and the series of C6 and C5 (and C21 and C23) should be between $50 \Omega$ and $33 \Omega$. The reactance of L 2 should match that of $1 / 2 \mathrm{C} 6^{\wedge}+\mathrm{C} 5$.
The ratio of C 5 to C 6 will determine coupling be-tween the two resonators, with a high ratio giving a narrow pass band.
As an example, for center frequency of $260 \mathrm{MHz} ;-3 \mathrm{~dB}$ BW of $150 \mathrm{MHz}, \mathrm{C} 6, \mathrm{C} 23=27 \mathrm{pF} ; \mathrm{C} 5, \mathrm{C} 21=68 \mathrm{pF} ; \mathrm{L} 1, \mathrm{~L} 3$ $=18 \mathrm{nH} ; \mathrm{L} 2=7.5 \mathrm{nH}$.

This has a flat passband over 80MHz. See Figure 6.
This filter is not intended as a band-defining filter, but simply to minimize noise BW prior to the ADC, and to minimize 2nd and 3rd originating in a drive amplifier. 2nd harmonic of 260 is down at 1.

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## QUICK START PROCEDURE



Figure 4. DC996A Artwork


Figure 5. Input Filter for DC996A Board

PUICK START PROCEDURG


Figure 6. Input Filter Frequency Response for DC996A Board


Figure 7. DC996B Board—Two Transformer Version


Figure 8. DC996B Artwork

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## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| DC996A General BOM |  |  |  |  |
| 1 | 0 | C4 (Option) | CAP~NPO~1.8pF~50V~0.25pF~0402 | AVX, 04025A1R8CAT2A |
| 2 | 1 | C8 | CAP~NPO~1.8pF~50V~0.25pF~0402 | AVX, 04025A1R8CAT2A |
| 3 | 1 | C12 | CAP X5R~0.01 FF~16V~10\% ~0402 | AVX, 0402YC103KAT |
| 4 | 15 | C15-16, C20, C22, C25-32, C34-36 | CAP $\sim 5 \mathrm{R} \sim 0.14 \mathrm{~F} \sim 10 \mathrm{~V} \sim 10 \% \sim 0402$ | AVX, 0402ZD104KAT |
| 5 | 0 | C10, C11 (Option) |  |  |
| 6 | 6 | C1-3, C6, C7, C23 | CAP $\sim$ X7R 0.01 $\mathrm{F} \sim 16 \mathrm{~V} \sim 10 \% \sim 0603$ | AVX, 0603YC103KAT |
| 7 | 2 | C18, C19 | CAP $\sim$ XR $\sim 0.1 \mu \mathrm{~F} \sim 16 \mathrm{~V} \sim 10 \% \sim 0603$ | AVX, 0603YC104KAT |
| 8 | 0 | C21 (Option) |  |  |
| 9 | 2 | C13, C17 | CAP $\sim$ X5R~2.2 $\mu$ F~10V~20\% 0805 | AVX, 0805ZD225MAT |
| 10 | 3 | C14, C24, C38 | CAP $\sim$ KR $\sim 4.7 \mu \mathrm{~F} \sim 10 \mathrm{~V} \sim 20 \% \sim 0805$ | AVX, 0805ZD475MAT |
| 11 | 0 | C5 (Option) |  |  |
| 12 | 4 | J2, J3, J4, J9 | HEADER~3X2~2mm | COMM_CON/2202S-06G2 |
| 13 | 2 | J5, J7 | CONN~SMA 50, EDGE-LAUNCH | E.F. Johnson, 142-0701-851 |
| 14 | 0 | L1 (Option) |  |  |
| 15 | 1 | L2 | RES 0 ${ }^{\text {_JUMPER~0603 }}$ | AAC, CJ06-000M |
| 16 | 0 | L3 (Option) |  |  |
| 17 | 19 | R13, R16-23, R30-35, R38-41 | RES~100 $2 \sim 5 \% \sim 1 / 20 \sim 0201$ | VISHAY, CRCW0201100RJNED |
| 18 | 1 | R15 | RES~100 $\sim 1 \% \sim 1 / 16 \sim 0402$ | VISHAY, CRCW0402100RFKED |
| 19 | 1 | R24 | RES~100k~1\%~1/16~0402 | VISHAY, CRCW0402100KFKED |
| 20 | 2 | R11-12 | RES 33.2 $2 \sim 1 \% \sim 1 / 16 \sim 0402$ | VISHAY, CRCW040233R2FKED |
| 21 | 2 | R1, R2 | RES 49.9 $\sim$ 1\% $1 / 16 \sim 0402$ | VISHAY, CRCW040249R9FKEA |
| 22 | 6 | R4, R5, R9, R10, R27, R28 | RES 4.99 $2 \sim 1 \% \sim 1 / 16 \mathrm{~W} \sim 0402$ | VISHAY, CRCW04024R99FKED |
| 23 | 3 | R25, R26, R29 | RES 4990 $2 \sim 1 \% \sim 1 / 16 \sim 0402$ | VISHAY, CRCW04024K99FKED |
| 24 | 0 | R3 (Option) |  |  |
| 25 | 2 | R14, R37 | RES $100 \Omega \sim 1 \% \sim 1 / 16 \mathrm{~W} \sim 0603$ | VISHAY, CRCW0603100RFKEA |
| 26 | 3 | R6-8 | RES 1000 $\sim$ 1\% $1 / 16 \mathrm{~W} \sim 0603$ | VISHAY, CRCW06031K00FKEB |
| 27 | 2 | R42, R43 | FERRITE BEAD~SMT~1206 | MURATA, BLM31PG330SN1L |
| 28 | 2 | T1, T2 | XFRM~RF~SMT~1:1 BALUN | MACOM, MABA-007159-000000 |
| 29 | 1 | U1 (Bal to 1298A) | IC~SERIAL_EEPROM~TSSOP8 | MICROCHIP, 24LCO25-I /ST |
| 30 | 2 | U3, U4 | BUFFER~LVDS~0CTAL | FAIRCHILD, FIN1108MTDX |
| 31 | 1 | U5 | BUFFER LVDSS SINGLE | FAIRCHILD, FIN1101K8X |
| 32 | 4 | TP1, TP2, TP4, TP5 | TURRET | MILL MAX, 2308-02-00-80-00-00-07-00 |
| 33 | 4 | Z (STAND-OFF) | STAND-OFF, NYLON 0.25'" tall | KEYSTONE, 8831(SNAP ON) |
| 34 | 5 |  | SHUNT, 0.079" Center | SAMTEC, 2SN-BK-G |
| 35 | 2 |  | STENCIL, 20X20 | STENCIL 996A, 20X20 |
| DC996A-P |  |  |  |  |
| 1 | 1 | U2 (DC996A-P) | IC ADC~130Msps~16-BIT~QFN-64 | LINEAR_TECH/LTC2208CUP\#PBF |
| 2 | 1 |  | FAB, PRINTED CIRCUIT BOARD | DEM0 CIRCUIT \#996A |
| DC996A-Q |  |  |  |  |
| 1 | 1 | U2 (DC996A-Q) | IC ADC 130Msps $\sim 14-\mathrm{BIT}$ QFN-64 | LINEAR_TECH/LTC2208CUP-14\#PBF |
| 2 | 1 |  | FAB, PRINTED CIRCUIT BOARD | DEM0 CIRCUIT \#996A |

## DEMO MANUAL DC996

## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| DC996B General BOM |  |  |  |  |
| 1 | 5 | C1-C3, C6-7 | CAP $\sim$ X7R $\sim 0.01 \mu \mathrm{~F} \sim 16 \mathrm{~V} \sim 10 \% \sim 0603$ | AVX/0603YC103KAT |
| 2 | 2 | C13, C17 | CAP $\sim$ X 2 R 2.2 $\mu$ F~10V~20\% 0805 | AVX/0805ZD225MAT |
| 3 | 3 | C14, C24, C38 | CAP $\sim$ XR $\sim 4.7 \mu \mathrm{~F} \sim 10 \mathrm{~V} \sim 20 \% \sim 0805$ | AVX/0805ZD475MAT |
| 4 | 15 | C15-16, C20, C22, C25-C32, C34-C36 | CAP $\sim$ XR $\sim 0.1 \mu \mathrm{~F} \sim 10 \mathrm{~V} \sim 10 \% \sim 0402$ | AVX/0402ZD104KAT |
| 5 | 0 | C18, C19(Option) | CAP $\sim$ X7R $\sim 0.1 \mu \mathrm{~F} \sim 16 \mathrm{~V} \sim 10 \% \sim 0603$ | AVX/0603YC104KAT |
| 6 | 1 | C4 (Also C9-C10 options) | CAP~NP0~8.2pF~50V~0.25pF~0402 | AVX/04025A8R2CAT2A |
| 7 | 2 | C5, C12 | CAP $\sim$ KR $\sim 0.01 \mu \mathrm{~F} \sim 16 \mathrm{~V} \sim 10 \% \sim 0402$ | AVX/0402YC103KAT |
| 8 | 3 | J2-4 | HEADER $\sim 3 \times 2 \sim 2 \mathrm{~mm}$ | COMM_CON/2202S-06G2 |
| 9 | 0 | J9 (Option) | HEADER $\sim 3 \times 2 \sim 2 \mathrm{~mm}$ | COMM_CON/2202S-06G2 |
| 10 | 2 | J5, J7 | CONN~SMA $50 \Omega$ EDGE-LAUNCH | AMPHENOL_CONNEX/132357 |
| 11 | 2 | R42-R43 | FERRITE BEAD SMT~1206 | MURATA/BLM31PG330SN1L |
| 12 | 2 | R9-R10 | RES~10』~1\% 1/16~0402 | AAC/CR05-10R0FM |
| 13 | 1 | R15 | RES $100 \Omega \sim 1 \% \sim 1 / 16 \sim 0402$ | AAC/CR05-1000FM |
| 14 | 1 | R37 | RES 100 $\sim$ 1\% 1/16W~0603 | AAC/CR16-1000FM |
| 15 | 19 | R13, R16-R23, R30-R35, R38-R41 | RES $100 \Omega \sim 5 \% \sim 1 / 20 \sim 0201$ | ACC/CR20-101JM |
| 16 | 3 | R6-8, R14 | RES 1 1 ~ 1\%~1/16W~0603 | AAC/CR16-1001FM |
| 17 | 1 | R24 | RES~100k~1\% 1/16~0402 | AAC/CR05-1003FM |
| 18 | 2 | R1-R2 | RES 49.9 ${ }^{\text {a }} 1 \% \sim 1 / 16 \sim 0402$ | AAC/CR05-49R9FM |
| 19 | 0 | R3 (OPTION) | RES 100 $\sim \sim 1 \% \sim 1 / 16 \mathrm{~W} \sim 0603$ | AAC/CR16-1000FM |
| 20 | 2 | R11-R12 | RES~33.2 $2 \sim 1 \% \sim 1 / 16 \sim 0402$ | AAC/CR05-33R2FM |
| 21 | 3 | R25, R26, R29 | RES 4990 $\sim \sim 1 \% \sim 1 / 16 \sim 0402$ | AAC/CR05-4991FM |
| 22 | 2 | R27-R28 | RES 10 $2 \sim 5 \% \sim 1 / 20 \sim 0201$ | PANASONIC, ERJ-1GEJ100C |
| 23 | 2 | R4-R5 | RES $5.1 \Omega \sim 1 \% \sim 1 / 16 \sim 0402$ | AAC/CR05-5R1FM |
| 24 | 1 | T3 | XFRM~RF~SMT~1:1 BALUN | M/A-COM, ETC1-1-13 (Leaded) M/A-COM, MABA-007159-000000 (PbF) |
| 25 | 4 | TP1-2, TP4-5 | TURRET | MILL_MAX/2308-2 |
| 26 | 1 | U1 | IC~Serial_EEPROM~TSSOP8 | MICROCHIP/24LCO25-I /ST |
| 27 | 2 | U3, U4 | BUFFER~LVDS~OCTAL | FAIRCHILD/FIN1108MTD |
| 28 | 1 | U5 | BUFFER~LVDS~SINGLE | FAIRCHILD/FIN1101K8X |
| 29 | 4 | Z (STAND-OFF) | STAND-OFF, NYLON 0.25" tall | KEYSTONE, 8831(SNAP ON) |
| 30 | 5 |  | SHUNT, 0.079" Center | SAMTEC, 2SN-BK-G |
| 31 | 2 |  | STENCIL, $20 \times 20$ | STENCIL 996B, 20X20 |
| DC996B-A |  |  |  |  |
| 1 | 1 | C8 | CAP~NPO~4.7pF~50V~0.25pF~0402 | AVX/04025A4R7CAT2A |
| 2 | 2 | C9-C10 | CAVP~NPO~8.2pF~50V~0.25pF~0402 | AVX/04025A8R2CAT2A |
| 3 | 1 | L1 | IND~56nH~5\% 0603 | MURATA/LQP18MN56NG02D |
| 4 | 2 | R36, R44 | RES~86.6~1\% 1/16W~0603 | AAC/CR16-86R6FM |
| 5 | 1 | R45 | RES 86.6~1\% 1/16~0402 | AAC/CR05-86R6FM |
| 6 | 1 | T1 | BALUN~RF~SMT~1:1 | M/A-COM, ETC1-1-13 (Leaded) M/A-COM, MABA-007159-000000 (PbF) |
| 7 | 1 | T2 | XFRM~RF~SMT~1:1CT | M/A-COM, ETC1-1T (Leaded) M/A-COM, MABAES0060 (PbF) |
| 8 | 1 | U2 (D/C 0619) | ADC~16BIT~130MSPS (Lot\# T23920.2) | LINEAR/LTC2208IUP\#PBF |
| 9 | 1 |  | FAB, PRINTED CIRCUIT BOARD | DEMO CIRCUIT 996B-A |

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## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| DC996B-B |  |  |  |  |
| 1 | 1 | C8 | CAP~NPO~1.8pF~50V~0.25pF~0402 | AVX/04025A1R8CAT2A |
| 2 | 2 | C9-C10 | CAP~NPO~3.9pF~50V~0.25pF~0402 | AVX/04025A3R9CAT2A |
| 3 | 1 | L1 | IND~18nH~5\% ~0603 | MURATA/LQP18MN18NG02D |
| 4 | 2 | R36, R44 | RES $43.2 \Omega \sim 1 \% \sim 1 / 16 \mathrm{~W} \sim 0603$ | AAC/CR16-43R2FM |
| 5 | 1 | R45 | RES~182 2 _JUMPER~0402 | AAC/CR05-1820FM |
| 6 | 1 | T1 | BALUN~RF~SMT~1:1 | M/A-COM, ETC1-1-13 (Leaded) M/A-COM, MABA-007159-000000 (PbF) |
| 7 | 1 | T2 | TRANSFORMER, WBC1-1L | COILCRAFT, WBC1-1L |
| 8 | 1 | U2 D/C 0619 | ADC 16-BIT~130Msps, Lot\# T23920.2 | LINEAR/LTC2208IUP\#PBF |
| 9 | 1 |  | FAB, PRINTED CIRCUIT BOARD | DEMO CIRCUIT \#996B-B |
| DC996B-C |  |  |  |  |


| 1 | 1 | C8 | CAP~NPO~4.7pF~50V~0.25pF~0402 | AVX/04025A4R7CAT2A |
| :---: | :--- | :--- | :--- | :--- |
| 2 | 2 | C9-C10 | CAP~NPO~8.2pF~50V~0.25pF~0402 | AVX/04025A8R2CAT2A |
| 3 | 1 | L1 | IND 56nH~5\% ~0603 | MURATA/LQP18MN56NG02D |
| 4 | 2 | R36, R44 | RES $\sim 86.6 \Omega \sim 1 \% \sim 1 / 16 W \sim 0603$ | AAC/CR16-86R6FM |
| 5 | 1 | R45 | RES~86.6 $\sim \sim 1 \% \sim 1 / 16 \sim 0402$ | AAC/CR05-86R6FM |
| 6 | 1 | T1 | BALUN $\sim$ RF~SMT~1:1 | M/A-COM, ETC1-1-13 (Leaded) <br> M/A-COM, MABA-007159-000000 (PbF) |
| 7 | 1 | T2 | XFRM~RF~SMT~1:1CT | M/A-COM, ETC1-1T (Leaded) <br> M/A-COMM, MABAES0060 (PbF) |
| 8 | 1 | U2 (Lot \#T23307.1) | ADC~14BIT~130MSPS (D/C 0604) | LINEAR/LTC2208IUP-14\#PBF |
| 9 | 1 |  | FAB, PRINTED CIRCUIT BOARD | DEMO CIRCUIT \#996B-C |

DC996B-D

| 1 | 1 | C8 | CAP~NPO~1.8pF~50V~0.25pF~0402 | AVX/04025A1R8CAT2A |
| :---: | :---: | :---: | :---: | :---: |
| 2 | 2 | C9-C10 | CAP~NPO~3.9pF~50V~0.25pF~0402 | AVX/04025A3R9CAT2A |
| 3 | 1 | L1 | IND~18nH~5\% 0603 | MURATA/LQP18MN18NG02D |
| 4 | 2 | R36, R44 | RES $43.2 \Omega \sim 1 \% \sim 1 / 16 \mathrm{~W} \sim 0603$ | AAC/CR16-43R2FM |
| 5 | 1 | R45 | RES $182 \Omega$ _JUMPER~0402 | AAC/CR05-1820FM |
| 6 | 1 | T1 | BALUN~RF~SMT~1:1 | $\begin{aligned} & \text { M/A-COM, ETC1-1-13 (Leaded) } \\ & \text { M/A-COM, MABA-007159-000000 (PbF) } \end{aligned}$ |
| 7 | 1 | T2 | TRANSFORMER, WBC1-1L | Coilcraft, WBC1-1L |
| 8 | 1 | U2 (Lot \#T23307.1) | ADC~14-BIT~130Msps (D/C 0604) | LINEAR/LTC2208IUP-14\#PBF |
| 9 | 1 |  | FAB, PRINTED CIRCUIT BOARD | DEMO CIRCUIT \#996B-D |
| DC966B-E |  |  |  |  |
| 1 | 1 | C8 | CAP~NPO~4.7pF~50V~0.25pF 0402 | AVX, 04025A4R7CAT2A |
| 2 | 2 | C9-10 | CAP~NPO~8.2pF~50V~0.25pF 0402 | AVX, 04025A8R2CAT2A |
| 3 | 1 | L1 | IND 56nH $\sim 5 \% 0603$ | MURATA, LQP18MN56NG02D |
| 4 | 2 | R36, R44 | RES 86.6 $2 \sim 1 \% \sim 1 / 16 \mathrm{~W} 0603$ | VISHAY, CRCW060386R6FKEA |
| 5 | 1 | R45 | RES 86.6 $2 \sim 1 \% \sim 1 / 160402$ | VISHAY, CRCW040286R6FKED |
| 6 | 1 | T1 | BALUN~RF~SMT~1:1 | M/A-COM, MABA-007159-000000 (PbF) |
| 7 | 1 | T2 | XFRM~RF~SMT~1:1CT | M/A-COM, MABAES0060 (PbF) |
| 8 | 1 | U2 | ADC~16-BIT~105Msps | LINEAR, LTC2217IUP\#PBF |
| 9 | 1 |  | FAB, PRINTED CIRCUIT BOARD | DEMO CIRCUIT 996B |

## DEMO MANUAL DC996

## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| DC966B-F |  |  |  |  |
| 1 | 1 | C8 | CAP~NPO~1.8pF~50V~0.25pF 0402 | AVX, 04025A1R8CAT2A |
| 2 | 2 | C9-10 | CAP~NPO~3.9pF~50V~0.25pF 0402 | AVX, 04025A3R9CAT2A |
| 3 | 1 | L1 | IND~18nH 5\% 0603 | MURATA, LQP18MN18NG02D |
| 4 | 2 | R36, R44 | RES 43.2 $2 \sim 1 \% \sim 1 / 16 \mathrm{~W} 0603$ | VISHAY, CRCW060343R2FKEA |
| 5 | 1 | R45 | RES $182 \Omega$ _JUMPER 0402 | VISHAY, CRCW0402182RFKED |
| 6 | 1 | T1 | BALUN~RF~SMT~1:1 | M/A-COM, MABA-007159-000000 (PbF) |
| 7 | 1 | T2 | TRANSFORMER, WBC1-1TL | Coilcraft, WBC1-1TLC |
| 8 | 1 | U2 | ADC~16-BIT~105Msps, | LINEAR, LTC2217IUP\#PBF |
| 9 | 1 |  | FAB, PRINTED CIRCUIT BOARD | DEM0 CIRCUIT \#996B |

DC966B-G

| 1 | 1 | C8 |
| :--- | :--- | :--- |
| 2 | 2 | C9-10 |
| 3 | 1 | L1 |
| 4 | 2 | R36, R44 |
| 5 | 1 | R45 |
| 6 | 1 | T1 |
| 7 | 1 | T2 |
| 8 | 1 | U2 |
| 9 | 1 |  |


| CAP~NPO~4.7pF~50V~0.25pF 0402 | AVX, 04025A4R7CAT2A |
| :---: | :---: |
| CAP~NPO~8.2pF~50V~0.25pF 0402 | AVX, 04025A8R2CAT2A |
| IND 56nH $5 \% 0603$ | MURATA, LQP18MN56NG02D |
| RES 86.6 $2 \sim 1 \% \sim 1 / 16 \mathrm{~W} 0603$ | VISHAY, CRCW060386R6FKEA |
| RES 86.6 $2 \sim 1 \% \sim 1 / 160402$ | VISHAY, CRCW040286R6FKED |
| BALUN~RF~SMT~1:1 | M/A-COM, MABA-007159-000000 (PbF) |
| XFRM~RF~SMT~1:1CT | M/A-COM, MABAES0060 (PbF) |
| ADC~16-BIT~80Msps | LINEAR, LTC2216IUP\#PBF |
| FAB, PRINTED CIRCUIT BOARD | DEMO CIRCUIT 996B |


| 1 | 1 | C8 |
| ---: | ---: | :--- |
| 2 | 2 | C9-10 |
| 3 | 1 | L1 |
| 4 | 2 | R36, R44 |
| 5 | 1 | R45 |
| 6 | 1 | T1 |
| 7 | 1 | T2 |
| 8 | 1 | U2 |
| 9 | 1 |  |


| CAP~NPO~1.8pF~50V~0.25pF 0402 | AVX, 04025A1R8CAT2A |
| :---: | :---: |
| CAP~NPO~3.9pF~50V~0.25pF 0402 | AVX, 04025A3R9CAT2A |
| IND~18nH 5\% 0603 | MURATA, LQP18MN18NG02D |
| RES $43.2 \Omega \sim 1 \% \sim 1 / 16 \mathrm{~W} 0603$ | VISHAY, CRCW060343R2FKEA |
| RES~182,_JUMPER 0402 | VISHAY, CRCW0402182RFKED |
| BALUN~RF~SMT~1:1 | M/A-COM, MABA-007159-000000 (PbF) |
| TRANSFORMER, WBC1-1TL | Coilcraft, WBC1-1TLC |
| ADC~16-BIT~80Msps, | LINEAR, LTC2216IUP\#PBF |
| FAB, PRINTED CIRCUIT BOARD | DEMO CIRCUIT \#996B |

DC966B-I

| 1 | 1 | C8 | CAP~NPO~4.7pF~50V~0.25pF 0402 | AVX, 04025A4R7CAT2A |
| :---: | :---: | :---: | :---: | :---: |
| 2 | 2 | C9-10 | CAP~NPO~8.2pF~50V~0.25pF 0402 | AVX, 04025A8R2CAT2A |
| 3 | 1 | L1 | IND 56nH $5 \% 0603$ | MURATA, LQP18MN56NG02D |
| 4 | 2 | R36, R44 | RES 86.6 $2 \sim 1 \% \sim 1 / 16 \mathrm{~W} 0603$ | VISHAY, CRCW060386R6FKEA |
| 6 | 1 | T1 (Bal to 1098A-F) | BALUN~RF~SMT~1:1 | M/A-COM, MABA-007159-000000 (PbF) |
| 7 | 1 | T2 (Bal to 1098A-C) | XFRM~RF~SMT~1:1CT | M/A-COM, MABAES0060 (PbF) |
| 8 | 1 | U2 | ADC~16-BIT~65Msps | LINEAR, LTC2215IUP\#PBF |
| 9 | 1 |  | FAB, PRINTED CIRCUIT BOARD | DEM0 CIRCUIT 996B |
| DC966B-J |  |  |  |  |
| 1 | 1 | C8 | CAP~NPO~1.8pF~50V~0.25pF 0402 | AVX, 04025A1R8CAT2A |
| 2 | 2 | C9-10 | CAP~NPO~3.9pF~50V~0.25pF 0402 | AVX, 04025A3R9CAT2A |
| 3 | 1 | L1 | IND 18nH $5 \% 0603$ | MURATA, LQP18MN18NG02D |
| 4 | 2 | R36, R44 | RES 43.2 $2 \sim 1 \% \sim 1 / 16 \mathrm{~W} 0603$ | VISHAY, CRCW060343R2FKEA |
| 5 | 1 | R45 | RES $182 \Omega$ JUMPER 0402 | VISHAY, CRCW0402182RFKED |
| 6 | 1 | T1 | BALUN~RF~SMT~1:1 | M/A-COM, MABA-007159-000000 (PbF) |
| 7 | 1 | T2 | TRANSFORMER, WBC1-1TL | Coilcraft, WBC1-1TLC |
| 8 | 1 | U2 | ADC~16-BIT~65Msps, | LINEAR/LTC2215IUP\#PBF |
| 9 | 1 |  | FAB, PRINTED CIRCUIT BOARD | DEMO CIRCUIT \#996B |

## DEMO MANUAL DC996

## SCHEMATIC DIAGRAM



## SCHEMATIC DIAGRAM



## DEMO MANUAL DC996

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