LTC2242-12/10, LTC2241-12/10 OR LTC2240-12/10

DESCRIPTION

Demonstration circuit 997 supports a family of 10/12 BIT 250, 210 and 170 MSPS ADCs. Each assembly features one of the following devices: LTC2242-12, LTC2241-12, LTC2240-12, LTC2242-10, LTC2241-10 or LTC2240-10 high speed, high dynamic range ADCs.

The versions of the 997B demo board that support the LTC2242 family of 10 and 12 BIT A/D converters are listed in Table 1. Depending on the required resolution and sample rate the DC997 is supplied with the appropriate A/D. The circuitry on the analog inputs is optimized for analog input frequencies from 10 MHz to 250 MHz.

Design files for this circuit board are available. Call the LTC factory.

Table 1. DC997B Variants

DC997 VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
997B-A	LTC2242-12	12-Bit	250Msps	10MHz < A_{IN} < 250MHz
997B-B	LTC2241-12	12-Bit	210Msps	10MHz < A_{IN} < 250MHz
997B-C	LTC2240-12	12-Bit	170Msps	10MHz < A_{IN} < 250MHz
997B-D	LTC2242-10	10-Bit	250Msps	10MHz < A_{IN} < 250MHz
997B-E	LTC2241-10	10-Bit	210Msps	10MHz < A_{IN} < 250MHz
997B-F	LTC2240-10	10-Bit	170Msps	10MHz < A_{IN} < 250MHz

Table 2. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage	Depending on sampling rate and the A/D converter provided, this supply must provide up to 500mA.	3.3V ±0.3V (10%); The 2.5V supply required by the ADC is regulated locally by U8 from the 3.3V
Analog input range	Depending on Sense Pin Voltage (at converter inputs)	$1V_{PP}$ to $2V_{PP}$
Logic Input Voltages: OE, $\overline{SHDN}$	Minimum Logic High	1.7V
	Maximum Logic Low	0.7V
Logic Output Voltage (FIN1108T LVDS Buffer)	Minimum Logic High @ -3.4mA w/100Ω Termination	1.2V +170mV
	Maximum Logic Low @ +3.4mA w/100Ω Termination	1.2V – 170mV
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Encode Clock Level	50 Ω Source Impedance. (Convert Clock input is capacitor coupled on board and terminated with 50Ω.)	$0.2V_{P-P}$ ⇔$2.5V_{P-P}$ Sine Wave or Square wave
Resolution	See Table 1	
Input frequency range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 997 is easy to set up to evaluate the performance of any of the LTC2242 family of High Speed LVDS output A/D converters - LTC2242-12, LTC2241-12, LTC2240-12, LTC2242-10, LTC2241-10 or LTC2240-10. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

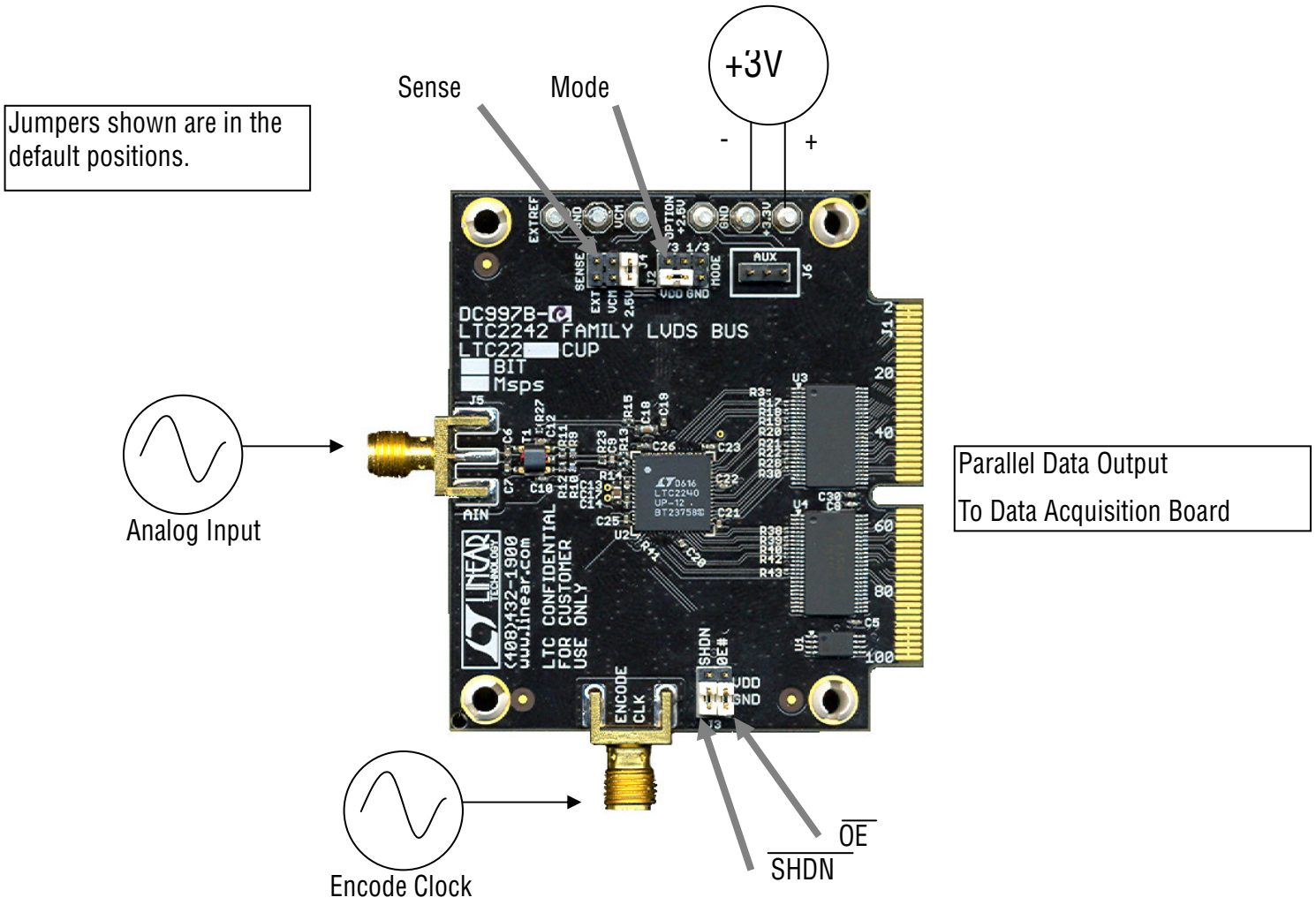


Figure 1. DC997 Setup

JUMPERS

The DC997 demonstration circuit board should have the following jumper settings:

❑ JP2 - MODE:

- VDD: 2's complement & disable Clock Duty Cycle Stabilizer (Default for LTC2240, 2241)
- 2/3: 2's complement & Clock Duty Cycle Stabilizer on (Default for LTC2242)
- 1/3: Offset Binary & Clock Duty Cycle Stabilizer on
- GND: Offset Binary & Clock Duty Cycle Stabilizer off

❑ JP3:

- SHDN & OE GND: Normal operation (Default)
- SHDN GND & OE Vdd: Normal operation with high output impedance
- SHDN Vdd & OE GND: Nap Mode with high output impedance
- SHDN Vdd & OE Vdd: Sleep Mode with high output impedance

❑ JP4 - SENSE:

- Select 2.5V for the $2V_{PP}$ input range (Default)
- Select VCM for the $1V_{PP}$ input range

POWER

If a DC890B is used to acquire data from the DC997, the DC890B should be connected to a USB port and provided an external 6V, 1Amp power supply. The DC890B will not enable LVDS mode without externally applied power present. Apply +3.3V across the pins marked "+3.3V" and "GND" on the DC997. The DC997 demonstration circuit requires up to 500 mA depending on the sampling rate and the A/D converter supplied.

While the DC890B data collection board is initially powered by the USB cable, it requires an external power supply of 6V on the 2.1mm power jack or the adjacent turrets (+) and (-) before the DC890B will enable LVDS mode.

ENCODE CLOCK

NOTE: THIS IS NOT A LOGIC LEVEL INPUT. Apply an encode clock to the SMA connector on the DC997 demonstration circuit board marked "ENCODE CLK". Refer to Table 2 for recommended level, impedance and coupling. For the best noise performance (SNR AND SFDR), the ENCODE CLK must be driven with a very low jitter source. When using a sinusoidal generator, the amplitude should be large, up to $2.5V_{P-P}$. Using bandpass filters on the ENCODE CLK and the Analog input [AIN] will improve the noise performance by reducing the wideband noise power of the signals. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broad band noise. The very high sampling bandwidth of the LTC2242 family of parts will fold multiple Nyquist bands of noise (if present) down to base band raising the noise floor.

[The LTC2242 family of ADCs provides a flexible Encode Clock interface capable of accommodating both single ended and differential sources from LVDS or sinusoidal inputs. See the LTC2242 data sheet for other Encode Clock drive options.]

ANALOG INPUT NETWORK

The input transformer and the RC network on the analog inputs are optimized for 10 to 250MHz. These components must be optimized for higher or lower input frequencies. Consult the LTC2242 data sheet for other frequency ranges.

Apply the analog input signal of interest to the SMA connector on the DC997 demonstration circuit board marked "AIN". This input is capacitive coupled to the input of a MaCom ETC1-1-13 balun or a flux coupled ETC1-1T transformer. (See Schematic)

DIGITAL OUTPUTS

The LVDS conversion clock output is available on pins [50, 52] of J2. The LVDS data samples are available on Pins [8-46, 56-82] for 12 BITS or [8-46, 56-70] for 10 BITS as LVDS pairs isolated by a ground pin between each set. The data samples can be collected via a logic analyzer, cabled to a development system through a SHORT 100 pin ribbon cable (available from Samtec - HSC8 series of high speed connectors) or directly via a DC890B FastDAACS data collection system.

SOFTWARE

The DC890B is controlled by the *PScope System Software* provided or downloaded from the Linear Technology website at http://www.linear.com/software/. If a DC890B was provided, follow the DC890 Quick Start Guide and the instructions below.

To start the data collection software if "*PScope.exe*", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC997 demonstration circuit is properly connected to the DC890, PSCOPE should automatically detect the DC997, and configure itself accordingly. If necessary the procedure below explains how to manually configure PSCOPE.

Under the "Configure" menu, go to "ADC Configuration...." Check the "Config Manually" box and use the following configuration options, see Figure 2:

Bits: 12 (or 10 for 10 bits parts)

Alignment: 15

FPGA Ld: LVDS

Channs: 1

Bipolar: Checked

Positive-Edge Clk: Unchecked

When evaluating 10 BIT performance using a 12 BIT part, select the 10 Bit part and PScope will automatically blank the last two LSBs when using a DC997 supplied with a 12 BIT ADC.

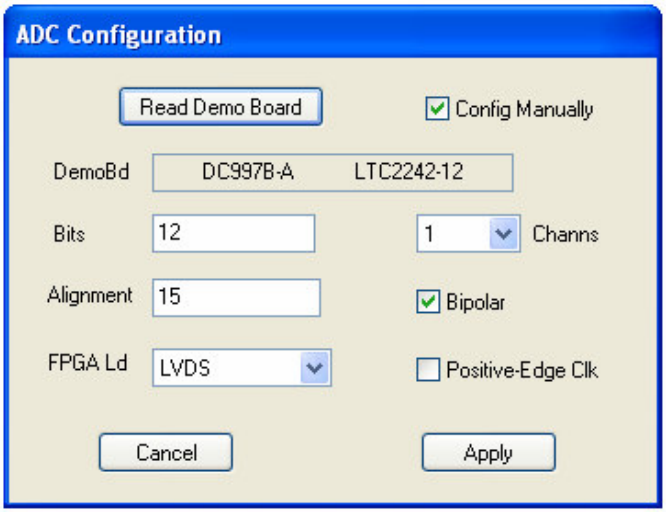
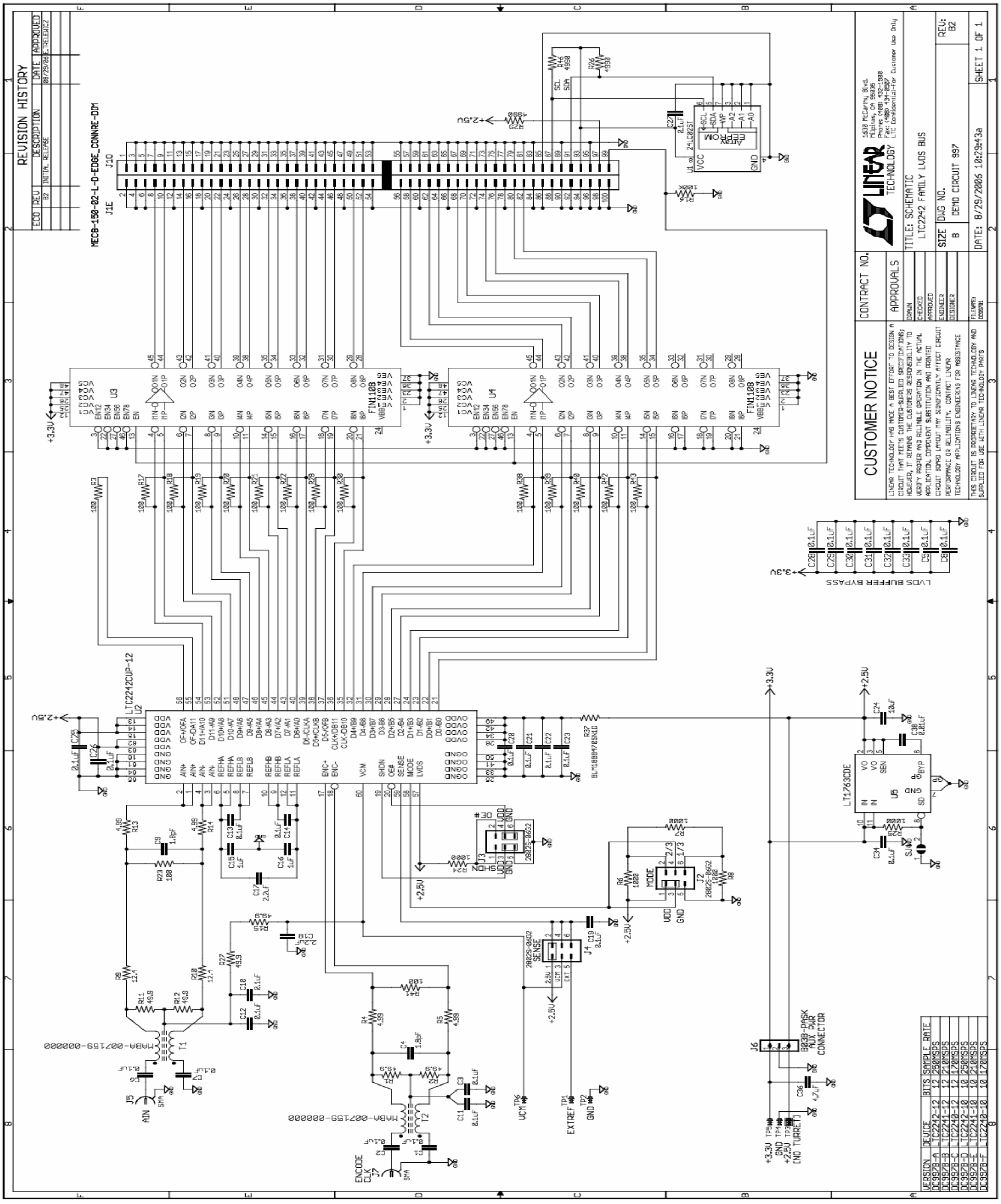


Figure 2. ADC Configuration

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for *PScope* is available in the DC890B Quick Start Guide and in the online help available within the *PScope* program itself.


REVISION HISTORY
CUSTOMER NOTICE
LVDS BUFFER BYPASS
TITLE: SCHEMATIC
LTC2242 FAMILY LVDS BUS
DEMO CIRCUIT 997
DATE: 8/29/2006 10:29:43a
SHEET 1 OF 1

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Data Conversion IC Development Tools ***category:***

Click to view products by Analog Devices ***manufacturer:***

Other Similar products are found below :

EVAL-AD5063EBZ EVAL-AD5422LFEBZ EVAL-AD7265EDZ EVAL-AD7641EDZ EVAL-AD7674EDZ EVAL-AD7719EBZ EVAL-AD7767-1EDZ EVAL-AD7995EBZ AD9114-DPG2-EBZ AD9211-200EBZ AD9251-20EBZ AD9251-65EBZ AD9255-125EBZ AD9284-250EBZ AD9613-170EBZ AD9627-125EBZ AD9629-20EBZ AD9709-EBZ AD9716-DPG2-EBZ AD9737A-EBZ AD9787-DPG2-EBZ AD9993-EBZ DAC8555EVM ADS5482EVM ADS8372EVM EVAL-AD5061EBZ EVAL-AD5062EBZ EVAL-AD5443-DBRDZ EVAL-AD5570SDZ EVAL-AD7450ASDZ EVAL-AD7677EDZ EVAL-AD7992EBZ EVAL-AD7994EBZ AD9119-MIX-EBZ AD9148-M5375-EBZ AD9204-80EBZ AD9233-125EBZ AD9265-105EBZ AD9265-80EBZ AD9608-125EBZ AD9629-80EBZ AD9648-125EBZ AD9649-20EBZ AD9650-80EBZ AD9765-EBZ AD9767-EBZ AD9778A-DPG2-EBZ ADS8322EVM LM96080EB/NOPB EVAL-AD5445SDZ