HMC291SE

v05.1216

4 dB LSB SILICON 2-BIT POSITIVE CONTROL DIGITAL ATTENUATOR, 0.7 - 4.0 GHz

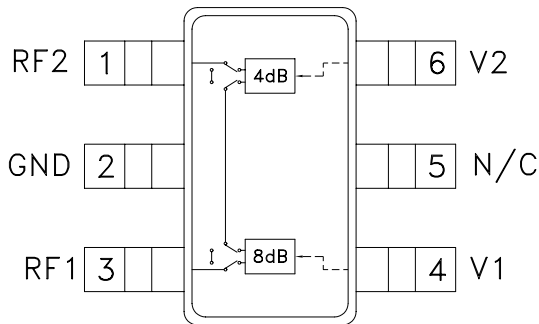### Typical Applications

The HMC291SE is ideal for:

• Cellular

• PCS, ISM, MMDS

• WLL Handset & Base Station

Features

RoHS Compliant Product

4 dB LSB Steps to 12 dB

Single Positive Control Per Bit, 0/+3V or +5V

Typical Step Error : ±0.3 dB

Miniature SOT 26 Package: 9 mm^2

Functional Diagram

General Description

The HMC291SE is a general purpose broadband 2-bit positive control silicon IC digital attenuator in 6 lead SOT26 surface mount plastic package. The insertion loss is typically in between 0.4 dB - 1 dB through operating frequency range. The attenuator bit values are 4 (LSB) and 8 dB for a total attenuation of 12 dB. State error is excellent at ± 0.4 dB typical with an IIP3 of up to 57 dBm. Two bit control voltage inputs, toggled between 0V and +3V or +5V, are used to select each attenuation state at less than 25 µA each. A single VDD supply voltage of +3V to +5V applied through an external 4.7K Ohm resistor is required.

Electrical Specifications,

T_A = +25°C, VDD = +3V to +5V & VCTL = 0/VDD (Unless Otherwise Stated)

| Parameter		Frequency	Min.	Typical	Max.	Units
Insertion Loss		0.7 - 1.4 GHz		0.5	0.65	dB
		1.4 - 2.3 GHz		0.5	0.65	dB
		2.3 - 2.7 GHz		0.6	0.7	dB
		2.7 - 4.0 GHz		0.8	1.32	dB
Attenuation Range		0.7 - 4.0 GHz		12		dB
Return Loss (RF1 & RF2, All Atten. States)		0.7 - 1.4 GHz	20	25		dB
		1.4 - 4.0 GHz	17	27		dB
State Error						
All Attenuation States		0.7 - 1.4 GHz		± (0.1 + 4% of Atten. Setting Max)		dB
All Attenuation States		1.4 - 2.3 GHz		± (0.2 + 2% of Atten. Setting Max)		dB
All Attenuation States		2.3 - 2.7 GHz		± (0.4 + 3% of Atten. Setting Max)		dB
All Attenuation States		2.7 - 4.0 GHz		± (0.4 + 4% of Atten. Setting Max)		dB
Input Power for 0.1 dB Compression (Input P0.1dB)	5V[1]	0.7 - 4.0 GHz		28		dBm
	3V			27		dBm
Input Third Order Intercept Point (IIP3)	5V	0.7 - 4.0 GHz	52	57	59	dBm
(Two-tone Input Power = 15 dBm Each Tone)	3V		52	54	56	dBm
Switching Characteristics		0.7 - 4.0 GHz				
t$_{RISE}$, t$_{FALL}$ (10/90% RF)				250		ns
t$_{ON}$, t$_{OFF}$ (50% CTL to 10/90% RF)				300		ns

[1] Compression point is above maximum input power

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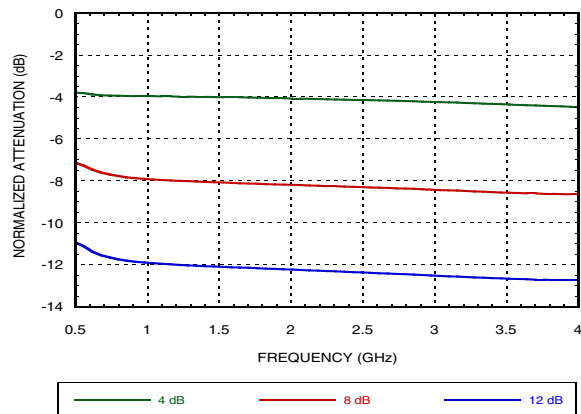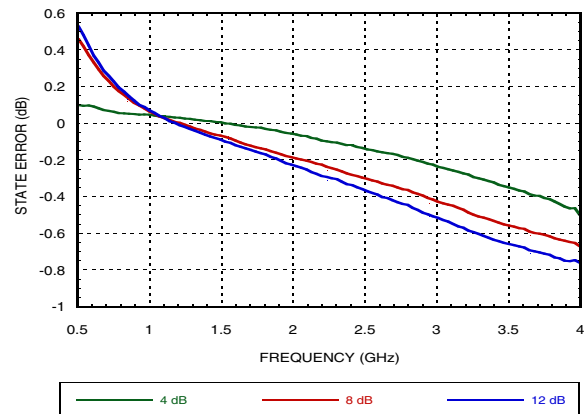**ATTENUATORS - ANALOG - SMT**

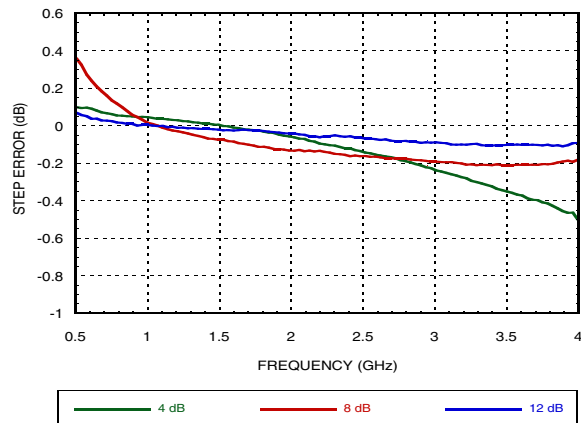### Insertion Loss
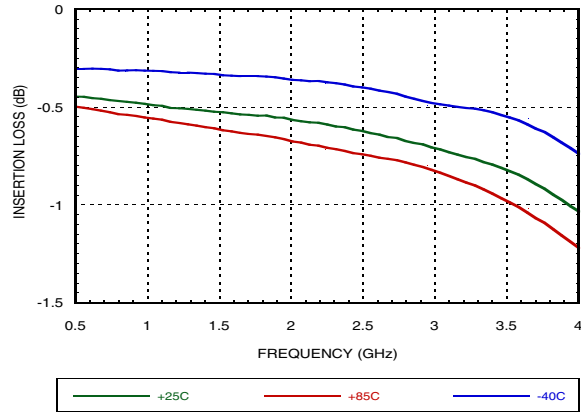
Return Loss RF1, RF2
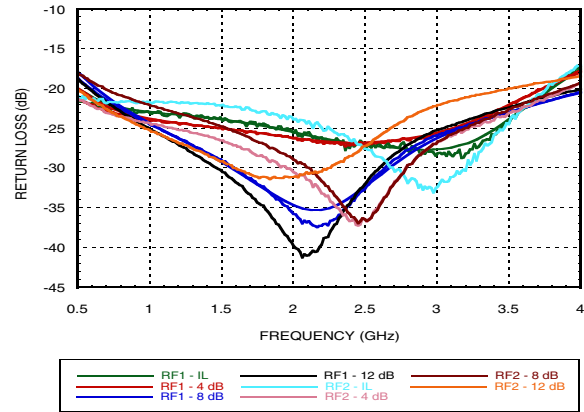
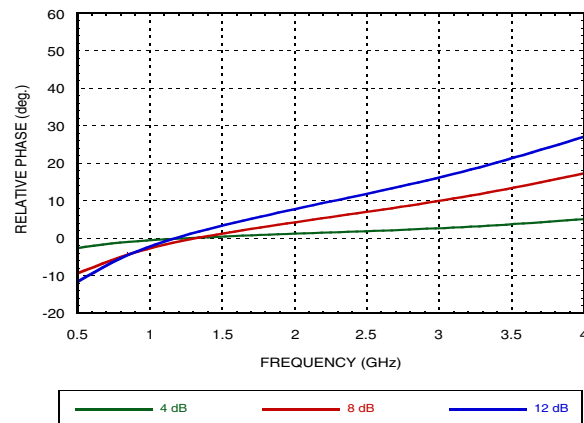### Normalized Attenuation vs. Attenuation State

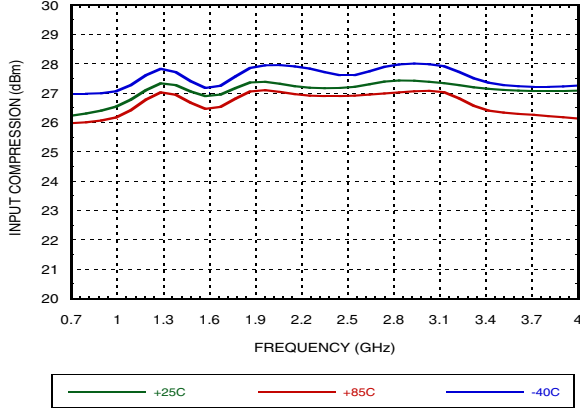### State Error vs. Attenuation State

Step Error vs. Frequency

Relative Phase vs. Frequency
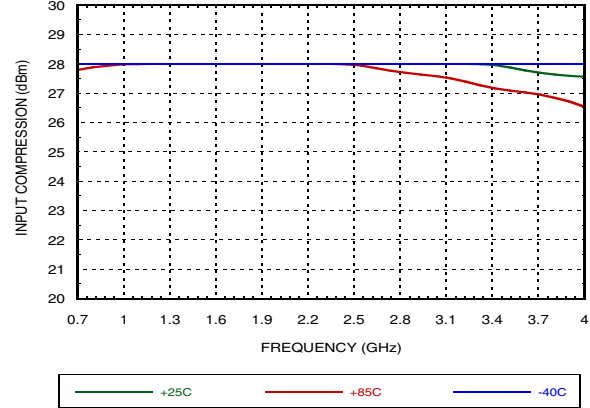
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ATTENUATORS - ANALOG - SMT

Input P0.1dB vs. Frequency at 3V over Temperature

Input P0.1dB vs. Frequency at 5V over Temperature[1]

IIP3 vs. Frequency at 3V over Temperature
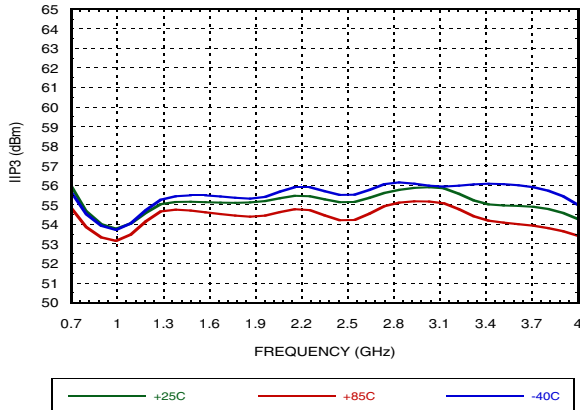
IIP3 vs. Frequency at 5V over Temperature
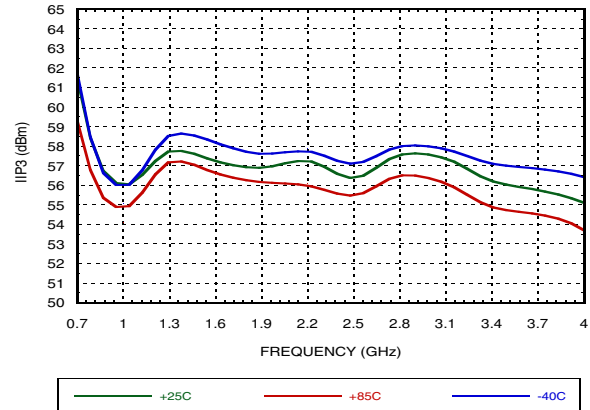
[1] Input P0.1dB is limited by maximum test power of 28 dBm.

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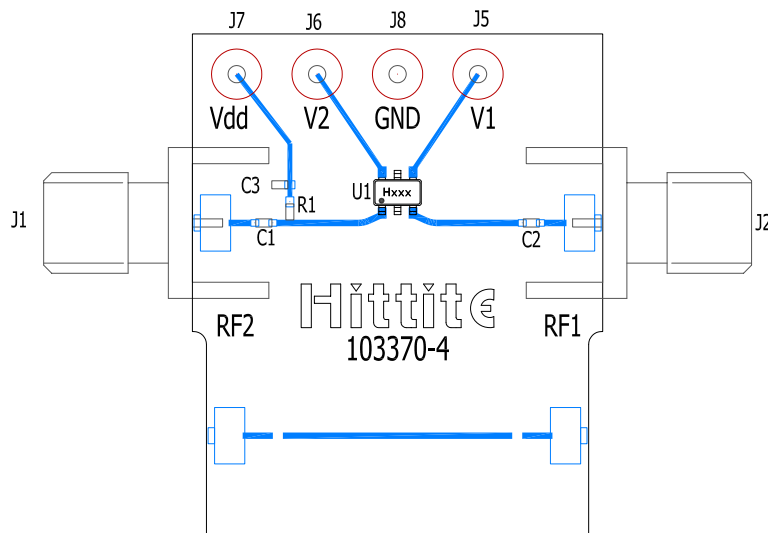
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Application Circuit

DC blocking capacitors C1 and C2 are required on RF1 and RF2. Choose C1 = C2 = 100 ~ 300 pF to allow lowest frequency of operation to pass with minimal loss. R1 = 4.7K Ohm is required to supply voltage to the circuit through either PIN 3 or PIN 1.
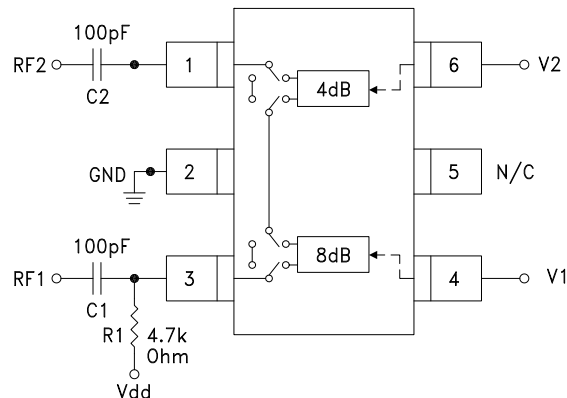
Evaluation Circuit Board

List of Materials for Evaluation PCB EV1HMC291SE [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J5 - J8	DC Pin
R1	4.7 kOhm Resistor, 0402 Pkg.
C1, C2	0402 Pkg. Capacitor, Select for Lowest Frequency of Operation
C3	1 nF capacitor, 0402 Pkg.
U1	HMC291SE Digital Attenuator
PCB [2]	103370 Evaluation PCB 1.5" x 1.5"

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board as shown is available from Analog Devices upon request.

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Truth Table

Control Voltage Input (VCTL)		Attenuation Setting RF1 - RF2
V1 8 dB	V2 4 dB	
High	High	Reference I.L.
High	Low	4 dB
Low	High	8 dB
Low	Low	12 dB Max. Atten.

Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Control & Bias Voltages

State	Bias Condition
Low	0 to +0.2V at 500 µA Max.
High	VDD ± 0.2V at 550 µA Max.

Note: VDD = +3V to 5V with ± 0.2V tolerance

Absolute Maximum Ratings

Control Voltage (V1, V2)	VDD + 0.5 VDC
RF Input Power	+28 dBm
Bias Voltage (VDD)	+8.0 Vdc
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
ESD Sensitivity (HBM)	Class 1C
ESD Sensitivity (FICDM)	Class IV

Outline Drawing
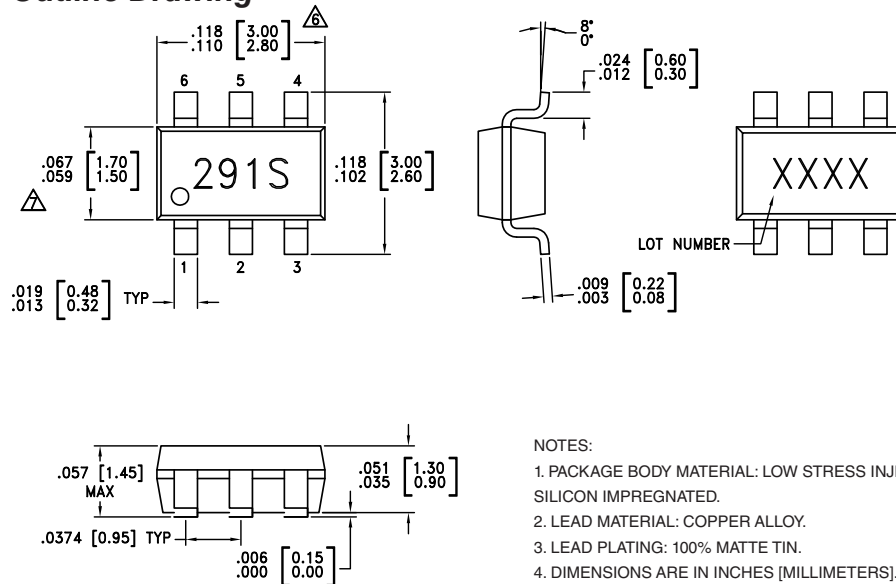
NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD MATERIAL: COPPER ALLOY.
3. LEAD PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. CHARACTERS TO BE HELVETICA MEDIUM, .030 HIGH, LASER OR WHITE INK, LOCATED APPROXIMATELY AS SHOWN.
6. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
7. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
8. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC291SE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	291S XXXX

[1] XXXX 4 digit lot number is on the bottom of package
[2] Max peak reflow temperature of 260°C

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