0.1 GHz to 3 GHz,1 dB LSB, 5-Bit, GaAs Digital Attenuator

Data Sheet

HMC470A

FEATURES

- **Attenuation range: 1 dB LSB steps to 31 dB**
- **Insertion loss: 1.7 dB typical at 3 GHz**
- **Excellent attenuation accuracy: 0.3 dB typical**
- **High Input linearity**
  - **0.1dB compression (P0.1dB): 27 dBm typical**
  - **Third-order intercept (IP3): 48 dBm typical**
- **High power handling: 27 dBm**
- **Low phase shift: 27° at 3 GHz**
- **Single-supply operation: 3 V to 5 V**
- **CMOS-/TTL-compatible parallel control**
- **16-lead, 3 mm × 3 mm LFCSP package**

APPLICATIONS

- **Cellular infrastructure**
- **Microwave radios and very small aperture terminals (VSATs)**
- **Test equipment and sensors**
- **IF and RF designs**

FUNCTIONAL BLOCK DIAGRAM

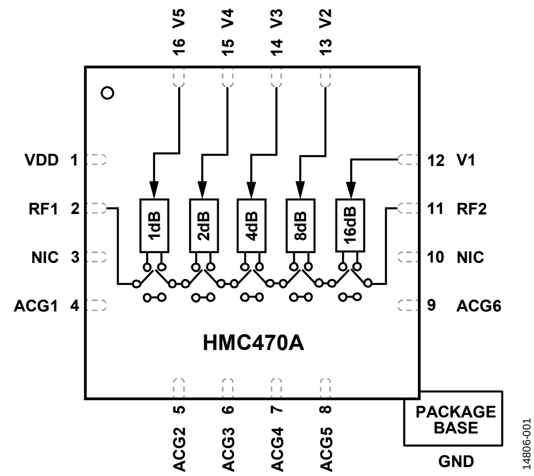

Figure 1.

GENERAL DESCRIPTION

The HMC470A is a 5-bit digital attenuator with a 31 dB attenuation control range in 1 dB steps.

The HMC470A offers excellent attenuation accuracy and high input linearity over the specified frequency range from 100 MHz to 3 GHz. However, this digital attenuator features ACG pins for external ac grounding capacitors to extend the operation below 100 MHz.

The HMC470A operates with a single positive supply voltage from 3 V to 5 V and provides CMOS-/TTL-compatible parallel control interface by incorporating an on-chip driver. The HMC470A comes in a RoHS compliant, compact, 3 mm × 3 mm LFCSP package.

Rev. A Document Feedback

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REVISION HISTORY

9/2017—Rev. 01.0716 to Rev. A

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

Change to Product Title ... 1
Updated Outline Dimensions ... 11

SPECIFICATIONS

V_{DD} = 3 V to 5 V, V_{CTL} = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.1		3.0	GHz
INSERTION LOSS		0.1 GHz to 1.5 GHz		1.3	1.6	dB
		1.5 GHz to 2.3 GHz		1.5	1.8	dB
		2.3 GHz to 3.0 GHz		1.7	2.0	dB
ATTENUATION						
Range		Between minimum and maximum attenuation states, 0.1 GHz to 3.0 GHz		31		dB
Step Size		Between any successive attenuation states, 0.1 GHz to 3.0 GHz		1		dB
Step Error		Between any successive attenuation states, 0.1 GHz to 33 GHz		<±0.2		dB
State Error		Referenced to insertion loss state				
		All attenuation states, 0.1 GHz to 2.3 GHz	−(0.3 + 2% of attenuation state)		+(0.3 + 2% of attenuation state)	dB
		1 dB to 15 dB attenuation states, 2.3 GHz to 3.0 GHz	−(0.3 + 3% of attenuation state)		+(0.3 + 3% of attenuation state)	dB
		16 dB to 31 dB attenuation states, 2.3 GHz to 3.0 GHz	−(0.3 + 6% of attenuation state)		+(0.3 + 6% of attenuation state)	dB
RETURN LOSS		RF1 and RF2 pins, all attenuation states, 0.1 GHz to 3.0 GHz		14		dB
RELATIVE PHASE		Between minimum and maximum attenuation states				
		0.1 GHz to 1.5 GHz		12		Degrees
		1.5 GHz to 3.0 GHz		27		Degrees
SWITCHING CHARACTERISTICS		Between all attenuation states				
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		50		ns
On and Off Time	t_{ON}, t_{OFF}	50% VCTL to 90% of RF output		70		ns
INPUT LINEARITY[1]		All attenuation states, 250 MHz to 3.0 GHz				
0.1 dB Compression	P0.1dB	VDD = 3 V		25		dBm
		VDD = 5 V		27		dBm
Third-Order Intercept	IP3	10 dBm per tone, 1 MHz spacing		50		dBm
SUPPLY CURRENT	I_{DD}			1.7		mA
DIGITAL CONTROL INPUTS		V1 to V5 pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		2.0		VDD	V
Current						
Low	I_{INL}			1		µA
High	I_{INH}			40		µA

[1] Input linearity performance degrades at frequencies less than 250 MHz; see Figure 16 to Figure 19.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	7 V
Digital Control Input Voltage	−1 V to V_{DD} +1 V
RF Input Power[1] (All Attenuation States, f = 250 MHz to 3 GHz, T_{CASE} = 85°C)	
V_{DD} = 3 V	25 dBm
V_{DD} = 5 V	27 dBm
Continuous Power Dissipation, P_{DISS} (T_{CASE} = 85°C)	0.5 W
Temperature	
Junction, T_J	150°C
Storage	−65°C to +150°C
Reflow[2] ((Moisture Sensitivity Level 3 (MSL3) Rating)	260°C
ESD Sensitivity	
Human Body Model (HBM)	250 V (Class 1A)

[1] For power derating at frequencies less than 250 MHz, see Figure 2.
[2] See the Ordering Guide for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

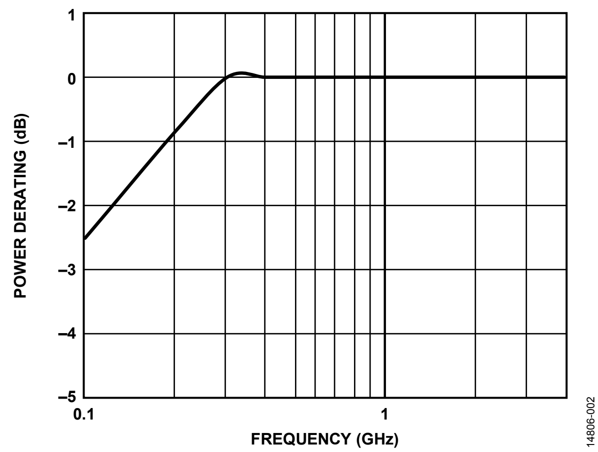


Figure 2. Power Derating at Frequencies Less Than 250 MHz

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

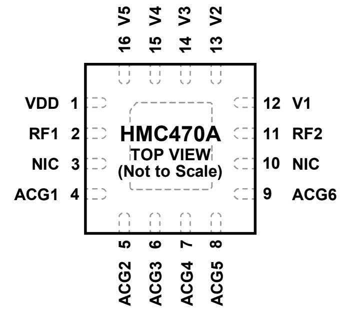
Package Type	θ_{JC}	Unit
HCP-16-1[1]	130[2]	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with five thermal vias. See JEDEC JESD51.
[2] The device is set to maximum attenuation state.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = THESE PINS ARE NOT INTERNALLY CONNECTED; HOWEVER, ALL DATA SHOWN HEREIN WAS MEASURED WHEN THESE PINS CONNECTED TO RF/DC GROUND OF EVALUATION BOARD.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

14806-003

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD	Power Supply.
2	RF1	This pin can be used as RF input or output of attenuator. This pin is dc-coupled to VDD and ac matched to 50 Ω. An external dc blocking capacitor is required. Select the capacitor value for the lowest frequency of operation.
3, 10	NIC	Not Internally Connected. These pins are not internally connected; however, all data shown herein was measured when these pins connected to RF/DC ground of evaluation board.
4 to 9	ACG1 to ACG6	AC Grounding Capacitor Pins. These pins can be left no connected when operating above 700 MHz. For frequencies less than 700 MHz, connect capacitors larger than 100 pF as close to the ACGx pins as possible. Select the capacitor value for the lowest frequency of operation.
11	RF2	This pin can be used as RF input or output of attenuator. This pin is dc-coupled to VDD V and ac matched to 50 Ω. An external dc blocking capacitor is required. Select the capacitor value for the lowest frequency of operation.
12 to 16	V1 to V5	Parallel Control Voltage Inputs. These pins select the required attenuation (see Table 5).
	EPAD	Exposed Pad. The exposed pad must be connected to ground for proper operation.

INTERFACE SCHEMATICS

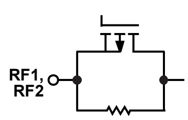


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Figure 4. RF1, RF2 Interface Schematic

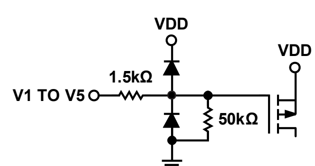

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Figure 5. Digital Control Input Interface

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

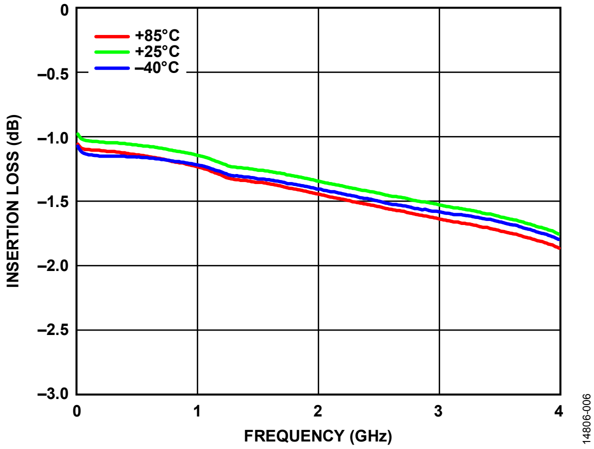


Figure 6. Insertion Loss vs. Frequency over Temperature

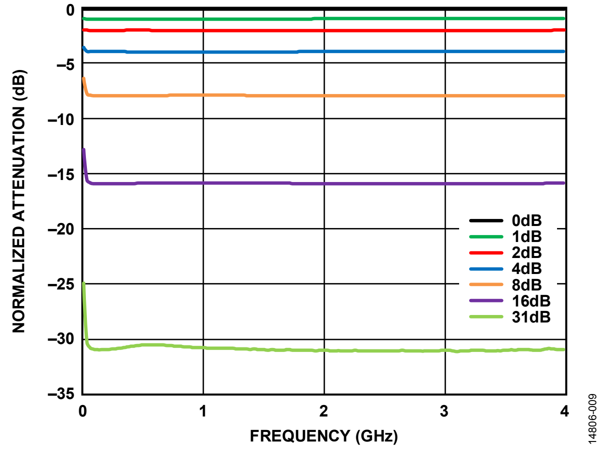


Figure 9. Normalized Attenuation vs. Frequency over Major Attenuation States

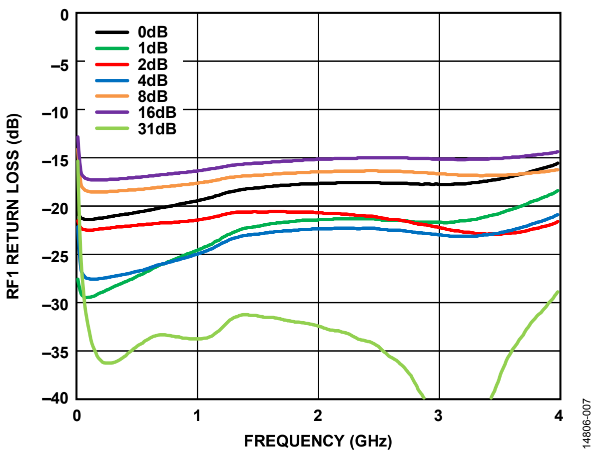


Figure 7. RF1 Return Loss vs. Frequency over Major Attenuation States

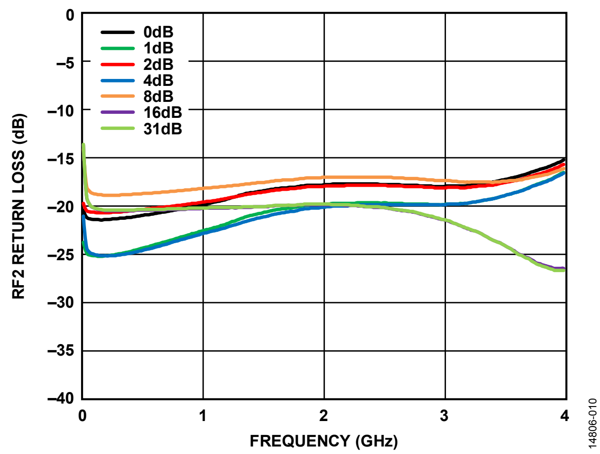


Figure 10. RF2 Return Loss vs. Frequency over Major Attenuation States

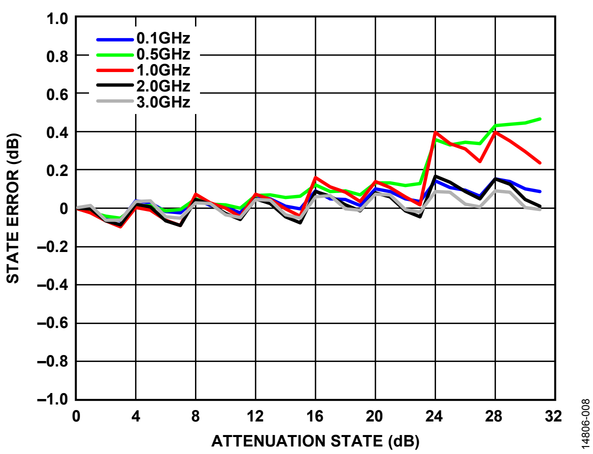


Figure 8. State Error vs. Attenuation State over Frequency

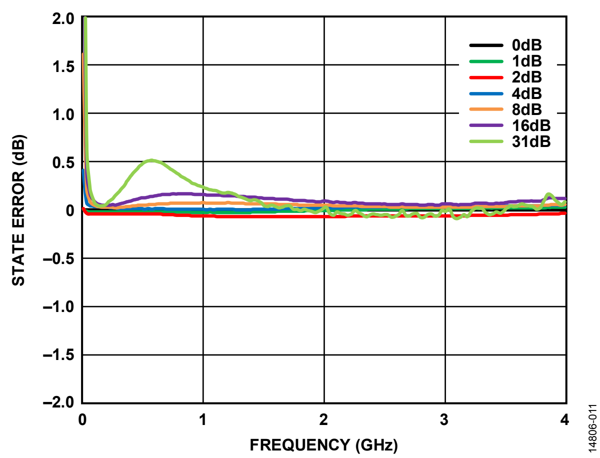


Figure 11. State Error vs. Frequency over Major Attenuation States

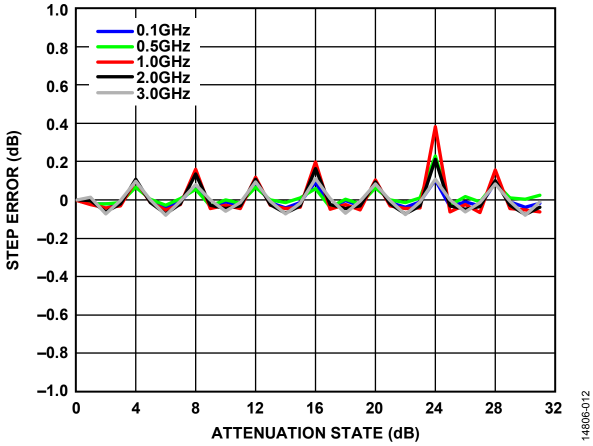


Figure 12. Step Error vs. Attenuation State over Frequency

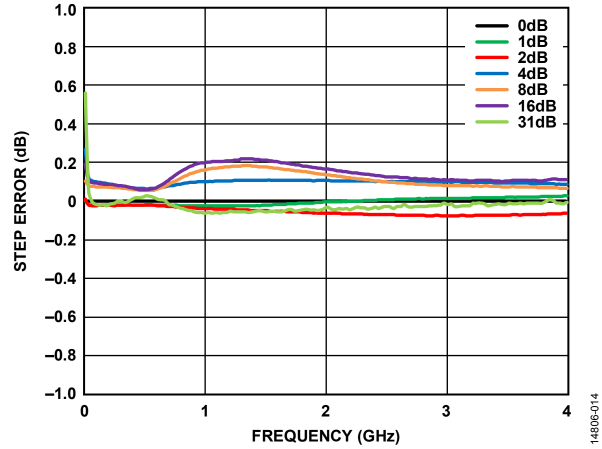


Figure 14. Step Error vs. Frequency over Major Attenuation States

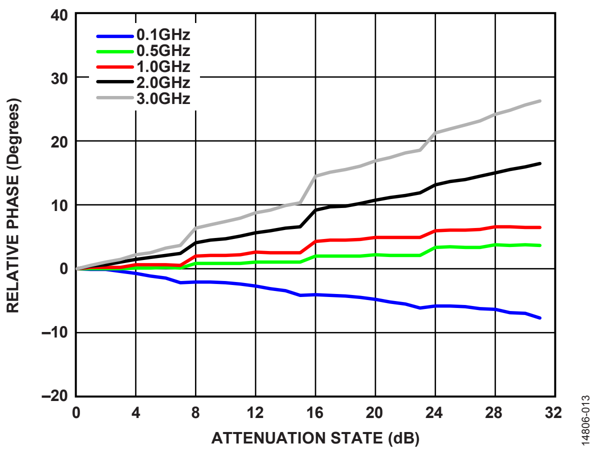


Figure 13. Relative Phase vs. Attenuation State over Frequency

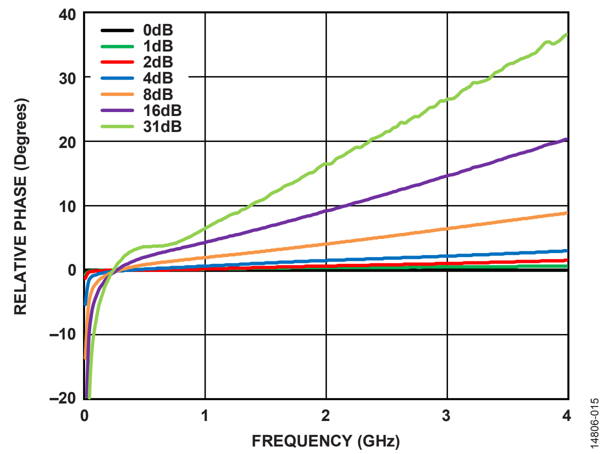


Figure 15. Relative Phase vs. Frequency over Major Attenuation States

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

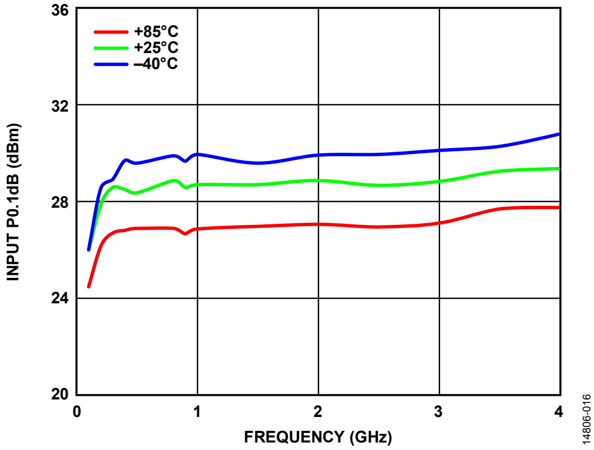


Figure 16. Input P0.1dB vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 5 V

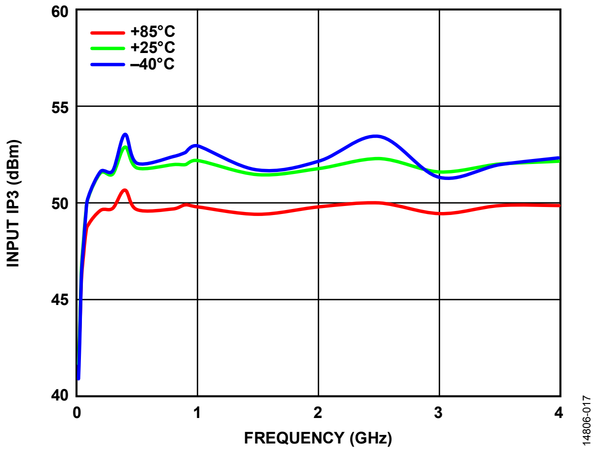


Figure 17. Input IP3 vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 5 V

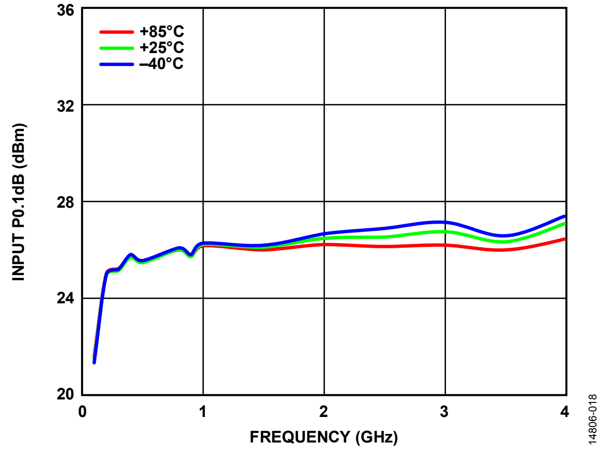


Figure 18. Input P0.1dB vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 3 V

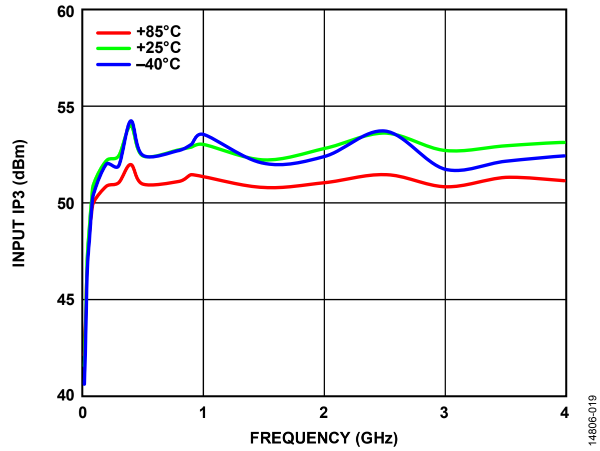


Figure 19. Input IP3 vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 3 V

THEORY OF OPERATION

The HMC470A incorporates a 5-bit attenuator that offers an attenuation range of 31 dB in 1 dB steps and a driver for CMOS-/TTL-compatible parallel control of the 5-bit attenuator. See Table 5 for the truth table.

Table 5. P4 to P0 Truth Table

Digital Control Input[1]					Attenuation
V1	**V2**	**V3**	**V4**	**V5**	**State (dB)**
High	High	High	High	High	0 dB (reference)
High	High	High	High	Low	1 dB
High	High	High	Low	High	2 dB
High	High	Low	High	High	4 dB
High	Low	High	High	High	8 dB
Low	High	High	High	High	16 dB
Low	Low	Low	Low	Low	31 dB

[1] Any combination of the control voltage input states shown in Table 5 provides an attenuation equal to the sum of the bits selected.

POWER SUPPLY

The HMC470A requires a single supply voltage applied to the VDD pin, and CMOS/TTL-compatible control voltages applied to the V1 to V5 pins. The ideal power-up sequence is as follows:

1. Connect the ground reference.
2. Power up VDD and VSS. The relative order is not important.
3. Apply the digital control inputs. The relative order of the digital control inputs is not important.
4. Apply an RF input signal to RF1 or RF2.

The power-down sequence is the reverse of the power-up sequence.

RF INPUT AND OUTPUT

The HMC470A is bidirectional. The RF1 and RF2 pins are internally matched to 50 Ω; therefore, they do not require external matching components. These pins are dc-coupled to VDD; therefore, dc blocking capacitors are required on RF lines.

ACGx PINS

The HMC470A is a positive bias GaAs attenuator so it requires floating capacitors between the attenuator bits and ground. The HMC470A uses on-chip floating capacitors that are sufficient for operation at frequencies greater than 700 MHz. The HMC470A also features the ACGx pins to externally connect larger floating capacitors. Select the value of external floating capacitors based on the minimum operating frequency, whereas the ACGx pins can be left open when operating above 700 MHz.

APPLICATIONS INFORMATION

EVALUATION BOARD

The HMC470A uses a 4-layer evaluation board. The copper thickness is 0.5 oz (0.7 mil) on each layer. The top dielectric material is 10 mil Rogers RO4350 for optimal high frequency performance, whereas the middle and bottom dielectric materials are FR-4 type materials to achieve an overall board thickness of 62 mil. RF and DC traces are routed on the top copper layer. The bottom and middle layers are grounded planes that provide a solid ground for the RF transmission lines. The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 16 mil and ground spacing of 13 mil to have a characteristic impedance of 50 Ω. For enhanced RF and thermal grounding, as many plated through vias as possible are arranged around transmission lines and under the exposed pad of the package.

Figure 20 shows the top view of the populated HMC470A Evaluation board, available from Analog Devices, Inc., upon request (see the Ordering Guide).

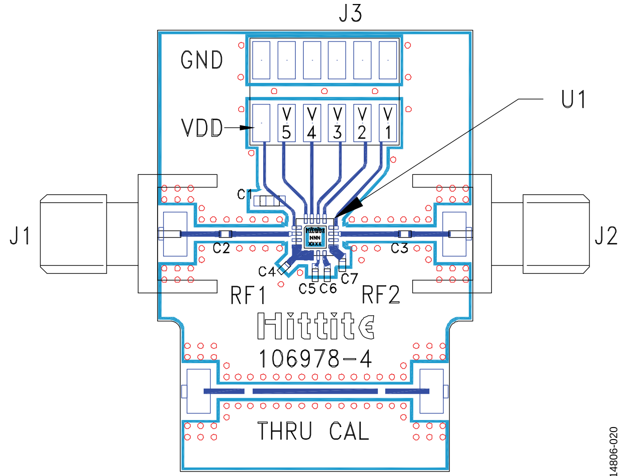


Figure 20. Populated Evaluation Board – Top View

The evaluation board is grounded from the 2 × 6-pin header, J3. The supply and digital control pins are also connected to the J3. A 1 nF decoupling capacitor is placed on the supply trace to filter high frequency noise.

The RF1 and RF2 ports are connected through 50 Ω transmission lines to the SMA connectors, J1 and J2, respectively. The RF1 and RF2 ports are ac-coupled with external 330 pF capacitors. A thru calibration line connects J9 and J10; this transmission line is used to measure the loss of the PCB over the environmental conditions being evaluated.

The ACG pins are connected to ground through 330 pF capacitors.

Figure 21 and Table 6 show the evaluation board schematic and bill of materials, respectively.

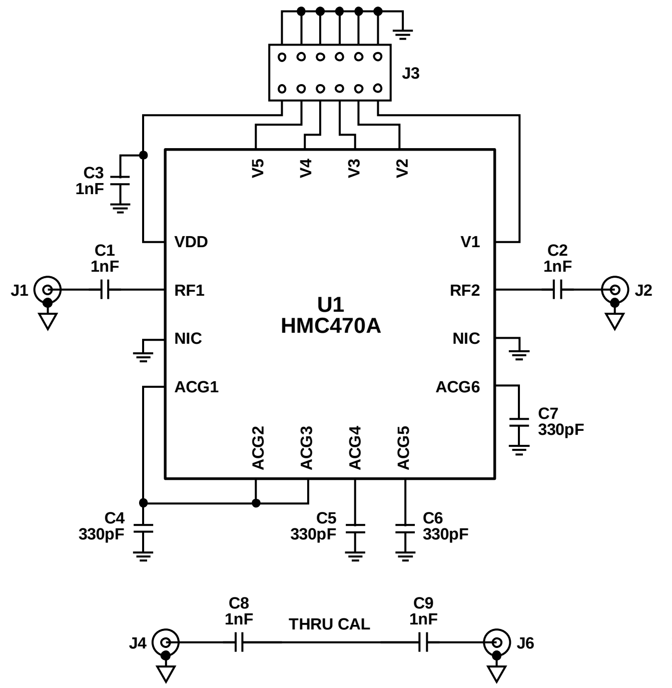
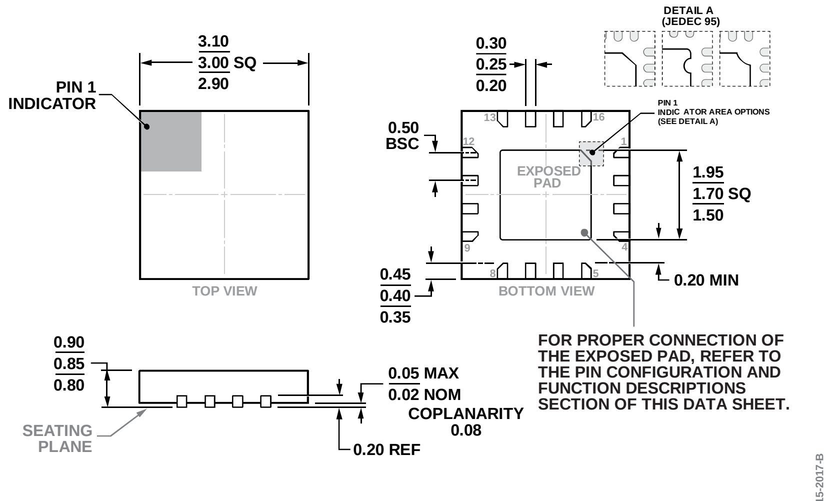


Figure 21. Evaluation Board Schematic

Table 6. List of Materials for EVAL-HMC470A

Item	Description
J1, J2	PCB mount, SMA connector
J3,	2 × 6-pin header
J4, J5	PCB mount, 2.9mm RF connector, do not insert
C1, C2	1 nF capacitor, 0402 package
C3	1 nF capacitor, 0603package
C4 to C7	330 pF capacitor, 0402 package
C8, C9	1 nF capacitor, 0402 package, do not insert
U1	HMC470A Digital Attenuator
PCB	106978-4 Evaluation PCB

OUTLINE DIMENSIONS



COMPLIANT WITH JEDEC STANDARDS MO-220-VEED-4.

Figure 22. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.85 mm Package Height
(HCP-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option	Branding[3]
HMC470ALP3E	−40°C to +85°C	MSL3	16-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-16-1	H470A XXXX
HMC470ALP3ETR	−40°C to +85°C	MSL3	16-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-16-1	H470A XXXX
EV1HMC470ALP3			Evaluation Board		

[1] All models are RoHS Compliant.
[2] See the Absolute Maximum Ratings section.
[3] XXXX is the 4-digit lot number.

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