

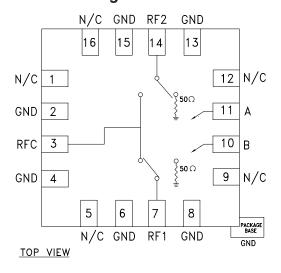
# GaAs MMIC SPDT NON-REFLECTIVE SWITCH, DC - 20 GHz

## Typical Applications

The HMC547ALP3E is ideal for:

- Basestation Infrastructure
- Fiber Optics & Broadband Telecom
- Microwave Radio & VSAT
- · Military Radios, Radar, & ECM
- Test Instrumentation

## **Functional Diagram**



#### **Features**

High Isolation: >50 dB up to 5 GHz

>40 dB up to 15 GHz

Low Insertion Loss: 1.8 dB @ 10 GHz

2.5 dB @ 20 GHz

Fast Switching

Non-Reflective Design

QFN SMT Package, 9 mm<sup>2</sup>

## **General Description**

The HMC547ALP3E is a general purpose broadband high isolation non-reflective GaAs pHEMT SPDT switch in low cost leadless QFN surface mount plastic package. Covering DC to 20 GHz, the switch offers high isolation and low insertion loss. The switch features >50 dB isolation up to 5 GHz and >40 dB isolation up to 15 GHz. The switch operates using complementary negative control voltage logic lines of -5/0V and requires no bias supply. The HMC547ALP3E are packaged in leadless QFN 3x3 mm surface mount packages.

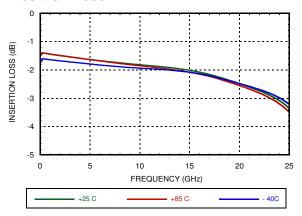
## Electrical Specifications, $T_A = +25^{\circ}$ C, With 0/-5V Control, 50 Ohm System

Paramete	er	Frequency	Min.	Тур.	Max.	Units
Insertion Loss		DC - 6.0 GHz DC - 10.0 GHz DC - 15.0 GHz DC - 20.0 GHz		1.7 1.8 2.0 2.5	2.1 2.2 2.4 3.0	dB dB dB dB
Isolation		DC - 6.0 GHz DC - 15.0 GHz DC - 20.0 GHz	43 35 31	48 40 36		dB dB dB
Return Loss RFC	"On State"	DC - 6.0 GHz DC - 20 GHz		17 15		dB dB
Return Loss RF1, RF2	"Off State"	DC - 6.0 GHz DC - 15.0 GHz DC - 20.0 GHz		26 17 11		dB dB dB
Input Power for 1 dB Compression		0.5 - 20.0 GHz	24	29		dBm
Input Third Order Intercept (Two-Tone Input Power= +7 dBm Each Tone)		0.5 - 10.0 GHz 0.5 - 20.0 GHz		47 45		dBm dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)		DC - 20 GHz		2 10		ns ns

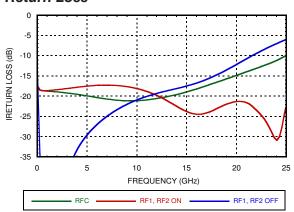


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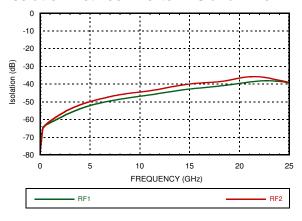
#### **Insertion Loss**



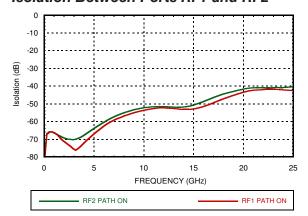
#### **Return Loss**



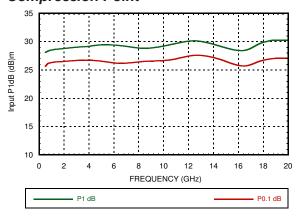
#### Isolation Between Ports RFC and RF1/RF2



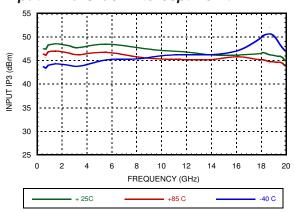
#### Isolation Between Ports RF1 and RF2



# Input P1dB and P0.1dB Compression Point



### Input Third Order Intercept Point





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## **Absolute Maximum Ratings**

RF Input Power (Vctl = -5V)	+30 dBm
Control Voltage Range (A & B)	+0.5V to -7.5 V
Hot Switch Power Level (Vctl = -5V)	+23 dBm
Channel Temperature	150 °C
Terminated Power Level (Vctl =-5V)	+25dBm
Thermal Resistance (Insertion Loss Path)	118 °C/W
Thermal Resistance (Terminated Path)	200 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

## **Control Voltages**

State	Bias Condition	
Low	0 to -0.2V @ 10 uA Max.	
High	-5V @ 3uA Typ. to -7V @ 40 uA Max. (± 0.5 Vdc)	

## **Truth Table**

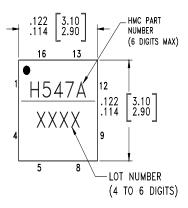
Control Input		Signal Path State		
Α	В	RFC to RF1	RFC to RF2	
High	Low	On	Off	
Low	High	Off	On	

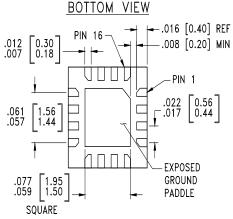


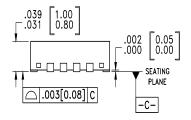


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## **Outline Drawing**







#### NOTES:

- 1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
- 2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
- 3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
- 4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
- 5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
- 6. CHARACTERS TO BE HELYETICA MEDIUM, .018 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
- 7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.
- 8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
- 9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
- 10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.
- 11. UNDERLINE THE LOT NUMBER TO DESIGNATE 2000A FIRST LAYER NITRIDE DIE FAB OPTION AS SPECIFIED BY THE PO

## Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC547ALP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL3 [1]	<u>H547A</u> XXXX

<sup>[1]</sup> Max peak reflow temperature of 260  $^{\circ}\text{C}$ 

<sup>[2] 4-</sup>Digit lot number XXXX

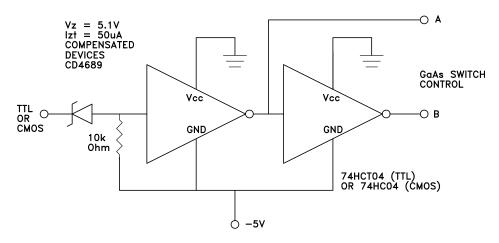


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## **Pin Descriptions**

Pin Number	Function	Description	Interface Schematic
1, 5, 9, 12, 16	N/C	This pin should be connected to PCB RF ground to maximize isolation	
2, 4, 6, 8, 13, 15	GND	Package bottom has exposed metal paddle that must also be connected to PCB RF ground.	⊖ GND =
3, 7, 14	RFC, RF1, RF2	This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required if RF line potential is not equal to 0V.	
10	В	See truth table and control voltage table.	R
11	А	See truth table and control voltage table.	c 

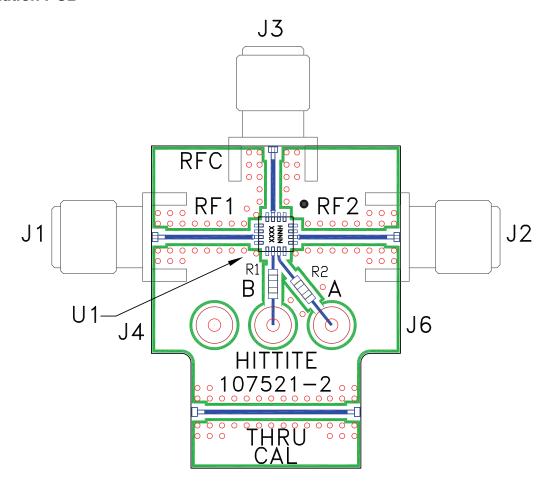
## **Suggested Driver Circuit**





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#### **Evaluation PCB**



### List of Materials for Evaluation EV1HMC547ALP3

Item	Description
J1 - J3	PCB Mount SRI SMA Connector
J4 - J6	DC Pin
R1 - R2	100 Ohm Resistor, 0603 Pkg.
U1	HMC547ALP3E SPDT Switch
PCB [2]	107521 Evaluation PCB

<sup>[1]</sup> Reference this number when ordering complete evaluation PCB

The circuit board used in the application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 Ohm impedance and the package ground leads and package bottom should be connected directly to the ground plane similar to that shown above. The evaluation circuit board shown above is available from Analog Devices Inc. upon request.

<sup>[2]</sup> Circuit Board Material: Rogers 4350

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