# HMC642

v00.0607

## GaAs MMIC 6-BIT DIGITAL PHASE SHIFTER, 9 - 12.5 GHz

### Typical Applications

The HMC642 is ideal for:

- EW Receivers
- Weather & Military Radar
- Satellite Communications
- Beamforming Modules
- Phase Cancellation

### Features

Low RMS Phase Error: 2.5°

Low Insertion Loss: 6.5 dB

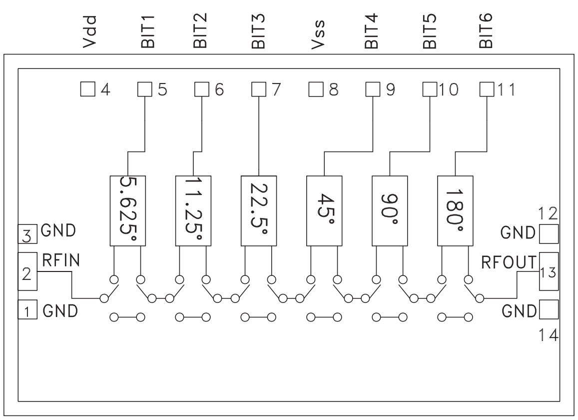
High Linearity: +41 dBm

Positive Control Voltage

360° Coverage, LSB = 5.625°

Die Size: 3.25 x 1.9 x 0.1 mm

### Functional Diagram




### General Description

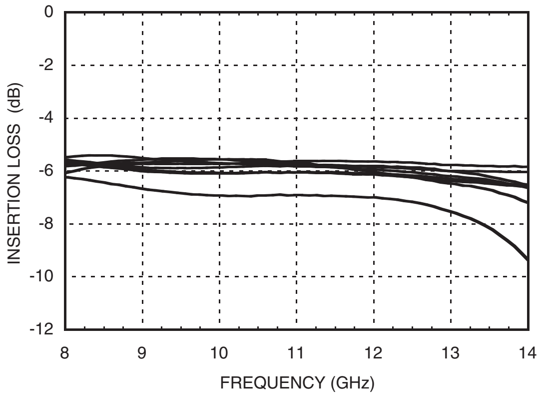
The HMC642 is a 6-bit digital phase shifter die which is rated from 9 to 12.5 GHz, providing 360 degrees of phase coverage, with a LSB of 5.625 degrees. The HMC642 features very low RMS phase error of 2.5 degrees and extremely low insertion loss variation of ±0.25 dB across all phase states. This high accuracy phase shifter is controlled with positive control logic of 0/+5V, and is internally matched to 50 Ohms with no external components.

### Electrical Specifications, $T_A$ = +25° C, Vee= -5V, Vdd= +5V, Control Voltage = 0/+5V, 50 Ohm System

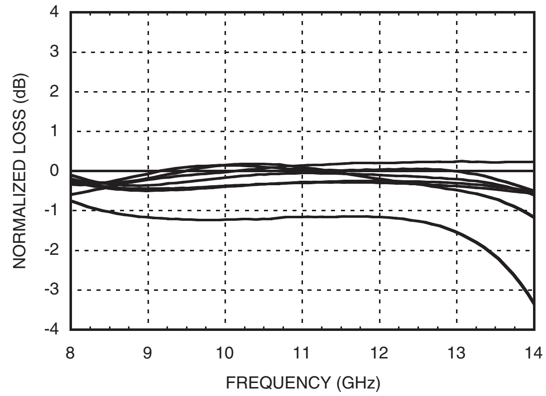
| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Frequency Range | 9 | | 12.5 | GHz |
| Insertion Loss* | | 6.5 | 8.5 | dB |
| Input Return Loss* | | 13 | | dB |
| Output Return Loss* | | 12 | | dB |
| Phase Error* | | ±5 | +15 / -8 | deg |
| RMS Phase Error | | 2.5 | | deg |
| Insertion Loss Variation* | | ±0.25 | | dB |
| Input Power for 1 dB Compression | | 28 | | dBm |
| Input Third Order Intercept | | 41 | | dBm |
| Control Voltage Current | | <250 | | μA |
| Bias Control Current | | <12 | | mA |

*Note: Major States Shown

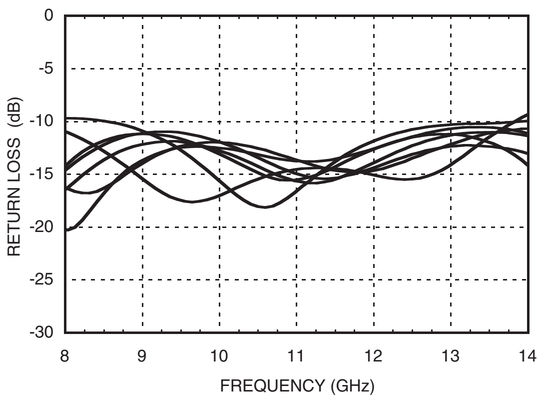
### Insertion Loss, Major States Only



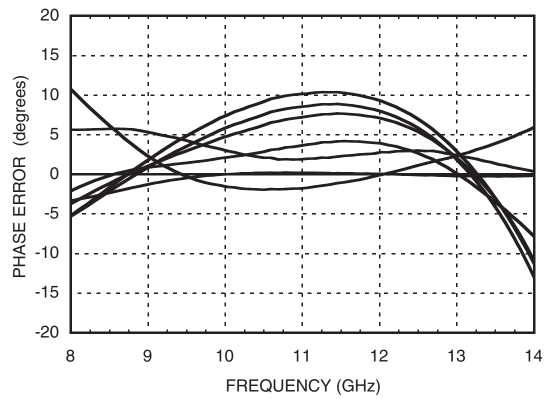

### Normalized Loss, Major States Only



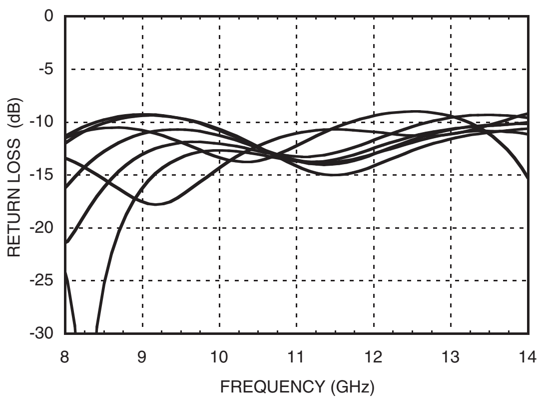

### Input Return Loss, Major States Only



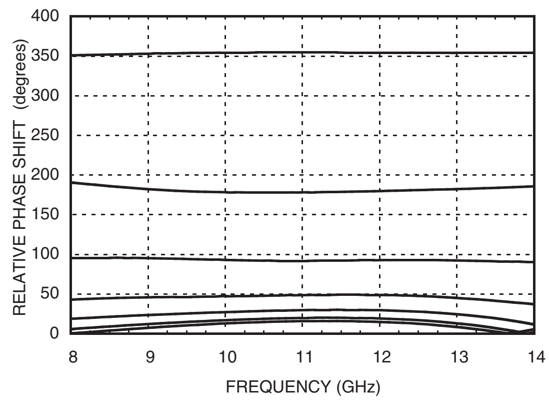

### Phase Error, Major States Only




### Output Return Loss, Major States Only




### Relative Phase Shift Major States, Including All Bits



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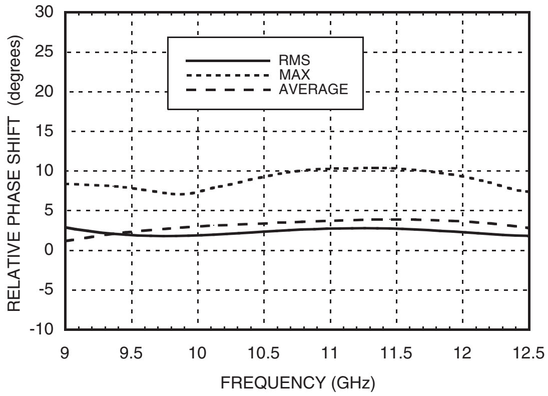
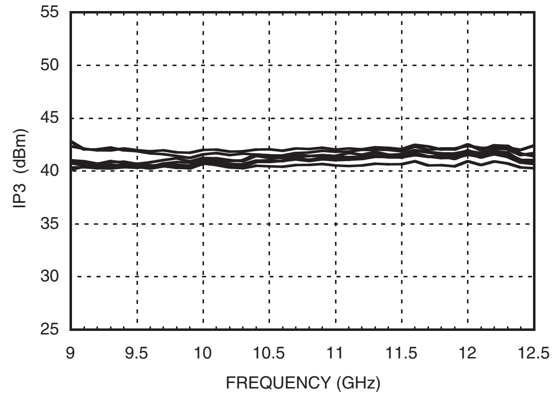
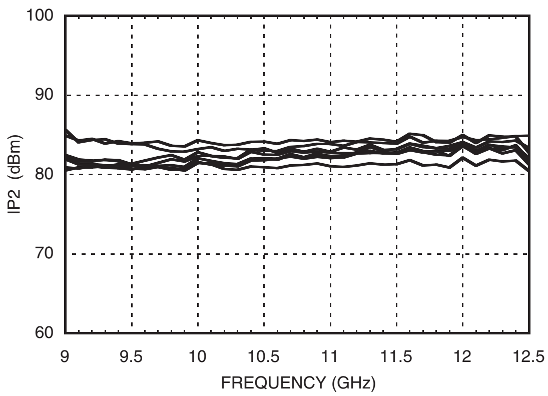
### Relative Phase Shift, RMS, Average, Max, All States



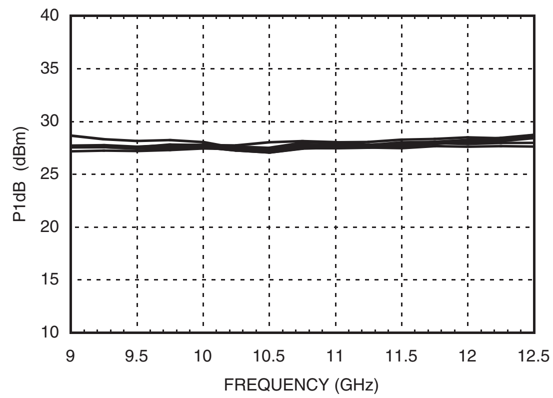

### Input IP3, Major States Only



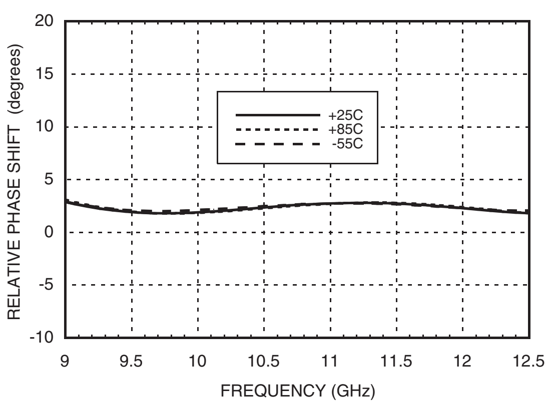

### Input IP2, Major States Only



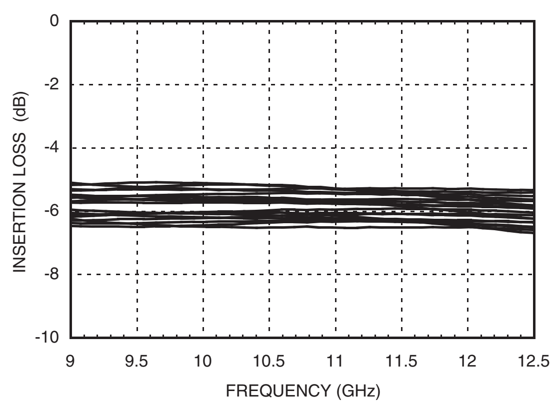

### Input P1dB, Major States Only




### RMS Phase Error vs. Temperature




### Insertion Loss vs. Temperature, Major States Only



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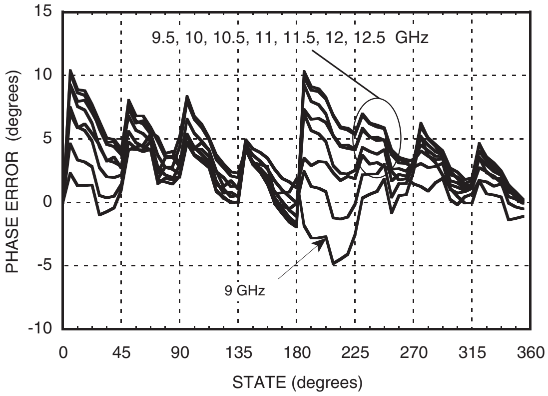
## GaAs MMIC 6-BIT DIGITAL PHASE SHIFTER, 9 - 12.5 GHz



### Phase Error vs. State




### Absolute Maximum Ratings

| | |
|---|---|
| Input Power (RFIN) | 30 dBm (T= +85 °C) |
| Bias Voltage Range (Vdd) | -0.2 to +12V |
| Bias Voltage Range (Vss) | +0.2 to -12V |
| Channel Temperature (Tc) | 150 °C |
| Thermal Resistance (channel to die bottom) | 60 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -55 to +85 °C |

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

### Truth Table

| Control Voltage Input | | | | | | Phase Shift (Degrees) RFIN - RFOUT |
|---|---|---|---|---|---|---|
| Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | |
| 0 | 0 | 0 | 0 | 0 | 0 | Reference* |
| 1 | 0 | 0 | 0 | 0 | 0 | 5.625 |
| 0 | 1 | 0 | 0 | 0 | 0 | 11.25 |
| 0 | 0 | 1 | 0 | 0 | 0 | 22.5 |
| 0 | 0 | 0 | 1 | 0 | 0 | 45.0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 90.0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 180.0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 354.375 |

Any combination of the above states will provide a phase shift approximately equal to the sum of the bits selected.

*Reference corresponds to monotonic setting

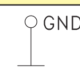
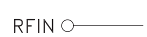
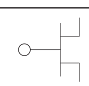
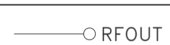
### Bias Voltage & Current

| Vdd | Idd |
|---|---|
| 5.0 | 5.6mA |
| Vss | Iss |
| -5.0 | 5.6mA |

### Control Voltage

| State | Bias Condition |
|---|---|
| Low (0) | 0 to 0.2 Vdc |
| High (1) | Vdd ±0.2 Vdc @ 35 µA Typ. |

### Pad Descriptions

| Pad Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1, 3, 12, 14 | GND | These pads and die bottom must be connected to RF/DC ground. |  |
| 2 | RFIN | This port is DC coupled and matched to 50 Ohms. |  |
| 4 | Vdd | Voltage supply. | |
| 5 - 7, 9 - 11 | BIT1, BIT2, BIT3, BIT4, BIT5. BIT6 | Control Input. See truth table and control voltage tables. |  |
| 8 | Vss | Voltage supply. | |
| 13 | RFOUT | This port is DC coupled and matched to 50 Ohms. |  |



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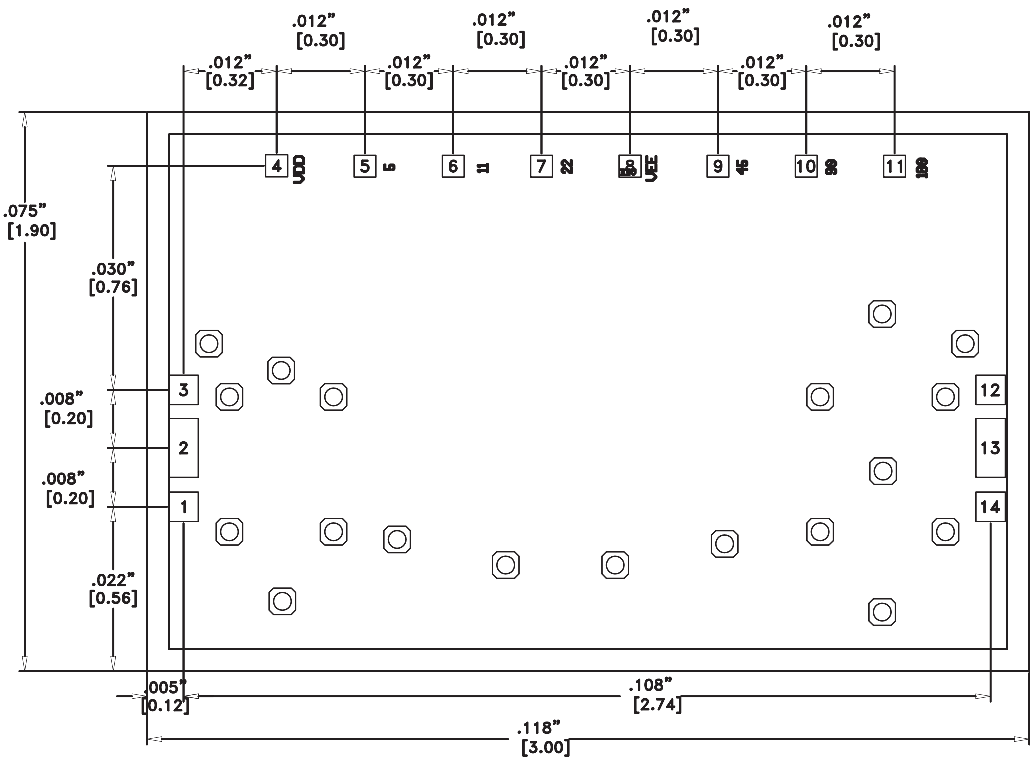
### Outline Drawing




### Die Packaging Information [1]

| Standard | Alternate |
|---|---|
| GP-1 (Gel Pack) | [2] |

*[1] Refer to the "Packaging Information" section for die packaging dimensions.*
*[2] For alternate packaging information contact Hittite Microwave Corporation.*

NOTES:
1. ALL DIMENSIONS IN INCHES (MILLIMETERS)
2. DIE THICKNESS IS 0.004
3. BACKSIDE METALLIZATION: GOLD
4. BACKSIDE METAL IS GROUND
5. BOND PADS METALLIZATION: GOLD
6. OVERALL DIE SIZE ±0.002



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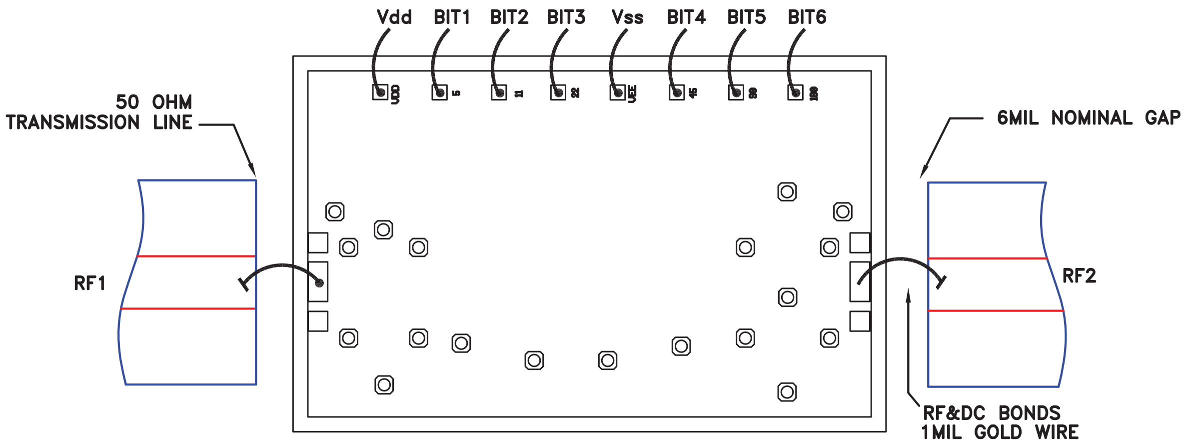
## Assembly Diagram




## Handling Precautions

*Follow these precautions to avoid permanent damage.*

**Storage:** All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

**Cleanliness:** Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

**Static Sensitivity:** Follow ESD precautions to protect against > ± 250V ESD strikes.

**Transients:** Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

**General Handling:** Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

## Mounting

*The chip is back-metallized and can be die mounted with electrically conductive epoxy. The mounting surface should be clean and flat.*

**Epoxy Die Attach:** Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

## Wire Bonding

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 deg. C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31mm (12 mils).



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