

20 dB GaAs MMIC 1-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 10 GHz

Typical Applications

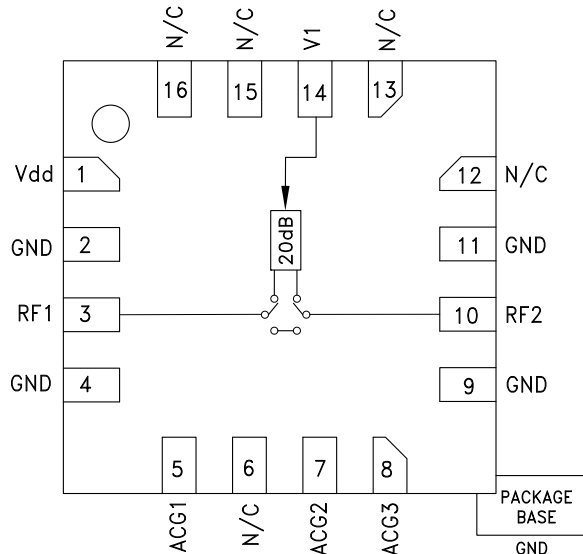
The HMC802ALP3E is ideal for both RF and IF applications:

- Test Equipment and Sensors
- ISM, MMDS, WLAN, WiMAX, WiBro
- Microwave Radio & VSAT
- Cellular Infrastructure

Features

- ± 0.6 dB Typical Step Error
- Low Insertion Loss: 3 dB
- High IP3: +55 dBm
- Single Control Line
- TTL/CMOS Compatible Control
- Single +5V Supply
- 16 Lead 3x3mm SMT Package: 9mm²

Functional Diagram



General Description

The HMC802ALP3E is a broadband bidirectional 1-bit GaAs IC digital attenuator in a low cost leadless surface mount package. This single positive control line digital attenuator utilizes off chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. Covering DC to 10 GHz, the insertion loss is less than 3 dB typical and attenuation accuracy is excellent at ±0.6 dB typical. The attenuator also features a high IIP3 of +55 dBm. One TTL/CMOS control input is used to select the attenuation state and a single Vdd bias of +5V is required.

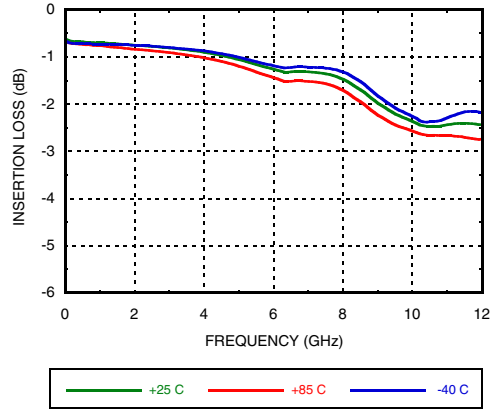
Electrical Specifications, $T_A = +25^\circ\text{C}$, With $V_{dd} = +5V$ & $V_{ctl} = 0/+5V$

| Parameter | Frequency (GHz) | Min. | Typ. | Max. | Units |
|--|-----------------|------|----------------------------------|------|-------|
| Insertion Loss | DC - 4 GHz | | 0.9 | 1.7 | dB |
| | 4 - 8 GHz | | 1.5 | 2.8 | dB |
| | 8 - 10 GHz | | 2.5 | 3.5 | dB |
| Attenuation Range | DC - 10 GHz | | 20 | | dB |
| Return Loss (RF1 & RF2, Both States) | DC - 6 GHz | | 25 | | dB |
| | 6 - 10 GHz | | 15 | | dB |
| Attenuation Accuracy: (Referenced to Insertion Loss) ¹ | DC - 6 GHz | -1.0 | -0.6/+0.5 | +0.6 | dB |
| | 6 - 8 GHz | -2.0 | -1.6/+0.5 | +0.6 | dB |
| | 8 - 10 GHz | -2.6 | -2.3/+0.8 | +1.2 | dB |
| Input Power for 0.1 dB Compression | DC - 10 GHz | | 27 | | dBm |
| Input Third Order Intercept Point (Two-Tone Input Power= 14 dBm Each Tone) | DC - 10 GHz | | 55 | | dBm |
| Switching Characteristics | DC - 10 GHz | | tRISE, tFALL (10/90% RF) | 70 | ns |
| | | | tON, tOFF (50% CTL to 10/90% RF) | 90 | ns |
| | | | | | |

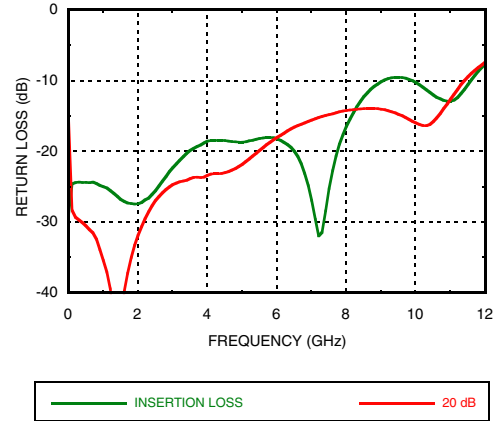
1. STEP SIZE IS 20DB FOR ALL FREQUENCY

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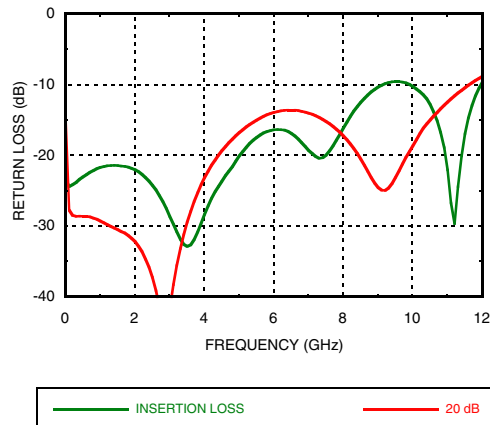
Insertion Loss



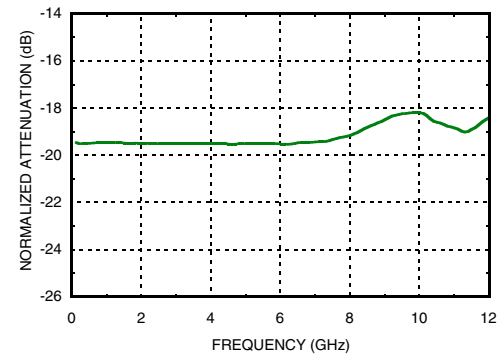
Input Return Loss



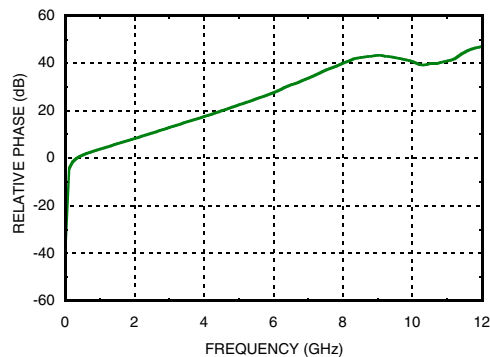
Output Return Loss



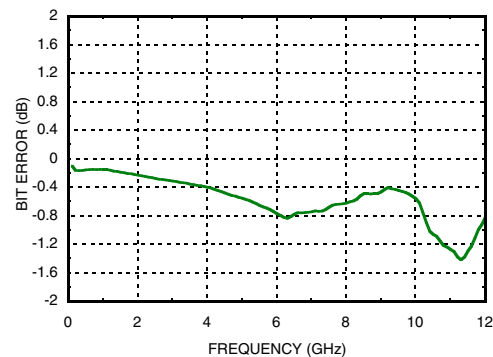
Relative Attenuation



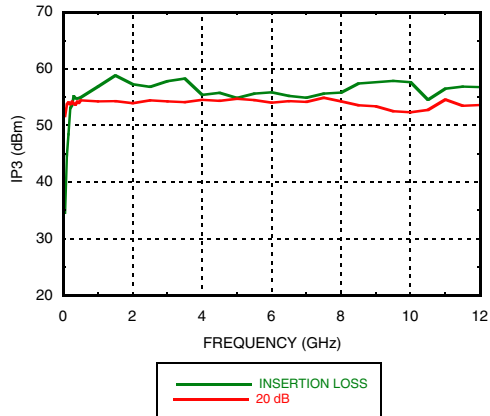
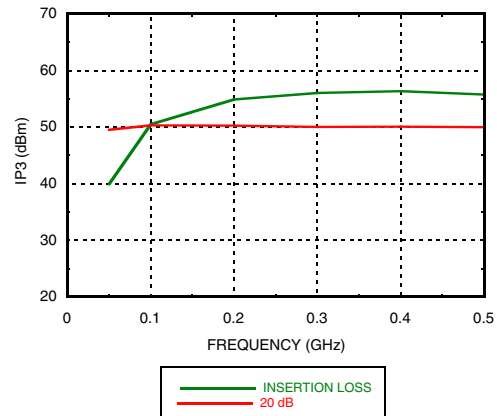
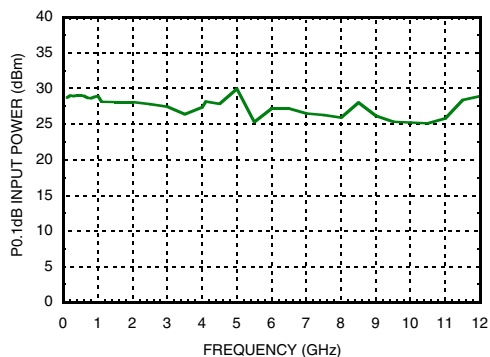
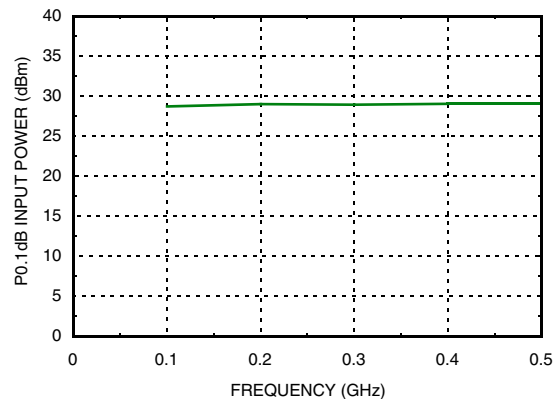
Relative Phase vs. Frequency



Bit Error vs. Frequency



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Input IP3 vs. Frequency

Input IP3 vs. Frequency (Low Frequency Detail)

Input Power for 1 dB Compression

Input Power for 0.1 dB Compression (Low Frequency Detail)

Truth Table

| Control Voltage Input | Attenuation State RF1 - RF2 |
|-----------------------|--------------------------------|
| V1 | |
| High | Reference Insertion Loss |
| Low | 20 dB |

Bias Voltage & Current

| Vdd = +5 Vdc ± 10% | |
|--------------------|-----------------|
| Vdd (Vdc) | Idd (Typ.) (mA) |
| 4.5 | 0.32 |
| 5.0 | 0.33 |
| 5.5 | 0.34 |

Control Voltage

| State | Bias Condition |
|-------|------------------------------|
| Low | 0 to +0.8V @ -1 μ A Typ. |
| High | +2 to +5V @ 30 μ A Typ. |

Note: Vdd = +5V

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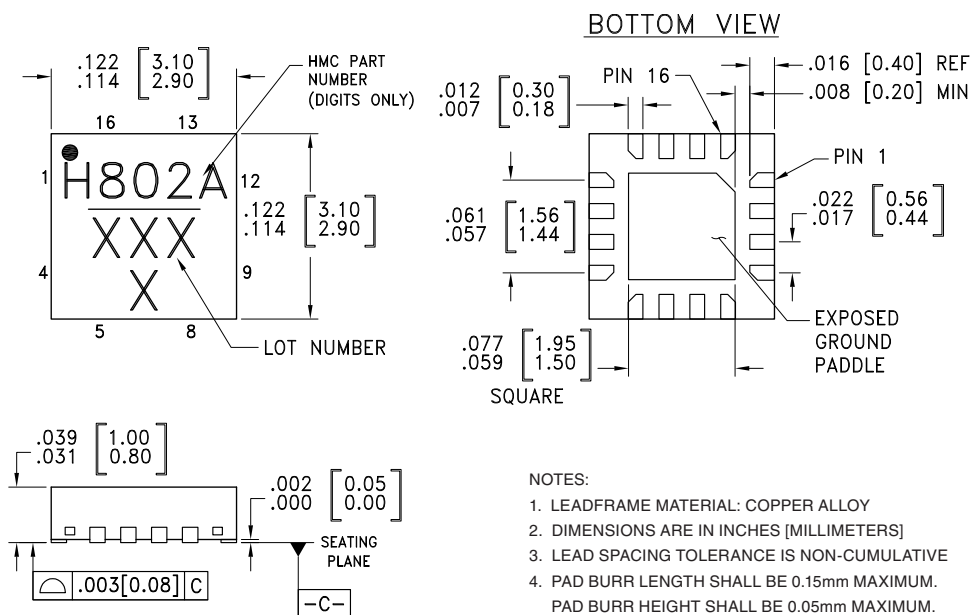
Absolute Maximum Ratings

| | |
|---|----------------|
| RF Input Power (DC - 10 GHz) | +29.3 dBm |
| Control Voltage Range (V1) | -1 to Vdd + 1V |
| Bias Voltage (Vdd) | +7 Vdc |
| Channel Temperature | 150 °C |
| Continuous P _{diss} (T = 85 °C) (derate 12 mW/°C above 85 °C) | 0.84 W |
| Thermal Resistance (channel to ground paddle) | 77.4 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |
| ESD Sensitivity (HBM) | Class 1A |



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

- LEADFRAME MATERIAL: COPPER ALLOY
- DIMENSIONS ARE IN INCHES [MILLIMETERS]
- LEAD SPACING TOLERANCE IS NON-CUMULATIVE
- PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.
PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
- PACKAGE WARP SHALL NOT EXCEED 0.05mm.
- ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
- REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information


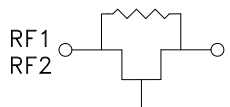
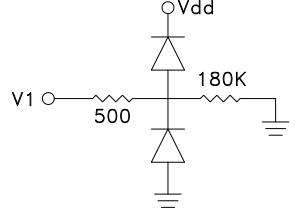
| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[2] |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC802ALP3E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL3 ^[1] | H802A XXXX |

[1] Max peak reflow temperature of 260 °C

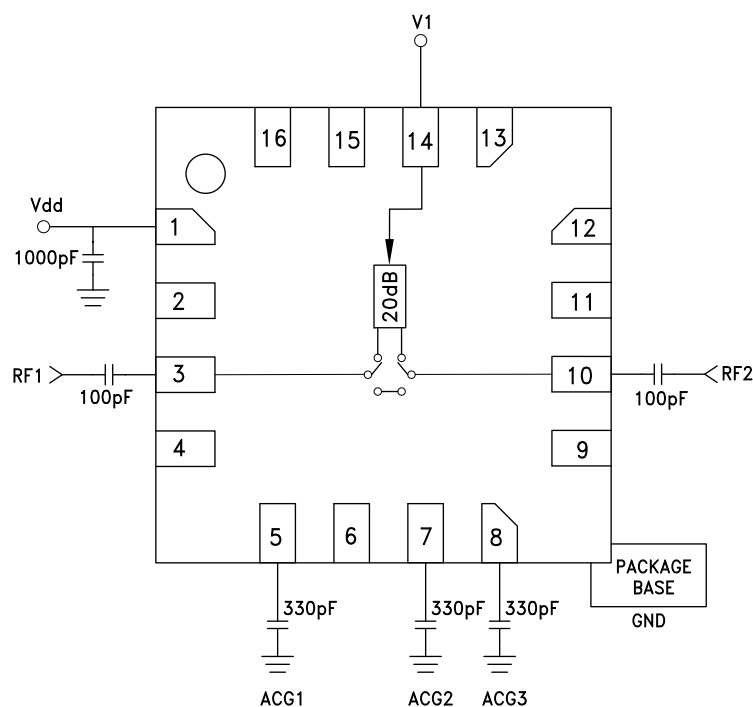
[2] 4-Digit lot number XXXX

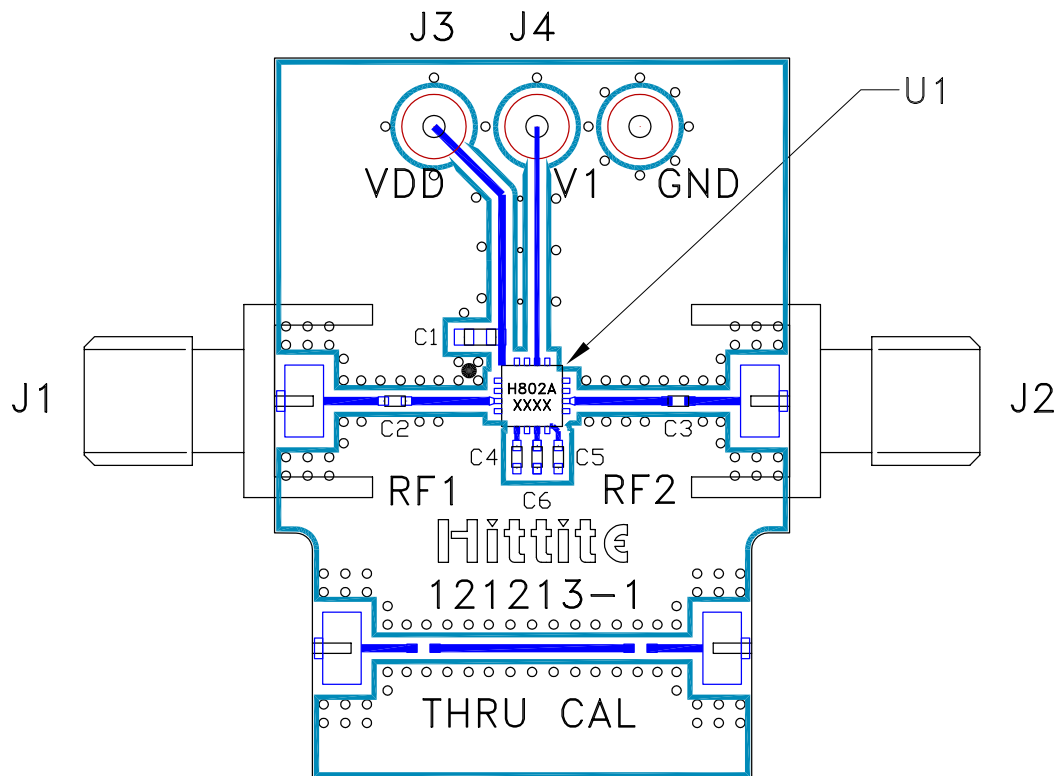
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Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|-------------------|------------------|--|--|
| 1 | Vdd | Supply Voltage. | |
| 2, 4, 9, 11 | GND | These pins and the exposed ground paddle must be connected to RF/DC ground. |  |
| 3, 10 | RF1, RF2 | These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation. |  |
| 5, 7, 8 | ACG1, ACG2, ACG3 | External capacitor to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible. | |
| 6, 12, 13, 15, 16 | N/C | The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally. | |
| 14 | V1 | See truth table and control voltage table. |  |

Application Circuit



**20 dB GaAs MMIC 1-BIT DIGITAL
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Evaluation PCB

List of Materials for Evaluation PCB EV1HMC802ALP3 [1]

| Item | Description |
|---------|--------------------------------|
| J1, J2 | PCB Mount SMA Connector |
| J3, J4 | DC Connector |
| C1 | 1000 pF Capacitor, 0603 Pkg. |
| C2, C3 | 100 pF Capacitor, 0402 Pkg. |
| C4 - C6 | 330 pF Capacitor, 0402 Pkg. |
| U1 | HMC802ALP3E Digital Attenuator |
| PCB [2] | 121213 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices Inc. upon request.

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