EV-21569-SOM ® Manual

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ANALOG DEVICES

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Regulatory Compliance

The *EV-21569-SOM* evaluation board is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer-end product or as a portion of a consumer-end product. The board is an open system design, which does not include a shielded enclosure and, therefore, may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The *EV-21569-SOM* evaluation board contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused boards in the protective shipping package.	

Contents

1 Preface

Thank you for purchasing the Analog Devices, Inc. System-on-Module (SoM) *EV-21569-SOM* evaluation board.

The *EV-21569-SOM* primarily hosts the ADSP-21569 audio processor, 8 Gbit of ISSI DDR3 memory, a 512 Mbit Quad SPI FLASH, voltage regulation, a FTDI UART to USB interface, and a high speed external connector array that contains all of the peripheral I/O signals. Through the high speed external connector array, the *EV-21569-SOM* is intended for use with a growing family of SoM carrier products that contain a variety of peripherals to support different applications. The SoM carrier base products that exist today are the *EV-SOMCRR-EZKIT* and *EV-SOMCRR-AUTO* .

The CrossCore Embedded Studio® (CCES) software development tool chain is required for a full evaluation of this hardware platform. The *EV-21569-SOM* can also be used in a limited standalone mode while not plugged into a SoM Carrier such as the *EV-SOMCRR-EZKIT* or *EV-SOMCRR-AUTO* . The standalone mode is useful for evaluating the CCES Software Development Tools and benchmarking software algorithms that do not require peripheral I/O.

The evaluation board is designed to be used in conjunction with the CCES 2.9.3 (or newer) development environment for advanced application code development and debug, with features that enable the ability to:

- Create, compile, assemble, and link application programs written in C++, C, and assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers

Purpose of This Manual

This manual provides instructions for installing the product hardware (board). This manual describes operation and configuration of the board components and provides guidelines for running code on the board.

Manual Contents

The manual consists of:

- ***Using the board***

Provides basic board information.

- *Hardware Reference*

  Provides information about the hardware aspects of the board.

- *Bill of Materials*

  A companion file in PDF format that lists all of the components used on the board is available on the website at http://www.analog.com/EV-21569-SOM .

- *Schematic*

  A companion file in PDF format documenting all of the circuits used on the board is available on the website at http://www.analog.com/EV-21569-SOM .

Technical Support

You can reach Analog Devices technical support in one of the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:

  http://ez.analog.com/community/dsp

- Submit your questions to technical support directly at:

  http://www.analog.com/support

- E-mail your questions about processors, DSPs, and tools development software from ***CrossCore Embedded Studio*** or ***VisualDSP++***®:

  If using CrossCore Embedded Studio or VisualDSP++ choose ***Help > Email Support***. This creates an e-mail to processor.tools.support@analog.com and automatically attaches your CrossCore Embedded Studio or VisualDSP++ version information and `license.dat` file.

- E-mail your questions about processors and processor applications to:

  processor.support@analog.com

  processor.china@analog.com

- Contact your Analog Devices sales office or authorized distributor. Locate one at:

  http://www.analog.com/adi-sales

Supported Integrated Circuit

This evaluation system supports the Analog Devices ADSP-21569 IC.

Supported Tools

Information about code development tools for the *EV-21569-SOM* evaluation board and ADSP-2156x product family is available at:

http://www.analog.com/EV-21569-SOM

Product Information

Product information can be obtained from the Analog Devices website and the online help system.

Analog Devices Website

The Analog Devices website, http://www.analog.com, provides information about a broad range of products - analog integrated circuits, amplifiers, converters, transceivers, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, MyAnalog.com is a free feature of the Analog Devices website that allows customization of a web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the web pages that meet your interests, including documentation errata against all manuals. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

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EngineerZone

EngineerZone is a technical support forum from Analog Devices, Inc. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

2 Using the Board

This chapter provides information on the major components and peripherals on the board, along with instructions for installing and setting up the emulation software.

Product Overview

Below is an image of the *EV-21569-SOM* board.

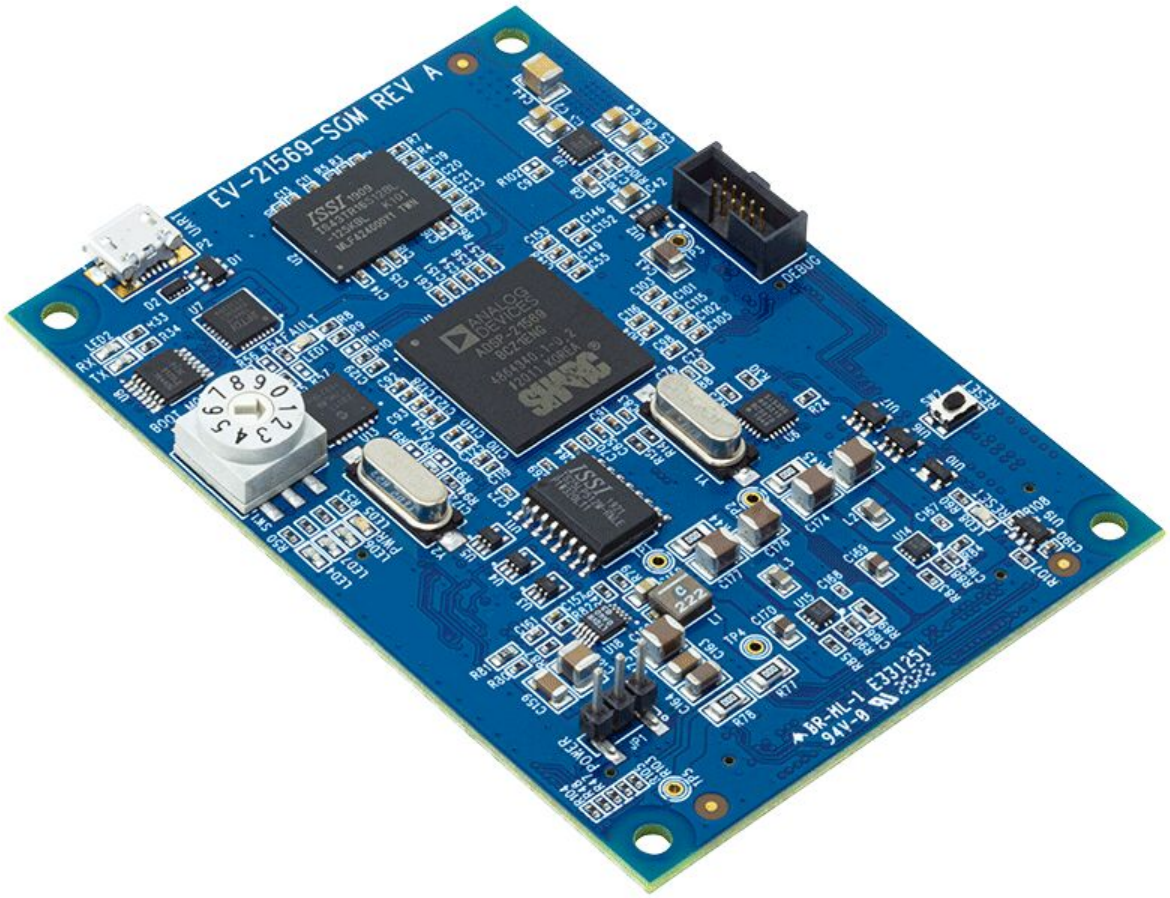

Figure 2-1: Board View

The board features:

- Analog Devices ADSP-21569 processor
  - 400 ball BGA
  - 25 MHz oscillator
- DDR3 Memory
  - 512Mx16 bit (8Gbit)
  - ISSI IS43TR16512BL-125KBL
  - 1.35V
- SPI Flash Quad (`SPI2`) Memory
  - 512Mbit
  - ISSI IS25LP512M - 512M-bit Serial Flash Memory with Dual and Quad SPI
  - Single/Dual/Quad SPI
- Debug Interface (JTAG)
  - JTAG 10-pin 0.05” header
- LEDs
  - 8 LEDs: one power (green), one board reset (red), three general-purpose (amber), one fault (red), and two UART LEDs (amber)
- Pushbuttons
  - One pushbutton, RESET
- SoM Interface Connector
  - DAI
  - SPORT
  - SPI
  - UART
  - TWI
  - Link Port
  - GPIO
  - MLB
  - `RESET`

- GND/3.3V/5V/12V output

Package Contents

Your *EV-21569-SOM* package contains the following items.

- *EV-21569-SOM* board

Contact the vendor where you purchased your *EV-21569-SOM* evaluation board or contact Analog Devices, Inc. if any item is missing.

Default Configuration

The *EV-21569-SOM* board is designed to run as a standalone unit.

The ***Default Hardware Setup*** figure shows the default settings for jumpers and switches and the location of the jumpers, switches, connectors, and LEDs. Confirm that your board is in the default configuration before using the board.

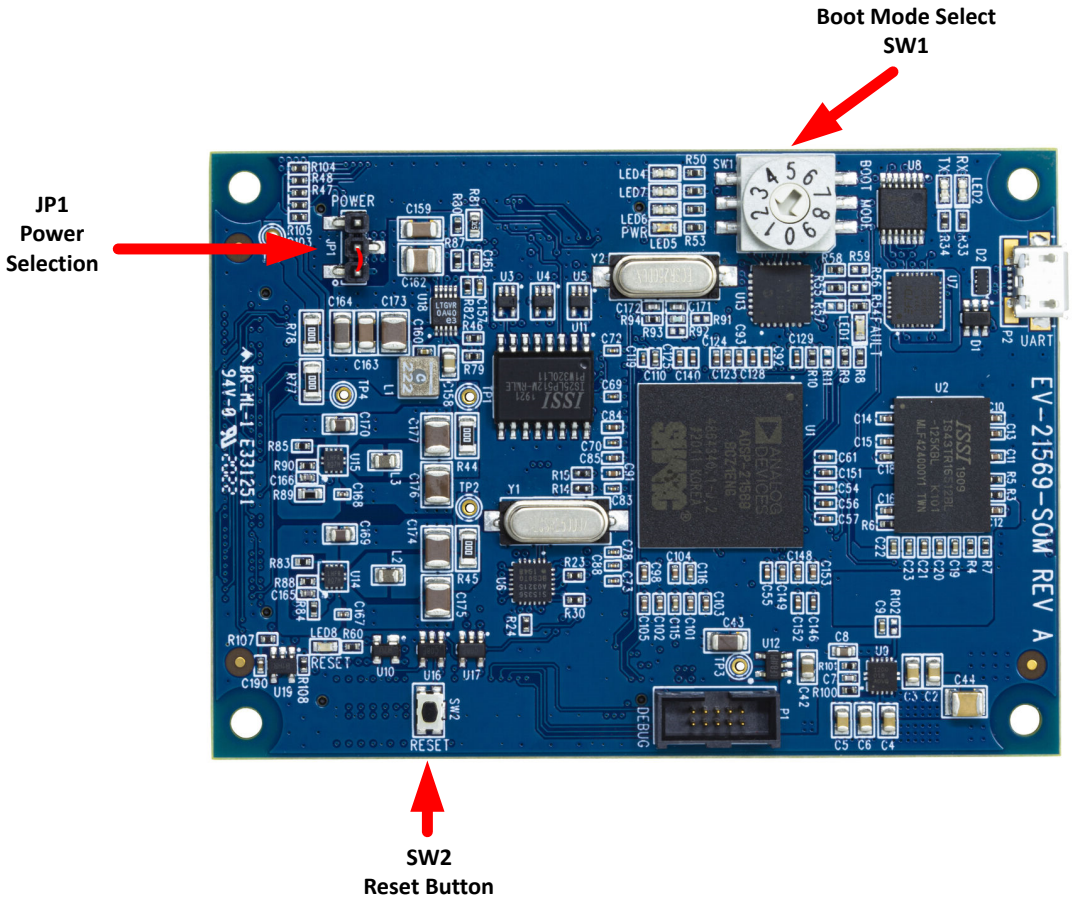

Figure 2-2: Default Hardware Setup

CrossCore Embedded Studio (CCES) Setup

Information on using the CCES tools is available at: https://analog.com/cces-quickstart

Debug Interface

The *EV-21569-SOM* provides a JTAG connection via `P1` . This is for attaching an emulator, such as the ICE-1000 or ICE-2000 to for debugging.

When the *EV-21569-SOM* is connected to a carrier board the Debug Agent on the carrier board can be used. To use this Debug Agent, all postions on SW1 (on the carrier board) must be in the ON position. If an emulator, such as the ICE-1000 or ICE-2000, is used instead all postions on SW1 must be in the OFF position.

Board Power

The *EV-21569-SOM* powered via `P2` when the board is in standalone mode. When in this mode the jumper on `JP1` should be on Pins 1-2 to select power input from `P2` . When the *EV-21569-SOM* is connected to a carrier board the power is supplied via the carrier board. When in this mode the jumper on `JP1` should be on Pins 2-3 to select power input from the carrier board.

Power-On-Self Test

The Power-On-Self-Test Program (POST) tests all the EZ-KIT carrier board peripherals and validates functionality as well as connectivity to the processor. Once assembled, each EZ-KIT carrier board is fully tested for an extended period of time with POST for all the compatible SoM modules. All EZ-KIT carrier boards are shipped with POST preloaded into flash memory. The POST is executed by resetting the board and connecting the USB To UART to your PC with an open terminal window. The POST also can be used as a reference for a custom software design or hardware troubleshooting.

Note that the source code for the POST program is included in the Board Support Package (BSP) along with the readme file that describes how the board is configured to run POST.

Example Programs

Example programs are provided with the *EV-21569-SOM* Board Support Package (BSP) to demonstrate various capabilities of the product. The programs can be found in the `EV-21569-SOM\examples` installation folder. Refer to the readme file provided with each example for more information.

Reference Design Information

A reference design info package is available for download on the Analog Devices Web site. The package provides information on the schematic design, layout, fabrication, and assembly of the board.

The information can be found at:

http://www.analog.com/EV-21569-SOM

FT232R - USB to UART

The FT232R is a USB-to-serial-UART interface with the following advanced features:

- Single chip USB to asynchronous serial data transfer interface
- Entire USB protocol handled on the chip. No USB specific firmware programming required
- Fully-integrated 1024 bit EEPROM storing device descriptors and CBUS I/O configuration
- Fully-integrated USB termination resistors
- Fully-integrated clock generation with no external crystal required, plus optional clock output selection enabling a glueless interface to an external MCU or FPGA
- Data transfer rates from 300 baud to 3 Mbaud (RS422, RS485, RS232) at TTL levels
- 128 byte receive buffer and 256 byte transmit buffer utilizing buffer smoothing technology to allow for high-data throughput
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Transmit and receive LED drive signals
- UART interface support for 7 or 8 data bits, 1 or 2 stop bits, and odd/even/mark/space/no parity
- FIFO receives and transmits buffers for high-data throughput
- Device supplied pre-programmed with unique USB serial number
- Supports bus-powered, self-powered and high-power bus-powered USB configurations
- Integrated +3.3V level converter for USB I/O
- Integrated level converter on UART and CBUS for interfacing to between +1.8V and +5V logic
- True 5V/3.3V/2.8V/1.8V CMOS drive output and TTL input
- Configurable I/O pin output drive strength
- Integrated power-on-reset circuit
- Fully-integrated AVCC supply filtering - no external filtering required.
- UART signal inversion option
- +3.3V (using external oscillator) to +5.25V (internal oscillator) single supply operation
- Low-operating and USB suspend current
- Low USB bandwidth consumption
- UHCI/OHCI/EHCI host controller compatible
- USB 2.0 full speed compatible

IS25LP512M - 512M-bit Serial Flash Memory with Dual and Quad SPI

The IS25LP512M Serial Flash memory offers a versatile storage solution with high flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" Flash is for systems that require limited space, a low pin count, and low power consumption. The device is accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which can also be configured to serve as multi-I/O (see pin descriptions).

The device supports Dual and Quad I/O, as well as standard, Dual Output, and Quad Output SPI. Clock frequencies of up to 133MHz allow for equivalent clock rates of up to 532MHz (133MHz x 4) which equates to 66.5Mbytes of data throughput. The IS25xE series of Flash adds support for DTR (Double Transfer Rate) commands that transfer addresses and read data on both edges of the clock.These transfer rates can outperform 16-bit Parallel Flash memories, allowing for efficient memory access to support XIP (eXecute In Place) operation.

The memory array is organized into programmable pages of 256/512 bytes. This family supports page program mode where 1 to 256/512 bytes of data are programmed in a single command.

QPI (Quad Peripheral Interface) supports 2-cycle instructions, further reducing instruction times. Pages can be erased in groups of 4Kbyte sectors, 32Kbyte blocks, 64K/256Kbyte blocks, and/or the entire chip. The uniform sector and block architecture allows for a high degree of flexibility so that the device can be utilized for a broad variety of applications requiring solid data retention.

IS43TR16512BL - 1Gx8, 512Mx16 8Gb DDR3 SDRAM

- Low Voltage (L): VDD and VDDQ = 1.35V + 0.1V, -0.067V - Backward compatible to 1.5V
- High speed data transfer rates with system frequency up to 933 MHz
- 8 internal banks for concurrent operation
- 8n-Bit pre-fetch architecture
- Programmable CAS Latency
- Programmable Additive Latency: 0, CL-1,CL-2
- Programmable CAS WRITE latency (CWL) based on tCK
- Programmable Burst Length: 4 and 8
- Programmable Burst Sequence: Sequential or Interleave
- BL switch on the fly
- Auto Self Refresh(ASR)
- Self Refresh Temperature(SRT)

- Refresh Interval: 7.8 µs (8192 cycles/64 ms) Tc= -40°C to 85°C 3.9 µs (8192 cycles/32 ms) Tc= 85°C to 95°C 1.95 µs (8192 cycles/16 ms) Tc= 95°C to 105°C 0.97 µs (8192 cycles/8 ms) Tc= 105°C to 115°C
- Partial Array Self Refresh
- Asynchronous RESET pin
- TDQS (Termination Data Strobe) supported (x8 only)
- OCD (Off-Chip Driver Impedance Adjustment)
- Dynamic ODT (On-Die Termination)
- Driver strength : RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Write Leveling
- Up to 200 MHz in DLL off mode

3 Hardware Reference

This chapter describes the hardware design of the *EV-21569-SOM* board.

System Architecture

The ***Block Diagram*** figure shows the board configuration.

Figure 3-1: Block Diagram

The *EV-21569-SOM* board is designed to demonstrate the ADSP-21569 processor's capabilities. The board has a 25 MHz input clock and runs at a max core clock frequency of 1GHz.

User I/O to the processor is provided in the form of two pushbuttons and three LEDs.

The software-controlled switches (SoftConfig) facilitate the switch multi-functionality by disconnecting the push-buttons from their associated processor pins and reusing the pins elsewhere on the board.

Software-Controlled Switches (SoftConfig)

On the board, most of the functionality traditionally controlled by mechanical switches and jumpers is controlled by I^2C software-controlled switches. The mechanical switches that remain are provided for the boot mode and push buttons. Reference any `SoftConfig*.c` file found in the installation directory for an example of how to set up the SoftConfig feature of the board through software. The SoftConfig section of this manual serves as a reference to any user that intends to modify an existing software example. If software provided by ADI is used, there should be little need to reference this section.

NOTE: Be careful when changing SoftConfig settings. When connecting extender cards, configure the settings to avoid conflict among interfaces so multiple signals are not driven on the same pins.

Overview of SoftConfig

In order to further clarify the use of electronic single FET switches and multi-channel bus switches, an example of each is illustrated and compared to a traditional mechanical switching solution. This is a generic example that uses similar FET and bus switch components that are on the board.

After this generic discussion, there is a detailed explanation of the SoftConfig interface specific to the *EV-21569-SOM* carrier board.

The ***Example of Individual FET Switches*** figure shows two individual FET switches (Pericom PI3A125CEX) with reference designators UA and UB. Net names ENABLE_A and ENABLE_B control UA and UB. The default FET switch enable settings in this example are controlled by resistors RA and RB, which pull the enable pin 1 of UA and UB to ground (low), respectively. In a real example, these enable signals are controlled by the Microchip I/O expander. The default pull-down resistors connect the signals EXAMPLE_SIGNAL_A and EXAMPLE_SIGNAL_B and also connect signals EXAMPLE_SIGNAL_C and EXAMPLE_SIGNAL_D. To disconnect EXAMPLE_SIGNAL_A from EXAMPLE_SIGNAL_B, the Microchip I/O expander is used to change ENABLE_A to a logic 1 through software that interfaces with the Microchip I/O expander. The same procedure for ENABLE_B disconnects EXAMPLE_SIGNAL_C from EXAMPLE_SIGNAL_D.

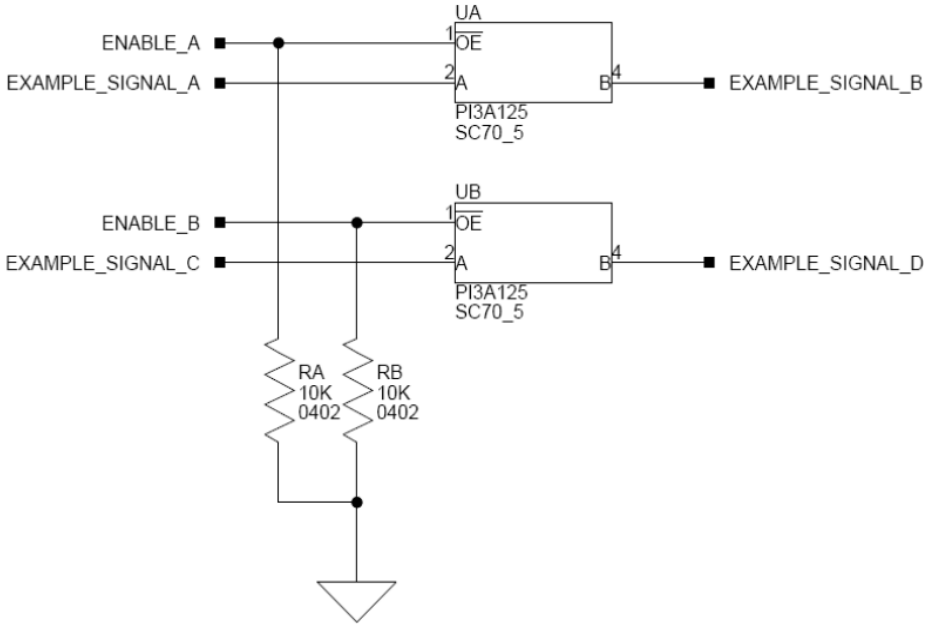

Figure 3-2: Example of Individual FET Switches

The following figure shows the equivalent circuit to the ***Example of Individual FET Switches*** figure but utilizes mechanical switches that are in the same package. The default is shown by black boxes located closer to the ***ON*** label of the switches. In order to disconnect these switches, physically move the switch to the OFF position.

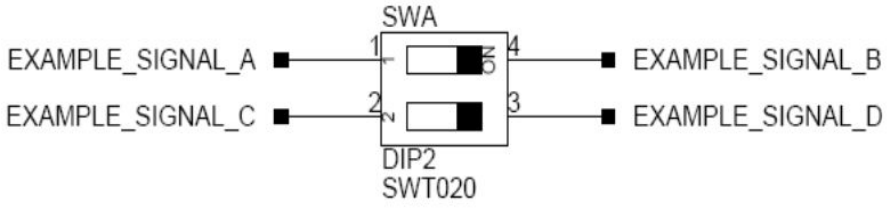

Figure 3-3: Example of a Mechanical Switch (Equivalent to Example of Individual FET Switches Figure)

The ***Example of Bus Switch*** figure shows a bus switch example, reference designator UC (Pericom PI3LVD512ZHE), selecting between lettered functionality and numbered functionality. The signals on the left side are multiplexed signals with naming convention letter_number. The right side of the circuit shows the signals separated into letter and number, with the number on the lower group (0B1) and the letter on the upper group (0B2). The default setting is controlled by the signal CONTROL_LETTER_NUMBER which is pulled low. This selects the number signals on the right to be connected to the multiplexed signals on the left by default. In this example, the Microchip I/O expander is not shown but controls the signal CONTROL_LETTER_NUMBER and allows the user to change the selection through software.

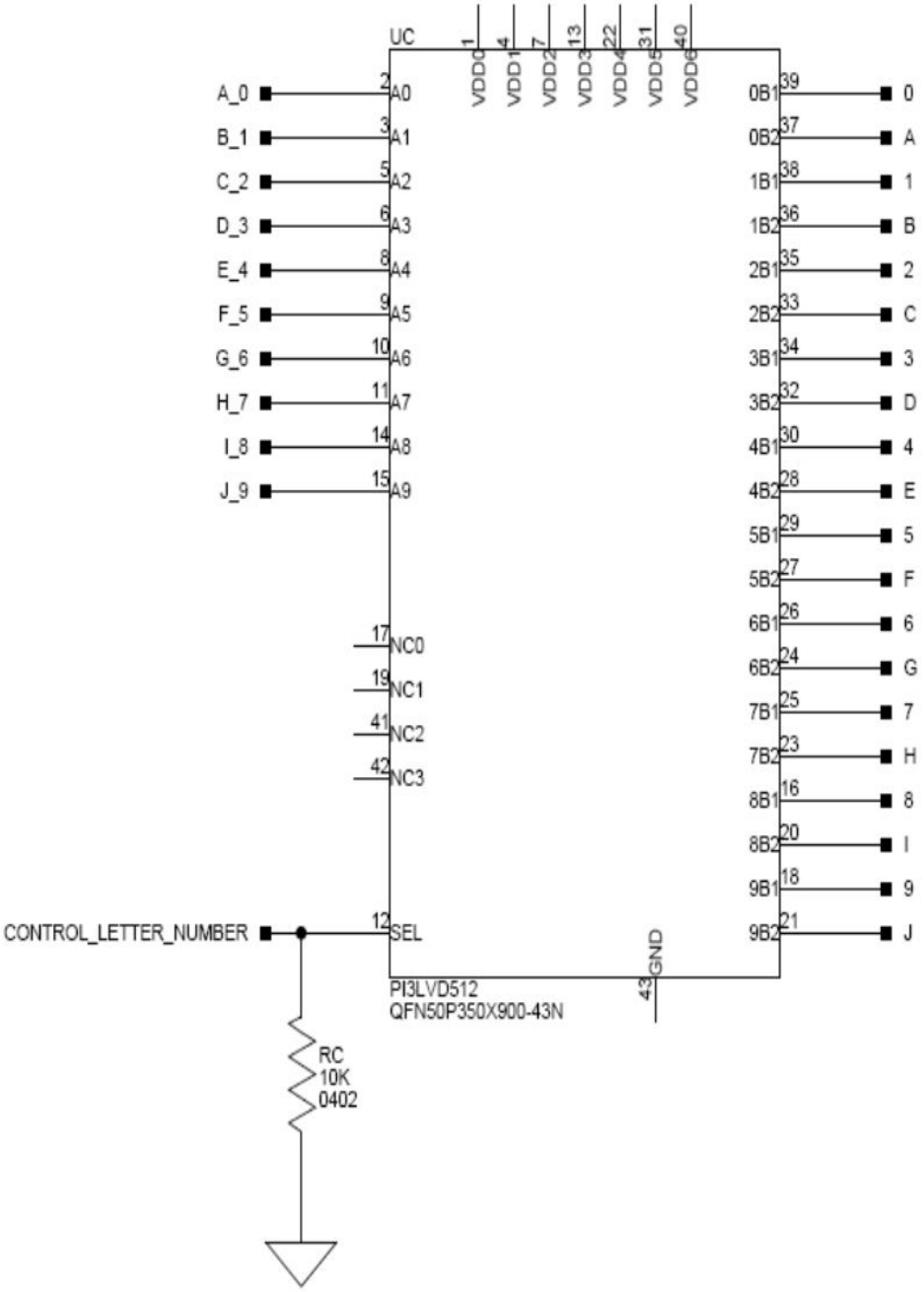

Figure 3-4: Example of a Bus Switch

The following figure shows the equivalent circuit to the ***Example of Bus Switch*** figure but utilizes mechanical switches. The default for reference designators SWC and SWD is illustrated by black boxes located closer to the ***ON*** label of the switches to enable the number signals by default. Also, note the default setting for reference designators SWE and SWF is OFF. In order to connect the letters instead of the numbers, the user physically changes all switches on SWC and SWD to the OFF position and all switches on SWE and SEF to the ON position.

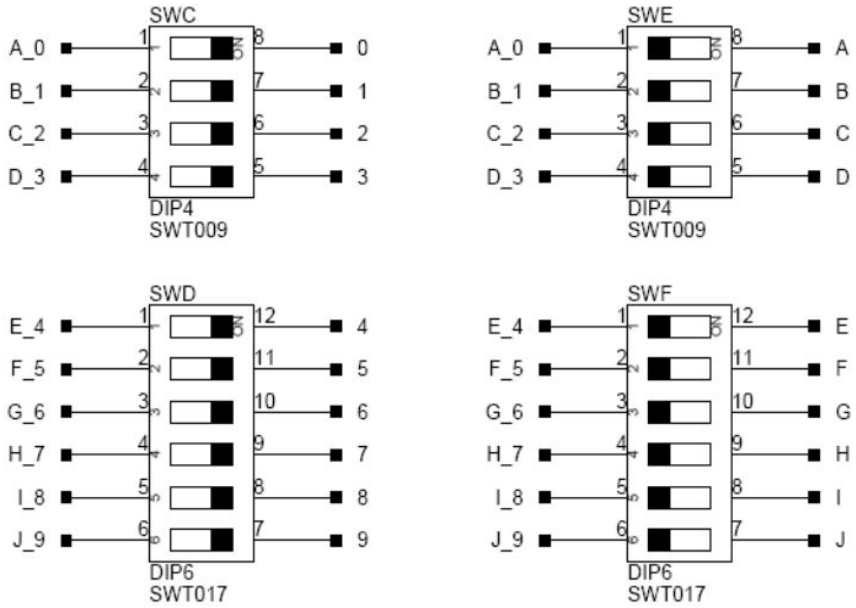

Figure 3-5: Example of a Mechanical Switch (Equivalent to Example of Bus Switch)

SoftConfig on the Board

Two Microchip MCP23017 GPIO expanders provide control for individual electronic switches. The TWI2 interface of the processor communicates with the Microchip devices. There are individual switches with default settings that enable basic board functionality.

The ***Default Processor Interface Availability*** table lists the processor and board interfaces that are available by default. Note that only interfaces affected by software switches are listed in the table.

Table 3-1: Default Processor Interface Availability

Interface	*Availability by Default*
UART0	USB to UART FTDI232RQ
SPI Flash	Quad mode enabled
LEDs	Enabled

Programming SoftConfig Switches

On the board, two Microchip MCP23017 devices exist. Each of these devices has the following programming characteristics:

- Each GPIO register controls eight signals (software switches).

GPIO Register	*Register Address*
GPIOA	0x12

GPIO Register	*Register Address*
GPIOB	0x13

- By default, the Microchip MCP23017 GPIO signals function as input signals.

  The signals must be programmed as output signals to override their default values. A zero is programmed into the register to enable the signal as an output. The following table shows the Microchip GPIO expander register addresses.

IODIR Register	*IODIR Register Address*
IODIRA	0x00
IODIRB	0x01

Each example in the Board Support Package (BSP) includes source files that program the soft switches, even if the default settings are being used. The `README` for each example identifies only the signals that are being changed from their default values. The code that programs the soft switches is located in the `SoftConfig_XXX.c` file in each example, where XXX is the name of the baord.

The ***I 2 C Hardware Address (0x21)*** and ***I 2 C Hardware Address (0x22)*** tables outline the default values for each of the two Microchip MCP23017 devices.

Table 3-2: I2C Hardware Address (0x21)

GPIO	*MCP23017 Register Address*	*Default Value*
GPIOA	0x12	0x02
GPIOB	0x13	0xC4

Table 3-3: I2C Hardware Address (0x22)

GPIO	*MCP23017 Register Address*	*Default Value*
GPIOA	0x12	0xE0
GPIOB	0x13	0xFF

The board schematic shows how the two Microchip GPIO expanders are connected to the board's ICs.

The ***Output Signals of Microchip GPIO Expander (U13 Port A)*** and ***Output Signals of Microchip GPIO Expander (U13 Port B)*** tables show the output signals of the Microchip GPIO expander (***U13***), with a TWI address of `0100 001X`, where `X` represents the read or write bit. The signals that control an individual FET have an entry in the ***FET*** column. The ***Component Connected*** column shows the board IC that is connected if the FET is enabled. The Microchip (`U13`) is controlling the enable signal of a FET switch. Also note that if a particular functionality of the processor signal is being used, it is in ***bold*** font in the ***Processor Signal*** column.

Table 3-4: Output Signals of Microchip GPIO Expander (U13 Port A)

Bit	*Signal Name*	*Description*	*FET*	*Processor Signal (if applicable)*	*Connected*	*Default*
0	LED6	GPIO LED		None	LED6	Low
1	LED7	GPIO LED		None	LED7	Low
2	LED4	GPIO LED		None	LED4	Low
3	SPI2FLASH_CS_EN	Enable SPI Flash CS	U3	PA_05/SPI2_SEL1/ OSPI_SEL1/SMC0_D05/ SPI2_SS	U11	High
4	SPI2D2_D3_EN	Enabel SPI Flash Quad Mode	U4 U5	PA_02/SPI2_D2/OSPI_D2/ TWI3_SCL/SMC0_D02/ TM0_ACLK3 PA_03/SPI2_D3/ OSPI_D3/TWI3_SDA/ SMC0_D03	U11	High
5	UART0_EN	Enable FTDI UART to USB	U8	PA_06/SPI0_CLK/UART0_TX/ OSPI_D4/SMC0_D06/ TM0_ACLK1 PA_07/ SPI0_MISO/UART0_RX/ OSPI_D5/SMC0_D07/ TM0_ACI0	U7	Low
6	UART0_FLOW_EN	Enables UART Flow Control on FTDI	U8	PA_08/SPI0_MOSI/ UART0_RTS/OSPI_D6/ SMC0_D08/TM0_ACLK2 PA_09/SPI0_SEL1/ UART0_CTS/OSPI_D7/ SMC0_D09/SPI0_SS	U7	Low
7	NOT USED					

Table 3-5: Output Signals of Microchip GPIO Expander (U13 Port B)

Bit	*Signal Name*	*Description*	*FET*	*Processor Signal (if applicable)*	*Connected*	*Default*
0	NOT USED					
1	NOT USED					
2	NOT USED					
3	NOT USED					
4	NOT USED					
5	NOT USED					
6	NOT USED					
7	NOT USED					

Switches

This section describes operation of the switches. The switch locations are shown in the ***Switch/Jumper Locations*** figure.

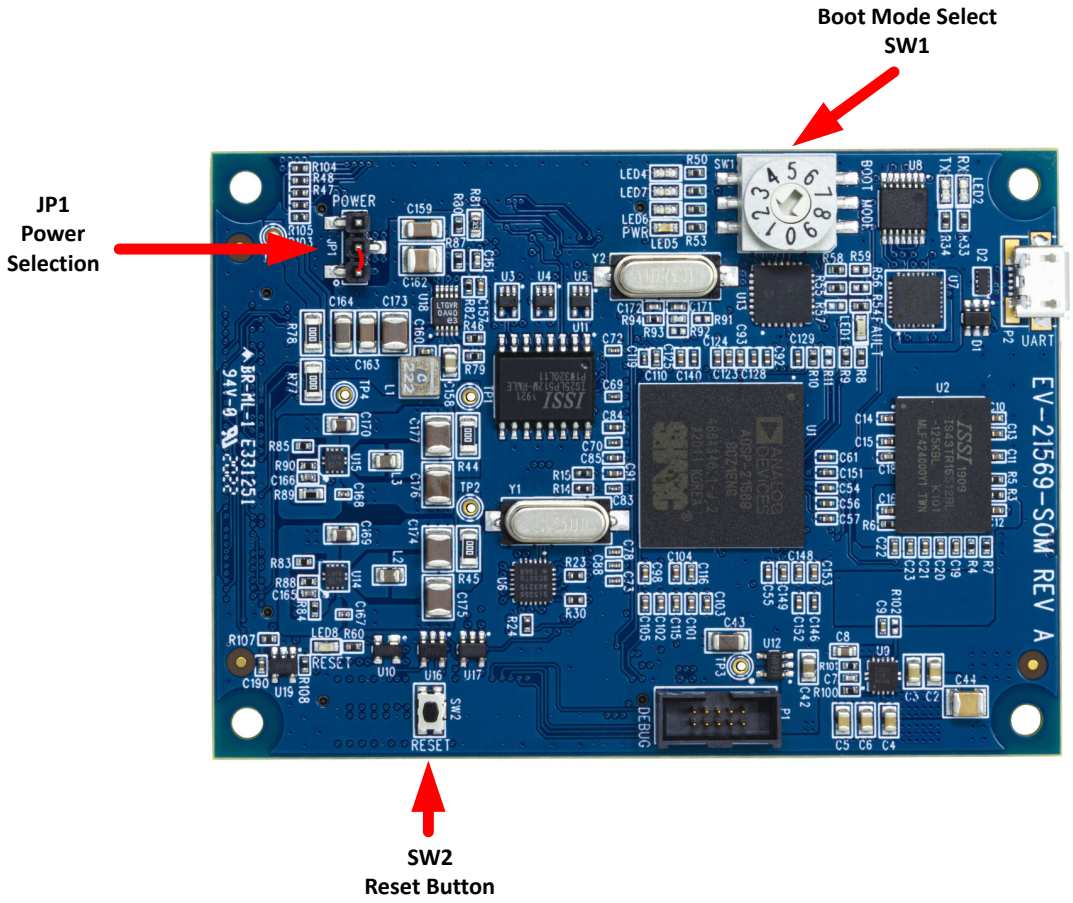

Figure 3-6: Switch/Jumper Locations

Boot Mode Select (SW1)

The Boot Mode selection switch selects between the different boot modes of the processor. The ***Boot Mode Switch*** table shows the available boot mode settings. By default, the processor boots from SPI2 master boot which uses the on-board SPI flash memory.

Table 3-6: Boot Mode Switch

Position	*Processor Boot Mode*
0	No Boot
1	***SPI Master Boot (Default)***
2	SPI Slave Boot
3	UART Boot
4	Link Port Boot
5	OSPI Master Boot
6	Reserved
7	Reserved

Reset Pushbutton (SW2)

The reset pushbutton resets the ADSP-21569 processor. The reset signal also is connected to the expansion connectors via the SYS_HWRST signal. Reset (LED8) is used to indicate when the board is in reset.

Jumpers

This section describes functionality of the configuration jumpers. The ***Switch/Jumper Locations*** figure shows the jumper locations.

Power (JP1)

The power jumper (JP1) selects the input power source to the *EV-21569-SOM* board. Pin 1-2 selects power input from the P2 USB port and Pin 2-3 selects Power from the SoM Interface Connectors. When using the EV-SOMCRR-EZKIT carrier board or other plug in carrier board, use Jumper setting Pin 2-3.

LEDs

This section describes the on-board LEDs. The ***LED Locations*** figure shows the LED locations.

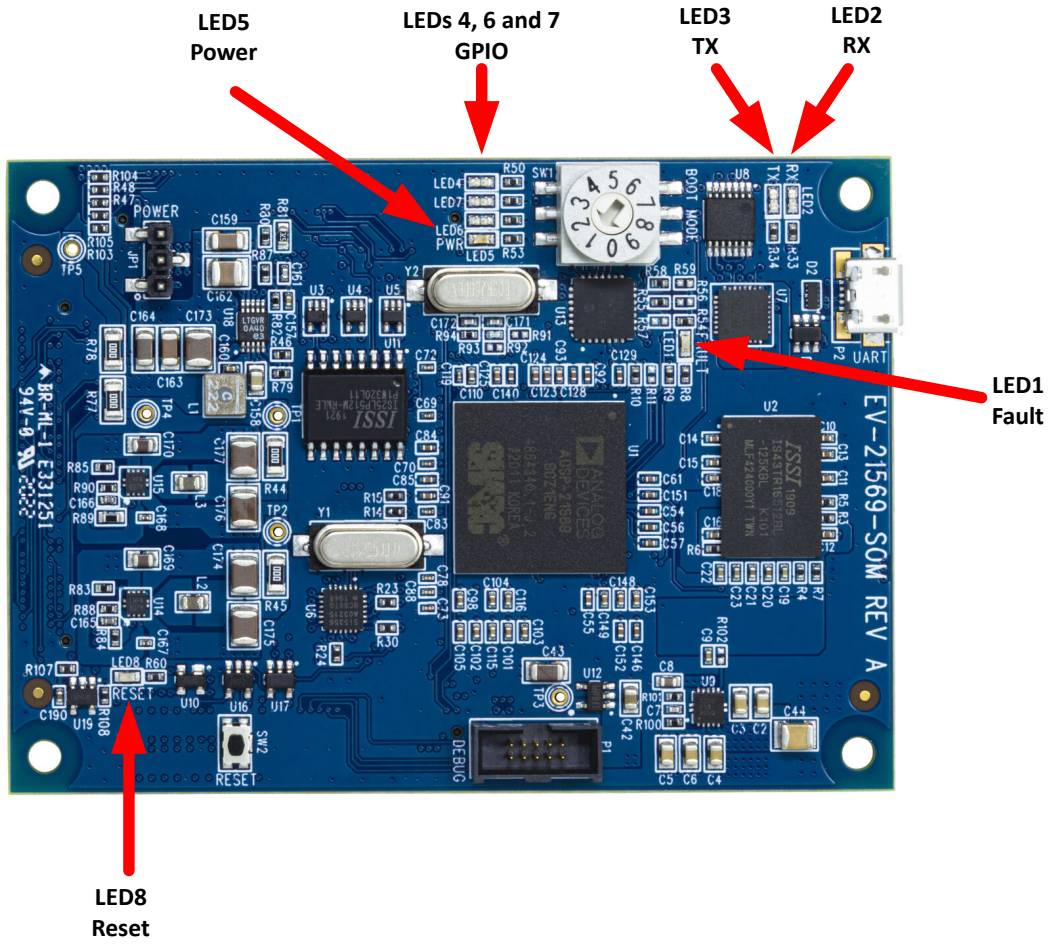

Figure 3-7: LED Locations

Fault (LED1)

When ON (red), it indicates a system fault. For more information, refer to the ADSP-2156xHardware Reference Manual.

Power (LED5)

When ON (green), it indicates that power is being supplied to the board properly.

GPIO (LED4, LED6, LED7)

Three LEDs are connected to the SoftConfig (see the ***GPIO LEDs*** table). The LEDs are active high and are turned ON (amber) by writing to the U13 SoftConfig IC.

Table 3-7: GPIO LEDs

Reference Designator	*Programmable Flag Pin*
LED4	SoftSwitch
LED6	SoftSwitch
LED7	SoftSwitch

Reset (LED8)

When ON (red), it indicates that the board is in reset. A master reset is asserted by pressing SW2 , which activates the LED. For more information, see Reset Pushbutton (SW2).

Connectors

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in the ***Connector Locations*** figure.

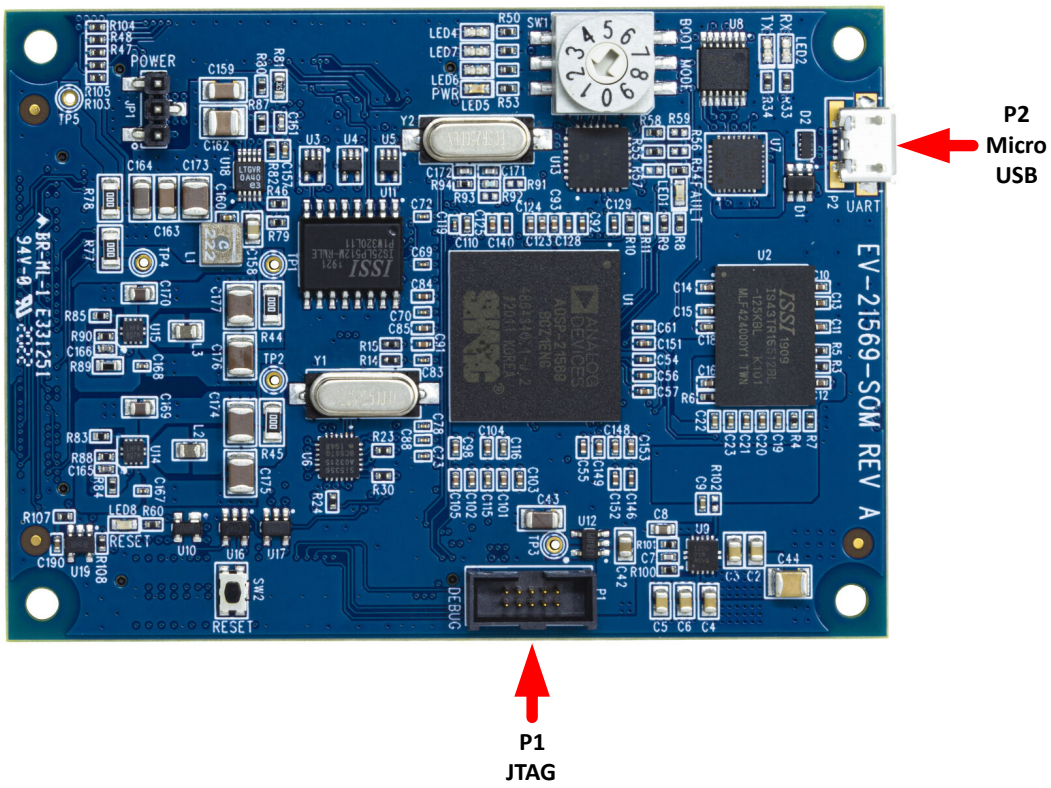

Figure 3-8: Connector Locations Top View

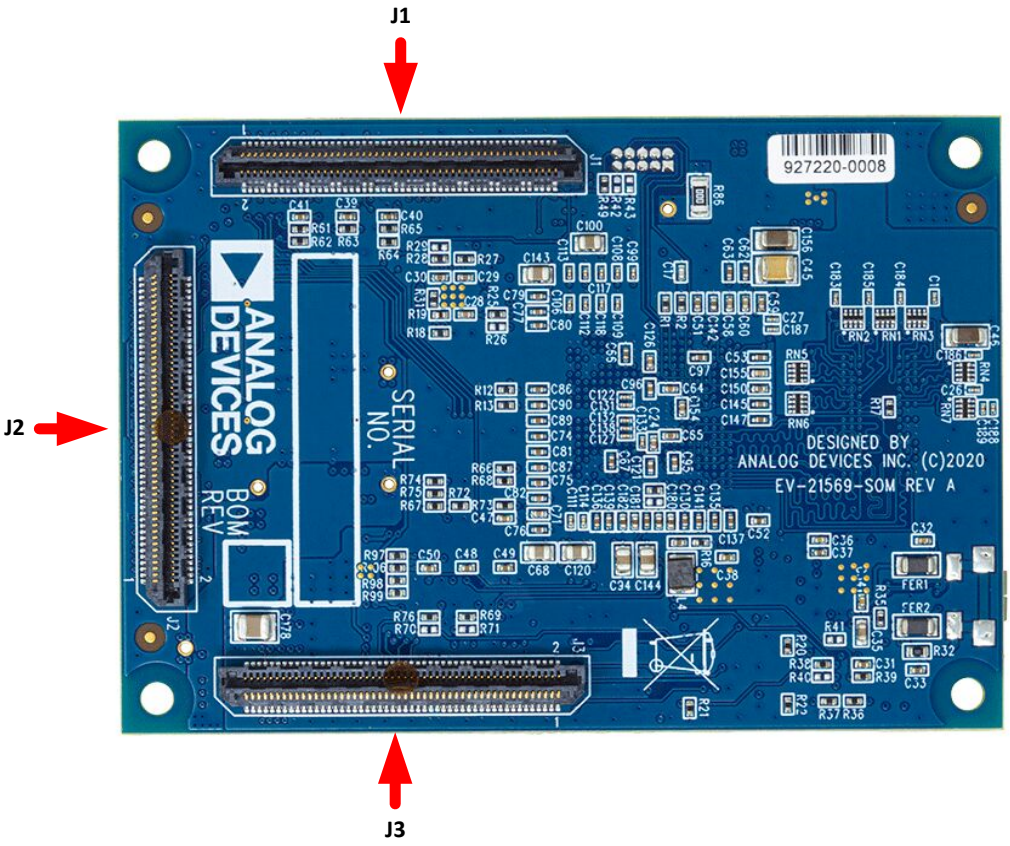

Figure 3-9: Connector Locations Bottom View

JTAG (P1)

The JTAG header provides debug connectivity for the processor. This is a 0.05" shrouded through-hole connector from SAMTEC (SHF-105-01-L-D-SM-K). This connector mates with ICE-1000, ICE-2000, and any newer Analog Devices emulators. For more information, see Debug Interface

MicroUSB Connector (P2)

USB Connection for FTDI RS232 to USB connection, and also power to SoM when JP1 pins 1-2 are set.

Part Description	*Manufacturer*	*Part Number*
MicroUSB 2.0	Hirose	ZX62D-AB-5P8(30)
Mating Cable		
USB A to MicroUSB	ANY	ANY

SoM Interface Connection (J1, J2, and J3)

The SoM Interface consists of three SAMTEC high speed connectors that provide the DSP peripheral signals for use with a plug in baseboard. The *SoM Connector* figure shows the connector locations on the back of the board.

These signals are based upon the peripheral signal needs, which allows multiple DSPs to be used with this connection. These connectors are self-mating and the pinout here reflects the connectors on the EV-21569-SOM.

The *SoM Interface A Connector (J1)*, *SoM Interface B Connector (J2)*, and *SoM Interface C Connector (J3)* tables show the signal associated with each pin on the connectors.

Table 3-8: SoM Interface A Connector (J1)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND1	21	DAI0_PIN10	41	DAI0_PIN20	61	NU	81	GPIO3
2	GND2	22	DAI1_PIN10	42	DAI1_PIN20	62	NU	82	NU
3	DAI0_PIN01	23	DAI0_PIN11	43	GND3	63	NU	83	GPIO4
4	DAI1_PIN01	24	DAI1_PIN11	44	GND4	64	NU	84	GPIO6
5	DAI0_PIN02	25	DAI0_PIN12	45	GND5	65	NU	85	GPIO5
6	DAI1_PIN02	26	DAI1_PIN12	46	GND6	66	NU	86	GPIO7
7	DAI0_PIN03	27	NU	47	NU	67	NU	87	GND9
8	DAI1_PIN03	28	NU	48	NU	68	NU	88	GPIO8
9	DAI0_PIN04	29	NU	49	NU	69	NU	89	NU
10	DAI1_PIN04	30	NU	50	NU	70	NU	90	GPIO9
11	DAI0_PIN05	31	NU	51	NU	71	NU	91	NU
12	DAI1_PIN05	32	NU	52	NU	72	NU	92	GPIO10
13	DAI0_PIN06	33	NU	53	NU	73	NU	93	NU
14	DAI1_PIN06	34	NU	54	NU	74	NU	94	GND10
15	DAI0_PIN07	35	NU	55	GND7	75	NU	95	NU
16	DAI1_PIN07	36	NU	56	GND8	76	NU	96	NU
17	DAI0_PIN08	37	NU	57	NU	77	GPIO1	97	NU
18	DAI1_PIN08	38	NU	58	NU	78	NU	98	NU
19	DAI0_PIN09	39	DAI0_PIN19	59	NU	79	GPIO2	99	NU
20	DAI1_PIN09	40	DAI1_PIN19	60	NU	80	NU	100	NU

Table 3-9: SoM Interface B Connector (J2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND1	21	OSPI_D7	41	TWI2_SDA	61	NU	81	LINKPORT0_D7

Table 3-9: SoM Interface B Connector (J2) (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
2	GND2	22	SPI1_SEL2b	42	UART2_RXb	62	GND8	82	LINKPORT1_D7
3	SP2_OSPI_MISO	23	SPI2_SEL2b	43	UART0_TXb	63	NU	83	LINKPORT0_D6
4	SPI0_CLK	24	GND3	44	UART2_RTSb	64	CAN0_TX	84	LINKPORT1_D6
5	SP2_OSPI_MOSI	25	GND4	45	UART0_RXb	65	NU	85	LINKPORT0_D5
6	SPI0_MISO	26	NU	46	UART2_CTSb	66	CAN0_RX	86	LINKPORT1_D5
7	SPI2_OSPI_D2	27	NU	47	UART0_RTSb	67	NU	87	LINKPORT0_D4
8	SPI0_MOSI	28	NU	48	GND6	68	GND	88	LINKPORT1_D4
9	SP2_OSPI_D3	29	NU	49	UART0_CTSb	69	NU	89	LINKPORT0_D3
10	SPI0_SSb	30	NU	50	GPIO1	70	CAN1_TX	90	LINKPORT1_D3
11	SP2_OSPI_CLK	31	TWI0_SCL	51	GND5	71	GND7	91	LINKPORT0_D2
12	SPI0_SEL2b	32	UART1_TXb	52	GPIO2	72	CAN1_RX	92	LINKPORT1_D2
13	SP2_OSPI_SSb	33	TWI0_SDA	53	NU	73	NU	93	LINKPORT0_D1
14	SPI1_CLK	34	UART1_RXb	54	NU	74	NU	94	LINKPORT1_D1
15	OSPI_D4	35	TWI1_SCL	55	NU	75	NU	95	LINKPORT0_D0
16	SPI1_MISO	36	UART1_RTSb	56	NU	76	NU	96	LINKPORT1_D0
17	OSPI_D5	37	TWI1_SDA	57	NU	77	NU	97	LINKPORT0_ACK
18	SPI1_MOSI	38	UART1_CTSb	58	NU	78	NU	98	LINKPORT1_ACK
19	OSPI_D6	39	TWI2_SCL	59	NU	79	GND9	99	LINKPORT0_CLK
20	SPI1_SSb	40	UART2_TXb	60	NU	80	GND10	100	LINKPORT1_CLK

Table 3-10: SoM Interface C Connector (J3)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND1	21	NU	41	GND7	61	NU	81	NU
2	GND2	22	GND4	42	CLK1	62	NU	82	GPIO3
3	NU	23	NU	43	NU	63	NU	83	NU
4	NU	24	NU	44	CLK2	64	NU	84	GPIO4
5	NU	25	GND3	45	NU	65	NU	85	GND11
6	NU	26	NU	46	GND8	66	NU	86	GPIO5
7	NU	27	NU	47	NU	67	NU	87	VDD_EXT
8	NU	28	NU	48	JTG0_TMS/ SWDIO	68	NU	88	GPIO6
9	NU	29	NU	49	NU	69	NU	89	VDD_VREF

Table 3-10: SoM Interface C Connector (J3) (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
10	NU	30	NU	50	JTG0_TCK/ SWCLK	70	NU	90	GND12
11	NU	31	NU	51	NU	71	NU	91	VDD_A
12	NU	32	NU	52	JTG0_TDO/SW0	72	NU	92	VDD_DMC
13	NU	33	NU	53	NU	73	NU	93	VDD_INT
14	NU	34	NU	54	JTG0_TDI	74	NU	94	$\overline{\text{SYS\_HWRST}}$
15	NU	35	NU	55	NU	75	NU	95	PWR_SEQ_GOOD
16	NU	36	GND5	56	$\overline{\text{JTG0\_TRST}}$	76	GND10	96	$\overline{\text{SoM\_Reset}}$
17	NU	37	NU	57	NU	77	NU	97	VDD1
18	NU	38	SYS_CLKOUT	58	$\overline{\text{TARGET\_RESET}}$	78	GPIO1	98	VSS1
19	NU	39	GND6	59	NU	79	NU	99	VDD2
20	NU	40	AUDIO_CLK	60	GND9	80	GPIO2	100	VSS2

Table 3-11: Mating Connector

Part Description	*Manufacturer*	*Part Number*
100-pin, 0.64 mm	SAMTEC	LSS-150-01-L-DV-A-K
Mating Connector		
100-pin, 0.64 mm	SAMTEC	LSS-150-01-L-DV-A-K

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