26.5 GHz, Integer N/Fractional-N, PLL Synthesizer

Data Sheet

ADF41513

FEATURES

1 GHz to 26.5 GHz bandwidth
Ultralow noise PLL
Integer N = −235 dBc/Hz, fractional-N = −231 dBc/Hz
High maximum PFD frequency
Integer N = 250 MHz, fractional-N = 125 MHz
25-bit fixed/49-bit variable fractional modulus mode
Single-ended reference input
3.3 V power supply, 3.3 V charge pump
Integrated 1.8 V logic capability
Phase resync
Programmable charge pump currents: 16× range
Digital lock detect
3-wire serial interface with register readback option
Hardware and software power-down mode
Operating range from −40°C to +105°C

APPLICATIONS

Test equipment and instrumentation
Wireless infrastructure
Microwave point to point and multipoint radios
Very small aperture terminal (VSAT) radios
Aerospace and defense

GENERAL DESCRIPTION

The ADF41513 is an ultralow noise frequency synthesizer that can be used to implement local oscillators (LOs) as high as 26.5 GHz in the upconversion and downconversion sections of wireless receivers and transmitters.

The ADF41513 is designed on a high performance silicon geranium (SiGe), bipolar complementary metal-oxide semiconductor (BiCMOS) process, achieving a normalized phase noise floor of −235 dBc/Hz. The phase frequency detector (PFD) operates up to 250 MHz (integer N mode)/ 125 MHz (fractional-N mode) for improved phase noise and spur performance. The variable modulus, Σ-Δ modulator allows extremely fine resolution when using a 49-bit divide value. The ADF41513 can be used as an integer N phase-locked loop (PLL), or it can be used as a fractional-N PLL with either a fixed modulus for subhertz frequency resolution or variable modulus for subhertz exact frequency resolution.

A complete PLL is implemented when the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). The 26.5 GHz bandwidth eliminates the need for a frequency doubler or divider stage, simplifying system architecture and reducing cost. The ADF41513 is packaged in a compact, 24-lead, 4 mm × 4 mm LFCSP.

FUNCTIONAL BLOCK DIAGRAM

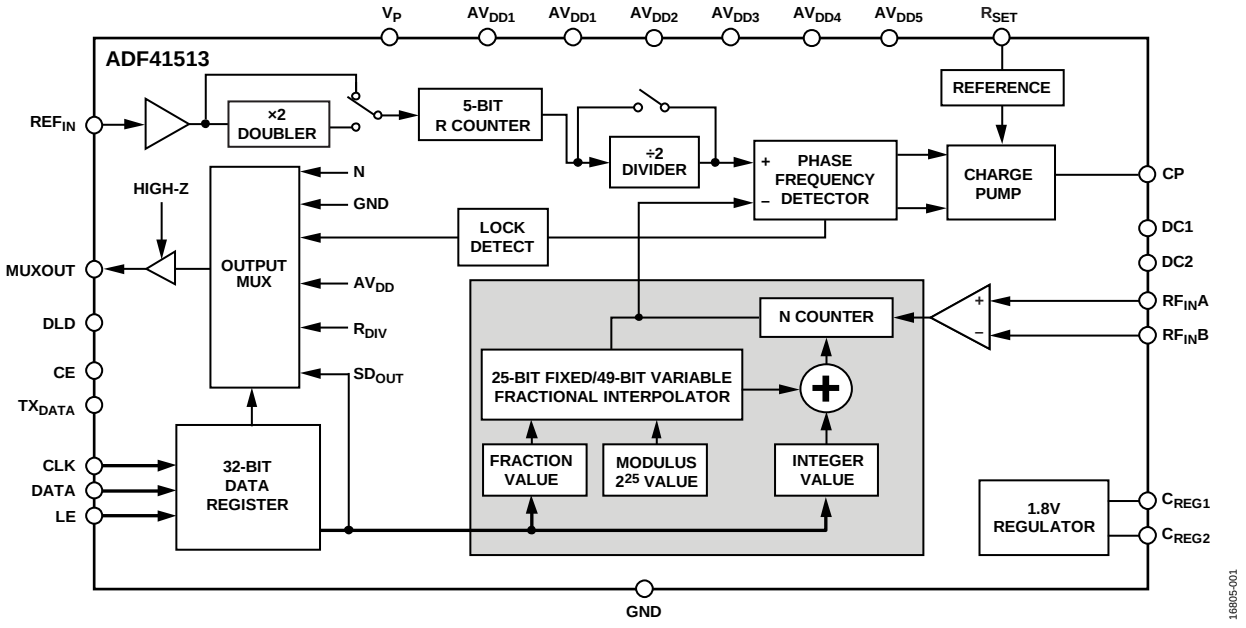

Figure 1.

Rev. 0 **Document Feedback**

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Technical Support www.analog.com

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REVISION HISTORY

1/2019—Revision 0: Initial Version

SPECIFICATIONS

$AV_{DDx} = AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = AV_{DD5} = V_P = 3.3$ V ± 5%, GND = 0 V, $R_{SET} = 1.8$ kΩ, dBm referred to 50 Ω, $T_A = T_{MIN}$ (−40°C) to T_{MAX} (+105°C), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RADIO FREQUENCY (RF) CHARACTERISTICS					
8/9 Prescaler					
RF Input Frequency (f_{RFIN}) Range	1		26.5	GHz	Recommended input power of −5 dBm to +5 dBm, operation at this frequency range is limited to 70°C to T_{MIN}
	1		24	GHz	Operation at this frequency range is T_{MAX} to T_{MIN}
RF Input Sensitivity		−11		dBm	Refer to Figure 10 and Figure 11 for more information
4/5 Prescaler					
f_{RFIN} Range	1		16	GHz	For lower frequencies, ensure slew rate > 320 V/µs
RF Input Sensitivity Range	−7		+5	dBm	Measured single-ended to $RF_{IN}A$ via a 1 pF series capacitor, 1 pF capacitor to GND on $RF_{IN}B$
INPUT REFERENCE FREQUENCY (REF_{IN}) CHARACTERISTICS					
REF_{IN} Input					
Frequency	10		800	MHz	
Voltage Range	0		1.8	V	
Sensitivity Range	−10		8	dBm	Biased at 1 V (ac coupling ensures 1 V bias), use square wave at low power and/or frequency to ensure slew rate is > 320 V/µs; for best inband phase noise performance, ensure slew rate > 500 V/µs
Capacitance			10	pF	
Current			±150	µA	
Doubler Input Frequency			225	MHz	Maximum reference frequency when the doubler is enabled
MAXIMUM PFD FREQUENCY					
Integer N Mode			250	MHz	
Fractional-N Mode			125	MHz	
N DIVIDER RANGE					
16-Bit N Divider Range					
Integer N Mode	20		511		4/5 prescaler
	64		1023		8/9 prescaler
Fractional-N Mode	23		511		4/5 prescaler
	75		1023		8/9 prescaler
CHARGE PUMP (CP)					
CP Current (I_{CP}) Sink and Source					Programmable
High Value		7.2		mA	With $R_{SET} = 1.8$ kΩ
Low Value		0.45		mA	
Absolute Accuracy		5		%	With $R_{SET} = 1.8$ kΩ
R_{SET} Range	1.8	2.7	10	kΩ	5% accuracy
I_{CP} Three-State Leakage		2		nA	$V_{CP} = 0.9$ V, $T_A = 25$°C
Sink and Source Current Matching		5		%	0.7 V ≤ CP voltage (V_{CP}) ≤ V_P − 0.7 V
I_{CP} vs. V_{CP}		5		%	0.7 V ≤ V_{CP} ≤ V_P − 0.7 V
I_{CP} vs. Temperature		5		%	$V_{CP} = V_P/2$

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
Input Voltage					
High (V_{IH})	1.4			V	The serial port interface (SPI) block can accept both 1.8 V or 3.3 V logic inputs
Low (V_{IL})			0.6	V	
Input Current (I_{INH}, I_{INL})			±1	µA	
Input Capacitance (C_{IN})			10	pF	
LOGIC OUTPUTS					
Output Voltage					
High (V_{OH})	1.4			V	MUXOUT voltage = 1.8 V, DLD voltage = 1.8 V
	2.6			V	MUXOUT voltage = 3.3 V, DLD voltage = 3.3 V
Low (V_{OL})			0.4	V	
Output High Current, Output Low Current (I_{OH}, I_{OL})			500	µA	
POWER SUPPLIES					
AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4}, AV_{DD5}, V_P	3.135	3.3	3.465	V	
I_{DD1}[1]		2	3.2	mA	Current drawn by AV_{DD1}
I_{DD2}[1]		63.5	88	mA	Current drawn by AV_{DD2}
I_{DD3}[1]		2.1	3.6	mA	Current drawn by AV_{DD3}
I_{DD4}[1]		1.45	2	mA	Current drawn by AV_{DD4}
I_{DD5}[1]		20	25	mA	Current drawn by AV_{DD5}
I_P		6	7	mA	Current drawn by V_P
I_{TOTAL}		95.1	128.8	mA	Total current drawn by AV_{DDx} and V_P
Power-Down Mode			100	µA	T_A = 25°C, CE is low, total of all rails
NOISE CHARACTERISTICS					
Normalized Phase Noise Floor (PN_{SYNTH})					
In Integer N Mode[2]		−235		dBc/Hz	PLL loop bandwidth (BW) = 1 MHz (Integer N mode)
In Fractional-N Mode[3]		−231		dBc/Hz	PLL loop BW = 1 MHz (fractional-N mode)
Normalized 1/f Noise (PN_{1_f})[3]		−128		dBc/Hz	10 kHz offset, normalized to 1 GHz
SPURIOUS SIGNALS					
Reference Spurious		−90		dBc	At reference = 100 MHz, PLL loop BW = 40 kHz
PFD Spurious		−87		dBc	At PFD = 50 MHz, PLL loop BW = 40 kHz
In-Band Integer Boundary Spurious		−45		dBc	10 kHz offset, PLL loop BW = 250 kHz

[1] T_A = 25°C, AV_{DDx} = 3.3 V (where x = 1, 2, 3, or 4), prescaler (P) = 8/9, f_{RFIN} = 26.5 GHz, REF_{IN} = 124 MHz, PFD frequency input (f_{PFD}) = 124 MHz.

[2] The synthesizer phase noise floor is estimated by measuring the inband phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10 log f_{PFD}. PN_{SYNTH} is the total phase noise measured at the VCO output (PN_{TOT}) − 10 log f_{PFD} − 20 log N.

[3] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF}, and at a frequency offset, f, is given by phase noise (PN) = P_{1_f} + 10 log(10 kHz/f) + 20 log(f_{RF}/1 GHz). Both the normalized phase noise floor and flicker noise are modeled in the ADIsimPLL.

TIMING CHARACTERISTICS

AV_{DDx} = AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = AV_{DD5} = V_P = 3.3 V ± 5%, GND = 0 V, R_{SET} = 1.8 kΩ, dBm referred to 50 Ω, T_A = T_{MIN} (−40°C) to T_{MAX} (+105°C), unless otherwise noted.

Table 2. Read and Write Timing

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
t_1	10	ns min	LE setup time
t_2	5	ns min	DATA to CLK setup time
t_3	5	ns min	DATA to CLK hold time
t_4	12.5	ns min	CLK high duration
t_5	12.5	ns min	CLK low duration
t_6	5	ns min	CLK to LE setup time
t_7	10	ns min	LE pulse width
t_8	20	ns max	LE setup time to MUXOUT when MUXOUT is configured as SPI output
t_9	20	ns max	CLK setup time to MUXOUT when MUXOUT is configured as SPI output

Timing Diagram

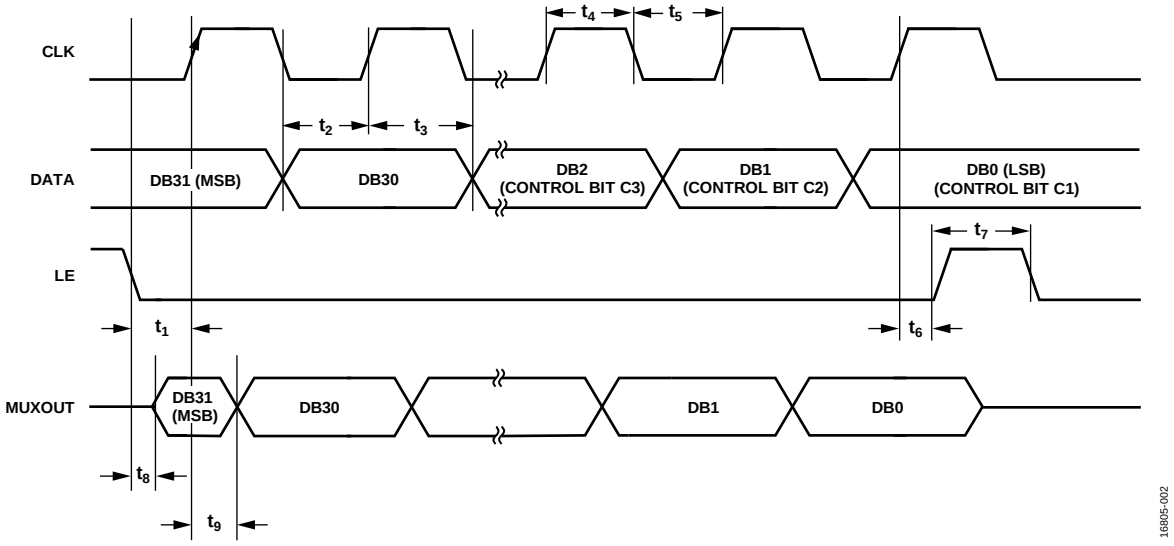

Figure 2. Read and Write Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DDx} to GND[1]	−0.3 V to +3.6 V
V_P to GND	−0.3 V to +3.6 V
V_P to AV_{DDx}	−0.3 V to +0.3 V
Digital Input/Output Voltage to GND	−0.3 V to AV_{DDx} + 0.3 V
Analog Input/Output Voltage to GND	−0.3 V to V_P + 0.3 V
$RF_{IN}A$, $RF_{IN}B$ to GND	−0.3 V to +3.6 V
$RF_{IN}A$ to $RF_{IN}B$[1]	±1.4 V
REF_{IN} to GND	−0.3 V to +2.1 V
Operating Temperature Range	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	
Operational	125°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Electrostatic Discharge (ESD)	
Charged Device Model	1250 V
Human Body Model	1500 V
Transistor Count	
CMOS	215,726
Bipolar	1625

[1] Approximately 13 dBm into a 50 Ω input.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

This device is a high performance RF IC with an electrostatic discharge (ESD) rating of <2 kV, and the device is ESD sensitive. Take proper precautions for handling and assembly.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-24-8[1]	48	38	°C/W

[1] The thermal resistance values are defined per the JESD51 standard.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

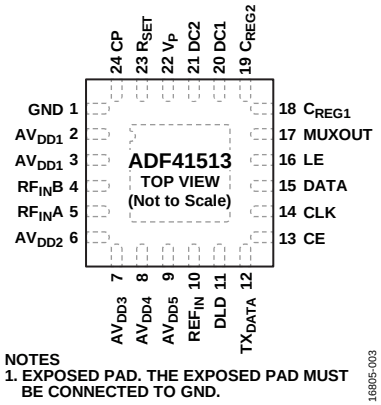

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground Pin.
2, 3	AV_{DD1}	PFD and Up and Down Digital Driver Power Supply. Pin 2 and Pin 3 can be tied together. With Pin 2 and Pin 3 tied together, place three parallel capacitors as close as possible to the AV_{DD1} pins: 10 µF, 100 nF, and 100 pF.
4	$RF_{IN}B$	Complementary Input to the RF Prescaler. In single-ended mode, decouple this pin to the ground plane with a small bypass capacitor, typically 100 pF.
5	$RF_{IN}A$	Input to the RF Prescaler. AC-couple this signal to the external VCO.
6	AV_{DD2}	RF Buffer and Prescaler Power Supply. Place three parallel capacitors as close as possible to the AV_{DD2} pin: 10 µF, 100 nF, and 100 pF.
7	AV_{DD3}	N Divider Power Supply. Place three parallel capacitors as close as possible to the AV_{DD3} pin: 10 µF, 100 nF, and 100 pF.
8	AV_{DD4}	R Divider and Lock Detector Power Supply. Place three parallel capacitors as close as possible to the AV_{DD4} pin: 10 µF, 1 µF, and 100 nF. Pin 8 powers the internal low dropout (LDO) regulator for the reference divider.
9	AV_{DD5}	Σ-Δ Modulator and SPI Power Supply. Place three parallel capacitors as close as possible to the AV_{DD5} pin: 10 µF, 1 µF, and 100 nF. This pin powers the internal LDO regulator for the Σ-Δ modulator.
10	REF_{IN}	Reference Input. The reference can accept either a single-ended CMOS (dc-coupled) or single-ended sine wave (ac-coupled). The single-ended input has a nominal threshold of 1 V and a dc equivalent input resistance of 20 kΩ.
11	DLD	Digital Lock Detect Pin. A logic high on this pin indicates PLL lock.
12	TX_{DATA}	Transmit Data Pin. Pin 12 is not used. Connect Pin 12 to GND.
13	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Registers do not hold their values when CE is low. This pin only supports 3.3 V logic inputs.
14	CLK	Serial Clock Input. CLK clocks in the serial data to the registers. The data is latched into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
15	DATA	Serial Data Input. The serial data is loaded most significant bit (MSB) first with the two least significant bits (LSBs) as the control bits. This input is a high impedance CMOS input.
16	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches. Select the latch using the control bits.
17	MUXOUT	Multiplexer Output. This multiplexer output allows the lock detect, the scaled RF, the scaled reference frequency, logic high, logic low, or register readback data to be accessed externally.
18	C_{REG1}	Internal 1.8 V Regulator Output Pin. Place three parallel capacitors as close to the C_{REG1} pin as possible: 4.7 µF, 100 nF, and 1 nF.
19	C_{REG2}	Internal 1.8 V Regulator Output Pin. Place three parallel capacitors as close to the C_{REG2} pin as possible: 4.7 µF, 100 nF, and 1 nF.
20	DC1	DC Bias Pin 1. Place a 1 µF capacitor in parallel with a 1 nF capacitor to ground, as close as possible to the DC1 pin.
21	DC2	DC Bias Pin 2. Place a 1 µF capacitor in parallel with a 1 nF capacitor to ground, as close as possible to the DC2 pin.
22	V_P	Charge Pump Power Supply.
23	R_{SET}	Maximum Charge Pump Current Setting Resistor. Connecting a resistor between the R_{SET} pin and GND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is $I_{CP\_MAX} = 12.96/R_{SET}$. For example, with R_{SET} = 2.7 kΩ, $I_{CP\ MAX}$ = 4.8 mA. The relationship between bleed current (I_{BLEED}) and R_{SET} is $I_{BLEED\_MIN} = 0.0103/R_{SET}$. For example, with R_{SET} = 2.7 kΩ, I_{BLEED_MIN} = 3.81 µA.

Pin No.	Mnemonic	Description
24	CP	Charge Pump Output. When enabled, this pin provides $\pm I_{CP}$ to the external loop filter, which in turn drives the external VCO.
	EPAD	Exposed Pad. The exposed pad must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

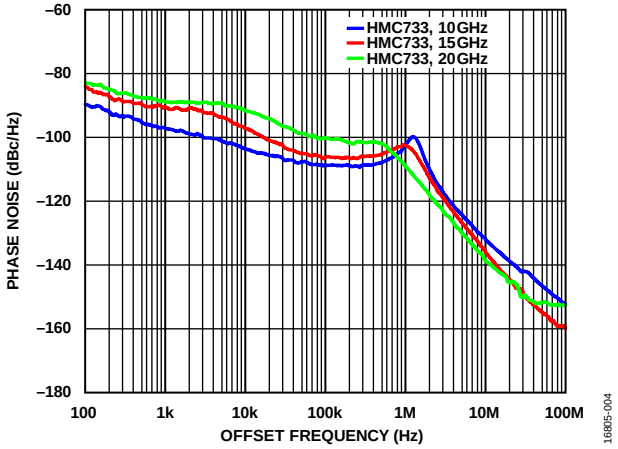

Figure 4. Phase Noise vs. Offset Frequency at 10 GHz, 15 GHz, and 20 GHz with the HMC733, I_{CP} = 3.5 mA, Integer N Mode

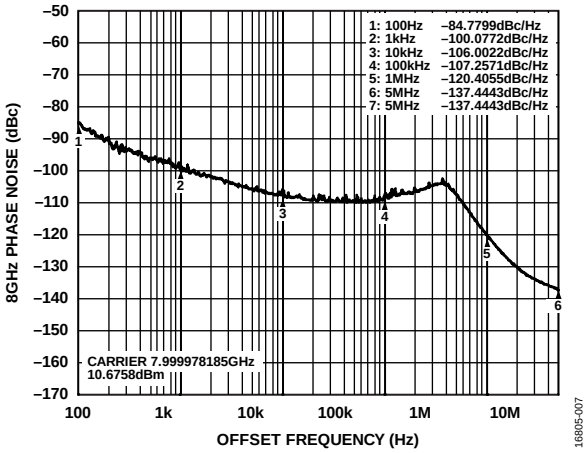

Figure 7. 8 GHz Phase Noise vs. Offset Frequency with the HMC509, I_{CP} = 3.5 mA, Fractional-N Mode

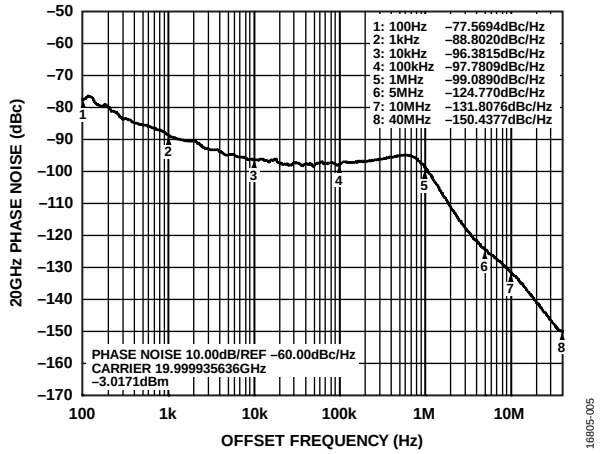

Figure 5. 20 GHz Phase Noise vs. Offset Frequency with the HMC733, I_{CP} = 3.5 mA, Fractional-N Mode

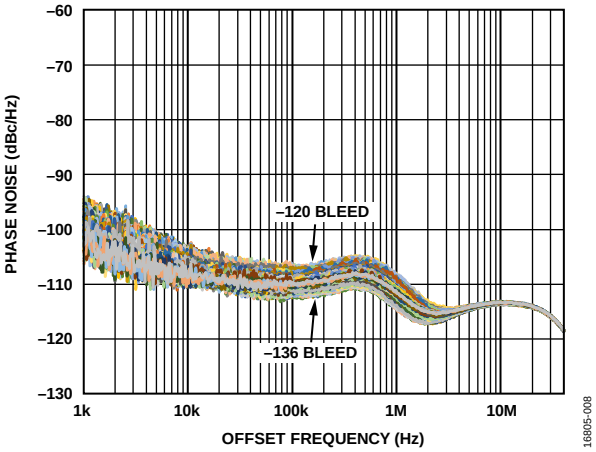

Figure 8. Phase Noise vs. Offset Frequency for Various Bleeds

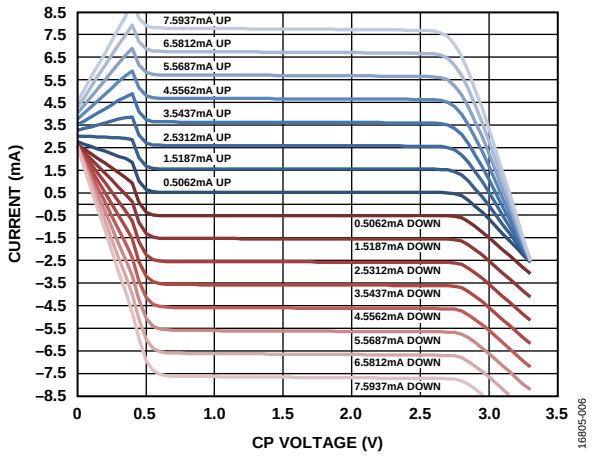

Figure 6. Current vs. CP Voltage, Charge Pump Compliance, R_{SET} = 1.8 kΩ

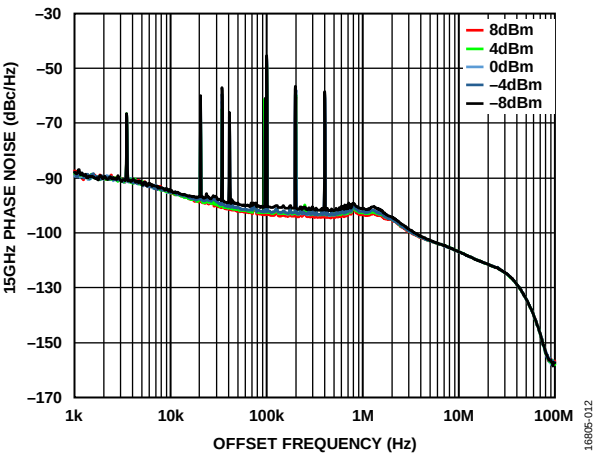

Figure 9. 15 GHz Phase Noise vs. Offset Frequency at Various REF_{IN} Powers, Fractional-N Mode, PFD = 100 MHz

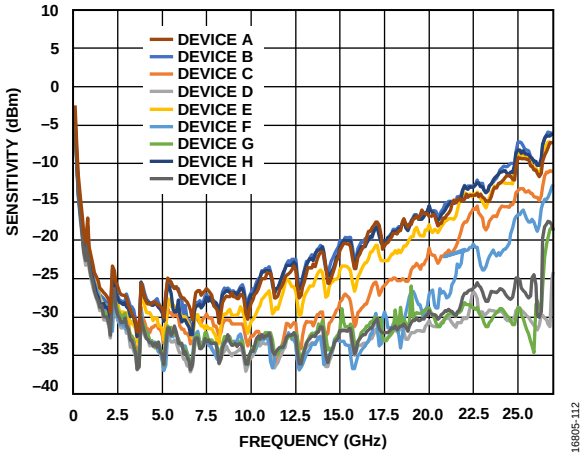

Figure 10. Sensitivity vs. Frequency for Multiple Soldered Devices

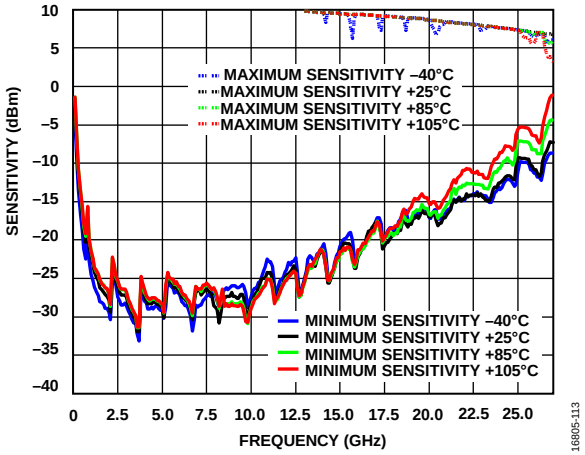

Figure 11. Sensitivity vs. Frequency at Various Temperatures for Device A

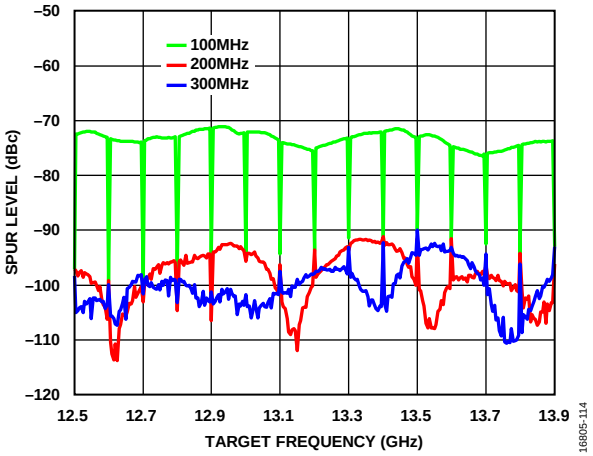

Figure 12. Spur Level vs. Target Frequency with the HMC584 VCO, REF_{IN} = 100 MHz, PFD = 100 MHz, PLL Loop BW = 80 kHz

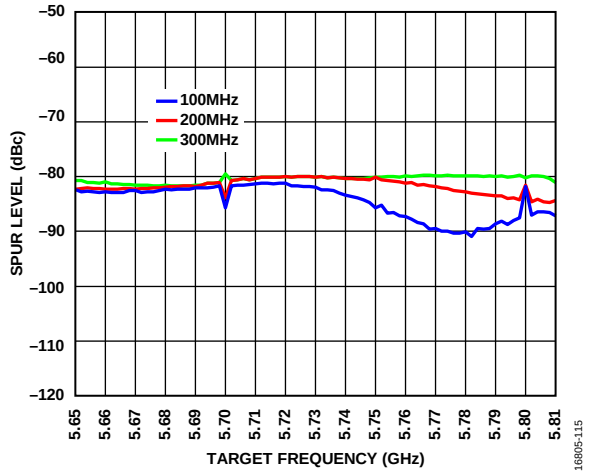

Figure 13. Spur Level vs. Target Frequency with Z-Communications V940ME03 VCO, REF_{IN} = 100 MHz, PFD = 100 MHz, PLL Loop BW = 80 kHz

THEORY OF OPERATION

REFERENCE INPUT

The reference input stage is shown in Figure 14. The reference input accepts an ac-coupled, single-ended signal. During power-down, this circuit remains active and draws the same current from AV_{DD4} as during normal operation. With no reference connected, AV_{DD4} drops to approximately 600 µA.

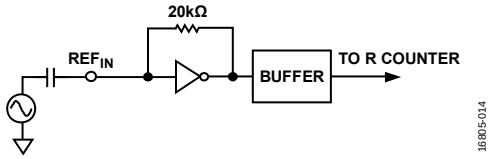

Figure 14. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 15. A two-stage limiting amplifier follows the RF input stage to generate the current mode logic (CML) clock levels needed for the prescaler. The $RF_{IN}A$ and $RF_{IN}B$ inputs require dc blocking capacitors to isolate the 1.65 V bias level from the input signal.

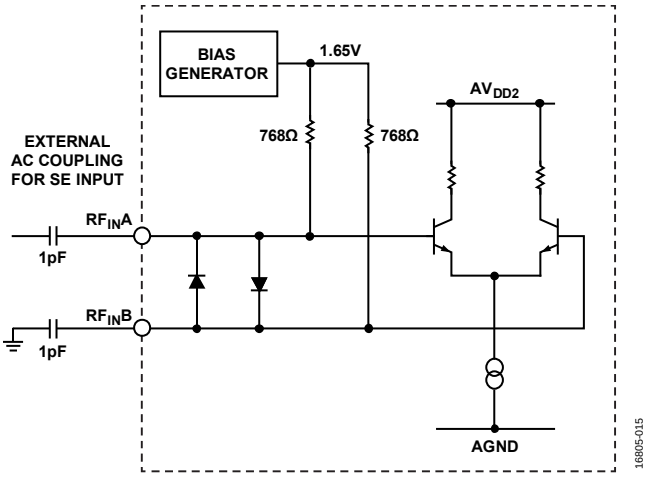

Figure 15. RF Input Stage

N DIVIDER AND R COUNTER

The N divider is used to divide the RF input signal down to the PFD frequency (f_{PFD}).

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \quad (1)$$

where:
REF_{IN} is the reference input frequency.
D is the REF_{IN} doubler bit value (0 or 1).
R is the preset divide ratio of the binary 5-bit programmable reference counter (1 to 32).
T is the REF_{IN} divide by 2 bit value (0 or 1).

The N divider value is generated by a Σ-Δ modulator. The ADF41513 contains two selectable Σ-Δ modulators. One modulator has a 25-bit fixed modulus (see Figure 16) and one has a variable modulus up to 49 bits (see Figure 17). Register 0, Bit 28 selects the modulator.

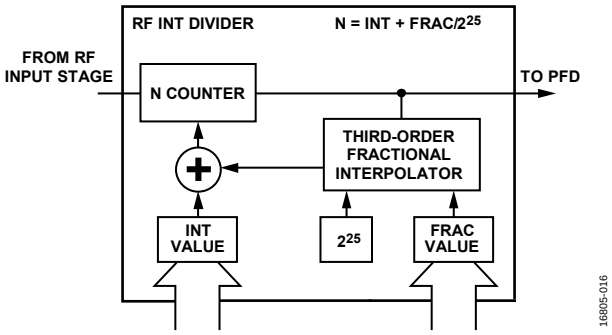

Figure 16. Fixed Modulus N Divider

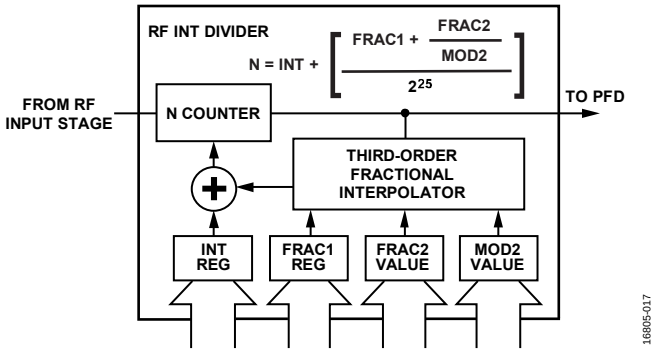

Figure 17. Variable Modulus N Divider

25-Bit Fixed Modulus (Register 0, Bit 28 = 0)

For the 25-bit fixed modulus, the RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = f_{PFD} \times (INT + (FRAC/2^{25})) \quad (2)$$

where:
RF_{OUT} is the RF VCO frequency.
INT is a 16-bit value set by Bits[19:4] in Register 0. In Integer N mode, *INT* is 20 to 511 for a 4/5 prescaler and 64 to 1023 for a 8/9 prescaler, and in fractional-N mode, *INT* is 23 to 511 for a 4/5 prescaler and 75 to 1023 for a 8/9 prescaler.
FRAC is a 25-bit value set by Bits[28:4], FRAC1, in Register 1.

The minimum RF output resolution is set by $f_{PFD}/2^{25}$. For example, if f_{PFD} = 100 MHz, the minimum resolution is 2.98 Hz.

By default, due to the architecture of the Σ-Δ modulator, there is a fixed ($f_{PFD}/2^{26}$) offset added or subtracted from the programmed output frequency. To remove this offset, set LSB_PI (Register 5, Bit 24).

Variable Modulus (R0, DB28 = 1)

For the variable modulus, the RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = f_{PFD} \times (INT + (FRAC1 + (FRAC2/MOD2))/2^{25}) \quad (3)$$

where:
RF_{OUT} is the output frequency of external VCO.
INT is a 16-bit value set by Bits[19:4] in Register 0. In Integer N mode, *INT* is 20 to 511 for a 4/5 prescaler and 64 to 1023 for a 8/9 prescaler, and in fractional-N mode, *INT* is 23 to 511 for a 4/5 prescaler and 75 to 1023 for a 8/9 prescaler.
FRAC1 is a 25-bit value set by Bits[28:4] in Register 1.
FRAC2 is a 24-bit value set by Bits[27:4] in Register 3.
MOD2 is a 24-bit value set by Bits[27:4] in Register 4.

The minimum RF output resolution is set by $f_{PFD}/2^{49}$. Therefore, for f_{PFD} = 100 MHz, the minimum resolution is 0.1776 μHz. To achieve this resolution, MOD2 must be set to its maximum of $(2^{24} - 1)$, which is 16,777,215.

Integer N Mode

When FRAC1 and FRAC2 are both equal to 0, the ADF41513 can operate in purely integer N mode, which improves the phase noise performance of the PLL and sets the frequency resolution to f_{PFD}. This feature is not automatic and must be manually set for Integer N channels. Bleed must also be disabled when using the ADF41513 in Integer N operation. See the Register 12 (R12) Map section for more information on programming the ADF41513 for Integer N operation.

R COUNTER

The 5-bit R counter allows REF_{IN} to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

PFD AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between these inputs. Figure 18 shows a PFD simplified schematic. The PFD includes a fixed delay element that sets the width of the antibacklash pulse, which is typically 1 ns. This pulse ensures that there is no dead zone in the PFD transfer function and produces a consistent reference spur level.

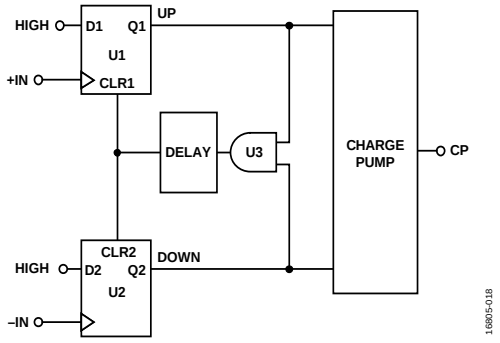

Figure 18. PFD Simplified Schematic

MUXOUT

The output multiplexer on the ADF41513 allows the user to access various internal nodes on the chip. The M4, M3, M2, and M1 bits in Register 12 (see the Register 12 (R12) Map section) controls the state of MUXOUT. Figure 19 shows the MUXOUT section in block diagram form. Many of these access points are useful for debugging. For example, select the N divider output to check if the N divider is functioning correctly. Most of the access points are self explanatory. Set the CLK_1 divider output signal to access the internal CLK_1 divider signal used for phase resync. During power-down (CE = logic low), MUXOUT is set to GND.

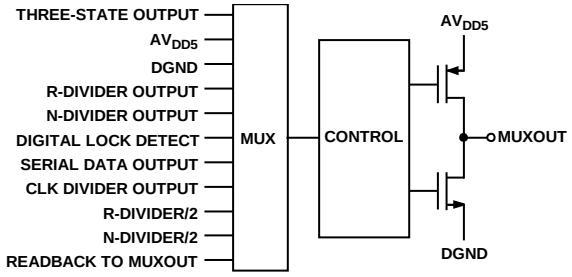

Figure 19. MUXOUT Schematic

LOCK DETECTOR

The lock detector compares the PFD output pulse width against a lock detector window. Measurements are performed every PFD comparison cycle when LD_CLK_SEL = 0 or every 32nd cycle when LD_CLK_SEL = 1. If the pulse width falls within the lock window, a counter is incremented. If the counter reaches the count set by LD_COUNT without an up or down pulse width exceeding the lock detect window and without a cycle slip occurring, lock is then declared by the lock detector.

When the lock detector has declared lock, the main mechanism to declare a loss of lock is for a cycle slip to occur. This cycle slip is usually caused by a frequency error at the phase detector input, causing the phase error to grow until the error exceeds 360°. The phase error then wraps around to 0°. This phase wrap around is a cycle slip.

A high level on MUXOUT indicates the PLL is in lock.

The lock detector window size, LD_COUNT, and LD_CLK_SEL all affect the sensitivity of the lock detector. Larger windows, smaller LD_COUNT values, and LD_CLK_SEL = 0 shorten the overall lock detect time and increase sensitivity. Smaller windows, larger LD_COUNT values, and LD_CLK_SEL = 1 increase the overall lock detect time and reduce sensitivity. Excessive lock detector sensitivity can cause multiple transitions between a locked state and out of lock state during frequency changes. Insufficient lock detector sensitivity can cause the detector to indicate an out of lock state when, in fact, the PLL is locked.

The window size can be adjusted between 0.9 ns and 11.5 ns with LDP, Bits[9:8] in Register 6 and LD bias, Bits[31:30] in Register 9. The ideal window size is halfway between the maximum window, set by the phase comparison period, t_{PFD} (10 ns for 100 MHz reference and R = 1), and the minimum is set by

$$(I_{BLEED}/I_{CP}) \times t_{PFD} \quad (4)$$

LD_COUNT can range from 2 counts to 8192 counts. The fastest lock indication requires two measurement cycles (20 ns with 100 MHz reference, R = 1, and LD_CLK_SEL = 0). In practice, the lock indication takes much longer because of the loop filter on the phase comparator. When LD_CLK_SEL = 1, a minimum 64 measurements are required (640 ns).

READBACK

Register data can be read by setting MUXOUT to serial data output. In this mode, the MUXOUT line concurrently transfers 32 bits of the previous written register value while clocking in 32 bits of write data.

To read back a specific register, chip revision code, or bit pattern, write 1000b to Bits[31:28], Register 12. Bits[19:14] in Register 12 set the data that is output from the MUXOUT pin when in readback mode.

To prevent spurious writes, the DATA pin must be held at logic low while a readback is taking place.

INPUT SHIFT REGISTERS

The ADF41513 contains a programmable digital block. Data is clocked into the 32-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to the chosen register on the rising edge of LE. The destination latch is determined by the state of the four control bits (C4, C3, C2, and C1) in the shift register. The following are the four LSBs: DB3, DB2, DB1, and DB0. The truth table for these bits is shown in Table 6. Figure 20 through Figure 22 show a summary of how the registers are programmed.

PROGRAM MODES

Table 6 and Figure 23 through Figure 36 show how to set up the program modes in the ADF41513.

Several settings in the ADF41513 are double buffered. These settings include MOD2, FRAC1, FRAC2, R counter value, reference doubler, CP current setting, RDIV2, phase word, prescaler, and CLK_1 divider. Two events must occur before the device uses a new value for any of the double buffered settings. First, the new value is latched into the device by writing to the appropriate register. Second, a new write must be performed on Register 0. For example, updating the FRAC1 value requires a write to Register 1 and a write to Register 0. Write to Register 1 first, followed by the write to Register 0. The frequency change begins after the write to Register 0. Double buffering ensures that the bits written to Register 1 do not take effect until after the write to Register 0.

Table 6. C4, C3, C2, and C1 Truth Table

Control Bits				
C4	**C3**	**C2**	**C1**	**Register**
0	0	0	0	R0
0	0	0	1	R1
0	0	1	0	R2
0	0	1	1	R3
0	1	0	0	R4
0	1	0	1	R5
0	1	1	0	R6
0	1	1	1	R7
1	0	0	0	R8
1	0	0	1	R9
1	0	1	0	R10
1	0	1	1	R11
1	1	0	0	R12
1	1	0	1	R13

REGISTER MAPS

INT REGISTER (R0)

RESERVED			VARIABLE MODULUS	RESERVED								16-BIT INTEGER VALUE (INT)															CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	V1	0	0	0	0	0	0	0	0	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	C4(0)	C3(0)	C2(0)	C1(0)

FRAC1 REGISTER (R1)

DITHER2	RESERVED		25-BIT FRAC1 VALUE (FRAC1) DBB																								CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
D1	0	0	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C4(0)	C3(0)	C2(0)	C1(1)

PHASE REGISTER (R2)

PHASE ADJUST	RESERVED															12-BIT PHASE VALUE (PHASE) DBB												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
PA1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C4(0)	C3(0)	C2(1)	C1(0)

FRAC2 REGISTER (R3)

RESERVED				24-BIT FRAC2 VALUE (FRAC2) DBB																								CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C4(0)	C3(0)	C2(1)	C1(1)

MOD2 REGISTER (R4)

RESERVED				24-BIT MOD2 VALUE (MOD2) DBB																								CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	M24	M23	M22	M21	M20	M19	M18	M17	M16	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C4(0)	C3(1)	C2(0)	C1(0)

NOTES
1. DBB MEANS DOUBLE-BUFFERED BITS.

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Figure 20. Register Summary for Register 0 (R0) to Register 4 (R4)

R DIVIDER REGISTER (R5)

DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DLD MODES		RESERVED	DBB CP CURRENT SETTING				LSB_P1	DBB PRESCALER	RDIV2 DBB	REFERENCE DOUBLER DBB	DBB 5-BIT R COUNTER					DBB 12-BIT CLK_1 DIVIDER VALUE													CONTROL BITS			
DL2	DL1	0	CPI4	CPI3	CPI2	CPI1	L1	P1	U2	U1	R5	R4	R3	R2	R1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C4(0)	C3(1)	C2(0)	C1(1)

FUNCTION REGISTER (R6)

DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BLEED CURRENT								BLEED POLARITY	BLEED ENABLE	RESERVED	INT MODE	ABP	LOL ENABLE	SD RESET	CP THREE-STATE PD ON	RESERVED						LDP		PD POLARITY	POWER DOWN	CP THREE-STATE COUNTER RESET		CONTROL BITS			
BC8	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BP1	BE1	0	IM1	A1	LOL1	SD1	CP1	1	0	0	0	0	0	LDP2	LDP1	PP1	PD	C31	CR1	C4(0)	C3(1)	C2(1)	C1(0)

CLOCK 2 REGISTER (R7)

DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RESERVED		LD_COUNT			LD_CLK_SEL	RESERVED		N DELAY		PS BIAS		CLK DIVIDER MODE		12-BIT CLK_2 DIVIDER VALUE												CLK DIV SEL		CONTROL BITS			
0	0	CN3	CN2	CN1	LD1	0	0	ND2	ND1	PB2	PB1	C2	C1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	CS2	CS1	C4(0)	C3(1)	C2(1)	C1(1)

RESERVED REGISTER (R8)

DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RESERVED																												CONTROL BITS			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(0)	C1(0)

RESERVED REGISTER (R9)

DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
LD BIAS		RESERVED																										CONTROL BITS			
LB2	LB1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(0)	C1(0)

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NOTES
1. DBB MEANS DOUBLE-BUFFERED BITS.

Figure 21. Register Summary for Register 5 (R5) to Register 9 (R9)

RESERVED REGISTER (R10)

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(1)	C1(0)

RESERVED REGISTER (R11)

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
PDS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(1)	C1(1)

MUXOUT REGISTER (R12)

MUXOUT				LOGIC LEVEL	RESERVED				MASTER RESET	RESERVED	LE SELECT	READBACK SELECT						RESERVED											CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
M4	M3	M2	M1	LL	0	0	0	0	MR1	0	L1	R6	R5	R4	R3	R2	R1	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(1)	C2(0)	C1(0)

RESERVED REGISTER (R13)

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(1)	C2(0)	C1(1)

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Figure 22. Register Summary for Register 10 (R10) to Register 13 (R13)

REGISTER 0 (R0) MAP

Frequency changes occur only on a write to Register 0.

Variable Modulus

Register 0, Bit 28 = 0 enables the 25-bit fixed modulus. Register 0, Bit 28 = 1 enables the variable modulus. See the N Divider and R Counter section for more information.

INT Value

Register 0, Bits[19:4] set the INT value. See the N Divider and R Counter section for more information.

REGISTER 1 (R1) MAP

DITHER2

Set Register 1, Bit 31 = 1 to enable the Σ-Δ modulator dither. Enabling DITHER2 can reduce fractional spurs.

FRAC1

Register 1, Bits[28:4] set the FRAC1 value. See the N Divider and R Counter section for more information. When using a fixed modulus, Bits[28:4] are the FRAC value.

INT REGISTER (R0)

RESERVED			VARIABLE MODULUS	RESERVED								16-BIT INTEGER VALUE (INT)															CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	V1	0	0	0	0	0	0	0	0	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	C4(0)	C3(0)	C2(0)	C1(0)

V1	VARIABLE MODULUS
0	25-BIT FIXED MODULUS
1	VARIABLE MODULUS

N16	N15	N14	N13	N12	N11	N10	···	N5	N4	N3	N2	N1	INTEGER WORD
0	0	0	0	0	0	0	...	0	0	0	0	0	NOT ALLOWED
0	0	0	0	0	0	0	...	0	0	0	0	1	NOT ALLOWED
0	0	0	0	0	0	0	...	0	0	0	1	0	NOT ALLOWED
.	.	.	.	.	.	.	...	.	.	.	.	.	.
0	0	0	0	0	0	0	...	1	0	0	1	1	NOT ALLOWED
0	0	0	0	0	0	0	...	1	0	1	0	0	20
0	0	0	0	0	0	0	...	1	0	1	0	1	21
.	.	.	.	.	.	.	...	.	.	.	.	.	.
0	0	0	0	0	0	1	...	1	1	1	1	0	1022
0	0	0	0	0	0	1	...	1	1	1	1	1	1023
0	0	0	0	0	1	0	...	0	0	0	0	0	NOT ALLOWED
.	.	.	.	.	.	.		.	.	.	.	.	.
1	1	1	1	1	1	1	...	1	1	1	1	1	NOT ALLOWED

INTEGER N MODE
PRESCALER 4/5: 20 ≤ INT ≤ 511
PRESCALER 8/9: 64 ≤ INT ≤ 1023
FRACTIONAL-N MODE
PRESCALER 4/5: 23 ≤ INT ≤ 511
PRESCALER 8/9: 75 ≤ INT ≤ 1023

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Figure 23. Register 0 (R0) Map

FRAC1 REGISTER (R1)

DITHER2	RESERVED																											CONTROL BITS			
																											DBB				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
D1	0	0	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C4(0)	C3(0)	C2(0)	C1(1)

D1	DITHER2
0	OFF
1	ON

F25	F24	···	F2	F1	FRAC1 WORD
0	0	...	0	0	0
0	0	...	0	1	1
0	0	...	1	0	2
0	0	...	1	1	3
.	.	...	.	.	.
.	.	...	.	.	.
.	.	...	.	.	.
1	1	...	0	0	33,554,428
1	1	...	0	1	33,554,429
1	1	...	1	0	33,554,430
1	1	...	1	1	33,554,431

NOTES
1. DBB MEANS DOUBLE-BUFFERED BITS.

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Figure 24. Register 1 (R1) Map

REGISTER 2 (R2) MAP

Phase Adjust

Set Register 2, Bit 31 to 1 to enable phase adjust. Phase adjust increases the phase of the output relative to the current phase. The phase change occurs after a write to Register 0.

$$Phase\ Shift = (Phase\ Value \times 360°)/2^{12} \quad (5)$$

Phase Value

Register 2, Bits[15:4] set the phase value for phase adjust. For example, setting the phase value = 512 increases the output phase by 45°.

If phase adjust is not used, set the phase value to 0.

REGISTER 3 (R3) MAP

FRAC2

Register 3, Bits[27:4] set the FRAC2 value. See the N Divider and R Counter section for more information. When using a fixed modulus, FRAC2 is ignored.

PHASE REGISTER (R2)

PHASE ADJUST	RESERVED	DBB 12-BIT PHASE VALUE (PHASE)	CONTROL BITS

DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
PA1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C4(0)	C3(0)	C2(1)	C1(0)

PA1	PHASE ADJUST
0	DISABLED
1	ENABLED

P12	P11	...	P2	P1	PHASE VALUE
0	0	...	0	0	0
0	0	...	0	1	1
0	0	...	1	0	2
0	0	...	1	1	3
.	.	...	.	.	.
.	.	...	.	.	.
.	.	...	.	.	.
1	1	...	0	0	4,092
1	1	...	0	1	4,093
1	1	...	1	0	4,094
1	1	...	1	1	4,095

NOTES
1. DBB MEANS DOUBLE-BUFFERED BITS.

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Figure 25. Register 2 (R2) Map

FRAC2 REGISTER (R3)

RESERVED	DBB 24-BIT FRAC2 VALUE (FRAC2)	CONTROL BITS

DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C4(0)	C3(0)	C2(1)	C1(1)

F24	F23	...	F2	F1	FRAC2 WORD
0	0	...	0	0	0
0	0	...	0	1	1
0	0	...	1	0	2
0	0	...	1	1	3
.	.	...	.	.	.
.	.	...	.	.	.
.	.	...	.	.	.
1	1	...	0	0	16,777,212
1	1	...	0	1	16,777,213
1	1	...	1	0	16,777,214
1	1	...	1	1	16,777,215

NOTES
1. DBB MEANS DOUBLE-BUFFERED BITS.

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Figure 26. Register 3 (R3) Map

REGISTER 4 (R4) MAP

MOD2

Register 4, Bits[27:4] set the MOD2 value. See the N Divider and R Counter section for more information. When using a fixed modulus, MOD2 is ignored.

REGISTER 5 (R5) MAP

DLD Modes

Register 5, Bits[31:30] set the digital lock detect (DLD) pin state. For normal digital lock detect, set Register 5, Bits[31:30] = 0b01. Other options tristate the pin and force a high or low logic level, as shown in Figure 28.

CP Current Setting

Register 5, Bits[28:25] set the charge pump current. Set these bits to the charge pump current that the loop filter is designed for based on the application of the user. The recommended practice is to design the loop filter for a charge pump current of 2.4 mA or 2.7 mA and then use the programmable charge pump current to fine tune the loop filter frequency response.

LSB_P1

Register 5, Bit 24 = 0 enables a 26th bit in the fixed modulus MOD value. Enabling the 26th bit reduces fractional spurs but the reduction also adds a fixed $f_{PFD}/2^{26}$ frequency offset to the output frequency. To disable this frequency offset, set Register 5, Bit 24 = 1.

Prescaler

The dual modulus prescaler (4/5 and 8/9) is set by Register 5, Bit 23. The prescaler, at the input to the N divider, divides down the f_{RFIN} signal so that the N divider can operate correctly. The prescaler is based on a synchronous 4/5 core. The prescaler setting affects the RF frequency and the minimum and maximum INT value as follows:

For Integer N mode,

- Prescaler 4/5: 20 ≤ INT ≤ 511, f_{RFIN_MAX} = 16 GHz
- Prescaler 8/9: 64 ≤ INT ≤ 1023, f_{RFIN_MAX} = 26.5 GHz

For fractional-N mode,

- Prescaler 4/5: 23 ≤ INT ≤ 511, f_{RFIN_MAX} = 16 GHz
- Prescaler 8/9: 75 ≤ INT ≤ 1023, f_{RFIN_MAX} = 26.5 GHz

RDIV2

Register 5, Bit 22 controls the reference divide by 2 block. See the N Divider and R Counter section for more information. This feature can provide a 50% duty cycle signal to the PFD.

Reference Doubler

Register 5, Bit 21 controls the reference doubler block. See the N Divider and R Counter section for more information.

R Counter

Register 5, Bits[20:16] control the R counter value. See the N Divider and R Counter section for more information.

CLK_1 Divider

Register 5, Bits[15:4] control the CLK_1 divider value. See the Phase Resync section for more information.

MOD2 REGISTER (R4)

RESERVED				24-BIT MOD2 VALUE (MOD2)																						CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	M24	M23	M22	M21	M20	M19	M18	M17	M16	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C4(0)	C3(1)	C2(0)	C1(0)

DBB

M24	M23	...	M2	M1	MOD2 WORD
0	0	...	0	0	0
0	0	...	0	1	1
0	0	...	1	0	2
0	0	...	1	1	3
.	.	...	.	.	.
.	.	...	.	.	.
.	.	...	.	.	.
1	1	...	0	0	16,777,212
1	1	...	0	1	16,777,213
1	1	...	1	0	16,777,214
1	1	...	1	1	16,777,215

NOTES
1. DBB MEANS DOUBLE-BUFFERED BITS.

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Figure 27. Register 4 (R4) Map

R DIVIDER REGISTER (R5)

DLD MODE	RESERVED	CP CURRENT SETTING (DBB)	LSB_P1	PRESCALER (DBB)	RDIV2 DBB	REFERENCE DOUBLER DBB	5-BIT R COUNTER (DBB)	12-BIT CLK_1 DIVIDER VALUE (DBB)	CONTROL BITS
DB31	DB30	DB29	DB28 DB27 DB26 DB25	DB24	DB23	DB22	DB21	DB20 DB19 DB18 DB17 DB16	DB15 DB14 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4	DB3 DB2 DB1 DB0
DL2	DL1	0	CPI4 CPI3 CPI2 CPI1	L1	P1	U2	U1	R5 R4 R3 R2 R1	D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	C4(0) C3(1) C2(0) C1(1)

DL2	DL1	DLD PIN
0	0	TRISTATE
0	1	DIGITAL LOCK DETECT
1	0	LOW
1	1	HIGH

U1	REFERENCE DOUBLER
0	DISABLED
1	ENABLED

U2	R DIVIDER
0	DISABLED
1	ENABLED

P1	PRESCALER
0	4/5
1	8/9

L1	LSB P1
0	ON: 0.5 LSB OFFSET
1	OFF: NO OFFSET

D12	D11	...	D2	D1	CLK_1 DIVIDER VALUE
0	0	...	0	0	0
0	0	...	0	1	1
0	0	...	1	0	2
0	0	...	1	1	3
.	.	...	.	.	.
.	.	...	.	.	.
.	.	...	.	.	.
1	1	...	0	0	4,092
1	1	...	0	1	4,093
1	1	...	1	0	4,094
1	1	...	1	1	4,095

R5	R4	R3	R2	R1	R COUNTER DIVIDE RATIO
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31
0	0	0	0	0	32

CPI4	CPI3	CPI2	CPI1	I_{CP} (mA) 2.7kΩ	I_{CP} (mA) 1.8kΩ
0	0	0	0	0.3	0.45
0	0	0	1	0.6	0.90
0	0	1	0	0.9	1.35
0	0	1	1	1.2	1.80
0	1	0	0	1.5	2.25
0	1	0	1	1.8	2.70
0	1	1	0	2.1	3.15
0	1	1	1	2.4	3.60
1	0	0	0	2.7	4.05
1	0	0	1	3.0	4.50
1	0	1	0	3.3	4.95
1	0	1	1	3.6	5.40
1	1	0	0	3.9	5.85
1	1	0	1	4.2	6.30
1	1	1	0	4.5	6.75
1	1	1	1	4.8	7.20

NOTES
1. DBB MEANS DOUBLE-BUFFERED BITS.

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Figure 28. Register 5 (R5) Map

REGISTER 6 (R6) MAP

Bleed Current

Register 6, Bits[31:24] set the bleed current. If the PD polarity is set to positive, the optimum bleed current is set by

$$Bleed\ Value = \text{floor}(90 \times (f_{PFD}/100\ \text{MHz}) \times (I_{CP\_CODE} + 1)/16) \quad (6)$$

where:
Bleed Value is the value programmed to Register 6, Bits[31:24].
I_{CP_CODE} is the charge pump current setting programmed to Register 5, Bits[28:25].
f_{PFD} is the PFD frequency in MHz.

If the PD polarity is set to negative, the optimum bleed current is set by

$$Bleed\ Value = \text{floor}(144 \times (f_{PFD}/100\ \text{MHz}) \times (I_{CP\_CODE} + 1)/16) \quad (7)$$

Bleed Polarity

Register 6, Bit 23 controls the polarity of the bleed current. Negative polarity is the typical usage.

Bleed Enable

In fractional-N mode of operation, charge pump linearity (and ultimately phase noise and spurious performance) is improved if the VCO and reference inputs to the phase detector operate with a phase offset. This phase offset is implemented by adding a constant bleed current at the output of the charge pump. Use bleed only when operating in fractional-N mode, that is, FRAC1 or FRAC2 not equal to 0. Set Register 6, Bit 22 = 1 to enable bleed.

INT Mode

Register 6, Bit 20 completely disables the fractional-N Σ-Δ modulator (SDM). Setting Register 6, Bit 20 = 1 disables the SDM so the ADF41513 operates purely in integer N mode. Disabling the SDM improves phase noise performance and changes the frequency resolution to f_{PFD}.

ABP

Register 6, Bit 19 affects the antibacklash pulse (ABP) width. The recommended setting for best figure of merit (FOM) is narrow (Register 6, Bit 19 = 1).

Loss of Lock (LOL) Enable

If digital lock detect is asserted when loss of lock is enabled and the reference signal is removed, digital lock detect goes low. Set Register 6, Bit 18 = 1 to enable loss of lock (recommended).

Sigma-Delta (SD) Reset

When Register 6, Bit 17 = 0 on a write to Register 0, the SDM is temporarily set to a fractional value of 0. The SD reset ensures a consistent fractional spur pattern but also results in a glitch in the output frequency when the N divider momentarily outputs FRAC = 0. Remove this glitch by setting Register 6, Bit 17 = 1 (recommended setting).

CP Three-State, PD on

When Register 6, Bit 16 = 1, the charge pump is in three-state mode but the phase detector (PD) is still operational. Set Register 6, Bit 16 = 0 for normal operation.

Lock Detector Precision (LDP)

Register 6, Bits[9:8] and Register 9, Bits[31:30] control the sensitivity of the digital lock detector. Lock detect precision (Register 6, Bits[9:8]) in conjunction with lock detector bias (Register 9, Bits[31:30]) adjusts the width of the digital lock detector window. Lock is declared when the PFD reference arrival time and divided VCO input arrival times consistently differ by less than the LDP value. Small LDP settings may cause a false out of lock indication when used with large bleed currents. See the Lock Detector section for more information.

Phase Detector (PD) Polarity

If using a noninverting loop filter and a VCO with a positive tuning slope, set the PD polarity to positive.

If using an inverting loop filter and a VCO with a negative tuning slope, set the PD polarity to positive.

If using a noninverting loop filter and a VCO with a negative tuning slope, set the PD polarity to negative.

If using an inverting loop filter and a VCO with a positive tuning slope, set the PD polarity to negative.

Power Down

Set Register 6, Bit 6 = 1 to perform a software power-down. All circuit blocks are disabled, and the chip enters a low power state drawing approximately 4 mA. Set Register 6, Bit 6 = 0 to reenable the chip. Register values are not lost during power-down. Only one power-down mode is available via Register 11, Bit 31. Set Register 11, Bit 31 = 1 to leave the internal 1.8 V N divider regulator on during power-down.

Note that Register 12, Bit 20 must be set to 0 when writing this power-down bit. Otherwise, the chip cannot be powered back on again by setting Register 6, Bit 6 = 0.

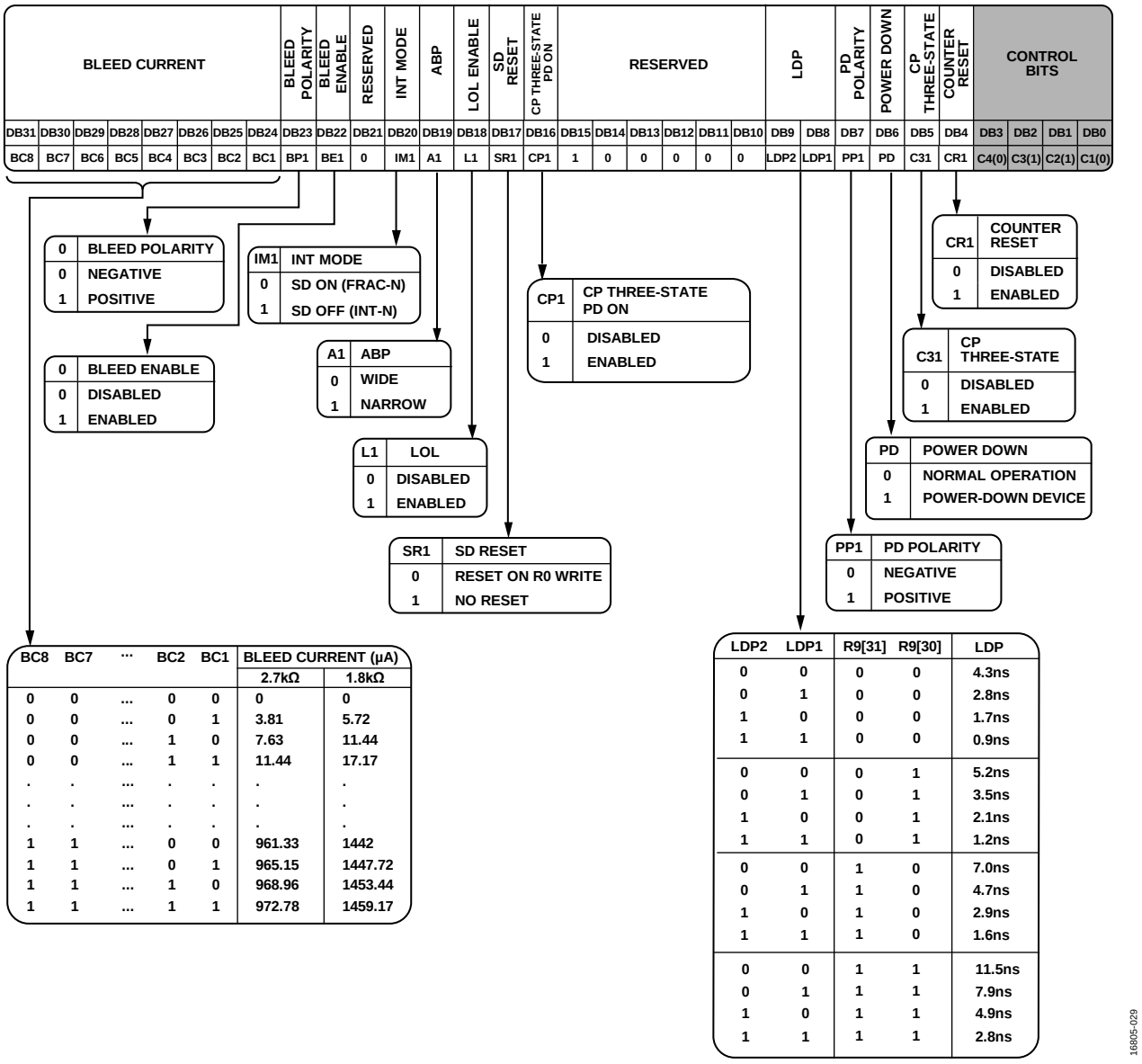
CP Three-State

Setting Register 6, Bit 5 = 1 puts the charge pump into three-state mode. Set Register 6, Bit 5 = 0 for normal operation.

Counter Reset

Setting Register 6, Bit 4 = 1 holds the N divider and R counter in reset, which results in no signals being received at the PFD.

FUNCTION REGISTER (R6)



BC8	BC7	...	BC2	BC1	BLEED CURRENT (µA)	
					2.7kΩ	1.8kΩ
0	0	...	0	0	0	0
0	0	...	0	1	3.81	5.72
0	0	...	1	0	7.63	11.44
0	0	...	1	1	11.44	17.17
.	.	...	.	.	.	.
.	.	...	.	.	.	.
.	.	...	.	.	.	.
1	1	...	0	0	961.33	1442
1	1	...	0	1	965.15	1447.72
1	1	...	1	0	968.96	1453.44
1	1	...	1	1	972.78	1459.17

LDP2	LDP1	R9[31]	R9[30]	LDP
0	0	0	0	4.3ns
0	1	0	0	2.8ns
1	0	0	0	1.7ns
1	1	0	0	0.9ns
0	0	0	1	5.2ns
0	1	0	1	3.5ns
1	0	0	1	2.1ns
1	1	0	1	1.2ns
0	0	1	0	7.0ns
0	1	1	0	4.7ns
1	0	1	0	2.9ns
1	1	1	0	1.6ns
0	0	1	1	11.5ns
0	1	1	1	7.9ns
1	0	1	1	4.9ns
1	1	1	1	2.8ns

Figure 29. Register 6 (R6) Map

REGISTER 7 (R7) MAP

Lock Detector Count (LD_COUNT)

LD_COUNT sets the initial value of the lock detect counter. See the Lock Detector section for more information about the operation of the lock detector.

Lock Detect Clock Select (LD_CLK_SEL)

The lock detector checks for lock on every phase comparison cycle when LD CLK SEL = 1. Otherwise, the lock detector checks for lock on every 32nd cycle. Use LD CLK SEL = 1 to speed up declaration of lock at the cost of reduced lock indication stability during frequency changes.

SDM to N Divider Timing Adjustment (N Delay)

This control adjusts the timing between the SDM output and the N divider. Set these bits to 0b01.

Prescaler (PS) Bias

Set these bits to 0b10.

CLK Divider Mode

Setting Register 7, Bits[19:18] = 0b10 enables a phase resync. See the Phase Resync section for more information.

When not using phase resync, set Register 7, Bits[19:18] = 0b00.

CLK_2 Divider Value

Register 7, Bits[17:6] control the CLK_2 divider value. The CLK_2 divider value controls the timing of the phase resync pulse. See the Phase Resync section for more information.

CLOCK 2 REGISTER (R7)

RESERVED	RESERVED	LD COUNT			LD CLK SEL	RESERVED		N DELAY		PS BIAS		CLK DIVIDER MODE		12-BIT CLK_2 DIVIDER VALUE												RESERVED		CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	LC3	LC2	LC1	LS1	0	0	ND2	ND1	PB2	PB1	C2	C1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	0	0	C4(0)	C3(1)	C2(1)	C1(1)

LC3	LC2	LC1	LOCK DETECTOR COUNT
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

LS1	LOCK DETECTOR CLOCK SELECT
0	$f_{PFD} \div 32$
1	f_{PFD}

ND2	ND1	SDM TO N DELAY
0	0	PROGRAM THIS VALUE
0	1	RESERVED
1	0	RESERVED
1	1	RESERVED

PB2	PB1	PRESCALER BIAS
0	0	RESERVED
0	1	RESERVED
1	0	PROGRAM THIS VALUE
1	1	RESERVED

C2	C1	CLK DIV MODE
0	0	CLK DIVIDER OFF
0	1	RESERVED
1	0	PHASE RESYNC
1	1	RESERVED

DB17	DB16	...	DB7	DB6	CLK_2 DIVIDER VALUE
0	0	...	0	0	0
0	0	...	0	1	1
0	0	...	1	0	2
0	0	...	1	1	3
.	.	...	.	.	.
.	.	...	.	.	.
.	.	...	.	.	.
1	1	...	0	0	4,092
1	1	...	0	1	4,093
1	1	...	1	0	4,094
1	1	...	1	1	4,095

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Figure 30. Register 7 (R7) Map

REGISTER 8 (R8) MAP

Set all reserved bits to zero.

REGISTER 9 (R9) MAP

Lock Detector Bias

The lock detector window size is set by adjusting the lock detector bias in conjunction with the lock detector precision bits (Register 6, Bits[9:8]). See the Lock Detector section.

RESERVED REGISTER (R8)

RESERVED																									CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(0)	C1(0)

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Figure 31. Register 8 (R8) Map

LOCK DETECTOR BIAS REGISTER (R9)

LD BIAS		RESERVED																									CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
LB2	LB1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(0)	C1(1)

LB2	LB1	LOCK DETECTOR BIAS
0	0	40µA
0	1	30µA
1	0	20µA
1	1	10µA

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Figure 32. Register 9 (R9) Map

REGISTER 10 (R10) MAP

Set all reserved bits to zero.

REGISTER 11 (R11) MAP

Power-Down Select

Only one power-down option is available. Program Register 11, Bit 31 = 1. Set Register 6, Bit 6 = 1 to power down the device.

RESERVED REGISTER (R10)

RESERVED																									CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(1)	C1(1)

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Figure 33. Register 10 (R10) Map

POWER-DOWN SELECT REGISTER (R11)

POWER-DOWN SELECT	RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
PDS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(1)	C1(1)

PDS	POWER-DOWN SELECT
0	RESERVED
1	PROGRAM THIS VALUE

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Figure 34. Register 11 (R11) Map

REGISTER 12 (R12) MAP

MUXOUT

Register 12, Bits[31:28] select the MUXOUT signal. Register data can be read either by selecting the serial data output or via a readback. Serial data output sends the 32 bits of register data that was written in the previous access. A readback sends the data as defined by the readback select bits, Register 12, Bits[19:14].

Logic Level

Register 12, Bit 27 selects the DLD and MUXOUT logic level.

Master Reset

Register 12, Bit 22 = 1 resets all registers to all zeros.

LE Select

Register 12, Bit 20 = 1 synchronizes the rising edge of LE on an SPI write with the falling edge of the reference signal. This recommended setting ensures there is no glitch from asynchronous loading. Set Register 12, Bit 20 = 0 if it is necessary to write data into the ADF41513 when no reference is present.

Readback Select

Register 12, Bits[19:14] select the value to be read back. For more information, see the Readback section.

MUXOUT REGISTER (R12)

MUXOUT				LOGIC LEVEL	RESERVED				MASTER RESET	RESERVED	LE SELECT	READBACK SELECT						RESERVED									CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
M4	M3	M2	M1	LL	0	0	0	0	MR1	0	L1	R6	R5	R4	R3	R2	R1	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(1)	C2(0)	C1(0)

LL	DLD AND MUXOUT LEVEL
0	1.8V LOGIC HIGH
1	3.3V LOGIC HIGH

L1	LE SEL
0	LE FROM PIN
1	LE SYNCHRONIZED WITH RISING EDGE OF R DIVIDER OUTPUT

MR1	MASTER RESET
0	NORMAL OPERATION
1	RESETS ALL REGISTERS

M4	M3	M2	M1	OUTPUT
0	0	0	0	THREE-STATE OUTPUT
0	0	0	1	DV_{DD}
0	0	1	0	DGND
0	0	1	1	R DIVIDER OUTPUT
0	1	0	0	N DIVIDER OUTPUT
0	1	0	1	RESERVED
0	1	1	0	DIGITAL LOCK DETECT
0	1	1	1	SERIAL DATA OUTPUT
1	0	0	0	READBACK
1	0	0	1	RESERVED
1	0	1	0	CLK1 DIVIDER OUTPUT
1	0	1	1	RESERVED
1	1	0	0	RESERVED
1	1	0	1	R DIVIDER/2
1	1	1	0	N DIVIDER/2
1	1	1	1	RESERVED

R6	R5	R4	R3	R2	R1	READBACK SELECT
0	0	0	0	0	0	32 ZEROS
0	0	0	0	0	1	R0
0	0	0	0	1	0	R1
0	0	0	0	1	1	R2
0	0	0	1	0	0	R3
0	0	0	1	0	1	R4
0	0	0	1	1	0	R5
0	0	0	1	1	1	R6
0	0	1	0	0	0	R7
0	0	1	0	0	1	R8
0	0	1	0	1	0	R9
0	0	1	0	1	1	R10
0	0	1	1	0	0	R11
0	0	1	1	0	1	R12
0	0	1	1	1	0	R13
0	0	1	1	1	1	INT (16-BIT R0[19:4] VALUE)
0	1	0	0	0	0	FRAC (7-BIT R1[10:4] VALUE)
0	1	0	0	0	1	32 ZEROS
0	1	0	0	1	0	RESERVED
0	1	0	0	1	1	REVISION CODE
0	1	0	1	0	0	RESERVED
0	1	0	1	0	1	RESERVED
0	1	0	1	1	0	RESERVED
0	1	0	1	1	1	RESERVED
0	1	1	0	0	0	RESERVED
1	0	0	1	0	1	RESERVED
1	0	0	1	1	1	RESERVED
1	0	1	0	0	0	RESERVED
1	1	0	1	0	1	RESERVED
1	1	0	1	1	0	RESERVED
1	1	0	1	1	1	RESERVED
1	1	1	0	0	0	RESERVED

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Figure 35. Register 12 (R12) Map

REGISTER 13 (R13) MAP

Set all reserved bits to zero.

RESERVED REGISTER (R13)

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(1)	C2(0)	C1(1)

16805-036

Figure 36. Register 13 (R13) Map

APPLICATIONS INFORMATION

INITIALIZATION SEQUENCE

The following sequence of registers is the correct sequence for initial power-up of the ADF41513 after the correct application of voltages to the supply pins:

1. Register 13
2. Register 12
3. Register 11
4. Register 10
5. Register 9
6. Register 8
7. Register 7
8. Register 6
9. Register 5
10. Register 4
11. Register 3
12. Register 2
13. Register 1
14. Register 0

RF SYNTHESIZER: A WORKED EXAMPLE OF 25-BIT FIXED MODULUS MODE

The following equation governs how to program the synthesizer:

$$RF_{OUT} = (INT + (FRAC1/2^{25})) \times f_{PFD} \quad (7)$$

where:
RF_{OUT} is the RF frequency output.
INT is the integer division factor.
FRAC1 is the fractional numerator.
f_{PFD} is the PFD frequency.

For example, in a system where a 12.102 GHz RF frequency output (RF_{OUT}) is required and a 100 MHz reference frequency input (REF_{IN}) is available, the frequency resolution, f_{RES}, is

$$f_{RES} = REF_{IN}/2^{25}$$

$$f_{RES} = 100\ MHz/2^{25}$$

$$= 2.98\ Hz$$

From Equation 1 and Equation 2,

$$f_{PFD} = (100\ MHz \times (1 + 0)/1) = 100\ MHz$$
$$12.102\ GHz = 100\ MHz \times (N + FRAC/2^{25})$$

Calculating the INT and FRAC values,

$$INT = \text{int}(RF_{OUT}/f_{PFD}) = 121$$

$$FRAC1 = (\text{int}(RF_{OUT}/f_{PFD}) - INT) \times 2^{25} = 671088.64 \approx 671089$$

where:
INT is the 16-bit INT value in Register 0.
FRAC1 is the 25-bit FRAC1 value in Register 1.
int() makes an integer of the argument in parentheses.

Note that 671088.64 is rounded to 671,089, resulting in a small frequency error. For exact frequency, use the variable modulus mode.

RF SYNTHESIZER: A WORKED EXAMPLE OF VARIABLE MODULUS MODE

The following is an example how to program the ADF41513 synthesizer:

$$RF_{OUT} = f_{PFD} \times (INT + (FRAC1 + (FRAC2/MOD2))/2^{25}) \quad (8)$$

where:
RF_{OUT} is the output frequency of the external VCO.
INT is a 16-bit value set by Bits[19:4] in Register 0. In Integer N mode, *INT* is 20 to 511 for a 4/5 prescaler and 64 to 1023 for a 8/9 prescaler, and in fractional-N mode, *INT* is 23 to 511 for a 4/5 prescaler and 75 to 1023 for a 8/9 prescaler.
FRAC1 is a 25-bit value set by Bits[28:4] in Register 1.
FRAC2 is a 24-bit value set by Bits[27:4] in Register 3.
MOD2 is a 24-bit value set by Bits[27:4] in Register 4.
f_{PFD} is the PFD frequency.

For example, in a system where a 12.102 GHz RF_{OUT} is required and a 100 MHz f_{PFD} is available,

$$INT = \text{int}(RF_{OUT}/f_{PFD}) = 121$$
$$FRAC1 = \text{int}(((RF_{OUT}/f_{PFD}) - INT) \times 2^{25}) = 671{,}088$$

where:
int() makes an integer of the argument in parentheses.

$$Remainder = FRAC2/MOD2 = 0.64$$

where:
FRAC2 = 64.
MOD2 = 100.

MODULUS

The choice of modulus (MOD) depends on the reference signal (REF_{IN}) available and the channel resolution (f_{RES}) required at the RF output.

REFERENCE DOUBLER AND REFERENCE DIVIDER

The on-chip reference doubler allows the input reference signal to be doubled. Doubling is useful for increasing the PFD comparison frequency. Setting the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves noise performance by 3 dB. It is important to note that the reference input cannot operate above 225 MHz when the reference doubler is on. The PFD maximum operating frequency is 250 MHz (integer N mode) or 125 MHz (fractional-N mode) due to a limitation in the speed of the Σ-Δ circuit.

The reference divide by 2 divides the reference signal by 2, resulting in a 50% duty cycle PFD frequency.

SPUR MECHANISMS

This section describes the two different spur mechanisms that arise with a PLL, and how to minimize them in the ADF41513.

Integer Boundary Spurs

Interactions between the RF VCO frequency and the reference frequency cause integer boundary spurs. When these frequencies are not integer related (the point of a fractional-N synthesizer), spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or difference frequency between an integer multiple of the reference and the VCO frequency. These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference where the difference frequency can be inside the loop bandwidth.

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. Feedthrough of low levels of on-chip reference switching noise, through the $RF_{IN}A$ pin or the $RF_{IN}B$ pin back to the VCO, can result in reference spur levels as high as −90 dBc. PCB layout must ensure adequate isolation between VCO traces and the input reference to avoid a possible feedthrough path on the board.

PHASE RESYNC

The output of a 25-bit fractional-N PLL can settle to any of the 2^{25} phase offsets with respect to the input reference. The phase resync feature in the ADF41513 produces a consistent output phase offset with respect to the input reference. This consistent output phase offset with respect to the input reference is necessary in applications where the output phase and frequency are important, such as digital beamforming. See the Phase Programmability section to program a specific RF output phase when using phase resync.

Phase resync is enabled by setting Register 7, Bits[19:18] = 0b10. When phase resync is enabled, an internal timer generates sync signals at intervals of t_{SYNC} given by the following formula:

$$t_{SYNC} = CLK_1 \times CLK_2 \times t_{PFD} \quad (9)$$

where:
CLK_1 is the decimal value programmed in Register 5, Bits[15:4].
CLK_2 is the decimal value programmed in Register 7, Bits[17:6].
t_{PFD} is the PFD reference period ($1/f_{PFD}$).

When a new frequency is programmed, the second sync pulse after the LE rising edge resynchronizes the output phase to the reference. Program the t_{SYNC} time to a value that is at least as long as the worst case lock time to guarantee that the phase resync occurs after the last cycle slip in the PLL settling transient.

In the example shown in Figure 37, t_{SYNC} is set to 550 µs. The second sync pulse and any later sync pulses are ignored.

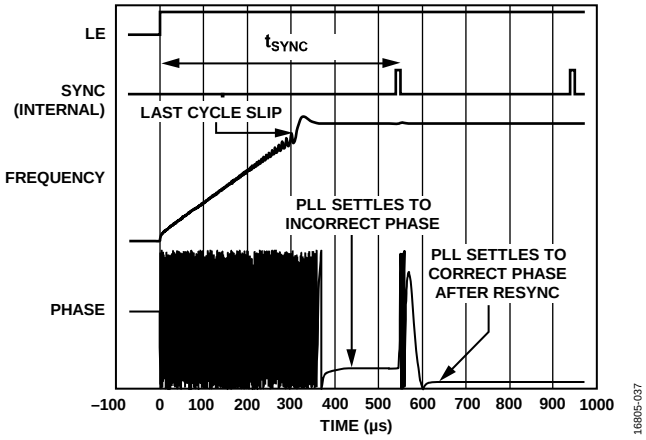
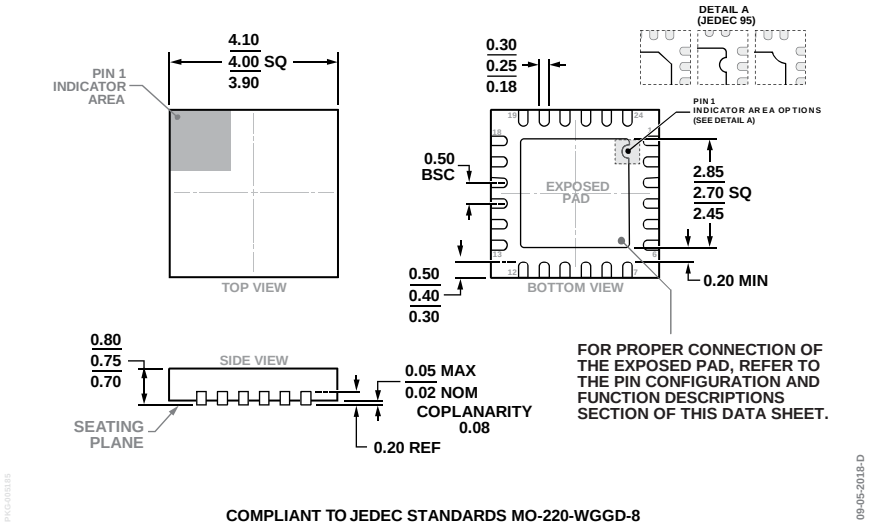


Figure 37. Phase Resync Example

Phase Programmability

The phase word in Register 2 controls the RF output phase. As this word is changed from 0 to 2^{12}, the RF output phase changes over a 360° range in steps of phase value × 360°/2^{12}.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8

Figure 38. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-8)
Dimensions shown in millimeters

ORDERING GUIDE

Parameter[1]	Temperature Range	Package Description	Package Option
ADF41513BCPZ	−40°C to +105°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-8
ADF41513BCPZ-RL7	−40°C to +105°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-8
EV-ADF41513SD1Z		Evaluation Board Without VCO	
EV-ADF41513SD2Z		Evaluation Board with On-Board VCO	

[1] Z = RoHS Compliant Part.

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