Fractional-N Frequency Synthesizer

Data Sheet

ADF4153A

FEATURES

RF bandwidth to 4 GHz
2.7 V to 3.3 V power supply
Separate V_P allows extended tuning voltage
Programmable fractional modulus
Programmable charge pump current
3-wire serial interface
Analog and digital lock detect
Power-down mode
Pin-compatible with ADF4106, ADF4110/ADF4111/ ADF4112/ADF4113, and ADF4153
Consistent RF output phase
Loop filter design possible with ADIsimPLL

APPLICATIONS

CATV equipment
Base stations for mobile radio (GSM, PCS, DCS, WiMAX, SuperCell 3G, CDMA, W-CDMA)
Wireless handsets (GSM, PCS, DCS, CDMA, W-CDMA)
Wireless LANs, PMR
Communications test equipment

GENERAL DESCRIPTION

The ADF4153A is a fractional-N frequency synthesizer that implements local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, and a programmable reference divider. A sigma-delta (Σ-Δ) based fractional interpolator allows programmable fractional-N division. The INT, FRAC, and MOD registers define an overall N divider ($N = (INT + (FRAC/MOD))$). In addition, the 4-bit reference counter (R counter) allows selectable REFIN frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and a voltage controlled oscillator (VCO).

A simple 3-wire interface controls all on-chip registers. The device operates with a power supply ranging from 2.7 V to 3.3 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

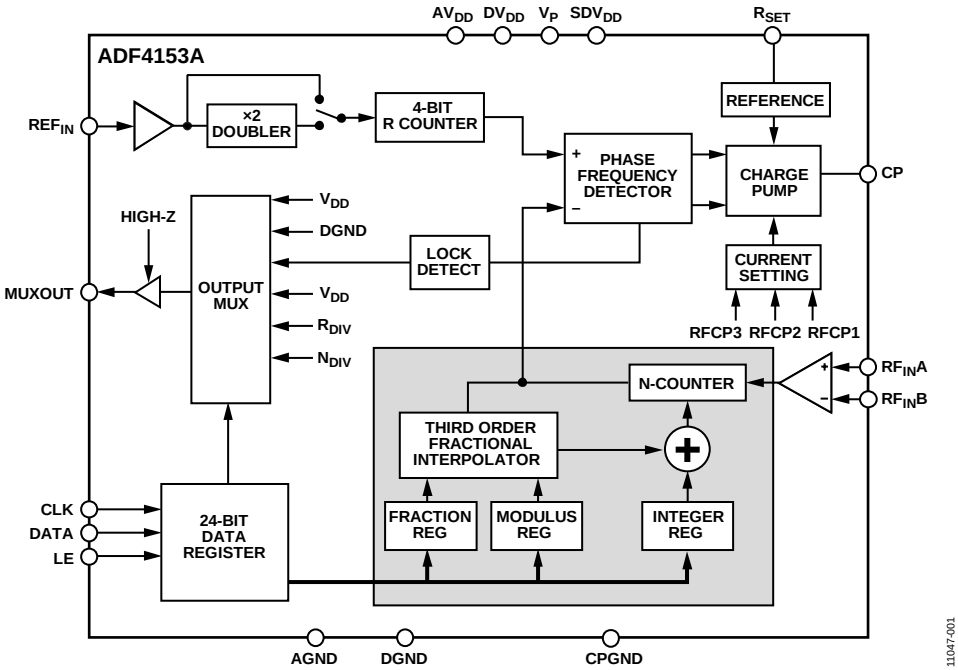

Figure 1.

Rev. A Document Feedback

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REVISION HISTORY

1/13—Rev. 0 to Rev. A

Added TSSOP Package ... Universal
Added Figure 3, Renumbered Sequentially ... 6
Updated Outline Dimensions ... 22
Changes to Ordering Guide ... 22

10/12—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = SDV_{DD} = 2.7 V to 3.3 V; V_P = AV_{DD} to 5.5 V; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted; dBm referred to 50 Ω.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF INPUT CHARACTERISTICS (3 V)					See Figure 12 for an input circuit
RF Input Frequency (RF_{IN})	0.5		4	GHz	−8 dBm minimum/0 dBm maximum
	1		4	GHz	−10 dBm minimum/0 dBm maximum
					For lower frequencies, ensure slew rate (SR) > 400 V/µs
REF_{IN} CHARACTERISTICS					See Figure 11 for an input circuit
REF_{IN} Input Frequency	10		250	MHz	For f < 10 MHz, use a dc-coupled, CMOS-compatible square wave; slew rate > 25 V/µs
REF_{IN} Input Sensitivity	0.7		AV_{DD}	V p-p	Biased at $AV_{DD}/2$[1]
REF_{IN} Input Capacitance			10	pF	
REF_{IN} Input Current			±100	µA	
PHASE DETECTOR					
Phase Detector Frequency			32	MHz	
CHARGE PUMP					
I_{CP} Sink/Source					Programmable; see Figure 19
High Value		5		mA	With R_{SET} = 4.7 kΩ
Low Value		312.5		µA	With R_{SET} = 4.7 kΩ
Absolute Accuracy		2.5		%	With R_{SET} = 4.7 kΩ
R_{SET} Range	3.0		10	kΩ	
I_{CP} Three-State Leakage Current		1		nA	Sink and source current
Sink and Source Matching		2		%	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V
I_{CP} vs. V_{CP}		2		%	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V
I_{CP} vs. Temperature		2		%	V_{CP} = V_P/2
LOGIC INPUTS					
V_{INH}, Input High Voltage	1.4			V	
V_{INL}, Input Low Voltage			0.6	V	
I_{INH}/I_{INL}, Input Current			±1	µA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	1.4			V	Open-drain 1 kΩ pull-up to 1.8 V
V_{OL}, Output Low Voltage			0.4	V	I_{OL} = 500 µA
POWER SUPPLIES					
AV_{DD}	2.7		3.3	V	
DV_{DD}, SD_{VDD}		AV_{DD}			
V_P	AV_{DD}		5.5	V	
I_{DD}		20	24	mA	
Low Power Sleep Mode		1		µA	
NOISE CHARACTERISTICS					
Normalized Phase Noise Floor (PN_{SYNTH})[2]		−223		dBc/Hz	PLL loop BW = 500 kHz
Normalized 1/f Noise (PN_{1_f})[3]		−121		dBc/Hz	Measured at 10 kHz offset, normalized to 1 GHz
Phase Noise Performance[4]					@ VCO output
1750 MHz Output[5]		−107		dBc/Hz	@ 5 kHz offset, 25 MHz PFD frequency

[1] AC coupling ensures $AV_{DD}/2$ bias.
[2] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log(N) (where N is the N divider value) and 10 log(F_{PFD}). PN_{SYNTH} = PN_{TOT} − 10 log(F_{PFD}) − 20 log(N).
[3] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, F_{RF}, and at an offset frequency, f, is given by PN = P_{1_f} + 10 log(10 kHz/f) + 20 log(F_{RF}/1 GHz). Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.
[4] The phase noise is measured with the EV-ADF4153ASD1Z and the Rohde & Schwarz FSUP spectrum analyzer operating in phase noise mode.
[5] f_{REFIN} = 100 MHz; F_{PFD} = 25 MHz; offset frequency = 5 kHz; RF_{OUT} = 1750 MHz; N = 70; loop BW = 20 kHz; lowest noise mode.

TIMING SPECIFICATIONS

AV_{DD} = DV_{DD} = SDV_{DD} = 2.7 V to 3.3 V; V_P = AV_{DD} to 5.5 V; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted; dBm referred to 50 Ω.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width

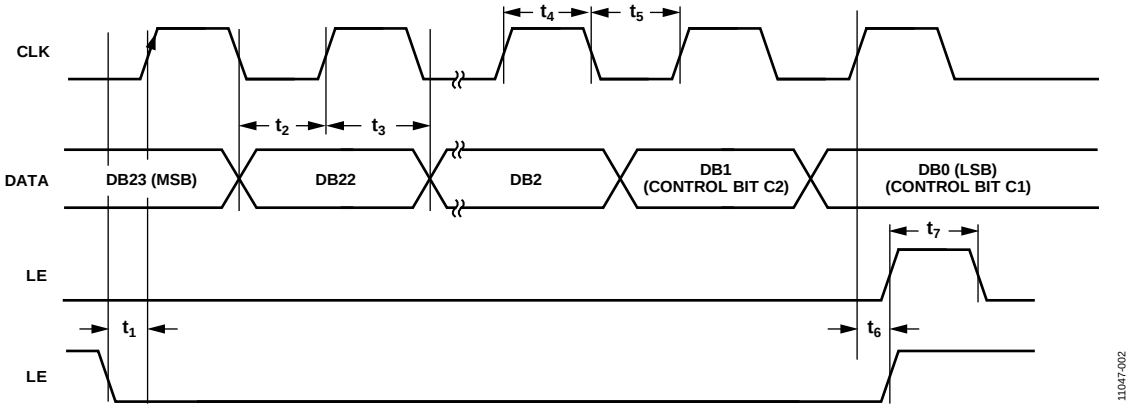

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, GND = AGND = DGND = 0 V,
V_{DD} = AV_{DD} = DV_{DD} = SDV_{DD}, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +4 V
DV_{DD} to AV_{DD}	−0.3 V to +0.3 V
SDV_{DD} to AV_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +5.8 V
V_P to V_{DD}	−0.3 V to +5.8 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN}, RF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	112°C/W
LFCSP θ_{JA} Thermal Impedance	30.4°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

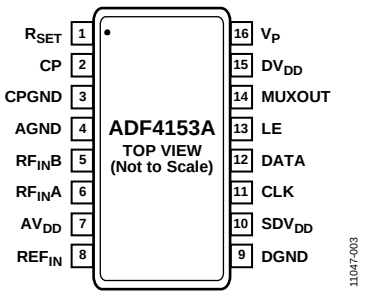

Figure 3. TSSOP Pin Configuration

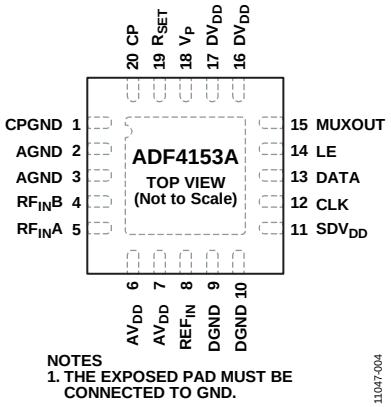

Figure 4. LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No. TSSOP	Pin No. LFCSP	Mnemonic	Description
1	19	R_{SET}	Connecting a resistor between R_{SET} and ground sets the maximum charge pump output current. The relationship between I_{CP} and R_{SET} is $$I_{CPMAX} = \frac{23.5}{R_{SET}}$$ where R_{SET} = 4.7 kΩ and I_{CPMAX} = 5 mA.
2	20	CP	Charge Pump Output. When enabled, CP provides ±I_{CP} to the external loop filter, which in turn drives the external VCO.
3	1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
5	4	$RF_{IN}B$	Complementary Input to the RF Prescaler. This pin should be decoupled to the ground plane with a small bypass capacitor, typically 100 pF (see Figure 12).
6	5	$RF_{IN}A$	Input to the RF Prescaler. This small signal input is normally ac-coupled from the VCO.
7	6, 7	AV_{DD}	Positive Power Supply for the RF Section. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. AV_{DD} has a value of 3 V ± 10%. AV_{DD} must have the same voltage as DV_{DD}.
8	8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100 kΩ (see Figure 11). This input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	SDV_{DD}	Σ-Δ Power. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. SDV_{DD} has a value of 3 V ± 10%. SDV_{DD} must have the same voltage as DV_{DD}.
11	12	CLK	Serial Clock Input. The serial clock is used to clock in the serial data to the registers. The data is latched into the shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first; the two LSBs are the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE is high, the data stored in the shift registers is loaded into one of four latches; the latch is selected using the control bits.
14	15	MUXOUT	This multiplexer output allows either the RF lock detect, the scaled RF, or the scaled reference frequency to be externally accessed.
15	16, 17	DV_{DD}	Positive Power Supply for the Digital Section. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} has a value of 3 V ± 10%. DV_{DD} must have the same voltage as AV_{DD}.
16	18	V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range of up to 5.5 V.
N/A	21	EPAD	Exposed Pad. The exposed pad must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

Settings for single-sideband plots and phase noise vs. temperature plot: loop bandwidth = 20 kHz, reference = 100 MHz, PFD = 25 MHz, carrier frequency = 1720.2 MHz, N = 68, MOD = 125, FRAC = 101, I_{CP} = 2.5 mA, VCO = Mini-Circuits ROS-1800+, evaluation board = EV-ADF4153ASD1Z, measurements taken on the Agilent E5052 signal source analyzer operating in phase noise mode.

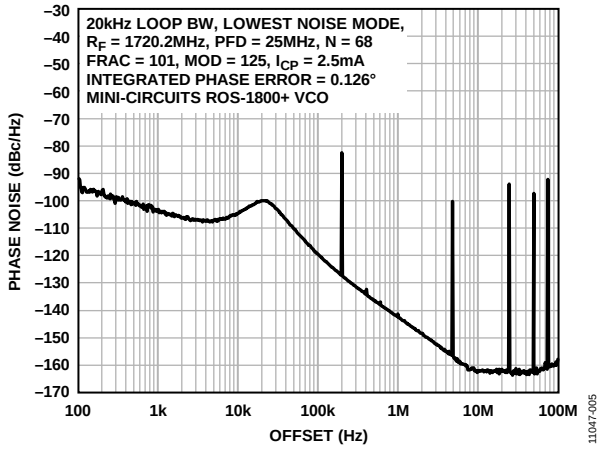

Figure 5. Single-Sideband Phase Noise Plot (Lowest Noise Mode)

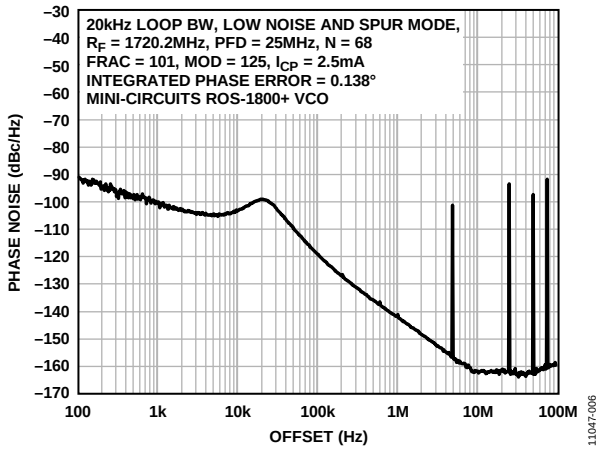

Figure 6. Single-Sideband Phase Noise Plot (Low Noise and Spur Mode)

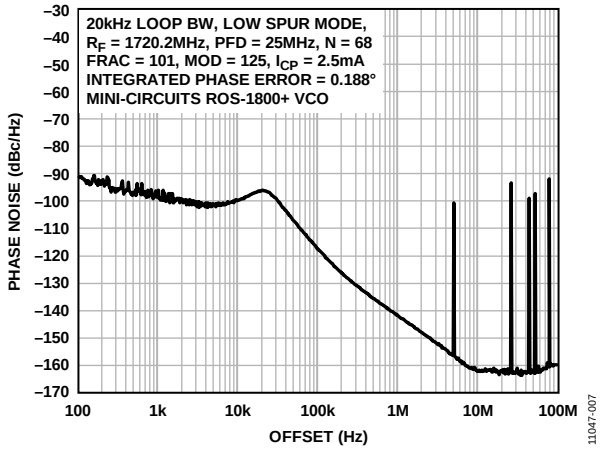

Figure 7. Single-Sideband Phase Noise Plot (Low Spur Mode)

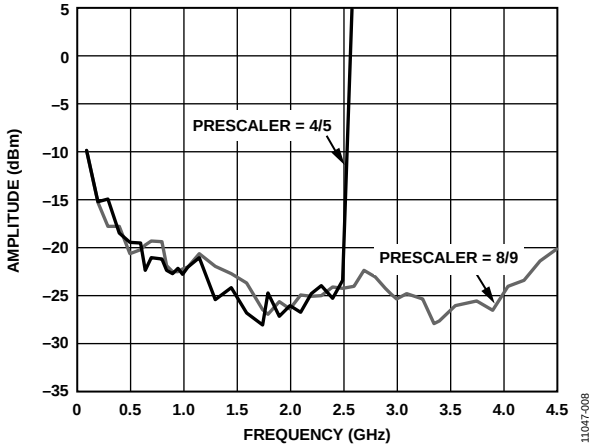

Figure 8. RF Input Sensitivity

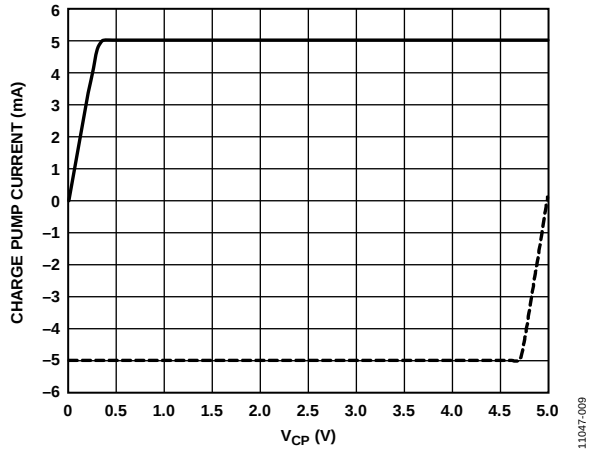

Figure 9. Charge Pump Output Characteristics

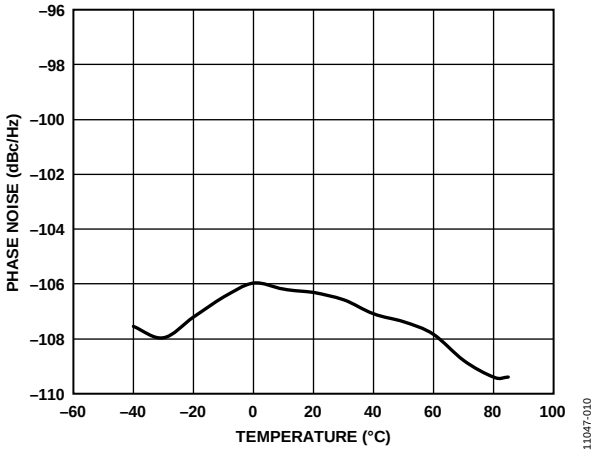

Figure 10. Phase Noise vs. Temperature

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 11. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

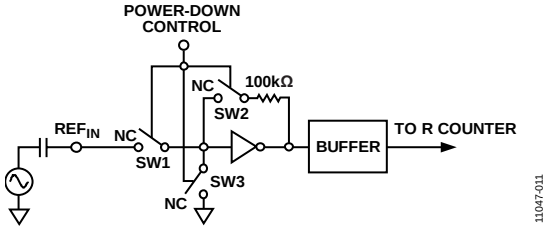

Figure 11. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 12. It is followed by a 2-stage limiting amplifier to generate the current-mode logic (CML) clock levels needed for the prescaler.

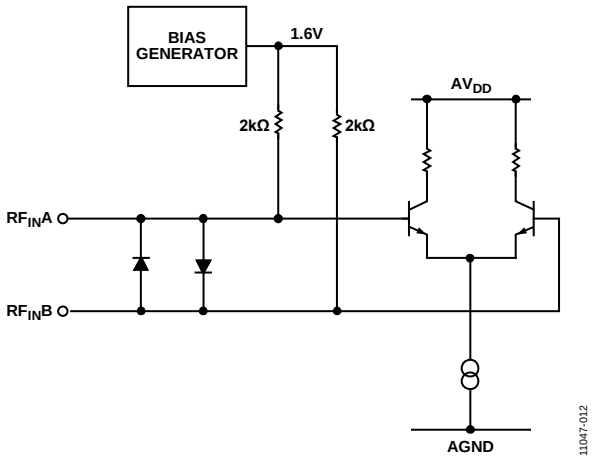

Figure 12. RF Input Stage

RF INT DIVIDER

The RF INT CMOS counter allows a division ratio in the PLL feedback counter. Division ratios from 31 to 511 are allowed.

INT, FRAC, MOD, AND R RELATIONSHIP

The INT, FRAC, and MOD values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the phase frequency detector (PFD). See the RF Synthesizer: A Worked Example section for more information. The RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = F_{PFD} \times (INT + (FRAC/MOD)) \quad (1)$$

where:
RF_{OUT} is the output frequency of the external voltage controlled oscillator (VCO).
INT is the preset divide ratio of the binary 9-bit counter (31 to 511).
FRAC is the numerator of the fractional division (0 to MOD − 1).
MOD is the preset fractional modulus (2 to 4095).

The PFD frequency is given by:

$$F_{PFD} = REF_{IN} \times (1 + D)/R \quad (2)$$

where:
REF_{IN} is the reference input frequency.
D is the REF_{IN} doubler bit.
R is the preset divide ratio of the binary 4-bit programmable reference counter (1 to 15).

RF R COUNTER

The 4-bit RF R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 15 are allowed.

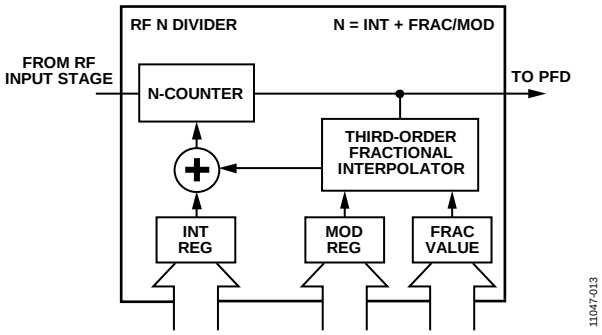

Figure 13. RF N Divider

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 14 is a simplified schematic of the phase frequency detector. The PFD includes a fixed delay element that sets the width of the antibacklash pulse, which is typically 1.8 ns. This pulse ensures that there is no dead zone in the PFD transfer function and gives a consistent reference spur level.

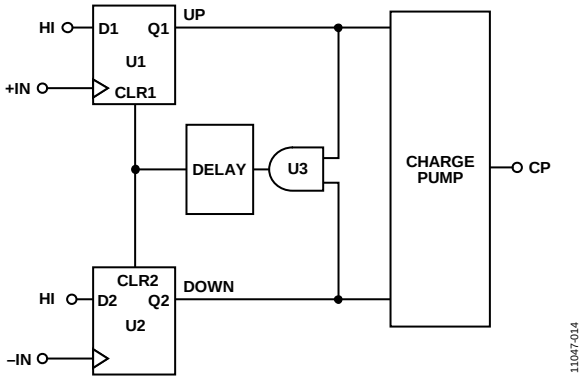

Figure 14. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4153A lets the user access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 (see Figure 18). Figure 15 shows the MUXOUT section in block diagram form.

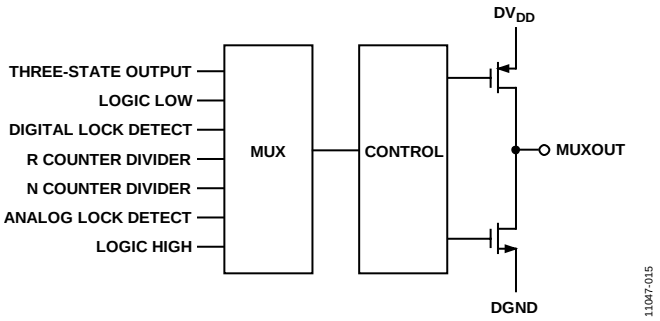

Figure 15. MUXOUT Schematic

INPUT SHIFT REGISTERS

The ADF4153A digital section includes a 4-bit RF R counter, a 9-bit RF N counter, a 12-bit FRAC counter, and a 12-bit modulus counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2 and C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in Figure 2. The truth table for these bits is shown in Table 5. Figure 16 shows a summary of how the registers are programmed.

Table 5. C2 and C1 Truth Table

Control Bits		
C2	**C1**	**Register**
0	0	N divider register
0	1	R divider register
1	0	Control register
1	1	Noise and spur register

PROGRAM MODES

Figure 16 through Figure 20 show how to set up the program modes in the ADF4153A.

The ADF4153A programmable modulus is double buffered. This means that two events have to occur before the part uses a new modulus value. First, the new modulus value is latched into the device by writing to the R divider register. Second, a new write must be performed on the N divider register. Therefore, to ensure that the modulus value is loaded correctly, the N divider register must be written to any time that the modulus value is updated.

REGISTER MAPS

N DIVIDER REG (R0)

FASTLOCK	9-BIT INTEGER VALUE (INT)									12-BIT FRACTIONAL VALUE (FRAC)											CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
FL1	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C2 (0)	C1 (0)

R DIVIDER REG (R1)

LOAD CONTROL	MUXOUT			RESERVED	PRESCALER	4-BIT R COUNTER				12-BIT INTERPOLATOR MODULUS VALUE (MOD)											CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P3	M3	M2	M1	0	P1	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C2 (0)	C1 (1)

CONTROL REG (R2)

RESYNC				REFERENCE DOUBLER	CP/2	CP CURRENT SETTING			PD POLARITY	LDP	POWER-DOWN	CP THREE-STATE	COUNTER RESET	CONTROL BITS	
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
S4	S3	S2	S1	U6	CP3	CP2	CP1	CP0	U5	U4	U3	U2	U1	C2 (1)	C1 (0)

NOISE AND SPUR REG (R3)

RESERVED	NOISE AND SPUR MODE				RESERVED			NOISE AND SPUR MODE	CONTROL BITS	
DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	T8	T7	T6	T5	0	0	0	T1	C2 (1)	C1 (1)

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Figure 16. Register Summary

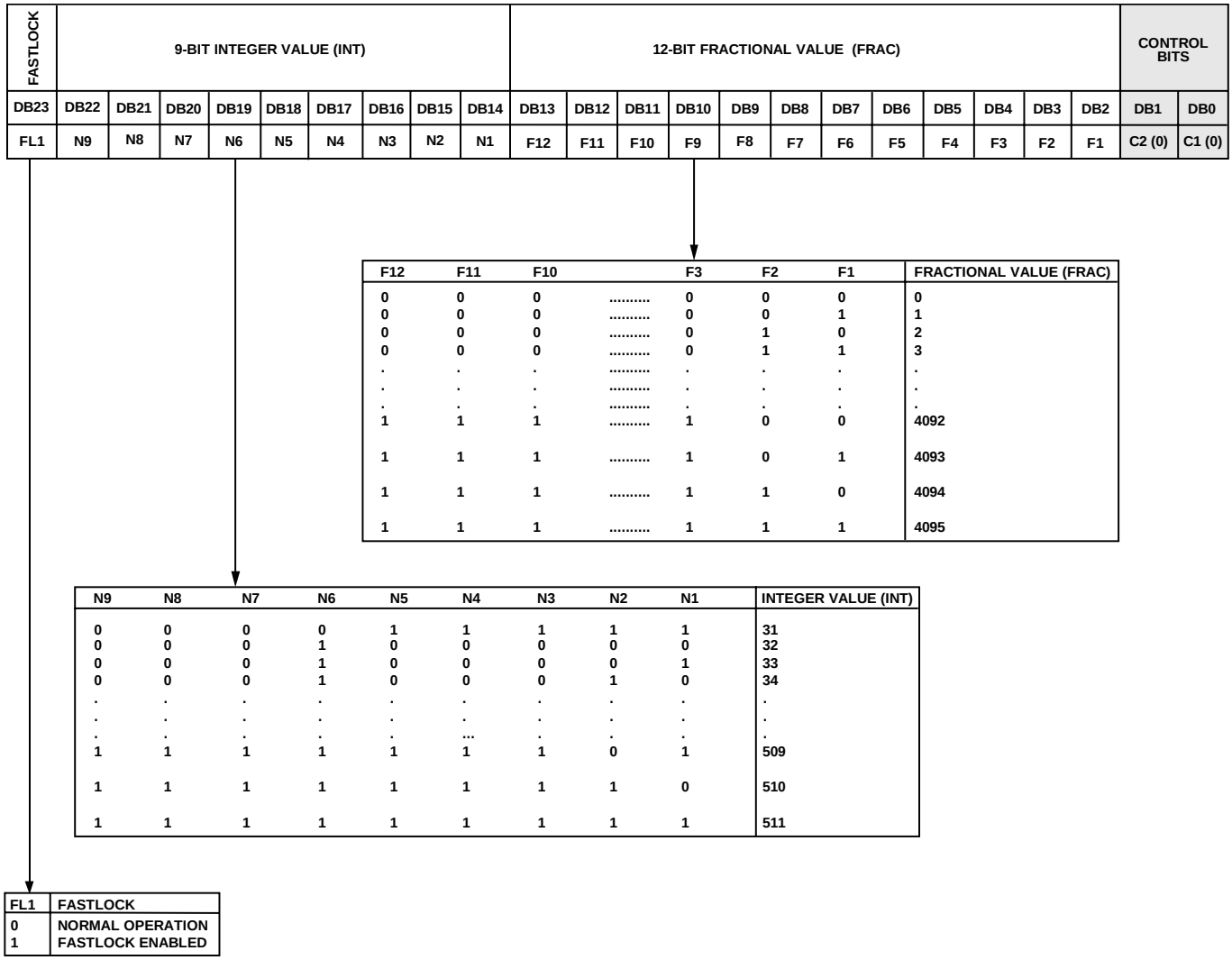


Figure 17. N Divider Register Map (R0)

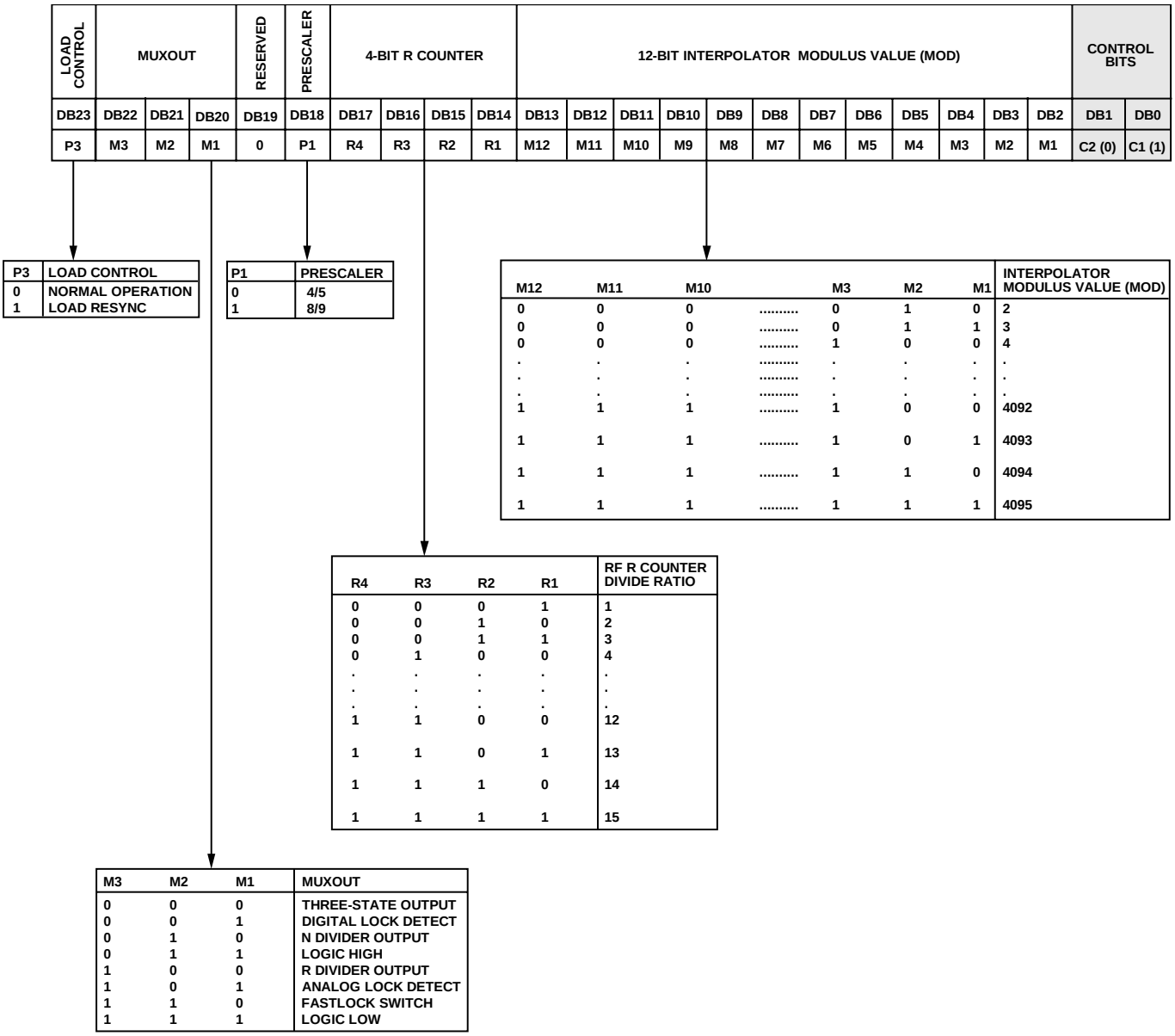
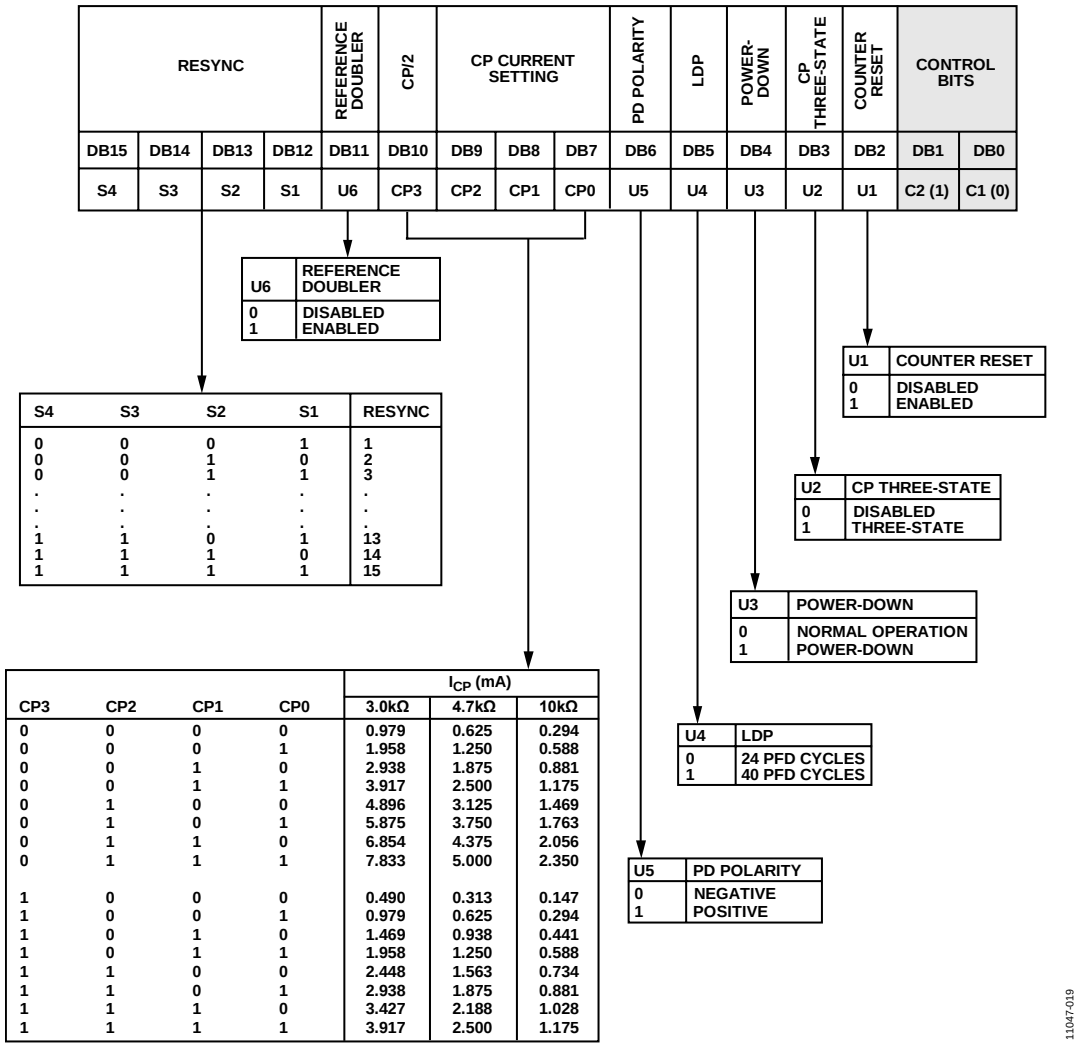


Figure 18. R Divider Register Map (R1)



S4	S3	S2	S1	RESYNC
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

				I_{CP} (mA)		
CP3	CP2	CP1	CP0	3.0kΩ	4.7kΩ	10kΩ
0	0	0	0	0.979	0.625	0.294
0	0	0	1	1.958	1.250	0.588
0	0	1	0	2.938	1.875	0.881
0	0	1	1	3.917	2.500	1.175
0	1	0	0	4.896	3.125	1.469
0	1	0	1	5.875	3.750	1.763
0	1	1	0	6.854	4.375	2.056
0	1	1	1	7.833	5.000	2.350
1	0	0	0	0.490	0.313	0.147
1	0	0	1	0.979	0.625	0.294
1	0	1	0	1.469	0.938	0.441
1	0	1	1	1.958	1.250	0.588
1	1	0	0	2.448	1.563	0.734
1	1	0	1	2.938	1.875	0.881
1	1	1	0	3.427	2.188	1.028
1	1	1	1	3.917	2.500	1.175

Figure 19. Control Register Map (R2)

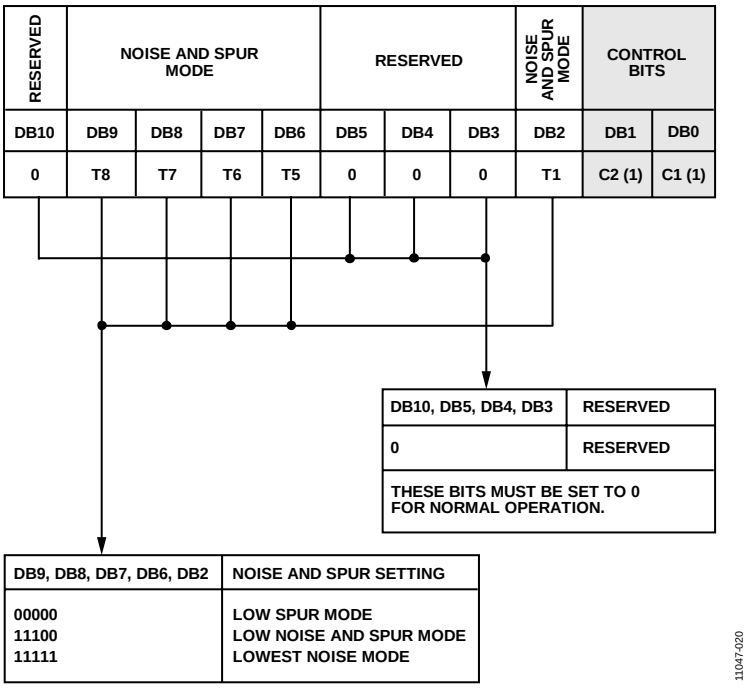


Figure 20. Noise and Spur Register (R3)

N DIVIDER REGISTER, R0

With R0[1, 0] set to [0, 0], the on-chip N divider register is programmed. Figure 17 shows the input data format for programming this register.

9-Bit INT Value

These nine bits control what is loaded as the INT value. This is used to determine the overall feedback division factor. It is used in Equation 1 (see the INT, FRAC, MOD, and R Relationship section).

12-Bit FRAC Value

These 12 bits control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall feedback division factor. It is also used in Equation 1. The FRAC value must be less than or equal to the value loaded into the MOD register.

Fastlock

When set to logic high, fastlock is enabled. This sets the charge pump current to its maximum value. When set to logic low, the charge pump current is equal to the value programmed into the function register. Also, if MUXOUT is programmed to setting the fastlock switch, MUXOUT is shorted to ground when the fastlock bit is 1 and is high impedance when this bit is 0.

R DIVIDER REGISTER, R1

With R1[1, 0] set to [0, 1], the on-chip R divider register is programmed. Figure 18 shows the input data format for programming this register.

Load Control

When set to logic high, the value being programmed in the modulus is not loaded into the modulus. Instead, it sets the resync delay of the Σ-Δ. This is done to ensure phase resync when changing frequencies. See the Phase Resync section for more information and a worked example.

MUXOUT

The on-chip multiplexer is controlled by DB22, DB21, and DB20 on the ADF4153A. See Figure 18 for the truth table.

Digital Lock Detect

The digital lock detect output goes high if there are 24 successive PFD cycles with an input error of less than 15 ns (for LDP is 0, see the Control Register, R2 section for a more thorough explanation of the LDP bit). It stays high until a new channel is programmed or until the error at the PFD input exceeds 30 ns for one or more cycles. If the loop bandwidth is narrow compared to the PFD frequency, the error at the PFD inputs may drop below 15 ns for 24 cycles around a cycle slip. Therefore, the digital lock detect may go falsely high for a short period until the error again exceeds 30 ns. In this case, the digital lock detect is reliable only as a loss-of-lock detector.

Prescaler (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the INT, FRAC, and MOD counters, determines the overall division ratio from the RF_{IN} to the PFD input.

Operating at CML levels, it takes the clock from the RF input stage and divides it down for the counters. It is based on a synchronous 4/5 core. When set to 4/5, the maximum RF frequency allowed is 2 GHz. Therefore, when operating the ADF4153A above 2 GHz, this must be set to 8/9. The prescaler limits the INT value.

With P = 4/5, N_{MIN} = 31.

With P = 8/9, N_{MIN} = 91.

4-Bit R Counter

The 4-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 15 are allowed.

12-Bit Interpolator MOD Value

These programmable bits set the fractional modulus. This is the ratio of the PFD frequency to the channel step resolution on the RF output. Refer to the RF Synthesizer: A Worked Example section for more information.

The ADF4153A programmable modulus is double buffered. This means that two events have to occur before the part uses a new modulus value. First, the new modulus value is latched into the device by writing to the R divider register. Second, a new write must be performed on the N divider register. Therefore, any time that the modulus value has been updated, the N divider register must then be written to in order to ensure that the modulus value is loaded correctly.

CONTROL REGISTER, R2

With R2[1, 0] set to [1, 0], the on-chip control register is programmed. Figure 19 shows the input data format for programming this register.

RF Counter Reset

DB2 is the RF counter reset bit for the ADF4153A. When this is 1, the RF synthesizer counters are held in reset. For normal operation, this bit should be 0.

RF Charge Pump Three-State

DB3 puts the charge pump into three-state mode when programmed to 1. It should be set to 0 for normal operation.

RF Power-Down

DB4 on the ADF4153A provides the programmable power-down mode. Setting this bit to 1 performs a power-down. Setting this bit to 0 returns the synthesizer to normal operation. While in software power-down mode, the part retains all information in its registers. Only when supplies are removed are the register contents lost.

When a power-down is activated, the following events occur:

1. All active dc current paths are removed.
2. The synthesizer counters are forced to their load state conditions.
3. The charge pump is forced into three-state mode.
4. The digital lock detect circuitry is reset.
5. The RF_{IN} input is debiased.
6. The input register remains active and capable of loading and latching data.

Lock Detect Precision (LDP)

When DB5 is programmed to 0, 24 consecutive PFD cycles of 15 ns must occur before digital lock detect is set. When this bit is programmed to 1, 40 consecutive reference cycles of 15 ns must occur before digital lock detect is set.

Phase Detector Polarity

DB6 in the ADF4153A sets the phase detector polarity. When the VCO characteristics are positive, this should be set to 1. When they are negative, it should be set to 0.

Charge Pump Current Setting

DB7, DB8, DB9, and DB10 set the charge pump current setting. This should be set to the charge pump current that the loop filter is designed with (see Figure 19).

REF_{IN} Doubler

Setting DB11 to 0 feeds the REF_{IN} signal directly to the 4-bit RF R counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding into the 4-bit R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of REF_{IN} become active edges at the PFD input.

When the doubler is enabled and the lowest spur mode is chosen, the in-band phase noise performance is sensitive to the REF_{IN} duty cycle. The phase noise degradation can be as much as 5 dB for the REF_{IN} duty cycles outside a 45% to 55% range. The phase noise is insensitive to the REF_{IN} duty cycle in the lowest noise mode and in the lowest noise and spur mode. The phase noise is insensitive to REF_{IN} duty cycle when the doubler is disabled.

The maximum allowed REF_{IN} frequency when the doubler is enabled is 30 MHz.

NOISE AND SPUR REGISTER, R3

With R3[1, 0] set to [1, 1], the on-chip noise and spur register is programmed. Figure 20 shows the input data format for programming this register.

Noise and Spur Mode

Noise and spur mode lets the user optimize a design either for improved spurious performance or for improved phase noise performance. When the low spur setting is chosen, dither is enabled. This randomizes the fractional quantization noise so that it resembles white noise rather than spurious noise. As a result, the part is optimized for improved spurious performance. This operation would normally be used when the PLL closed-loop bandwidth is wide, for fast-locking applications. (Wide-loop bandwidth is seen as a loop bandwidth greater than 1/10 of the RF_{OUT} channel step resolution (f_{RES}).) A wide-loop filter does not attenuate the spurs to the same level as a narrow-loop bandwidth.

When the low noise and spur setting is enabled, dither is disabled. This optimizes the synthesizer to operate with improved noise performance. However, the spurious performance is degraded in this mode compared to the low spur setting.

To further improve noise performance, the lowest noise setting option can be used, which reduces the phase noise. As well as disabling the dither, it also ensures that the charge pump is operating in an optimum region for noise performance. This setting is extremely useful where a narrow-loop filter bandwidth is available. The synthesizer ensures extremely low noise and the filter attenuates the spurs. The typical performance characteristics give the user an idea of the trade-off in a typical W-CDMA setup for the different noise and spur settings.

RESERVED BITS

These bits should be set to 0 for normal operation.

INITIALIZATION SEQUENCE

The following initialization sequence should be followed upon powering up the part:

1. Write all zeros to the noise and spur register. This ensures that all test modes are cleared.
2. Write again to the noise and spur register, this time selecting which noise and spur mode is required. For example, writing Hexadecimal 0003C7 to the part selects lowest noise mode.
3. Enable the counter reset in the control register by writing a 1 to DB2; also select the required settings in the control register. If using the phase resync function, set the resync bits to the required settings.
4. Load the R divider register (with load control DB23 set to 0).
5. Load the N divider register.
6. Disable the counter reset by writing a 0 to DB2 in the control register.

The part now locks to the set frequency.

If using the phase resync function, an extra step is needed after Step 3. This involves loading the R divider register with load control = 1 and the required delay interval in place of the MOD value. The previous sequence can then be followed, ensuring that in Step 4 the value of MOD is written to the R divider register with load control = 0.

See the Spur Consistency and Phase Resync sections for more information on the phase resync feature.

RF SYNTHESIZER: A WORKED EXAMPLE

The following equation governs how the synthesizer is programmed:

$$RF_{OUT} = [INT + (FRAC/MOD)] \times [F_{PFD}] \quad (3)$$

where:
RF_{OUT} is the RF frequency output.
INT is the integer division factor.
$FRAC$ is the fractionality.
MOD is the modulus.

The PFD frequency is given by:

$$F_{PFD} = [REF_{IN} \times (1 + D)/R] \quad (4)$$

where:
REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit.
R is the RF reference division factor.

For example, in a GSM 1800 system, where 1.8 GHz RF frequency output (RF_{OUT}) is required, a 13 MHz reference frequency input (REF_{IN}) is available and a 200 kHz channel resolution (f_{RES}) is required on the RF output. With REF_{IN} doubler (D) set to 0 and reference division (R) set to 1, from Equation 4:

$$F_{PFD} = [13 \text{ MHz} \times (1 + 0)/1] = 13 \text{ MHz} \quad (5)$$

$$MOD = F_{PFD}/f_{RES}$$

$$MOD = 13 \text{ MHz}/200 \text{ kHz} = 65$$

$$1.8 \text{ G} = 13 \text{ MHz} \times (INT + FRAC/65)$$

where $INT = 138$; $FRAC = 30$ (6)

MODULUS

The choice of modulus (MOD) depends on the PFD frequency (which depends on the available reference signal REF_{IN}) and the channel resolution (f_{RES}) required at the RF output. For example, a GSM system with 13 MHz REF_{IN} sets the modulus to 65. This means that the RF output resolution (f_{RES}) is the 200 kHz (13 MHz/65) necessary for GSM. With dither off, the fractional spur interval depends on the modulus values chosen. See Table 6 for more information.

REFERENCE DOUBLER AND REFERENCE DIVIDER

The reference doubler on-chip allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves noise performance by 3 dB. It is important to note that the PFD cannot be operated above specified limits due to a limitation in the speed of the Σ-Δ circuit of the N divider.

12-BIT PROGRAMMABLE MODULUS

Unlike most other fractional-N PLLs, the ADF4153A lets the user program the modulus over a 12-bit range. This means that the user can set up the part in many different configurations for the application, when combined with the reference doubler and the 4-bit R counter.

The following is an example of an application that requires 1.75 GHz RF and 200 kHz channel step resolution. The system has a 13 MHz reference signal.

One possible setup is feeding the 13 MHz directly to the PFD and programming the modulus to divide by 65. This results in the required 200 kHz resolution.

Another possible setup is using the reference doubler to create 26 MHz from the 13 MHz input signal. This 26 MHz is then fed into the PFD. The modulus is now programmed to divide by 130. This also results in 200 kHz resolution and offers superior phase noise performance over the previous setup.

The programmable modulus is also very useful for multi-standard applications. If a dual-mode phone requires PDC and GSM 1800 standards, the programmable modulus is of great benefit. PDC requires 25 kHz channel step resolution, whereas GSM 1800 requires 200 kHz channel step resolution. A 13 MHz reference signal can be fed directly to the PFD. The modulus is programmed to 520 when in PDC mode (13 MHz/520 = 25 kHz). The modulus is reprogrammed to 65 for GSM 1800 operation (13 MHz/65 = 200 kHz). It is important that the PFD frequency remains constant (13 MHz). This lets the user design one loop filter that can be used in both setups without running into stability issues. It is the ratio of the RF frequency to the PFD frequency that affects the loop design. By keeping this relationship constant, the same loop filter can be used in both applications.

FASTLOCK WITH SPURIOUS OPTIMIZATION

As mentioned in the Noise and Spur Mode section, the part can be optimized for spurious performance. However, in fast-locking applications, the loop bandwidth needs to be wide, and therefore the filter does not provide much attenuation of the spurs. The programmable charge pump can be used to get around this issue. The filter is designed for a narrow-loop bandwidth so that steady-state spurious specifications are met. This is designed using the lowest charge pump current setting.

To implement fastlock during a frequency jump, the charge pump current is set to the maximum setting for the duration of the jump by asserting the fastlock bit in the N divider register. This widens the loop bandwidth, which improves lock time. To maintain loop stability while in wide bandwidth mode, the loop filter needs to be modified. This is achieved by switching in a resistor (R1A) in parallel with the damping resistor in the loop filter (see Figure 21). MUXOUT needs to be set to the fastlock switch to use the internal switch. For example, if the charge pump current is increased by 16, the damping resistor, R1, needs to be decreased by ¼ while in wide bandwidth mode.

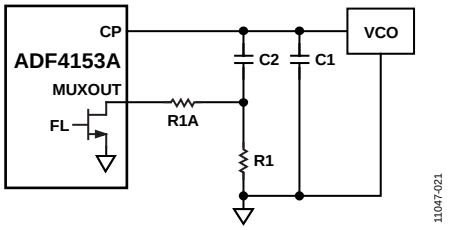


Figure 21. ADF4153A with Fastlock

The value of R1A is then chosen so that the total parallel resistance of R1 and R1A equals 1/4 of R1 alone. This gives an overall 4× increase in loop bandwidth, while maintaining stability in wide bandwidth mode.

When the PLL has locked to the new frequency, the charge pump is again programmed to the lowest charge pump current setting by setting the fastlock bit to 0. The internal switch opens and the damping resistor reverts to its original value. This narrows the loop bandwidth to its original cutoff frequency to allow better attenuation of the spurs than the wide-loop bandwidth.

SPUR MECHANISMS

The following section describes the three different spur mechanisms that arise with a fractional-N synthesizer and how to minimize them in the ADF4153A.

Fractional Spurs

The fractional interpolator in the ADF4153A is a third-order Σ-Δ modulator (SDM) with a modulus (MOD) that is programmable to any integer value from 2 to 4095. In low spur mode (dither enabled), the minimum allowed value of MOD is 50. The SDM is clocked at the PFD reference rate (F_{PFD}) that allows PLL output frequencies to be synthesized at a channel step resolution of F_{PFD}/MOD.

In lowest noise mode and low noise and spur mode (dither off), the quantization noise from the Σ-Δ modulator appears as fractional spurs. The interval between spurs is F_{PFD}/L, where L is the repeat length of the code sequence in the digital Σ-Δ modulator. For the third-order modulator used in the ADF4153A, the repeat length depends on the value of MOD, as shown in Table 6.

Table 6. Fractional Spurs with Dither Off

Condition (Dither Off)	Repeat Length	Spur Interval
If MOD is divisible by 2, but not 3	2 × MOD	Channel step/2
If MOD is divisible by 3, but not 2	3 × MOD	Channel step/3
If MOD is divisible by 6	6 × MOD	Channel step/6
Otherwise	MOD	Channel step

In low spur mode (dither enabled), the repeat length is extended to 2^{21} cycles, regardless of the value of MOD, which makes the quantization error spectrum look like broadband noise. This can degrade the in-band phase noise at the PLL output by as much as 10 dB. Therefore, for lowest noise, dither off is a better choice, particularly when the final loop BW is low enough to attenuate even the lowest frequency fractional spur.

Integer Boundary Spurs

Another mechanism for fractional spur creation is interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (which is the point of a fractional-N synthesizer), spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or difference frequency between an integer multiple of the reference and the VCO frequency.

These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference where the difference frequency can be inside the loop bandwidth, therefore, the name integer boundary spurs.

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. One such mechanism is feedthrough of low levels of on-chip reference switching noise out through the RF_{IN} pin back to the VCO, resulting in reference spur levels as high as –90 dBc. Ensure that in the PCB layout that the VCO is well separated from the input reference to avoid a possible feed-through path on the board.

SPUR CONSISTENCY

When jumping from Frequency A to Frequency B and then back again using some fractional-N synthesizers, the spur levels often differ each time Frequency A is programmed. However, in the ADF4153A, the spur levels on any particular channel are always consistent.

PHASE RESYNC

The output of a fractional-N PLL can settle to any one of MOD phase offsets with respect to the input reference, where MOD is the fractional modulus. The phase resync feature in the ADF4153A can be used to produce a consistent output phase offset with respect to the input reference. This is necessary in applications where the output phase and frequency are important, such as digital beam-forming.

When phase resync is enabled, an internal timer generates sync signals at intervals of t_{SYNC} given by the following formula:

$$t_{SYNC} = RESYNC \times RESYNC\_DELAY \times t_{PFD}$$

where t_{PFD} is the PFD reference period.

RESYNC is the decimal value programmed in Bits DB[15…12] of Register R2 and can be any integer in the range of 1 to 15. If RESYNC is programmed to its default value of all zeros, then the phase resync feature is disabled.

If phase resync is enabled, then RESYNC_DELAY must be programmed to a value that is an integer multiple of the value of MOD. RESYNC_DELAY is the decimal value programmed into the MOD bits (DB[13…2] of Register R1 when load control (Bit DB23 of Register R1) = 1.

When a new frequency is programmed, the second next sync pulse after the LE rising edge is used to resynchronize the output phase to the reference. The t_{SYNC} time should be programmed to a value that is at least as long as the worst-case lock time. Doing so guarantees that the phase resync occurs after the last cycle slip in the PLL settling transient.

In the example shown in Figure 22, the PFD reference is 25 MHz and MOD = 125 for a 200 kHz channel spacing. t_{SYNC} is set to 400 µs by programming RESYNC = 10 and RESYNC_DELAY = 1000.

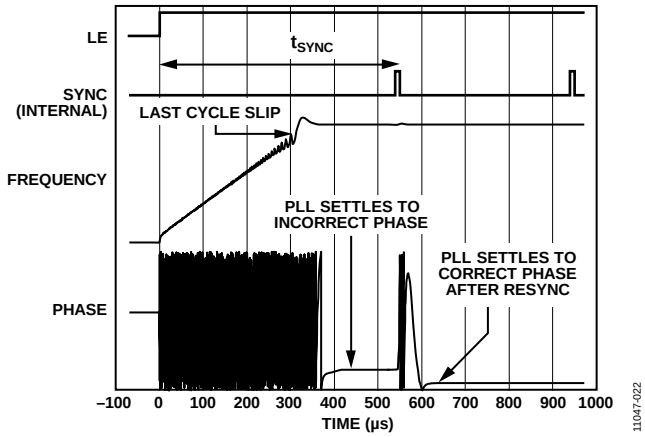


Figure 22. Phase Resync Example

FILTER DESIGN—ADIsimPLL

A filter design and analysis program is available to help the user implement PLL design. Visit www.analog.com/pll for a free download of the ADIsimPLL™ software. The software designs, simulates, and analyzes the entire PLL frequency domain and time domain response. Various passive and active filter architectures are allowed.

INTERFACING

The ADF4153A has a simple SPI®-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When latch enable (LE) is high, the 22 bits that are clocked into the input register on each rising edge of SCLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the register truth table.

The maximum allowable serial clock rate is 20 MHz.

ADuC812 Interface

Figure 23 shows the interface between the ADF4153A and the ADuC812 MicroConverter®. Because the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4153A needs a 24-bit word, which is accomplished by writing three 8-bit bytes from the MicroConverter to the device. After the third byte is written, the LE input should be brought high to complete the transfer.

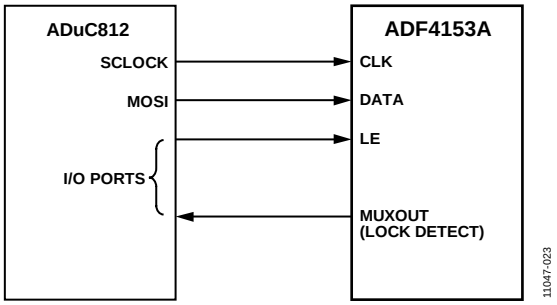


Figure 23. ADuC812 to ADF4153A Interface

When operating in this mode, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 180 kHz.

ADSP-21xx Interface

Figure 24 shows the interface between the ADF4153A and the ADSP-21xx digital signal processor. As discussed previously, the ADF4153A needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

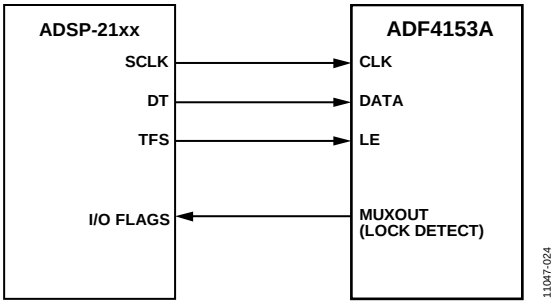


Figure 24. ADSP-21xx to ADF4153A Interface

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the chip scale package (CP-20) are rectangular. The printed circuit board (PCB) pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the PCB should be at least as large as this exposed pad. On the PCB, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the PCB thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with one ounce of copper to plug the via. The user should connect the PDB thermal pad to AGND.

APPLICATIONS INFORMATION

LOCAL OSCILLATOR FOR A GSM BASE STATION TRANSMITTER

Figure 25 shows the ADF4153A being used with a VCO to produce the local oscillator (LO) for a GSM base station transmitter.

The reference input signal is applied to the circuit at REF_{IN} and, in this case, is terminated in 50 Ω. A 25 MHz reference is used, which is fed directly to the PFD. To achieve 200 kHz channel spacing, a modulus of 125 is necessary. Note that with a modulus of 125, which is not divisible by 2, 3, or 6, subfractional spurs are avoided. See the Spur Mechanisms section for more information.

The charge pump output of the ADF4153A drives the loop filter.

The charge pump current is I_{CP} = 5 mA. ADIsimPLL is used to calculate the loop filter. It is designed for a loop bandwidth of 20 kHz and a phase margin of 45 degrees.

The loop filter output drives the VCO, which in turn is fed back to the RF input of the PLL synthesizer. It also drives the RF output terminal. A T-circuit configuration provides 50 Ω matching between the VCO output, the RF output, and the RF_{IN} terminal of the synthesizer.

In a PLL system, it is important to know when the loop is in lock. This is achieved by using the MUXOUT signal from the synthesizer. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer. One of these is the lock detect signal.

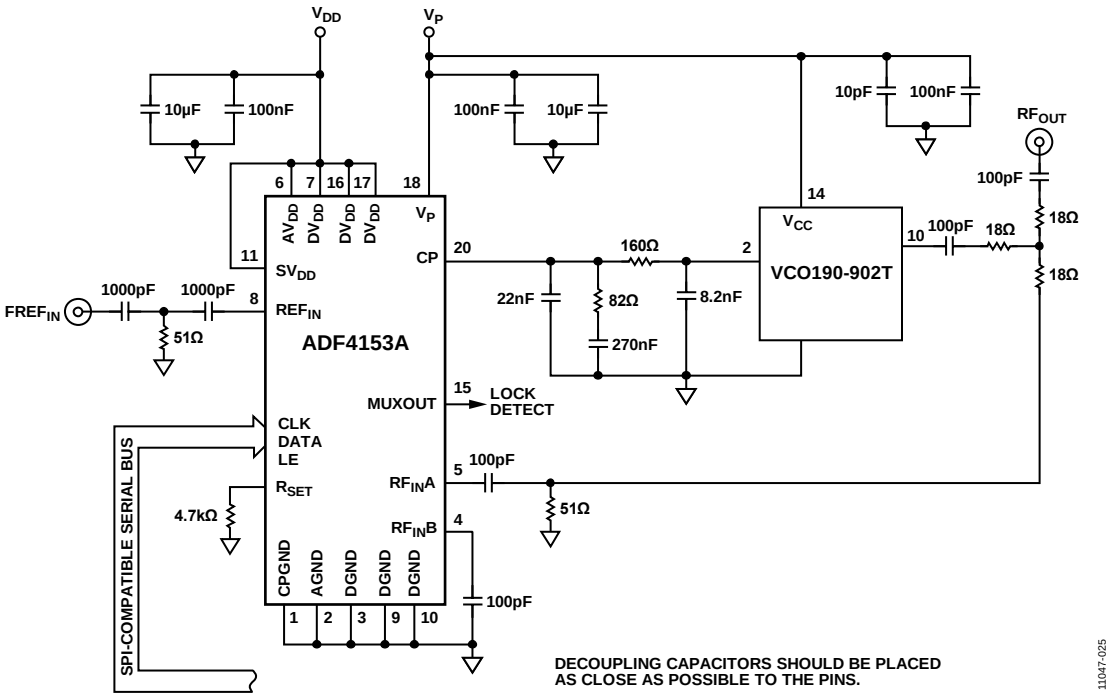


Figure 25. Local Oscillator for a GSM Base Station Transmitter

OUTLINE DIMENSIONS

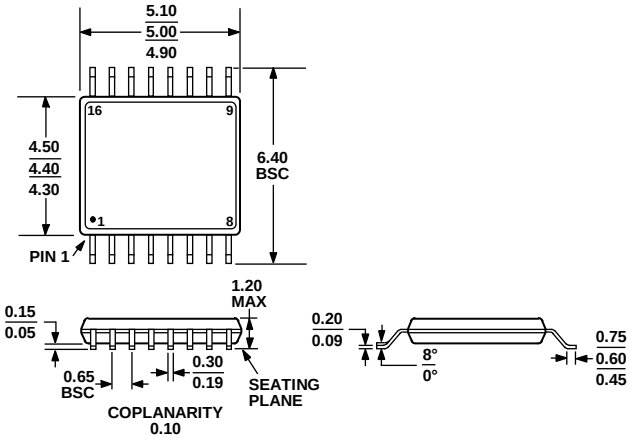


Figure 26. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeter

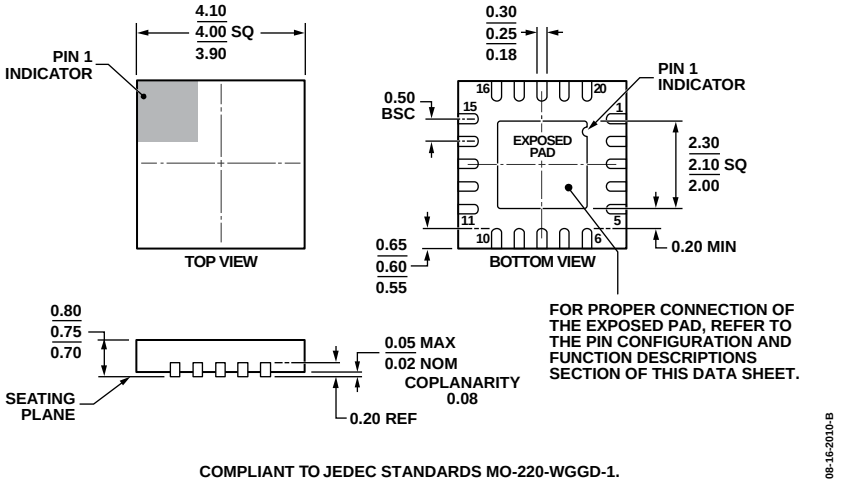


Figure 27. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF4153ABCPZ	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4153ABCPZ-RL7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4153ABRUZ	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4153ABRUZ-RL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP	RU-16
EV-ADF4153ASD1Z		Evaluation board for ADF4153A in LFCSP package	

[1] Z = RoHS Compliant Part.

NOTES

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D11047-0-1/13(A)

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