33 GHz to 40 GHz, GaAs, pHEMT, MMIC, 1 W Power Amplifier with Power Detector

Data Sheet

HMC7229

FEATURES

32 dBm P_{SAT} with 22% PAE
P1dB P_{OUT}: 31.5 dBm
High OIP3: 39.5 dBm
High gain: 24.5 dB
50 Ω matched input/output

APPLICATIONS

Point to point radios
Point to multipoint radio
VSAT and SATCOM

GENERAL DESCRIPTION

The HMC7229 is a four-stage, gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), 1 W power amplifier with an integrated temperature compensated on-chip power detector, operating between 33 GHz and 40 GHz. The HMC7229 provides a typical range of 23 dB to 24.5 dB of gain and a range of 30 dBm to 32 dBm of saturated output power (P_{SAT}) with 12% to 22% (typical) power added efficiency (PAE) range across a band of 33 GHz to 40 GHz from a 6 V supply. With an excellent OIP3 with a range of 37 dBm to 39.5 dBm across a band of 33 GHz to 40 GHz, the HMC7229 is ideal for linear applications such as high capacity point to point or point to multipoint radios or very small aperture terminal (VSAT)/satellite communications (SATCOM) applications demanding 32 dBm of efficient saturated output power. The radio frequency (RF) input/output ports are internally matched and dc blocked for easy integration into higher level assemblies.

FUNCTIONAL BLOCK DIAGRAM

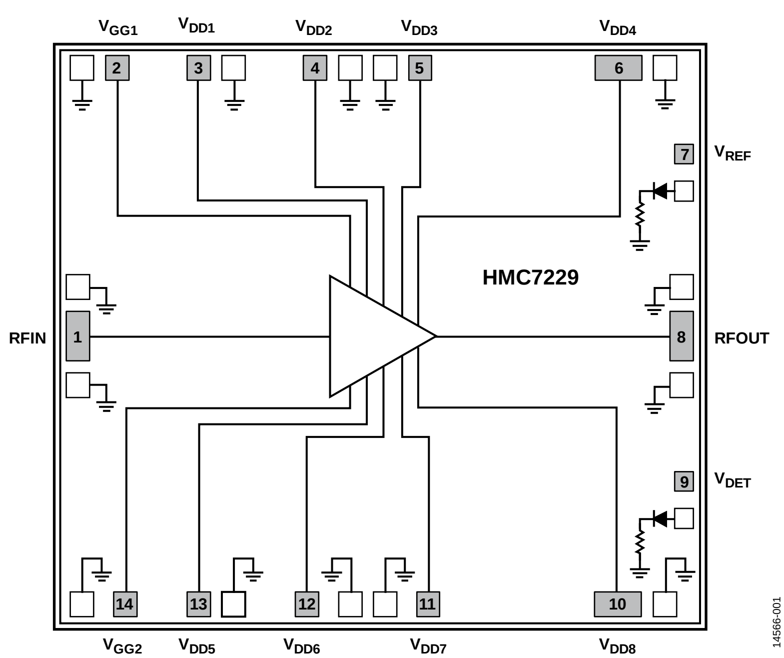

Figure 1.

Rev. D **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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7/2017—Rev. 0 to Rev. A

Changed HMC7229CHIPS to HMC7229 ... Throughout

6/2016—Revision 0: Initial Version

SPECIFICATIONS

33 GHz TO 35 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = V_{DD5} = V_{DD6} = V_{DD7} = V_{DD8} = 6 V, I_{DQ} = 1200 mA.[1, 2]

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			33		35	GHz
GAIN			21	23		dB
Gain Variation over Temperature				0.035		dB/°C
RETURN LOSS						
Input				7		dB
Output				15		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		29.5	31.5		dBm
Saturated Output Power	P_{SAT}			32		dBm
Power Added Efficiency	PAE	PAE taken at saturated output power		22		%
Output Third-Order Intercept	OIP3	Measurement taken at P_{OUT}/tone = 20 dBm		39.5		dBm
SUPPLY CURRENT	I_{DQ}[3]		800		1200	mA
SUPPLY VOLTAGE	V_{DD}		5		6	V

[1] Recommended bias conditions.
[2] Adjust the V_{GGx} supply voltage between −2 V and 0 V to achieve I_{DQ} = 1200 mA.
[3] I_{DQ} is the drain current without applying RF power.

35 GHz TO 37 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = V_{DD5} = V_{DD6} = V_{DD7} = V_{DD8} = 6 V, I_{DQ} = 1200 mA.[1, 2]

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			35		37	GHz
GAIN			22.5	24.5		dB
Gain Variation over Temperature				0.044		dB/°C
RETURN LOSS						
Input				9.5		dB
Output				20		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		28.5	30.5		dBm
Saturated Output Power	P_{SAT}			31		dBm
Power Added Efficiency	PAE	PAE taken at saturated output power		16		%
Output Third-Order Intercept	OIP3	Measurement taken at P_{OUT}/tone = 20 dBm		39		dBm
SUPPLY CURRENT	I_{DQ}[3]		800		1200	mA
SUPPLY VOLTAGE	V_{DD}		5		6	V

[1] Recommended bias conditions.
[2] Adjust the V_{GGx} supply voltage between −2 V and 0 V to achieve I_{DQ} = 1200 mA.
[3] I_{DQ} is the drain current without applying RF power.

37 GHz TO 40 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = V_{DD5} = V_{DD6} = V_{DD7} = V_{DD8} = 6 V, I_{DQ} = 1200 mA.[1, 2]

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			37		40	GHz
GAIN			21.5	23.5		dB
Gain Variation over Temperature				0.045		dB/°C
RETURN LOSS						
Input				9.5		dB
Output				13		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		27.5	29.5		dBm
Saturated Output Power	P_{SAT}			30		dBm
Power Added Efficiency	PAE	PAE taken at saturated output power		12		%
Output Third-Order Intercept	OIP3	Measurement taken at P_{OUT}/tone = 20 dBm		37		dBm
SUPPLY CURRENT	I_{DQ}[3]		800		1200	mA
SUPPLY VOLTAGE	V_{DD}		5		6	V

[1] Recommended bias conditions.
[2] Adjust the V_{GGx} supply voltage between −2 V and 0 V to achieve I_{DQ} = 1200 mA.
[3] I_{DQ} is the drain current without applying RF power.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Drain Bias Voltage (V_{DD})	7 V
RF Input Power (RFIN)	21 dBm
Channel Temperature	175°C
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 107 mW/°C Above 85°C)	9.7 W
Thermal Resistance, $θ_{JC}$ (Channel to Bottom Die)	9.3°C/W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C
ESD Sensitivity, Human Body Model (HBM)	Class 0, passed 150 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

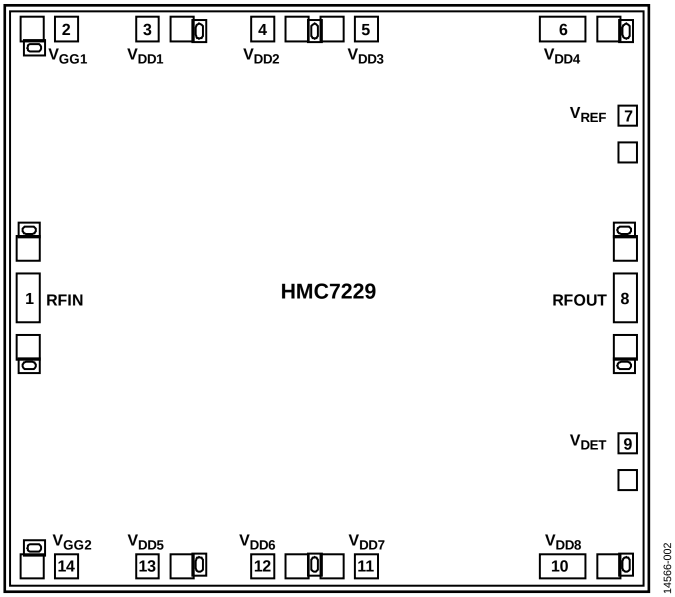

Figure 2. Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	Mnemonic	Description
1	RFIN	RF Input. This pad is ac-coupled and matched to 50 Ω.
2, 14	V_{GG1}, V_{GG2}	Gate Controls for the Power Amplifier. Adjust the V_{GG1} or V_{GG2} supply voltage to achieve recommended bias current. External 100 pF, 10 nF, and 4.7 µF bypass capacitors are required.
3 to 6, 10 to 13	V_{DD1} to V_{DD8}	Drain Bias Voltages. External 100 pF, 10 nF, and 4.7 µF bypass capacitors are required.
7	V_{REF}	DC Voltage of the Diode. This pad is biased through an external detector circuit used for temperature compensation of V_{DET} (see Figure 35).
8	RFOUT	RF Output. This pin is ac-coupled and matched to 50 Ω.
9	V_{DET}	DC Voltage Representing the RF Output Power. This pad is rectified by the diode that is biased through an external resistor (see Figure 35).
Die Bottom	GND	Die Bottom. The die bottom must be connected to RF/dc ground. See Figure 9 for the interface schematic.

INTERFACE SCHEMATICS

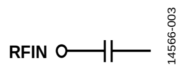

Figure 3. RFIN Interface Schematic

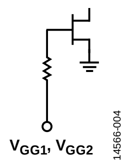

Figure 4. V_{GG1}, V_{GG2} Interface Schematic

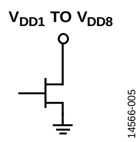

Figure 5. V_{DD1} to V_{DD8} Interface Schematic

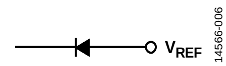

Figure 6. V_{REF} Interface Schematic

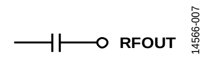

Figure 7. RFOUT Interface Schematic

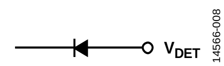

Figure 8. V_{DET} Interface Schematic

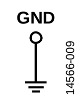

Figure 9. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

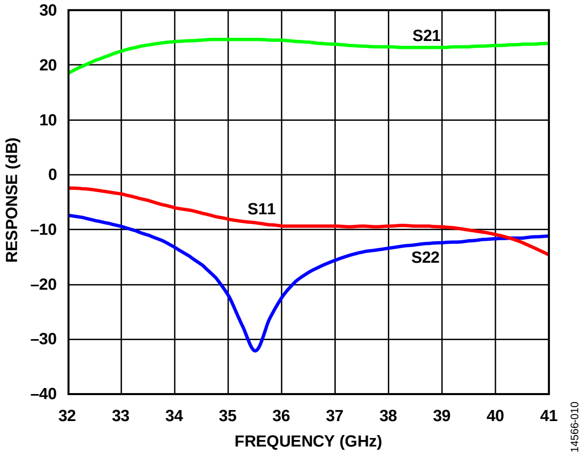

Figure 10. Response Gain and Return Loss vs. Frequency

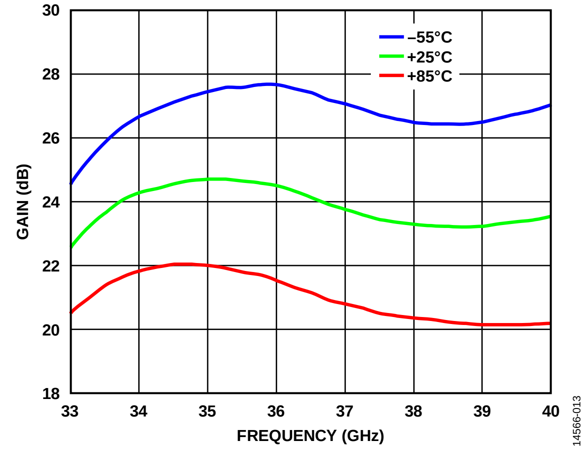

Figure 13. Gain vs. Frequency at Various Temperatures

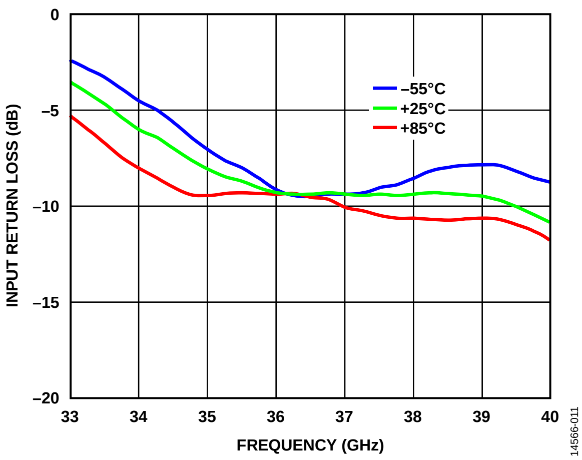

Figure 11. Input Return Loss vs. Frequency at Various Temperatures

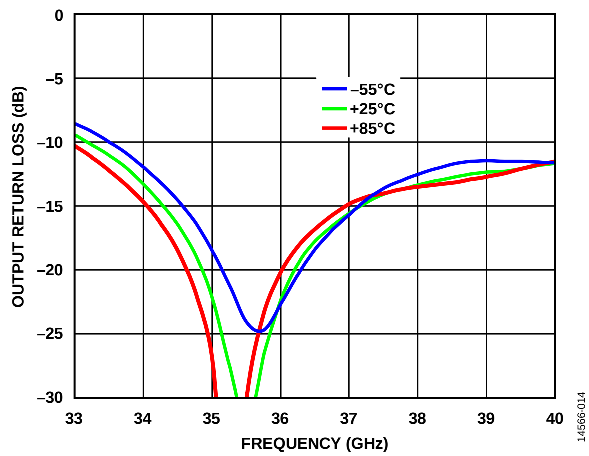

Figure 14. Output Return Loss vs. Frequency at Various Temperatures

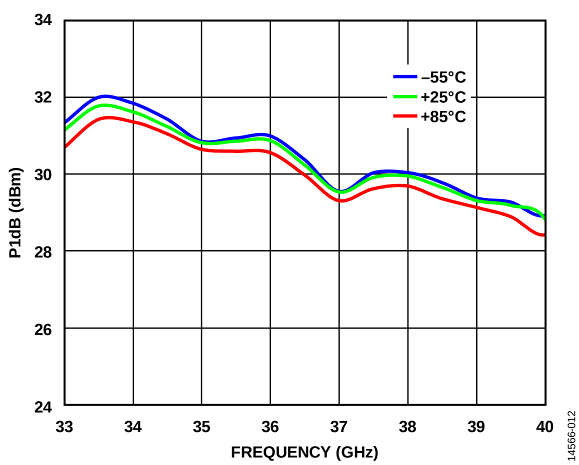

Figure 12. P1dB vs. Frequency at Various Temperatures

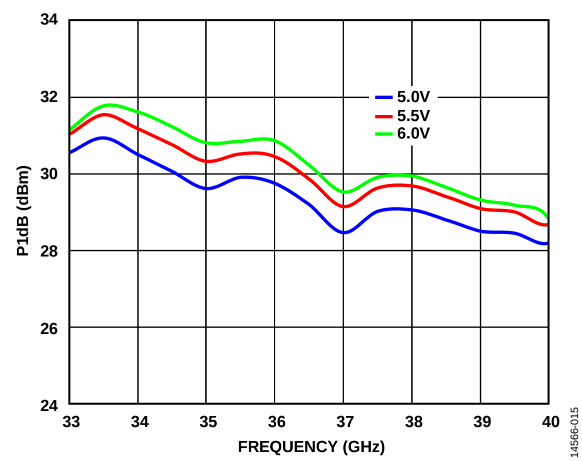

Figure 15. P1dB vs. Frequency at Various Supply Voltages

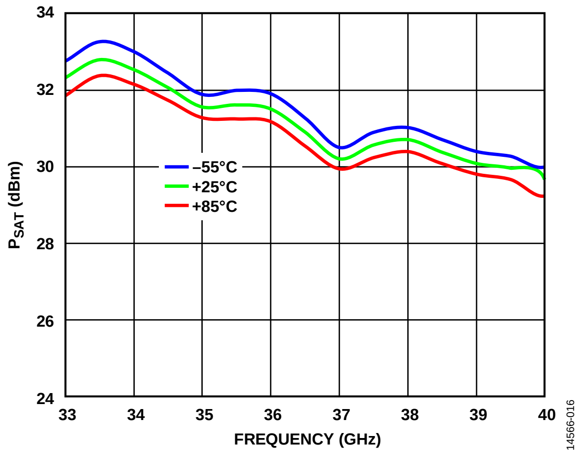

Figure 16. P_{SAT} vs. Frequency at Various Temperatures

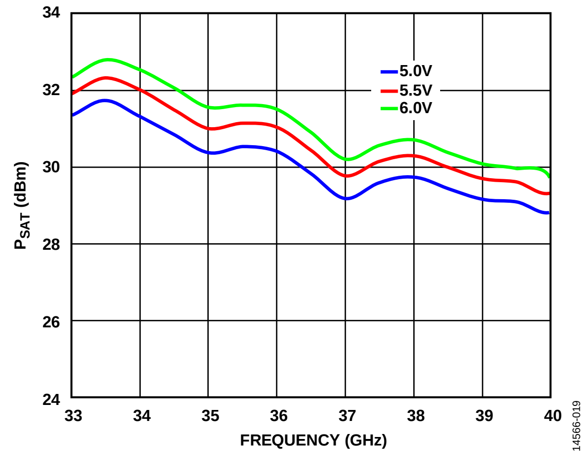

Figure 19. P_{SAT} vs. Frequency at Various Supply Voltages

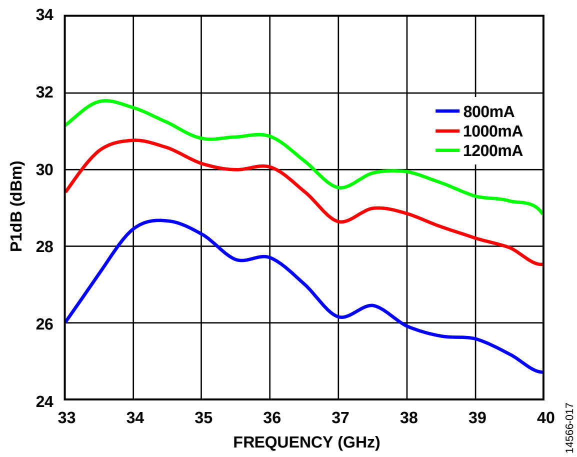

Figure 17. P1dB vs. Frequency at Various Supply Currents

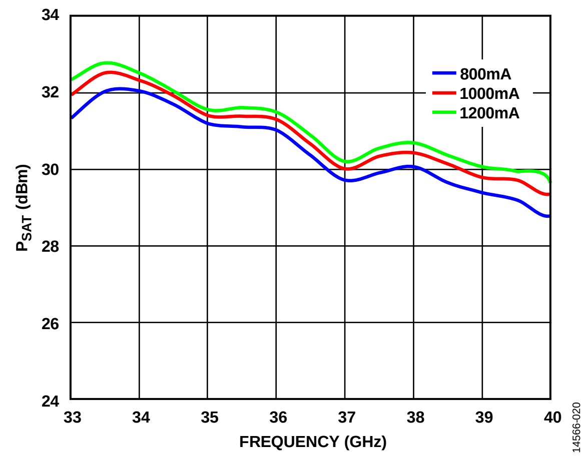

Figure 20. P_{SAT} vs. Frequency at Various Supply Currents

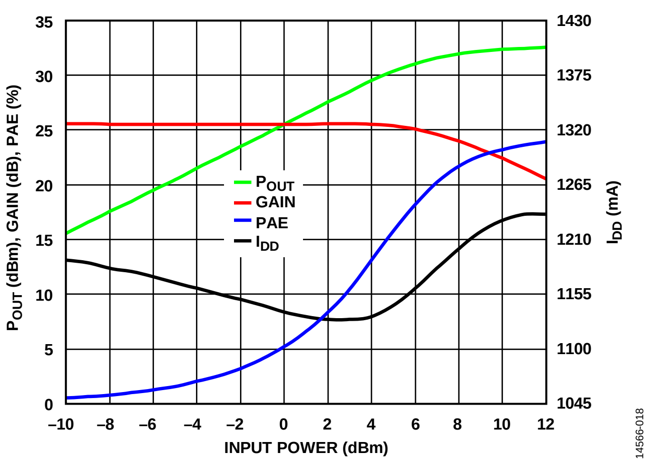

Figure 18. Power Compression at 34 GHz
(I_{DD} is Drain Current With RF Power Applied)

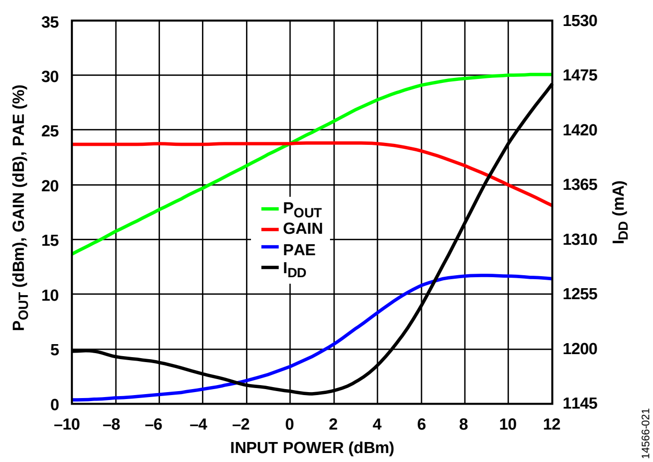

Figure 21. Power Compression at 39 GHz

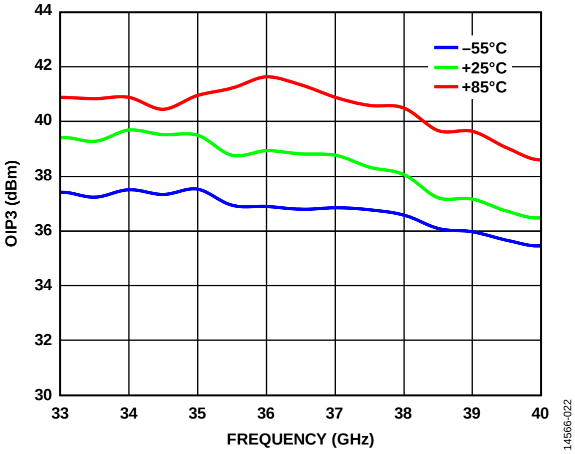

Figure 22. Output IP3 vs. Frequency at Various Temperatures

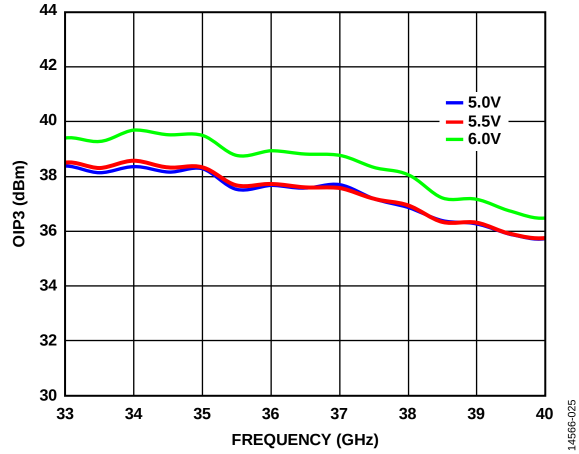

Figure 25. Output IP3 vs. Frequency at Various Supply Voltages

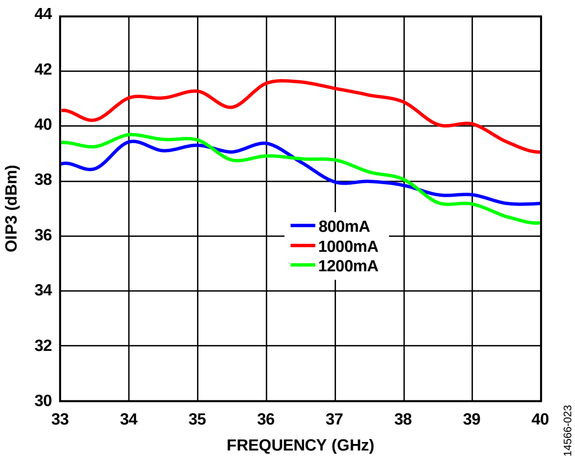

Figure 23. Output IP3 vs. Frequency at Various Supply Current

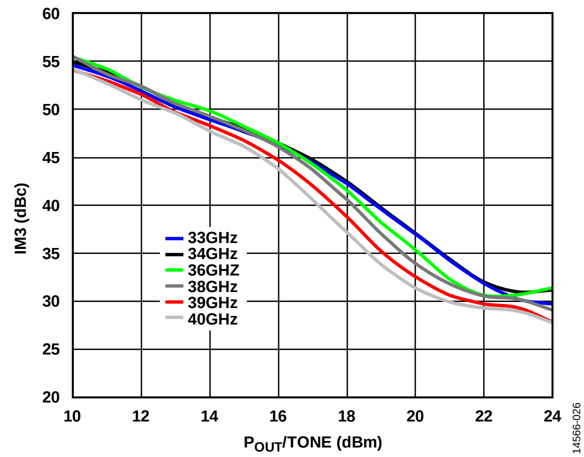

Figure 26. IM3 vs. P_{OUT}/Tone for Various Frequencies at V_{DD} = 5.5 V

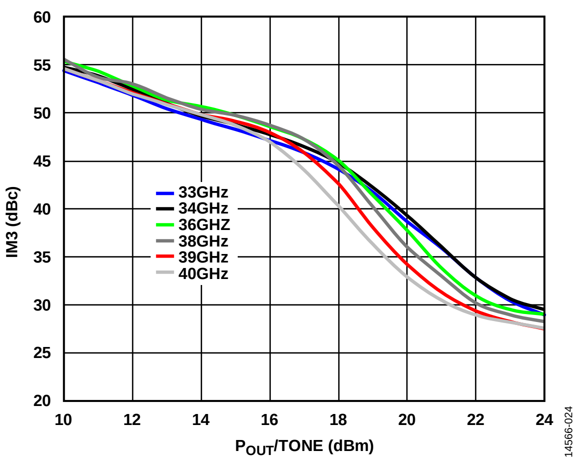

Figure 24. Third-Order Intermodulation (IM3) vs. P_{OUT}/Tone for Various Frequencies at V_{DD} = 6 V

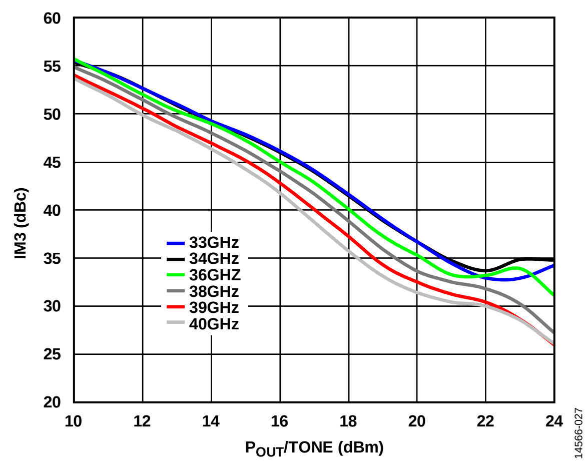

Figure 27. IM3 vs. P_{OUT}/Tone for Various Frequencies at V_{DD} = 5 V

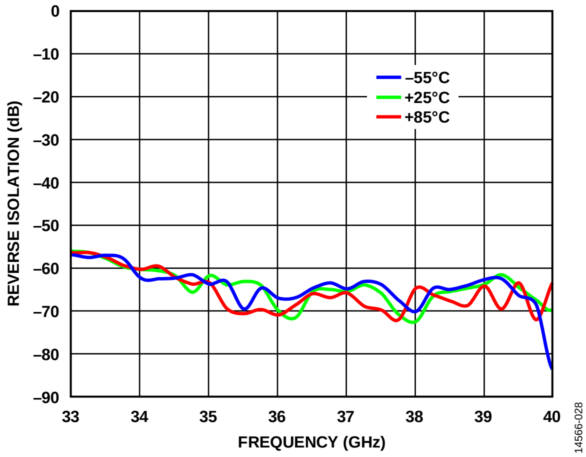

Figure 28. Reverse Isolation vs. Frequency for Various Temperatures

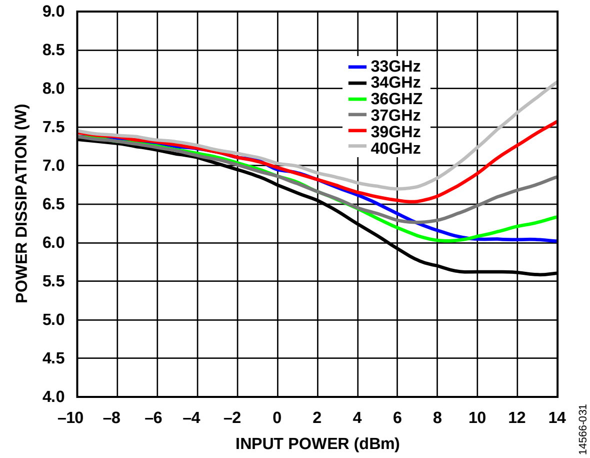

Figure 31. Power Dissipation vs. Input Power for Various Frequencies at T_A = 85°C

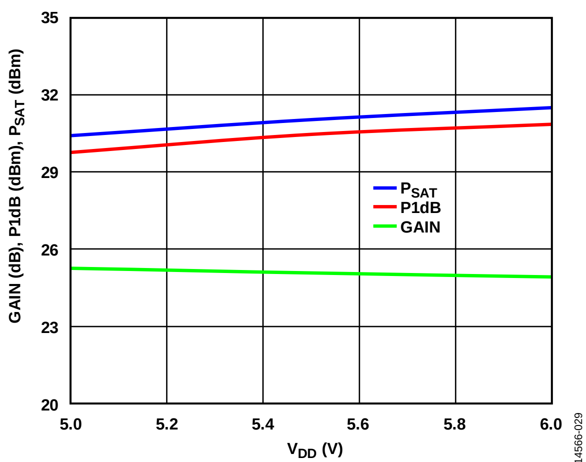

Figure 29. Gain, P1dB, and P_{SAT} vs. Supply Voltage (V_{DD}) at 36 GHz

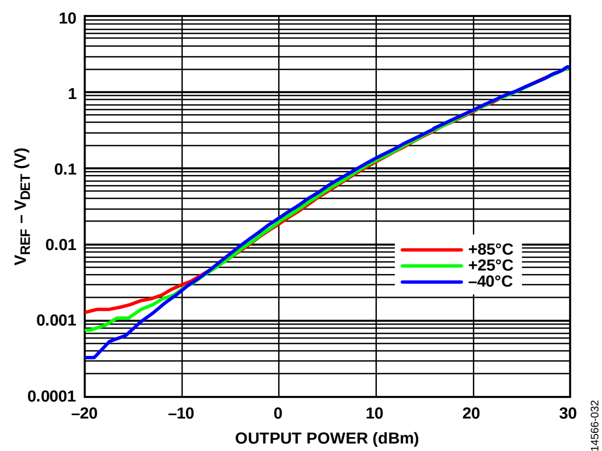

Figure 32. Detector Voltage (V_{REF} – V_{DET}) vs. Output Power for Various Temperatures at 38.5 GHz

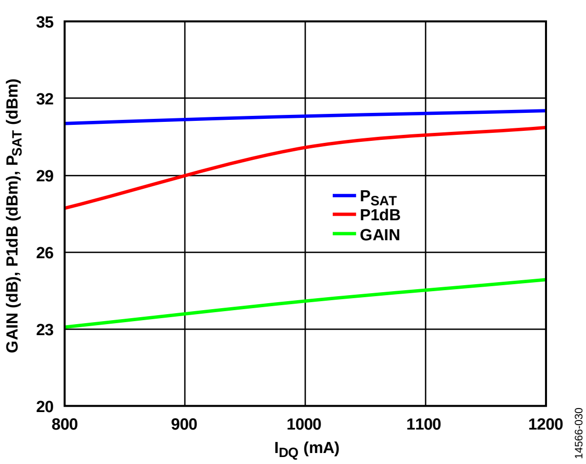

Figure 30. Gain, P1dB, and P_{SAT} vs. Supply Current (I_{DQ}) at 36 GHz

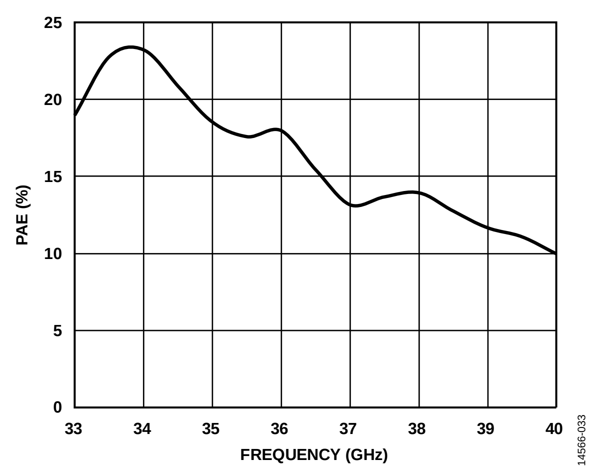

Figure 33. PAE at P_{SAT} vs. Frequency

THEORY OF OPERATION

The HMC7229 is a GaAs, pHEMT, MMIC, 1 W power amplifier consisting of four gain stages in series. Figure 34 shows a simplified functional block diagram of the HMC7229.

The input signal of the HMC7229 is evenly divided into two paths and each path is amplified through the four independent gain stages. The amplified signals are then combined at the RF output. A portion of the RF output signal is directionally coupled to a diode for detection of the RF output power. When the diode is dc biased, it rectifies the RF power and makes it available for measurement as a dc voltage at V_{DET}. To allow for temperature compensation of V_{DET}, a symmetrically located and identical detector circuit, minus the coupled RF power, is available via V_{REF}. As shown in Figure 32, taking the difference of $V_{REF} - V_{DET}$ provides a temperature compensated signal that is proportional to the RF output power.

The HMC7229 has single-ended input and output ports with impedances nominally matched to 50 Ω internally over the frequency range from 33 GHz to 40 GHz. Consequently, the HMC7229 can be directly inserted into a 50 Ω system with no impedance matching circuitry required.

Impedances nominally matched to a 50 Ω system also means that multiple HMC7229 amplifiers can be cascaded back to back without external matching circuitry.

Similarly, multiple HMC7229 can be used with power dividers at the RF input and power combiners at the RF output to obtain higher output power levels.

The input and output impedances are sufficiently stable compared to the variations in temperature and supply voltage that no impedance matching compensation is required.

It is critical to supply very low inductance ground connections to the backside of the HMC7229, ensuring stable operation. Guidance on mounting the HMC7229 is given in the Mounting and Bonding Techniques for Millimeter Wave GaAs MMICs section.

To achieve the best performance from the HMC7229 and not to damage the device, do not exceed the absolute maximum ratings.

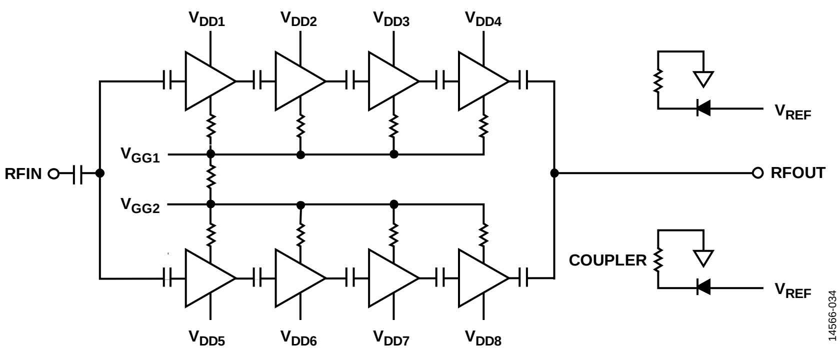

Figure 34. Simplified Functional Block Diagram

APPLICATIONS INFORMATION

BIASING PROCEDURES

The basic connections for operating the HMC7229 are shown in Figure 35 and the Theory of Operation section. The RF input and RF output are ac-coupled by internal dc block capacitors. Follow the recommended bias sequencing to avoid damaging the amplifier.

The amplifier gate bias can be supplied using either the V_{GG1} pin or V_{GG2} pin. Use the V_{DD1} to V_{DD8} pins while applying the drain bias to the amplifier. Testing to gather data for the HMC7229 data sheet used the V_{GG1} pin with the V_{DD1} to V_{DD8} pins connected together.

Use the following recommended bias sequence during power-up:

1. Connect GND to RF/dc ground.
2. Set V_{GG1} or V_{GG2} to −2 V.
3. Set V_{DD1} to V_{DD8} to 6 V.
4. Increase V_{GG1} or V_{GG2} to achieve a typical I_{DQ} = 1200 mA.
5. Apply an RF signal the device.

Use the following recommended bias sequence during power-down:

1. Turn off the RF signal.
2. Decrease V_{GG1} or V_{GG2} to −2 V to achieve I_{DQ} = 0 mA.
3. Decrease V_{DD1}, V_{DD2}, V_{DD3}, and V_{DD4} to 0 V.
4. Increase V_{GG1} or V_{GG2} to 0 V.

The bias conditions listed at V_{DD} = 6 V, I_{DQ} = 1200 mA is a recommended operating point to receive optimum performance from the HMC7229. The data used in this data sheet is taken with the recommended bias conditions (see the Specifications section).

Using the HMC7229 in a different bias condition may provide different performance than the performance shown in the Typical Performance Characteristics section.

The V_{DET} and V_{REF} pins are the output pins for the internal power detector. The V_{DET} pin is the dc voltage output pin representing the RF output power rectified by the internal diode, biased through an external resistor.

The V_{REF} pin is the dc voltage output pin representing the reference diode voltage, which is biased through an external resistor. The reference diode voltage compensates the temperature variation effects on both the V_{REF} and V_{DET} diodes. Figure 35 shows a suggested circuit to read out the output voltage in correlation with the RF output power.

TYPICAL APPLICATION CIRCUIT

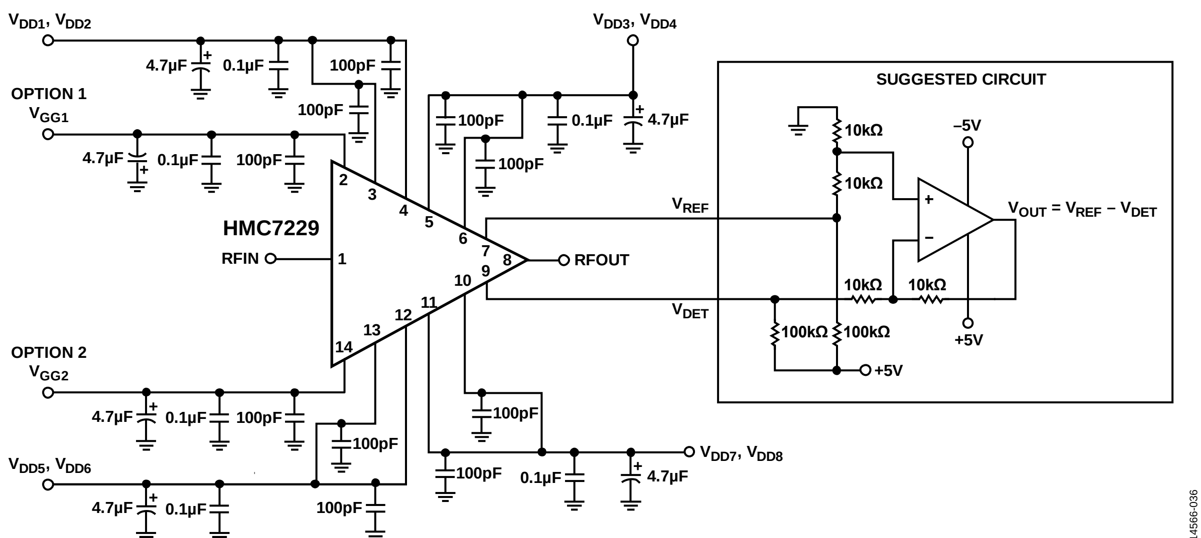

Figure 35. Typical Application Circuit

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETER WAVE GaAs MMICs

Attach the HMC7229 directly to the ground plane eutectically or with a conductive epoxy. To route the RF signal to and from the HMC7229, use a 50 Ω microstrip transmission line on 0.127 mm (0.005 inches) thick alumina, thin film substrates (see Figure 36).

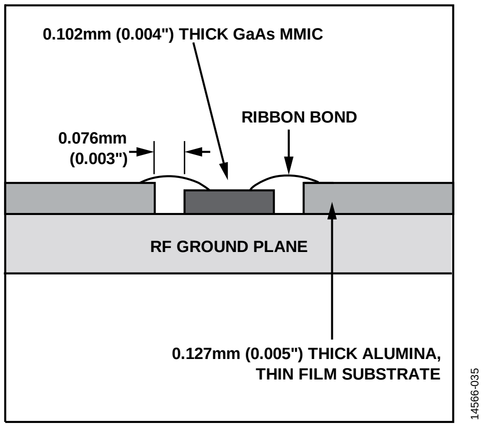

Figure 36. Routing RF Signals

To minimize the bond wire length, place microstrip substrates as close to the HMC7229 as possible. Typical chip to substrate spacing is 0.076 mm to 0.152 mm (0.003 inches and 0.006 inches).

HANDLING PRECAUTIONS

To avoid permanent damage to the device, adhere to the following precautions:

- All bare HMC7229 ship in either waffle or gel-based ESD protective containers, sealed in an ESD protective bag. After opening the sealed ESD protective bag, store all chips in a dry nitrogen environment.
- Handle the HMC7229 in a clean environment. Never use liquid cleaning systems to clean the chip.
- Follow ESD precautions to protect against ESD strikes.
- While applying bias, suppress instrument and bias supply transients. To minimize inductive pickup, use shielded signal and bias cables.
- Handle the HMC7229 along the edges with a vacuum collet or a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and must not be touched with a vacuum collet, tweezers, or fingers.

MOUNTING

The HMC7229 is back metallized and can be die mounted onto a system with Au/Sn eutectic preforms or with electrically conductive epoxy. The mounting surface must be clean and flat.

Eutectic Die Attach

It is best to use an 80% Au/20% Sn preform with a work surface temperature of 255°C and a tool temperature of 265°C. When the work surface is 255°C and tool temperature is 265°C, 90% nitrogen/10% hydrogen gas is applied to the work surface, maintain the tool tip temperature at 290°C. Do not expose the HMC7229 to a temperature greater than 320°C for more than 20 sec. No more than 3 sec of scrubbing is required for attachment.

Epoxy Die Attach

The ABLETHERM 2600BT is recommended for chip attachment. Apply a minimum amount of epoxy to the mounting surface so a thin epoxy fillet is observed around the perimeter of the HMC7229 after placing the device into position on the surface. Cure the epoxy per the schedule provided by the manufacturer.

Wire Bonding

RF bonds made with 0.003 in. × 0.0005 in. Au ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. DC bonds of 1 mil (0.025 mm) diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

ASSEMBLY DIAGRAM

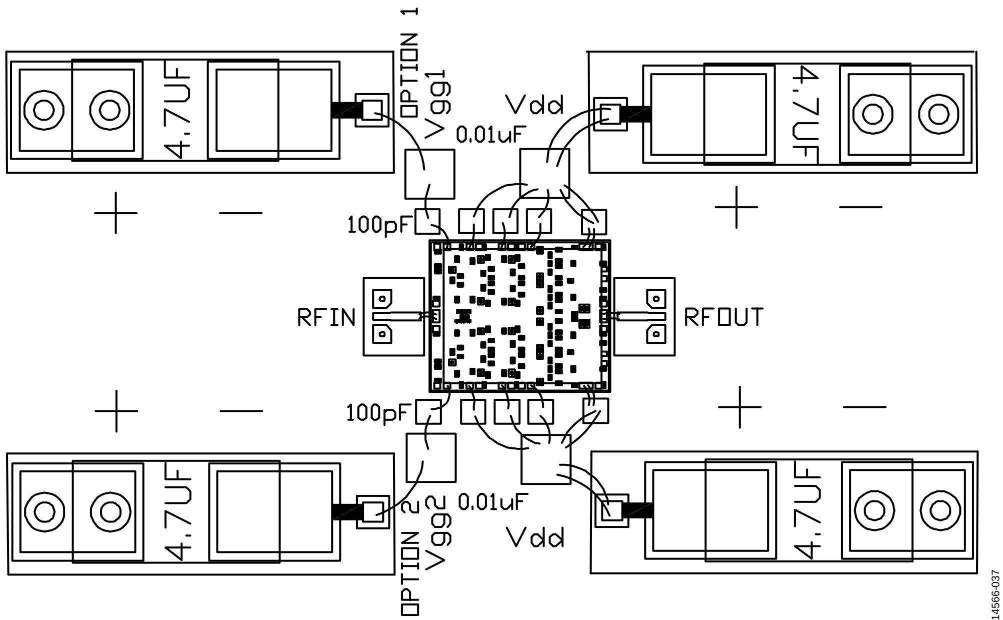

Figure 37. Assembly Diagram

OUTLINE DIMENSIONS

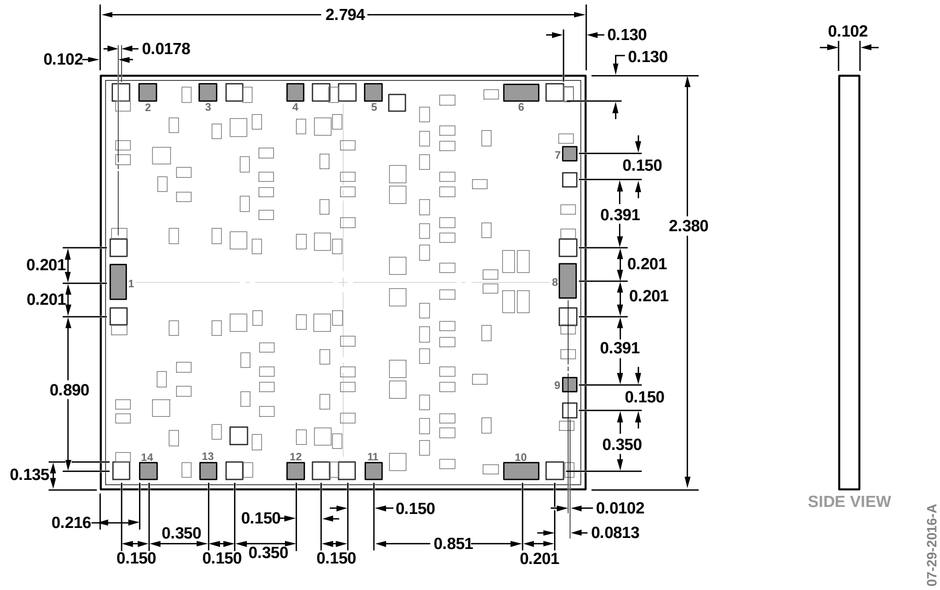

Figure 38. 14-Pad Bare Die [CHIP]
(C-14-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
HMC7229	−55°C to +85°C	14-Pad Bare Die [CHIP]	C-14-4
HMC7229-SX	−55°C to +85°C	14-Pad Bare Die [CHIP]	C-14-4

[1] The HMC7229 and HMC7229-SX are RoHS compliant parts.